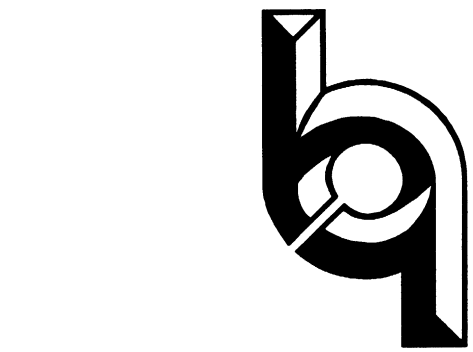

BENCHMARQ

Benchmarq . . . The brains behind the battery. ™

1997
Data Book

BENCHMARQ® Microelectronics, Inc.
17919 Waterview Parkway
Dallas, Texas 75252
Fax: (972) 437-9198
Tel: (972) 437-9195
E-mail: benchmarq@benchmarq.com
World Wide Web: http://www.benchmarq.com

BENCHMARQ 1997 Data Book

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Our Products

At Benchmarq, we provide integrated circuit and module solutions for power-sensitive and portable electronics systems.

Power-sensitive AC-powered systems in the office and industry must gracefully deal with the loss of power, maintaining the integrity of important data and self-sufficiently continuing critical operation. Portable systems share the design requirements of their powercord-bound counterparts, but add entirely new challenges—including power supervision, energy management, data security, and size minimization.

The product families described in this data book directly address these requirements, taking full advantage of advanced analog and digital VLSI technologies and state-of-the-art battery and packaging expertise. Power supervision, energy management, size reduction, nonvolatility, data security, and retrofit capability are integral to Benchmarq's product line.

Our Commitment

When you choose to integrate Benchmarq products within your own, be assured that Benchmarq is committed to providing the specific solutions you need today and to developing creative solutions to the growing challenges of tomorrow---supported by the best customer service and the highest overall quality.

The drive for excellence in all dimensions of quality is a cornerstone of our company.

Data Book Organization

This data book is organized into general information sections and product family sections.

You can locate information in this book in several ways.

Chapters 1 through 6 contain detailed product information. Chapter 7 includes packaging information, and Chapter 8 describes Benchmarq's commitment to quality and the processes we use to ensure reliability in our products. Chapter 9 lists sales offices and distributors.

For More Information ...

If you haven't found it here . . . **Ask!**

Benchmarq maintains an updated product listing on the World Wide Web at the URL listed below. Browse the Benchmarq Home Page for the latest Benchmarq product information and sales office locations at:

http://www.benchmarq.com

To send us e-mail to be added to our mailing list or to get further information, contact Benchmarq at:

benchmarq@benchmarq.com

Additional Benchmarq information is available from your Benchmarq distributor or sales office (listed in the back of this Data Book), or by contacting Benchmarq Customer Service at (800) 966-0011 or **(972) 437-9195.**

Table of Contents

Table of Contents

Fast Charge IC Summary and Selection Guide

Benchmarq's Fast Charge ICs provide fast charge control, current regulation support, and pre-charge qua cation and conditioning for rechargeable batteries.

- ➤ Fast charging and conditioning of nickel cadmium, nickel metal hydride, lead acid, lithium ion, or rechargeable alkaline batteries
- > Flexible current regulation support:
  - Frequency-modulated linear (lowest cost)
  - Switch-mode (most efficient)
  - Gating control (external regulator)
- ● Easily integrated into systems or as a stand-alone charger
- ● Direct LED outputs display battery and charge status
- ● Fast charge termination by delta tempera —— delta time, negative delta voltage, peak voltage detect, minimum current, maximum temperature, maximum voltage, and maximum time
- ● Optional top-off and maintenance charging
- ● Discharge-before-charge option

Variable-rate charging uses excess supply current to charge batteries during system operation

Fast Charge IC Selection Guide

Battery Technology	Charge Control Output	Termination Method	Key Features	Pins / Package	Part Number	Page Number
NiMH NiCd	Single	-ΔV, peak voltage, time	Low power and small size	8/.300" DIP, 8/.150" SOIC	bq2002	1-1
NiMH NiCd	Single	-ΔV, PVD, max. temp., time	Low power and small size	8/.300" DIP, 8/.150" SOIC	bq2002C	1-11
NiMH NiCd	Single	ΔT/Δt, max. temp., time	Low power and small size	8/.300" DIP, 8/.150" SOIC	bq2002T	1-19
NiMH NiCd	Single	-ΔV, ΔT/Δt, max. temp., voltage, and time	Includes PWM	16/.300" DIP, 16/.300" SOIC	bq2003	1-31
NiMH NiCd	Single	-ΔV, peak voltage, ΔT/Δt, max. temp., voltage, and time	PWM and low-power mode	16/.300" DIP, 16/.150" SOIC	bq2004	1-87
NiMH, NiCd Li-Ion	Single	-ΔV, peak voltage, ΔT/Δt, max. temp., voltage, and time	PWM, pulsed precharge conditioning	16/.300" DIP, 16/.150" SOIC	bq2004E	1-111
NiMH NiCd	Dual	-ΔV, ΔT/Δt, max. temp., voltage, and time	Sequential charger	20/.300" DIP, 20/.300" SOIC	bq2005	1-131
NiMH NiCd	Single	-ΔV, peak voltage, max. temp, voltage, and time	LCD/LED display	24/.300" DIP, 24/.300" SOIC	bq2007	1-171
Lead Acid	Single	max. voltage, min. current, $-\Delta^2V$, temp., and time	Temp. compensated thresholds	16/.300" DIP, 16/.150" SOIC	bq2031	1-209
Lithium Ion	Single	max. voltage, min current	1% voltage regulation	16/.300" DIP, 16/.150" SOIC	bq2054	1-273
Rechargeable Alkaline	Single	maximum voltage	2-cell charging	8/.300" DIP, 8/.150" SOIC	bq2902	1-305
Rechargeable Alkaline	Single	maximum voltage	3- or 4-cell charging	14/.300" DIP, 14/.150" SOIC	bq2903	1-313

Benchmarq's bq2053 and bq2058 Lithium Ion Pack Protection ICs provide reversible overvoltage, undervoltage, and overcurrent protection for lithium ion battery packs.

- Protects two to four Lithium Ion series cells from overvoltage, undervoltage, and overcurrent
- Designed for battery pack integration
  - Small outline package, minimal external components and space, and low cost
  - Drives external N-FET switches
- User-selectable thresholds mask-programmable by Benchmarq
- bq2053 operating current:
  - < 40µA for 4-cell configuration
  - < 20µA for 3-cell configuration
  - < 15µA for 2-cell configuration
  - < 1µA sleep mode
- bq2058 operating current:
  - < 60µA for 3-cell or 4-cell configuration

Pack Protection IC Selection Guide

Battery Technology	Protection Types	Key Features	Pins / Package	Part Number	Page Number
Lithium Ion	Overvoltage, overcurrent, and undervoltage	2–4 cells Very low power	8/.150" SOIC	bq2053	1-257
Lithium Ion	Overvoltage, overcurrent, and undervoltage	3 or 4 cells Very low power	16/.150" SOIC	bq2058	1-293

Nonvolatile SRAM Summary and Selection Guide

Benchmarq's NVSRAMs integrate—in a single-DIP package—extremely low standby power SRAM, nonvolatile control circuitry, and a long-life lithium cell. The NVSRAMs combine secure nonvolatility (more than 10 years in the absence of power) with standard SRAM pinouts and fast unlimited read/write operation.

- Data retention in the absence of power
- Automatic write-protectionduring power-up/power-down cycles
- Industry-standard pinout
- Conventional SRAM operation; unlimited write cycles
- 10 or 5 years minimum data retention in the absence of power
- Battery internally isolated until power is first supplied
- Industrial temperature range available

Nonvolatile SRAM Selection Guide

Density	Configuration	Technology	Access Time (ns)	Minimum Data-Retention Time	Pins / Package	Part Number[1]	Page Number
64 Kb	8 Kb x 8	NVSRAM	70, 85[2], 150[2], 200	10 years	28 / DIP	bq4010/ bq4010Y	6-1
256 Kb	32 Kb x 8	NVSRAM	70[2], 100, 150[2], 200	10 years	28 / DIP	bq4011/ bq4011Y	6-11
1 Mb	128 Kb x 8	NVSRAM	70[2], 85[2], 120	10 years	32 / DIP	bq4013/ bq4013Y	6-21
2 Mb	256 Kb x 8	NVSRAM	85,120	10 years	32 / DIP	bq4014/ bq4014Y	6-31
	128 Kb x 16	NVSRAM	85,120	10 years	40 / DIP	bq4024/ bq4024Y	6-71
4 Mb	512 Kb x 8	NVSRAM	70, 85, 120	10 years	32 / DIP	bq4015/ bq4015Y	6-41
	256 Kb x 16	NVSRAM	85,120	5 years	40 / DIP	bq4025/ bq4025Y	6-81
8Mb	1024 Kb x 8	NVSRAM	70	10 years	36 / DIP	bq4016 bq4016Y	6-51
16Mb	2048 Kb x 8	NVSRAM	70	5 years	36 / DIP	bq4017 bq4017Y	6-61

Notes:
1. "Y" version denotes 10% Vcc tolerance.
2. "Y" version available in -40°C to +85°C industrial temperature range.
3. See data sheet for details.

Nonvolatile Controller Summary and Selection Guide

Benchmarq's nonvolatile controllers provide power monitoring, write-protection, and supply switching to convert standard SRAM or PSRAM and a backup battery into a reliable, predictable nonvolatile memory. The nonvolatile controller modules are complete battery-backup solutions including an encapsulated 130mAh lithium cell that is isolated until power is applied.

- Power monitoring and switching for 3V battery-backup applications
- ➤ 5V Vcc operation
- ➤ Automatic write-protection during power-up/power-down cycles
- ➤ Automatic switching from Vcc to first backup battery and from first backup battery to second backup battery
- Reset output option for system power-on reset
- Less than 10ns chip enable propagation delay
- 5% or 10% supply operation
- Control up to four banks of SRAM
- Module/DIP or SOIC packages

Nonvolatile Controller Selection Guide

SRAM Banks Controlled	Battery Monitor Outputs	Reset Output	I_{OUT} (Typ.)	Pins / Package	Part Number	Page Number
1			160 mA	8/ NDIP, NSOIC	bq2201	4-1
2		✓	160 mA	16/ NDIP, NSOIC	bq2202	4-9
2	J	J	160 mA	16/ NDIP, NSOIC	bq2203A	4-17
4			160 mA	16/ NDIP, NSOIC	bq2204A	4-25
2		✓	160 mA	12/ DIP module	bq2502	4-33

Real-Time Clock Summary and Selection Guide

Benchmarq's real-time clocks (RTCs) provide highly integrated clock/calendar solutions for microcomputer-based designs. Each module is a completely self-contained unit, including IC, crystal, and a battery ensuring operation for 10 years in the absence of power. The very compact, low-power *ICs* need only a battery and a crystal for operation. NVSRAM controller versions allow users to make inexpensive SRAM nonvolatile for data and configuration storage in computers, portable equipment, office machines and other applications.

- Clock/calendar counts seconds through years with daylight savings and leap-year adjustments
- ➤ IBM PC AT-compatible clocks include:
  - 5- or 3-Volt operation
  - 114 or 242 bytes of user nonvolatile RAM storage
  - 32KHz output for power management
- Completely self-contained modules operate for more than 10 years in the absence of power
- SRAM-based clocks feature:
  - SRAM interface
  - Up to 512Kbytes of NVSRAM
  - CPU Supervisor
- One minute per month clock accuracy in modules
- Nonvolatile control for an external SRAM
- IC versions require only a crystal and battery

Real-Time Clock Selection Guide

Onboard RAM (bytes)	NVRAM Control	Bus Interface	Voltage	32kHz Output	CPU Super-visor	Pins / Package	Part Number	Page Number
114		Muxed	5V			24 I DIP, SOIC 28 / PLCC	bq3285	5-1
242		Muxed	5V	J		24 / DIP, SOIC, SSOP 28 / PLCC	bq3285E	5-21
242		Muxed	5V	✓		24 I SOIC, SSOP	bq3285EC	5-45
242		Muxed	3V	✓		24 / DIP, SOIC, SSOP	bq3285L	5-21
242		Muxed	3V	✓		24 I SOIC, SSOP	bq3285LC	5-45
114		Muxed	5V			24 / DIP module	bq3287/ bq3287A	5-69
242		Muxed	5V	J		24 / DIP module	bq3287E/ bq3287EA	5-73
114	✓	Muxed	5V			24 / DIP, SOIC 28 / PLCC	bq4285	5-77
114	J	Muxed	5V	✓		24 / DIP, SOIC, SSOP, 28 / PLCC	bq4285E	5-97
114	J	Muxed	3V	J		24 / DIP, SOIC, SSOP	bq4285L	5-97
114	✓	Muxed	5V			24 / DIP module	bq4287	5-123
114	J	Muxed	5V	J		24 / DIP module	bq4287E	5-129
32K		SRAM	5V			28 / DIP module	bq4830Y	5-135
32K		SRAM	5V		J	32 / DIP module	bq4832Y	5-149
128K		SRAM	5V		✓	32 / DIP module	bq4842Y	5-165
0	J	SRAM	5V		J	28 / DIP, SOIC	bq4845/Y	5-181
0	J	SRAM	5V		J	28 / DIP module	bq4847/Y	5-199
512K		SRAM	5V			32 / DIP module	bq4850Y	5-203
512K		SRAM	5V		J	36 / DIP module	bq4852Y	5-217

NVSRAM Cross-Reference

Density	Dallas Semiconductor	SGS-Thomson	Benchmarq
64Kb	DS1225AB DS1225AD/Y	MK48Z08 MK48Z18	bq4010 bq4010Y
256Kb	DS1230AB DS1230Y DS1630AB DS1630Y	M48Z30 M48Z30Y - -	bq4011 bq4011Y Contact factory Contact factory
1Mb	DS1245AB DS1245Y DS1645AB DS1645Y DS1645EE	M48Z128 M48Z128Y - - -	bq4013 bq4013Y Contact factory Contact factory Contact factory
2Mb	- DS1249Y DS1658AB DS1658Y	M48Z256 M48Z256Y M46Z128 M46Z128Y	bq4014 bq4014Y bq4024 bq4024Y
4Mb	DS1650 DS1650Y - -	M48Z512 M48Z512Y M46Z256 M46Z256Y	bq4015 bq4015Y bq4025 bq4025Y

Real-Time Clock Cross-Reference

Dallas Semiconductor	SGS-Thomson	Benchmarq
DS1285/885	-	bq3285P
DS1285Q/885Q	-	bq3285Q
DS1285S/885S	-	bq3285S
DS1287/887	MK48T87B24	bq3287MT
DS1287A/887A	-	bq3287AMT
DS14285	-	bq4285P
DS14285S	-	bq4285S
DS14285Q	-	bq4285Q
DS14287	-	bq4287MT
DS1643	M48T18	bq4830Y[1]
DS1644	-	bq4830Y
DS1646	-	bq4842Y[2]

Notes: 1. Memory upgrade.

2. Benchmarq's bq4842 additional features: microprocessorreset, watchdog monitor, clock alarm, periodic interrupt.

Nonvolatile Controllers Cross-Reference

Dallas Semiconductor	Benchmarq
DS1210	bq2201PN[4]
DS1210S	bq2201SN[1,4]
DS1218	bq2201PN[5]
DS1218S	bq2201SN[5]
DS1221	bq2204APN[3,4]
DS1221S	bq2204ASN[2,3,4]

Notes: 1. Benchmarq's bq2201SN is a small 8-pin, 150-mil SOIC, compared to the DS1210S, which is a 16-pin, 300-mil SOIC.

2. Benchmarq's bq2204ASN is a small 16-pin, 150-mil SOIC, compared to the DS1221S, which is a 16-pin, 300-mil SOIC.

3. Optional "security feature" DS1221 pins are no-connect on the bq2204A.

4. Benchmarq's bq2201 and bq2204A do not incorporate a "check battery status" function.

Benchmarq's standard products are available in several packages and operating ranges. A valid order number is a sequence of:

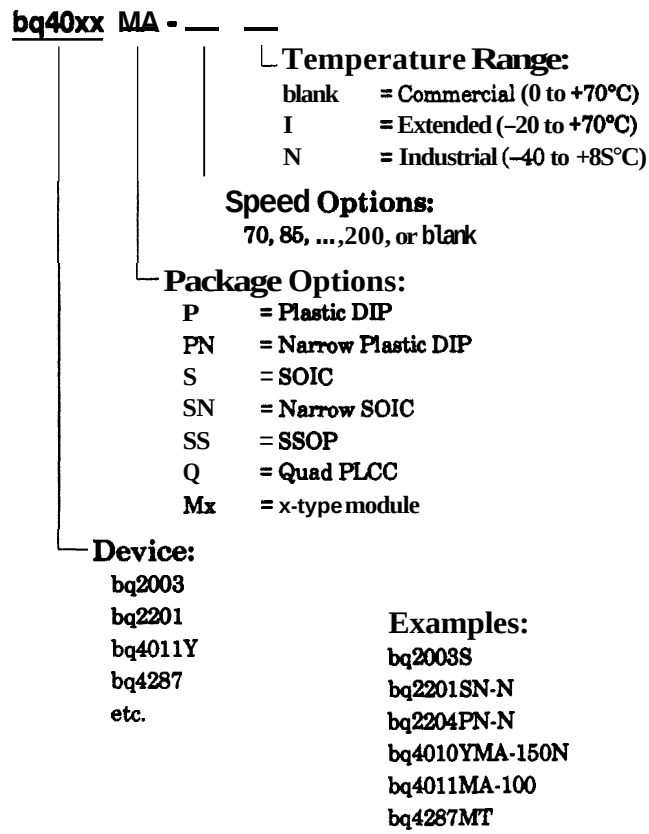
Device

Package Options

Speed Options

Temperature Range

Valid options for a specific device are defined in the ordering information section at the end of its data sheet. Contact your Benchmarq sales office about non-standard requirements or to place an order. Sales offices are listed at the end of this data book.



Data Sheet Types

Product information data sheets progress in detail as the product goes from design to full production.

The three types of data sheets are defined below.

- Advance Information: Benchmarq Advance Information data sheets provide information for early product planning. These data sheets describe a product in the design or development stage. Specifications may change in any manner.
- Preliminary: Benchmarq Preliminary data sheets provide preliminary specifications for product design. They describe a product through its early production stage. Supplementary data may be published at a later date.
- Final: Benchmarq data sheets not labeled Advance Information or Preliminary are considered Final. They describe a product in full production and provide specifications for product design.

Benchmarq reserves the right to make changes to any products without notice.

Engineering Prototype

Prior to full production, Benchmarq may provide limited quantities of Engineering Prototypes. Engineering Prototypes are suitably tested for evaluation and restricted use. Any necessary errata data accompanies engineering prototype parts. They are marked with the part number and are identified as Engineering Prototypes.

Electrostatic Discharge (ESD) and Integrated Circuit (IC) Handling

Benchmarq ICs, as all ICs, are sensitive to electrostatic discharge (ESD). Although Benchmarq ICs are designed to withstand high ESD voltages, improper handling may cause damage. Standard ESD-prevention handling procedures should be followed. ESD-prevention considerations include proper grounding of operators, work surfaces and chip-handling equipment; appropriately high relative humidity levels; and use of antistatic handling and packaging materials. The ICs should be stored and shipped in antistatic tubes. The antistatic tubes containing the ICs must be brought to the same potential as the work area/operator before the individual ICs are handled.

BENCHMARQ

bq2002

Fast Charge IC

Features

- Fast charge of nickel cadmium or nickel-metal hydride batteries
- Direct LED output displays charge status
- Fast charge termination by -ΔV, peak voltage detection (PVD), maximum temperature and maximum time
- Internal band-gap voltage reference
- Optional top-off charge
- Selectable pulse trickle charge rates
- Low-power mode
- 8-pin 300-mil DIP or 150-mil SOIC

General Description

The bq2002 Fast Charge IC is a low-cost CMOS battery charge controller providing reliable charge termination for both NiCd and Nii battery applications. Controlling a current-limited or constant-current supply allows the bq2002 to be the basis for a cost-effective stand-alone or system-integrated charger. The bq2002 integrates fast charge with optional top-off and pulsed trickle control in a single IC for charging one or more NiCd or NiMH battery calls.

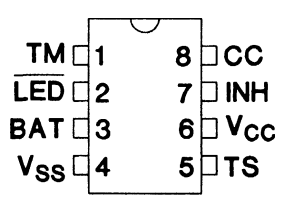
Fast charge is initiated on application of the charging supply or battery replacement. Fur safety, fast charge is inhibited if the battery temperature and voltage are outside configured limits.

Fast charge is terminated by any of the following:

- Peak voltage detection (PVD)
- Negative delta voltage (-ΔV)
- Maximum temperature
- Maximum time

After fast charge, the bq2002 optionally tope-off and pulse-trickles the battery per the pre-configured limits. Fast charge may be inhibited using the INH pin. The bq2002 may also be placed in low-standby-power mode to reduce system power consumption.

Pin Connections



8-Pin DIP or
Narrow SOIC

PN-55

Pin Names

TM	Tier mode select input	TS	Temperature sense input
$\overline{LED}$	Charging status output	Vcc	5.0V ±20% power
BAT	Battery voltage input	INH	Charge inhibit input
Vss	System ground	CC	Charge control output

Pin Descriptions

TM — **Timer mode *input***

TM is a three-level input that controls the settings for the fast charge safety timer, voltage termination mode, top-off, pulse-trickle, and voltage hold-off time.

$\overline{\text{LED}}$ — **Charging** output **status**

This open-drain output **indicates** the charging status.

BAT — Battery input **voltage**

BAT is the battery voltage sense input. This potential is generally developed by a high-impedance resistor divider network connected between the positive and negative terminals of the battery.

Vss — **System ground**

TS — Temperature **sense** input

This input is for an external battery temperature monitoring thermistor.

Vcc — **Vcc supply input**

5.0V ±20% power input.

INH — **Charge** inhibit input

When high, the **bq2002** suspends the fast charge in **progress.** When returned low, the **bq2002** resumes operation at the point where initially suspended.

CC — Charge control output

CC is an **open-drain output** that is **used** to control the charging **current** to the battery. CC switching to high impedance (Z) enables charging current to **flow,** and low to inhibit charging current. CC is modulated to **provide top-off,** if enabled, and pulse trickle.

Functional Description

Figure 1 **illustrates** the charge control status during a **bq2002** charge cycle. **Figure** 2 outlines the various **bq2002** operational states and their associated conditions, which are described in detail in the following sections.

Charge Action Control

The **bq2002** initiates a charge action by the application of power on V_{CC} or by battery replacement. Control of the charge action is then determined by inputa from TM, TS, and BAT.

Following charge initiation, the **bq2002** checks for acceptable battery voltage and temperature. If the battery voltage or temperature is **outside** of the fast charge **limits,** pulse-trickle **initiates** at a rate determined by the TM pin. If the battery temperature and voltage **are** valid at charge initiation, fast charge **begins.**

The **bq2002** then **tests** for the full-charge conditions: **-ΔV,** PVD, maximum temperature, or maximum time.

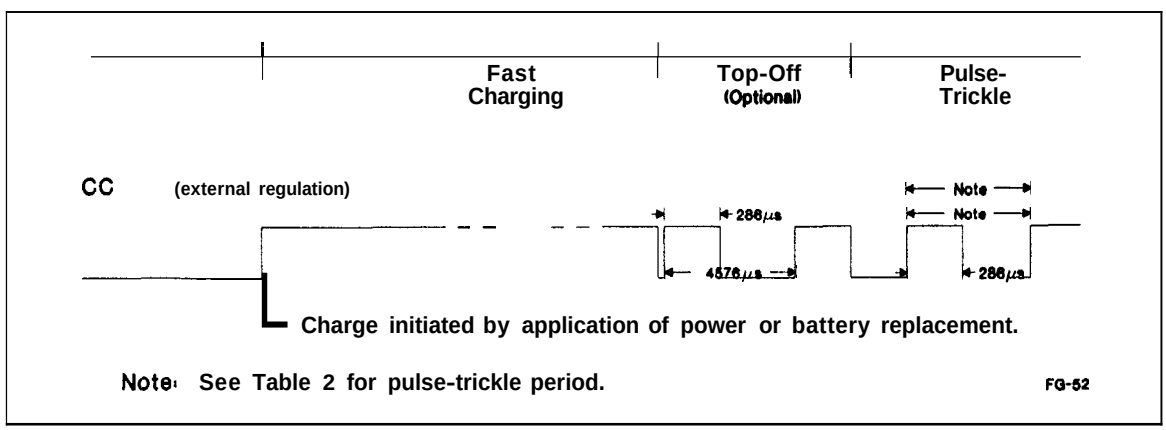


Figure 1. Example Charging Action Events

Charge Status Indication

A fast charge in progress is uniquely indicated when the LED pin goes low. The LED pin is driven to the high-Z state for all conditions other than fast charge. *Figure* 2 outlines the state of the LED pin during charge.

Battery Voltage and Temperature Measurements

Battery voltage and temperature are monitored for maximum allowable values. The voltage presented on the battery sense input, BAT, should represent a single-cell potential for the battery under charge. A resistor-divider ratio of:

$$\frac{R1}{R2} = N - 1$$

is recommended to maintain the battery voltage within the valid range, where N ie the number of cells, R1 is the resistor connected to the positive battery terminal, and R2 is the resistor connected to the negative battery terminal. See Figure 3.

Note: This reaistor-divider network input impedance to BAT should be above 200KΩ to protect the bq2002.

A ground-referenced negative temperature coefficient thermistor placed in close proximity to the battery may be used as a low-cost temperature-to-voltage transducer. The temperature sense voltage input at TS is developed using a resistor-thermistor network between Vcc and Vss. Sea Figure 3.

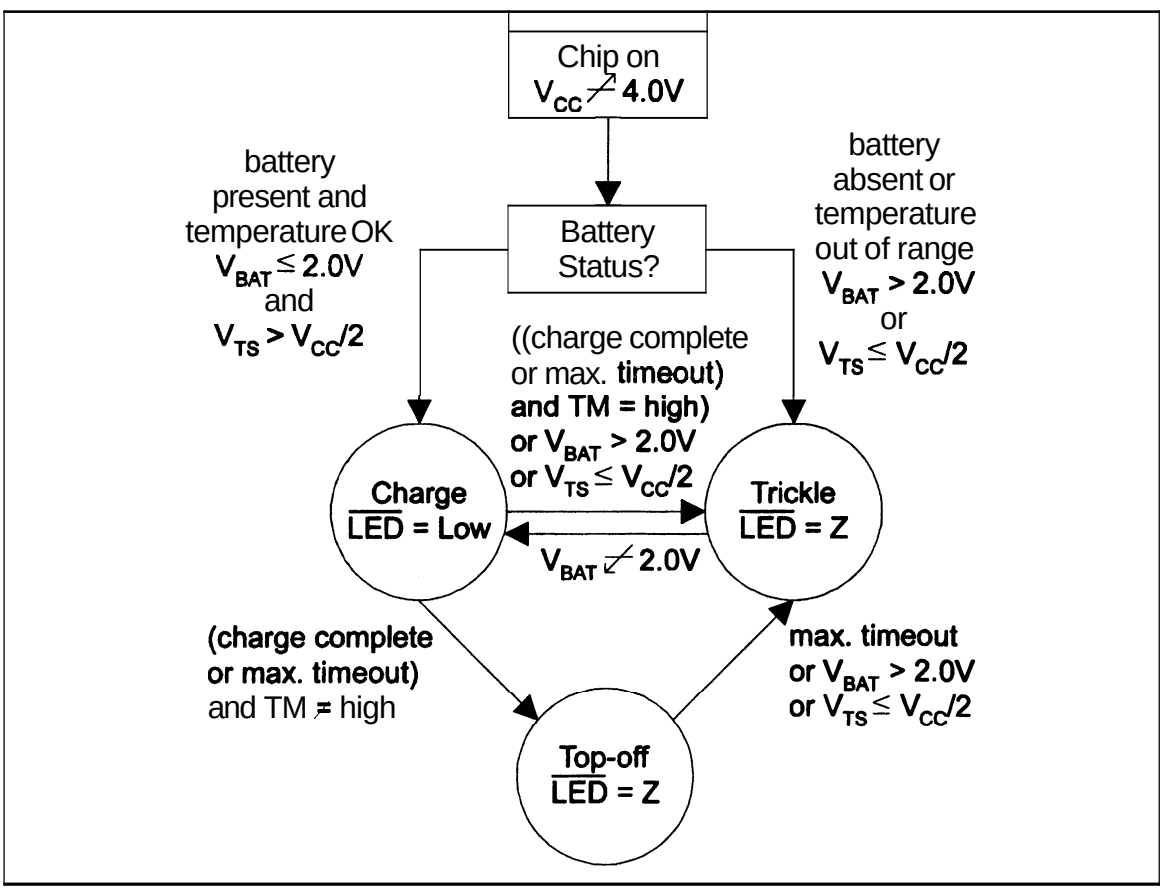


Figure 2. Operational Summary

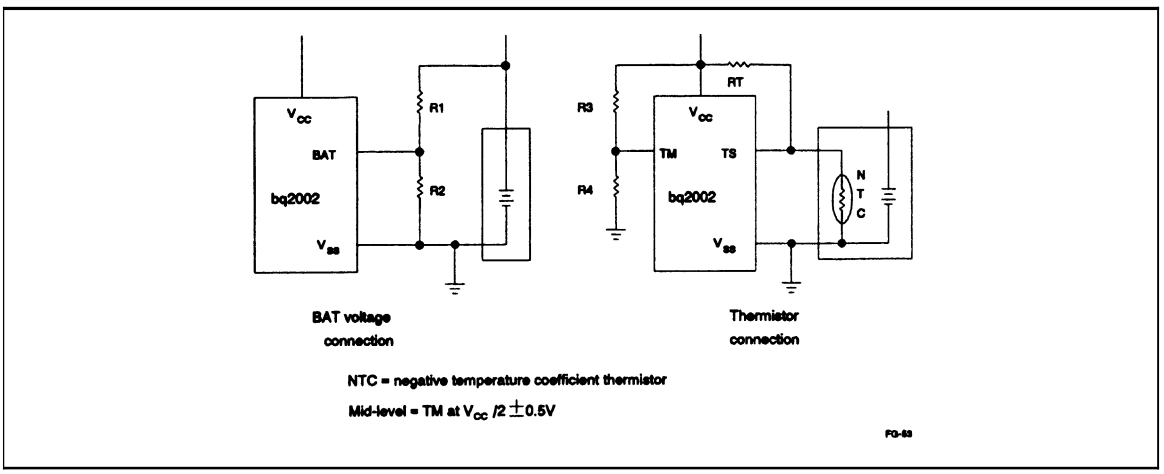


Figure 3. Voltage and Temperature Limit Measurement

TM Pin

The TM pin is a three-level pin used to select the various charge timer, top-off, voltage termination mode. trickle rates, and voltage hold-off periods. Table 1 describes the various states selected by the TM pin. The mid-level selection input is developed by a resistor divider between Vcc and ground. See Figure 3.

Charge Initiation

Application of power or battery voltage falling from above 2V initiates a charge action. If the battery is within the configured temperature and voltage limits, the bq2002 begins fast charge. The valid battery voltage range is BAT < 2V. The valid temperature range is TS > 0.5 • V_{CC}. If the battery voltage or temperature is outside of these limits, the bq2002 pulse-trickle charges until the next valid charge initiation.

The bq2002 continues to fast charge the battery until termination by one or more of the four possible termination conditions:

- Peak voltage detection (PVD)
- Negative delta voltage (-ΔV)
- Maximum time
- Maximum temperature (TCO)

V_{BAT} > V_{MCV} stops fast charge or top-off.

Voltage Termination Hold-off

A hold-off time occurs at the start of fast charging. During the hold-off time, the PVD and -AV terminations are disabled (see Table 1). Once past the initial fast charge hold-off time, the PVD and -AV terminations are re-enabled. Maximum temperature is not affected by the hold-off period.

PVD and -AV Termination

The bq2002 has two modes for voltage termination depending on the state of TM. For standard -ΔV (TM = high), if V_{BAT} is lower than any previously measured value by 12mV typical, the fast charge phase of the charge action is terminated. For PVD termination (TM = low or mid), a threshold of 0 to 5mV typical is used. The PVD and -ΔV tests are valid for: 1V < BAT < 2V.

Maximum Time and Temperature

The bq2002 also terminates fast charge for maximum temperature (TCO) and maximum time. TCO reference levels provide the maximum limits for battery temperature during fast charge. If this limit is exceeded, then fast charge or optional top-off charge is terminated.

Maximum time selection is programmed using the TM pin. Time settings are available for corresponding charge rates of C/2, 1C, and 2C.

Top-off Charge

An optional top-off charge phaee is selected to follow fast charge termination for 1C and C/2 rates. This may be necessary to accommodate battery chemistries that have a tendency to terminate charge prior to achieving full capacity. With top-off enabled, charging continues after fast charge termination for a period of time selected by the TM pin (see Table 1). During top-off, the CC pin is modulated at a duty cycle of 286µs active for every 4290µs inactive. This results in an average rate 1/16th that of the fast charge rate. Maximum time and temperature (TCO) terminations are the only methods enabled during top-off.

Pulse-Trickle Charge

Pulse-trickle is ueed to compensate for self-diecharge while the battery is idle in the charger. The battery is pula-trickle charged after fast charge or top off by driving the CC pin active for a period of 286µs for every 18.0ms of inactivity for 1C and 2C selections, and 286µs for every 8.86ms of inactivity for C/2 selection This results in a trickle rate of C/64 for the top-off enabled mode and C/32 otherwise.

Charge Inhibit

Fast charge and top-off may be inhibited by using the INH pin of the bq2002. When high, the bq2002 suspends all fast charge and top-off activity and the internal charge timer control. INH freezes the current state of LED until inhibit is removed. Temperature detection h not *affected* by the INH pin. During charge inhibit, the bq2002 continues to pulse-trickle *charge* the battery per the TM eelection When INH returns low, charge control and the charge timer resume from the point where INH went active.

Low-Power Mode

When BAT is driven above V_{PD}, the bq2002 assumes a low-power operational etate. Both the CC pin and the LED pin are driven to the high-Z etate. The operating current of the bq2002 is reduced to less than 1µA in this mode. Subsequently, when BAT returns to a value below V_{PFD}, trickle *charge* is initiated.

Table 1. Fast Charge Safety Time/Hold-Off/Top-Off Table

Corresponding Fast Charge Rate	TM	Termination	Fad Charge Top-off and Safety Time (minutes)	PVD and -AV Hold-Off Time (seconds)	Top-Off Rate	Pulse-Trickle Rate	Pulsed Trickle Period (ma)
			Typical	Typical			
C/2	Mid	PVD	160	600	C/32	C/64	9.14
1C	Low	PVD	80	300	C/16	C/64	18.3
2C	High	-AV	40	150	Disabled	C/32	18.3

Notes: $T_A = 25°C$, $V_{CC} = 5.0V$.

Mid = 0.5 • V_{CC}.

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	V_{CC} relative to V_{SS}	-0.3	+7.0	V	
V_T	DC voltage applied on any pin excluding Vcc relative to Vss	-0.3	+7.0	V	
T_{OPR}	Operating ambient temperature	0	+70	°C	Commercial
T_{STG}	Storage temperature	-40	+85	°C	
T_{SOLDER}	Soldering temperature		+260	°C	10 sec max.
T_{BIAS}	Temperature under bias	-40	+85	°C	

Note: Permanent device damage may occur if **Absolute Maximum Ratings are** exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may *affect* device reliability.

DC Thresholds (T_A = 0 to 70°C; V_{CC} ±20%)

Symbd	Parameter	Rating	Tderance	Unit	Notes
V_{TCO}	Temperature cutoff	0.5 • V_{CC}	±5%	V	$V_{TS} \leq V_{TCO}$ inhibits charge
V_{MCV}	Maximum cell voltage	2	±5%	V	$V_{BAT} > V_{MCV}$ inhibits/terminates charge

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Condition	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.0	15.0	6.0	V	
V_{DET}	-ΔV, PVD detect voltage	1	-	2	V	
V_{BAT}	Battery input	0		V_{CC}	V	
V_{TS}	Thermistor input	0.5		V_{CC}	V	TS < 0.5V prohibited
V_{IH}	Logic input high	0.5			V	INH
	Logic input high	V_{CC} - 0.5			V	TM
V_{IM}	Logic input mid	$\frac{V_{CC}}{2}$ - 500mV	-	$\frac{V_{CC}}{2}$ + 500mV	V	TM
V_{IL}	Logic input low			0.1	V	INH
	Logic input low		-	0.5	V	TM
V_{OL}	Logic output low	-	-	0.8	V	$\overline{LED}$, CC, I_{OL} = 10mA
V_{PD}	Power down	V_{CC} - 1.5		V_{CC} - 0.5		$V_{BAT} \geq V_{PD}$ max. powers down bq2002; $V_{BAT} < V_{PD}$ min. = normal operation.
I_{CC}	supply current	-	-	250	µA	Outputs unloaded, V_{CC} = 5.1V
I_{SB}	Standby current			1	µA	V_{CC} = 5.1V, V_{BAT} = V_{PD}
I_{OL}	$\overline{LED}$, CC sink	10			mA	@V_{OL} = V_{SS} + 0.8V
I_L	Input eakage			±1	µA	INH, CC. V = V_{SS} to V_{CC}
I_{OZ}	Output leakage in high-Z state	-5	-	-	µA	$\overline{LED}$, CC

Note: All voltages relative to V_{SS}.

Impedance

Symbol	Parameter	Minimum	Typical	Maximum	Unit
R_{BAT}	Battery input impedance	50			MR
R_{TS}	TS input impedance	50			MΩ

Timing (TA = 0 to +70°C; VCC ±10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
d_{FCV}	Fast charge safety time variation	0.80	1.0	1.20		

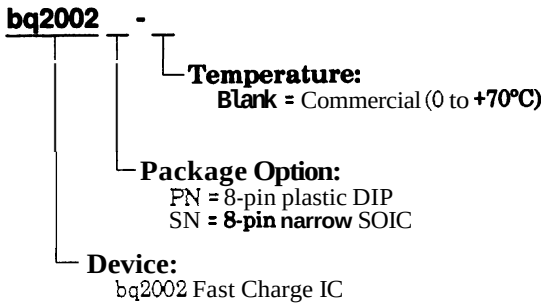
Note: Typical is at T_A = 25°C, V_{CC} = 5.0V.

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	3	Was: Table 1 gave the bq2002 Operational Summary. Is: Figure 2 gives the bq2002 Operational Summary.	Changed table to figure.
1	5	Added Termination column to table and Top-off values.	Added column and values.

Note: Change 1 = Sept. 1996 B changes from July 1994.

Ordering Information



bq2002C

Fast Charge IC

1

Features

- Fast charge of nickel cadmium or nickel-metal hydride batteries
- Direct LED output displays charge statue
- Fast charge termination by -ΔV, peak voltage detection (PVD), maximum temperature, and maximum time
- Selectable pulse trickle charge rates
- Low-power mode
- &pin 300-mil DIP or 150-mil SOIC

General Description

The bq2002C Fast Charge IC is a low-cost CMOS battery charge controller providing reliable charge termination for both NiCd and NiMH battery applications. Controlling a current-limited or constant-current supply allows the bq2002C to be the basis for a cost-effective stand-alone or system-integrated charger. The bq2002C integrates fast charge with pulsed trickle control in a single IC for charging one or more NiCd or NiMH battery.

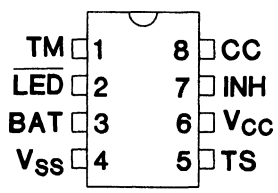
Fast charge is initiated on application of the charging supply or battery replacement. For safety, fast charge is inhibited if the battery temperature and voltage are outside configured limits.

Fast charge is terminated by any of the following:

- Peak voltage detection (PVD)
- Negative delta voltage (-ΔV)
- Maximum temperature
- Maximum time

After fast charge, the bq2002C pulse-trickle charges the battery according to the pre-configured limits. Fast charge may be inhibited using the INH pin. The bq2002C may also be placed in low-standby-power mode to reduce system power consumption.

Pin Connections



8-Pin DIP or
Narrow SOIC

PN-55

Pin Names

TM	Timer mode select input	TS	Temperature sense input
$\overline{LED}$	Charging status output	V_{CC}	5.0V ±20% power
BAT	Battery voltage input	INH	Charge inhibit input
V_{SS}	System ground	CC	Charge control output

Pin Descriptions

TM **Timer mode input**

TM is a three-level input that controls the settings for the fast charge safety timer, voltage termination mode, pulse trickle, and voltage hold-off time.

$\overline{LED}$ **Charging output status**

This open-drain output indicates the charging status.

BAT **Battery input voltage**

BAT is the battery voltage sense input. This potential is generally developed by a high-impedance resistor divider network connected between the positive and negative terminals of the battery.

V_{SS} **System ground**

TS **Temperature sense input**

This input is for an external battery temperature monitoring thermistor.

V_{CC} **V_{CC} supply input**

5.0V ±20% power input.

INH **Charge inhibit input**

When high, the bq2002C suspends the fast charge in progress. When returned low, the bq2002C resumes operation at the point where initially suspended.

CC **Charge control output**

CC is an open-drain output that is used to control the charging current to the battery. CC switching to high impedance (Z) enables charging current to flow, and low to inhibit charging current. CC is modulated to provide pulse trickle.

Functional Description

Figure 1 illustrates the charge control statue during a bq2002C charge cycle. Table 1 outlines the various bq2002C operational states and their associated conditions, which are described in detail in the following sections.

Charge Action Control

The bq2002C initiates a charge action by the application of power on V_{CC} or by battery replacement. Control of the charge action is then determined by the inputs from TM, TS, and BAT.

Following charge initiation, the bq2002C checks for acceptable battery voltage and temperature. If the battery voltage or temperature is outside of the fast charge limits (charge pending), pulse-trickle initiates at a rate determined by the TM pin. If the battery temperature and voltage *are* valid at charge initiation, fast charge begins.

The bq2002C then tests for the full-charge conditions: -ΔV, PVD, maximum temperature, or maximum time.

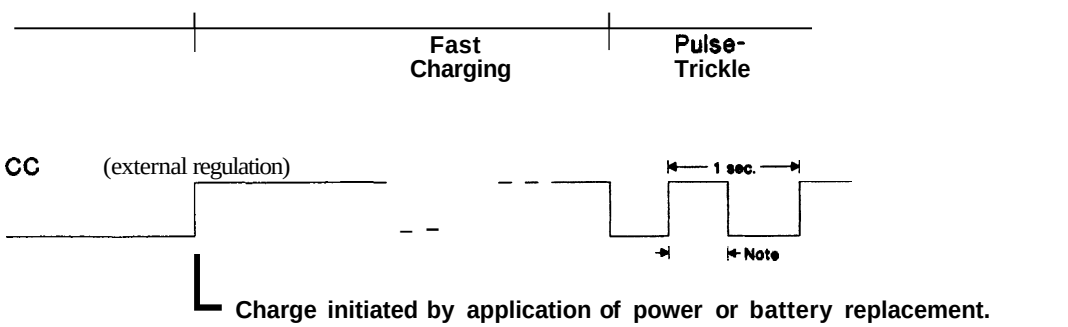


Figure 1. Example Charging Action Events

Charge Status Indication

A fast charge in progress is uniquely indicated when the LED pin goes low. The LED pin is driven low for 500msec, then high-Z for 500msec during the charge pending state. The LED pin is driven to the high-Z state for charge complete. Table 1 outlines the state of the LED pin during charge.

Battery Voltage and Temperature Measurements

Battery voltage and temperature are monitored for maximum allowable values. The voltage presented on the battery sense input, BAT, should represent a single-cell potential for the battery under charge. A resistor-divider ratio of:

$$\frac{R1}{R2} = N - 1$$

is recommended to maintain the battery voltage within the valid range, where N is the number of cells, R1 is the resistor connected to the positive battery terminal, and R2 is the resistor connected to the negative battery terminal. See Figure 2.

Note: This resistor-divider network input impedance to BAT should be above 200KΩ to protect the bq2002C.

A ground-referenced negative temperature coefficient thermistor placed in close proximity to the battery may be used as a low-cost temperature-to-voltage transducer. The temperature sense voltage input at TS is developed using a reahtor-thermistor network between V_{CC} and V_{SS}. See Figure 2.

Table 1. bq2002C Operational Summary

Charge Action State	Conditions	CC Output	$\overline{LED}$
Battery absent	$V_{BAT} \geq V_{MCV}$	Trickle charge activated for period specified in Table 2	High Z
Charge initiation	V_{CC} applied, V_{BAT} drops from 2 V_{MCV} to < V_{MCV} (battery replaced)	–	–
Charge pending	$V_{TS} < V_{TCO}$ or $V_{BAT} < V_{LBAT}$	Trickle charge activated for period specified in Table 2	500ms low 500ms high-Z
Fast charging	Charge initiation occurred and $V_{TS} > V_{TCO}$ and $V_{LBAT} < V_{BAT} < V_{MCV}$	High Z	Low
Charge complete	-ΔV or PVD or maximum time or maximum temperature'	–	High Z
Trickle	Charge complete or Charge Pend	Trickle charge activated for period specified in Table 2	–
Charge inhibit	INH high	Trickle charge activated for period specified in Table 2	–[2]
Low power	$V_{BAT} > V_{PD}$	High Z	High Z

Notes: 1. $V_{BAT} > V_{MCV}$ stops fast charge.
2. LED reflects state prior to inhibit.

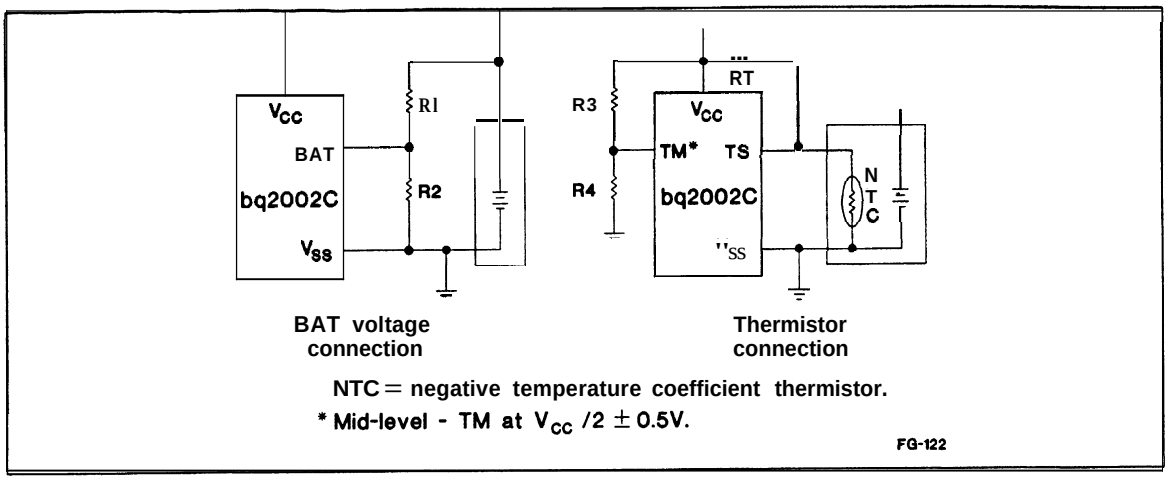


Figure 2. Voltage and Temperature Limit Measurement

TM Pin

The TM pin is a three-level pin used to select the various charge timer, voltage termination mode, trickle rates and voltage hold-off periods. Table 2 describes the various states selected by the TM pin. The mid-level selection input is developed by a resistor divider between Vcc and ground. See Figure 2.

Charge Initiation

Application of power or battery voltage falling from above 2V initiates a charge action. If the battery is within the configured temperature and voltage limits, the bq2002C begins fast charge. The valid battery voltage range is V_{LBAT} < BAT < 2V. The valid temperature range is TS > 0.5 • V_{CC}. If the battery voltage or temperature is outside of these limits, the bq2002C pulse-trickle charges until the temperature and voltage are within specified limits.

The bq2002C continues to fast charge the battery until termination by one or more of the four possible termination conditions:

- Peak voltage detection (PVD)
- Negative delta voltage (-AV)
- Maximum time
- Maximum temperature (TCO)

V_{BAT} > V_{MCV} stops fast charge.

Voltage Termination Hold-off

A hold-off time occurs at the start of fast charging. Duriig the hold-off time, the PVD and -AV terminations are disabled (see Table 2). Once past the initial fast charge hold-off time, the PVD and -AV terminations are re-enabled. Maximum temperature is not affected by the hold-off period.

PVD and -ΔV Termination

The bq2002C has two modes for voltage termination depending on the state of TM. For standard -AV (TM = high), if V_{BAT} is lower than any previously measured value by 12mV typical, the fast charge phase of the charge action is terminated. For PVD termination (TM = low or mid), a threshold of 0 to 5mV typical is used. The PVD and -AV tests are valid for: 1V < BAT < 2V.

Maximum Time and Temperature

The bq2002C also terminates fast charge for maximum temperature (TCO) and maximum time. TCO reference levels provide the maximum limits for battery temperature during fast charge. If this limit is exceeded, then fast charge is terminated.

Maximum time selection is programmed using the TM pin. Time settings are available for corresponding charge rates of C/2, 1C, and 2C.

Top-Off Charge

A .optional top-off charge phase is selected to follow fast charge termination for 1C and C/2 rates. This may be necessary to accommodate battery chemistries that have a tendency to terminate charge prior to achieving full capacity. With top-off enabled, charging continues after fast charge termination for a period of time selected by the TM pin (see Table 2). During top-off, the CC pin is modulated at a duty cycle of 73ms active for every 1097ms inactive. This results in an average rate 1/16th that of the fast charge rate. Maximum time and temperature (TCO) terminatione are the onlv methods enabled during top-off.

Pulse-Trickle Charge

Pulse-trickle is used to compensate for self-discharge while the battery is idle in the charger. The battery is pulse–trickle charged after fast charge by driving the CC pin active for a period specified in Table 2. This results in a trickle rate of C/32 for all modes.

Charge Inhibit

An input stimulus can be applied to the INH input pin to synchronize the voltage sampling at the BAT input pin, providing design/application flexibility. A low-high-low pulse can be applied to this input to synchronize sampling on the falling edge, if the input pulse width is greater than 100ns but less than 3.5ms (synchronized charge termination). Time between these input pulses must be less than the synchronized period specified in Table 2, or the bq2002C enables 'free-run' voltage-based detection (automatic charge termination). If the INH input remains high for greater than 12ms, the bq2002C resets the voltage-baaed history used for PVD or -AV detection. This condition (pause) also suspends the charge timer and fast charge or top-off activity until the INH pin returns low. A pause condition must precede a transition from automatic charge termination to synchronized charge termination.

Low-Power Mode

When BAT is driven above V_{PD}, the bq2002C assumes a low-power operational state. Both the CC pin and the LED pin are driven to the high-Z state. The operating current of the bq2002C is reduced to less than 1µA in this mode. Subsequently, when BAT returns to a value below V_{PFD}, trickle charge is initiated.

Table 2. Fast Charge Safety Time/Hold-Off Table

Corresponding Fast Charge Rate	TM	Fast Charge and Safety Time (minutes)	PVD and -ΔV Hold-Off Time (seconds)	Pulse-Trickle Rate	Pulse Trickle Period (seconds)	Pulse-Trkkk Pulse Width (ms)	Synchronized Period (seconds)
		Typical	Typical				
C/2	Mid	160	300	C/32	1	62	9.4
1C	Low	80	150	C/32	1	31	18.7
2C	High	40	75	C/32	1	15	18.7

Notes: T_A = 25°C, V_{CC} = 5.0V.

Mid = 0.5 • Vcc.

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Vcc relative to Vss	-0.3	+7.0	V	
V_T	DC voltage applied on any pin excluding Vcc relative to Vss	-0.3	+7.0	V	
T_{OPR}	Operating ambient temperature	0	+70	°C	Commercial
T_{STG}	Storage temperature	-40	+85	°C	
T_{SOLDER}	Soldering temperature		+260	°C	10 sec max.
T_{BIAS}	Temperature under bias	-40	+85	°C	

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds (T_A = 0 to 70°C; VCC ±20%)

Symbol	Parameter	Rating	Tolerance	Unit	Notes
V_{TCO}	Temperature cutoff	0.5 • Vcc	±5%	V	$V_{TS} \le V_{TCO}$ inhibits charge
V_{MCV}	Maximum cell voltage	2	±5%	V	$V_{BAT} > V_{MCV}$ inhibits/terminates charge
V_{LBAT}	Minimum cell voltage	0.84	±20%	V	$V_{BAT} < V_{LBAT}$ pends charge

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Condition	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.0	5.0	6.0	V	
V_{DET}	-ΔV, PVD detect voltage	1		2	V	
V_{BAT}	Battery input	0		V_{CC}	V	
V_{TS}	Thermistor input	0.5		V_{CC}	V	TS < 0.5V prohibited
V_{IH}	Logic input high	0.5			V	INH
	Logic input high	V_{CC} - 0.5			V	TM
V_{IM}	Logic input mid	$\frac{V_{CC}}{2}$ - 500mV		$\frac{V_{CC}}{2}$ + 500mV	V	TM
V_{IL}	Logic input low			0.1	V	INH
	Logic input low			0.5	V	TM
V_{OL}	Logic output low			0.8	V	$\overline{LED}$, CC, I_{OL} = 10mA
V_{PD}	Power down	V_{CC} - 1.5		Vcc - 0.5	V	$V_{BAT} \geq V_{PD}$ max. powers down bq2002C; $V_{BAT} < V_{PD}$ min. = normal operation.
I_{CC}	Supply current			500	µA	Outputs unloaded, V_{CC} = 5.1V
I_{SB}	Standby current			1	µA	V_{CC} = 5.1V, V_{BAT} = V_{PD}
I_{OL}	$\overline{LED}$, CC sink	10			mA	@V_{OL} = V_{SS} + 0.8V
I_L	Input leakage			±1	µA	INH, CC, V = V_{SS} to V_{CC}
I_{OZ}	Output leakage in high-Z state	-5			µA	$\overline{LED}$, CC

Note: All voltages relative to Vss.

Impedance

Symbol	Parameter	Minimum	Typical	Maximum	Unit
R_{BAT}	Battery input impedance	*50*			MR
R_{TS}	TS input impedance	50			MR

Timing (T_A = 0 to +70°C; V_{CC} ±10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
d_{FCV}	Fast charge safety time variation	0.88	1.0	1.12		

Note: Typical is at T_A = 25°C, V_{CC} = 5.0V.

Ordering Information

bq2002C -

Temperature:
Blank = Commercial (0 to +70°C)

Package Option:
PN = 8-pin plastic DIP
SN = 8-pin narrow SOIC

Device:
bq2002C Fast Charge IC

bq2002T

Fast Charge IC With ΔT/Δt

Features

- Fast charge of nickel cadmium or nickel-metal hydride batteries
- Direct LED output displays charge status
- Fast charge termination by Δ temperature/Δ time, maximum temperature, and maximum time
- Optional top-off charge
- Selectable pulse-trickle charge rates
- Low-power mode
- 8-pin 300-mil DIP or 150-mil SOIC

General Description

The bq2002T Fast Charge IC is a low-cost CMOS battery charge controller providing reliable charge termination for both NiCd and NiMH battery applications. Controlling a current-limited or constant-current supply allows the bq2002T to be the basis for a cost-effective stand-alone or system-integrated charger. The bq2002T integrates fast charge with optional top-off and pulsed trickle control in a single IC for charging one or more NiCd or NiMH cells.

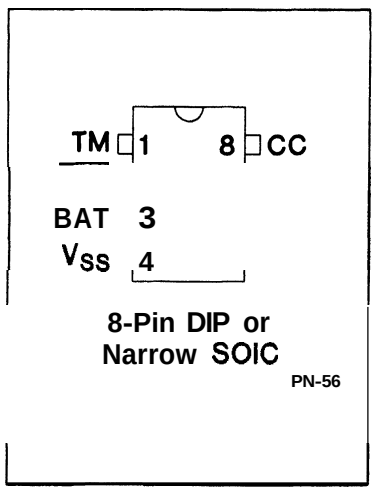
Fast charge is initiated on application of the charging supply or battery replacement. For safety, fast charge is inhibited if the battery temperature and voltage are outside configured limits.

Fast charge is terminated by any of the following:

- Delta temperature/delta time (ΔT/Δt)
- Maximum temperature
- Maximum time

After fast charge, the bq2002T optionally tops-off and pulse-trickle the battery per the pre-configured limits. Fast charge may be inhibited using the INH pin. The bq2002T may also be placed in low-standby-power mode to reduce system power consumption.

Pin Connections



Pin Names

TM	Timer mode select input	TS	Temperature sense input
$\overline{LED}$	Charging status output	Vcc	5.0V ±20% power
BAT	Battery voltage input	INH	Charge inhibit input
Vss	System ground	CC	Charge control output

Pin Descriptions

TM **Timer mode input**

TM is a three-level input that controls the settings for the fast charge safety timer, top-off, and pulse-trickle.

$\overline{LED}$ **Charging output status**

This open-drain output indicates the charging status.

BAT **Battery input voltage**

BAT is the battery voltage sense input. This potential is generally developed by a high-impedance resistor divider network connected between the positive and negative terminals of the battery.

V_{SS} **System ground**

TS **Temperature sense input**

This input is for an external battery temperature monitoring negative temperature coefficient (NTC) thermistor.

V_{CC} **V_{CC} supply input**

5.0V ±20% power input.

INH **Charge inhibit Input**

When high, the bq2002T suspends the fast charge in progress. When returned low, the bq2002T resumes operation at the point where initially suspended.

CC **Charge control output**

CC is an open-drain output that is used to control the charging current to the battery. CC switching to high impedance (Z) enables charging current to flow, and low to inhibit charging current. CC is modulated to provide top-off, if enabled, and pulse-trickle.

Functional Description

Figure 1 illustrates the charge control status during a bq2002T charge cycle. Figure 2 outlines the various bq2002T operational states and their associated conditions, which are described in detail in the following sections.

Charge Action Control

The bq2002T initiates a charge action by the application of power on V_{CC} or by battery replacement. Control of the charge action is then determined by inputs from TM, TS, and BAT.

Following charge initiation, the bq2002T checks for acceptable battery voltage and temperature. If the battery voltage or temperature is outside of the fast charge limits, pulse-trickle initiates at a rate determined by the TM pin. If the battery temperature and voltage are valid at charge initiation, fast charge begins.

The bq2002T then tests for the full-charge conditions: $\Delta T/\Delta t$, maximum temperature, or maximum time.

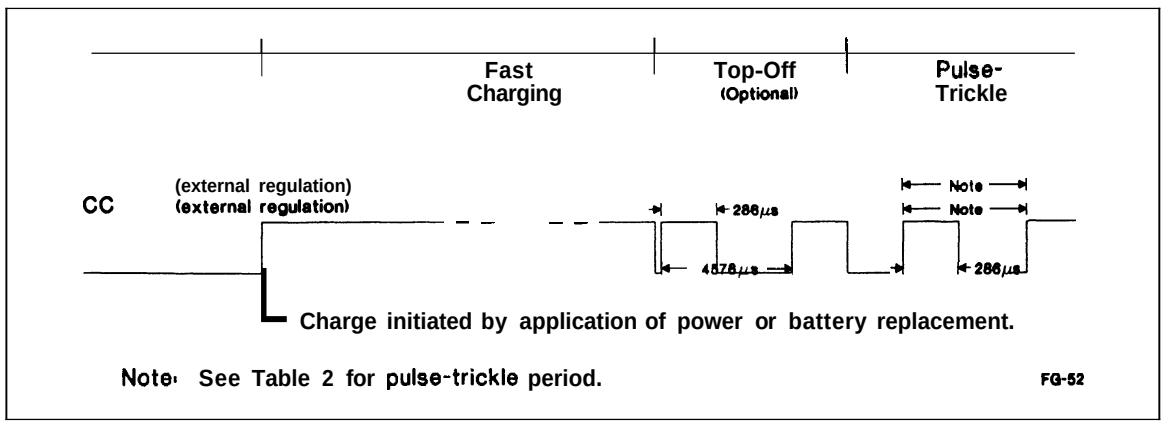


Figure 1. Example Charging Action Events

Charge Status Indication

A fast charge in progress is uniquely indicated when the $\overline{LED}$ pin goes low. The $\overline{LED}$ pin is driven to the high-Z state for all conditione other than fast charge pend. inhibit, or fast charge. Figure 2 outlines the state of the $\overline{LED}$ pin during a charge cycle.

Battery Voltage and Temperature Measurements

Battery voltage and temperature are monitored for maximum allowable values. The voltage presented on the battery sense input, BAT, should represent a single-cell potential for the battery under charge. A resistor-divider ratio of:

$$\frac{R1}{R2} = N - 1$$

is recommended to maintain the battery voltage within the valid range, where N is the number of cells, R1 is the resistor connected to the positive battery terminal, and R2 is the resistor connected to the negative battery terminal. *See* Figure 3.

Note: This resistor-divider network input impedance to BAT should be above 200KΩ to protect the bq2002T.

A ground-referenced negative temperature coefficient thermistor placed in close proximity to the battery should be used as a low-cost temperature-to-voltage transducer. The temperature senee voltage input at TS is developed using a resistor-thermistor network between Vcc and Vss. *See* Figure 3.

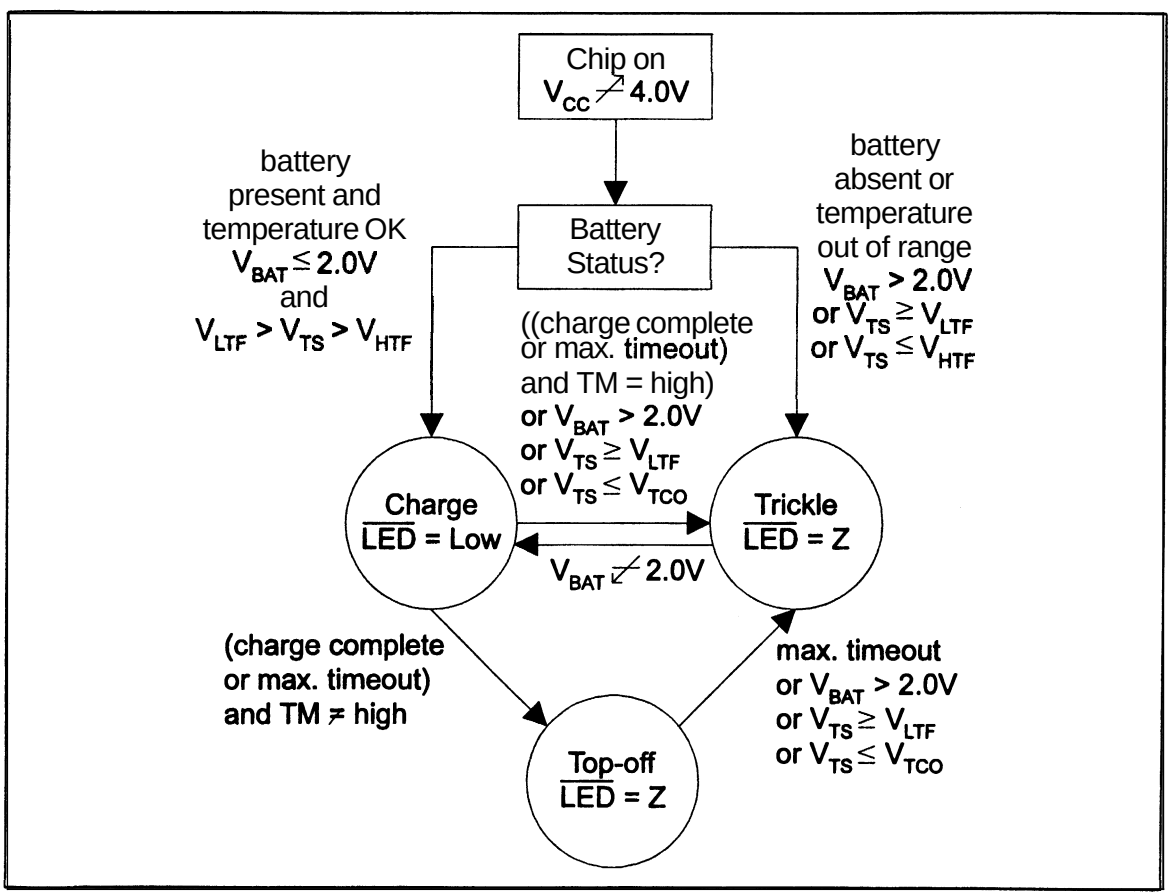


Figure 2. Operational Summary

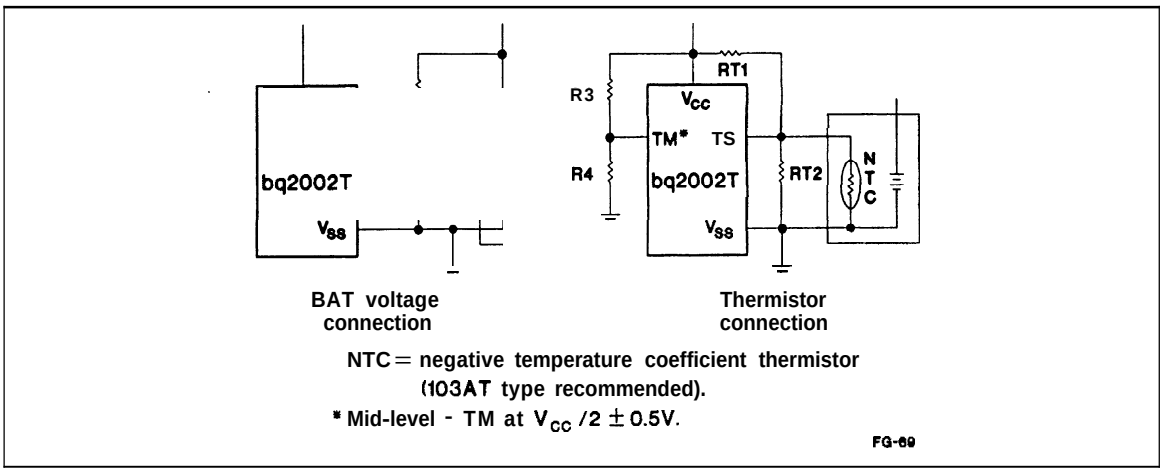


Figure 3. Voltage and Temperature Limit Measurement

TM Pin

The TM pin is a three-level pin used to select the various charge timer, top-off, voltage termination mode, trickle rates, and voltage hold-off periods. Table 1 describes the various states selected by the TM pin. The mid-level selection input is developed by a resistor divider between Vcc and ground. See Figure 3.

Charge Initiation

Application of power or battery voltage falling from above 2V initiates a charge action. If the battery is within the configured temperature and voltage limits, the bq2002T begins fast charge. The valid battery voltage range is BAT < 2V. The valid temperature range is between the internal low-temperature fault reference (V_{LTF} = 0.4 • Vcc) and the external hot-temperature fault reference (V_{HTF} = 0.25 • Vcc). If the battery voltage or temperature is outside of these limits, the bq2002T pulse-trickle charges until the battery enters the valid charge range. The hot-temperature cut-off reference (V_{TCO} = 0.225 • Vcc) provides hysteresis between the maximum temperature cut-off and the valid charge temperature.

The bq2002T continues to fast charge the battery until termination by one or more of the three possible termination conditions:

- Delta temperature/delta time (ΔT/Δt)
- Maximum time
- Maximum temperature (TCO)

$V_{BAT} > V_{MCV}$ stops fast charge or top-off.

ΔT/Δt Fast Charge Termination

The bq2002T uses ΔT/Δt fast charge termination. The bq2002T makes a termination decision based on delta temperature/delta time (ΔT/Δt) every 19 seconds typical. If V_{TEMP} is 25.6mV (typical) less than the voltage measured 60 seconds previously, the fast charge phase of the charge is terminated.

The ΔT/Δt test is valid only for:

$$0.225 \cdot Vcc \leq V_{TEMP} \leq 0.4 \cdot Vcc$$

Using the recommended resistor divider network and thermistor, this represents a detection threshold of 1°C/minute typical at 30°C. The valid charge temperature range corresponds to 10°C (LTF), 43°C (HTF), and 50°C (TCO), respectively.

Maximum Time and Temperature

The bq2002T also terminates fast charge for maximum temperature (TCO) and maximum time. TCO reference level (V_{TCO} = 0.225 • Vcc) provides the maximum limit for battery temperature during fast charge. Once fast charge is initiated, exceeding TCO terminates fast charge or optional top-off charge.

Maximum time selection is programmed using the TM pin. Time settings are available for corresponding charge rates of C/4, 1C, and 2C.

Top-off Charge

An optional top-off charge phase is selected to follow fast charge termination for 1C and C/4 rates. This may be necessary to accommodate battery chemistries that have a tendency to terminate charge prior to achieving full capacity. With top-off enabled, charging continuea after fast charge termination for a period of time selected by the TM pin (see Table 1). During top-off, the CC pin is modulated at a duty cycle of 286µs active for every 4290µs inactive. This results in an average rate 1/16th that of the fast charge rate. Maximum time and temperature (TCO) terminations are the only methods enabled during top-off,

Pulse-Trickle Charge

Pulse-trickle is used to compensate for self-discharge while the battery is idle in the charger. The battery is pulse-trickle charged after fast charge or top off by driving the CC pin active for a period of 286µs for every 72.9ms of inactivity for 1C and 2C selections, and 286µs for every 17.9ms of inactivity for C/4 selection. This results in a trickle rate of C/256 for the 1C rate and the C/4 rate, and C/128 for the 2C rate.

Charge Inhibit

Fast charge and top-off may be inhibited by using the INH pin of the bq2002T. When high, the bq2002T suspends all fast charge and top-oft activity and the internal charge timer. *Fast charge termination due to maximum temperature is not affected by the ZNH pin.* INH freezes the current state of LED until inhibit is removed. During charge inhibit, the bq2002T continues to pulse-trickle charge the battery per the TM selection. When INH returns low, charge control and the charge timer resume from the point where INH went active and the ΔT/Δt circuit is reset.

Low-Power Mode

When BAT is driven above V_{PD}, the bq2002T assumes a low-power operational state. Both the CC pin and the LED pin are driven to the high-Z state. The operating current of the bq2002T is reduced to less than 6pA in this mode. Subsequently, when BAT returns to a value below V_{PD}, trickle charge is initiated. A new charge cycle begins when BAT falls below 2V.

Table 1. Fast Charge Safety Timepop-Off Table

Corresponding Fast Charge Rate	TM	Fwt Charge Top-off and Safety Time (minutes) Typical	Top-Off Rate	Pulse-Trickle Rate	Pulse-Trickle Period (ms)
C/4	Mid	320	C/64		18.3
1C	Low	80	C/16	C/256	73.1
2C	High	40	Disabled	C/128	73.1

Notes: $T_A = 25°C$, $V_{CC} = 5.0V$.

Mid = 0.5 • Vcc.

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	V_{CC} relative to V_{SS}	-0.3	+7.0	V	
V_T	DC voltage applied on any pin excluding Vcc relative to Vss	-0.3	+7.0	V	
T_{OPR}	Operating ambient temperature	0	+70	°C	Commercial
T_{STG}	Storage temperature	-40	+85	°C	
T_{SOLDER}	Soldering temperature		+260	°C	10 sec max.
T_{BIAS}	Temperature under bias	-40	+85	°C	

Note: Permanent device damage may *occur* if Absolute Maximum Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds (T_A = 0 to 70°C; V_{CC} ±20%)

Symbd	Parameter	Rating	Tolerance	Unit	Notes
V_{TCO}	Temperature cutoff	0.225 • Vcc	±5%	V	$V_{TS} \le V_{TCO}$ inhibits charge
V_{HTF}	High-temperature fault	0.25 • Vcc	±5%	V	$V_{HTF} \le V_{TS} \le V_{LTF}$ initiates charge
V_{LTF}	Low-temperature fault	0.4 • Vcc	±5%	V	$V_{TS} > V_{LTF}$ inhibits charge
V_{MCV}	Maximum cell voltage	2	±5%	V	$V_{BAT} > V_{MCV}$ inhibits/terminates charge

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.0	5.0	6.0	V	
V_{BAT}	Battery input	0		V_{CC}	V	
V_{TS}	Thermistor input	0.5		V_{CC}	V	TS < 0.5V prohibited
V_{IH}	Logic input high	0.5			V	INH
	Logic input high	Vcc - 0.5			V	TM
V_{IM}	*Logic* input mid	$\frac{V_{CC}}{2}$ - 500mV		$\frac{V_{CC}}{2}$ + 500mV	V	TM
V_{IL}	*Logic* input low			0.1	V	INH
	Logic input low			0.5	V	TM
V_{OL}	*Logic output low*			0.8	V	$\overline{LED}$, CC, I_{OL} = 10mA
V_{PD}	Power down	Vcc - 1.5		V_{CC} - 0.5	V	$V_{BAT} \geq V_{PD}$ max. powers down bq2002T; $V_{BAT} < V_{PD}$ min. = normal operation.
I_{CC}	Supply current			500	µA	Outputs unloaded, V_{CC} = 5.1V
I_{SB}	Standby current			1	pi	V_{CC} = 5.1V, V_{BAT} = V_{PD}
I_{OL}	$\overline{LED}$, CC sink	10			mA	@V_{OL} = V_{SS} + 0.8V
I_L	Input leakage			±1	µA	INH, TM, V = V_{SS} to V_{CC}
I_{OZ}	Output leakage in high-Z state	-5			µA	$\overline{LED}$, CC

Note: All voltages relative to V_{SS}.

Impedance

Symbol	Parameter	Minimum	Typical	Maximum	Unit
R_{BAT}	Battery input impedance	50			MΩ
R_{TS}	TS input impedance	60			MΩ

Timing (TA = 0 to +70°C; VCC ±10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Note8
d_{FCV}	Fast charge safety time variation	0.80	1.0	1.20		

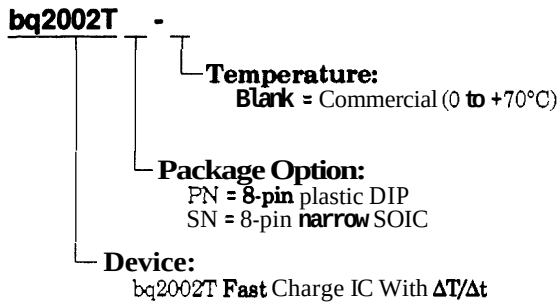
Note: Typical is at T_A = 25°C, V_{CC} = 5.0V.

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	3	Was: Table 1 gave the bq2002 Operational Summary. Is: Figure 2 gives the bq2002 Operational Summary.	Changed table to figure.
1	5	Added Top-off values.	Added values.

Note: Change 1 = Sept. 1996 B changes from Aug. 1994.

Ordering Information



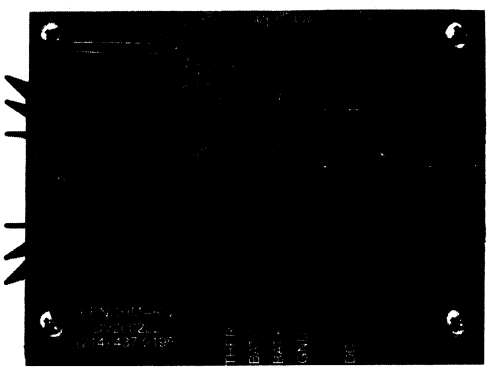
Product Brief DV2002L2/TL2

Fast Charge Development System

Control of LM317 Linear Regulator

Features

- bq2002 fast charge control evaluation and development
- Charge current sourced from an on-board linear regulator (up to 1.5 A)
- Fast charge of 4, 5, 6, 8, or 10 NiCd or NiMH cells (contact Benchmarq for other cell counts)
- Fast charge termination by negative delta voltage (-ΔV) or peak voltage detect, maximum temperature and maximum time
- -ΔV/peak voltage detect, hold-off, top-off, maximum time, and number of cells are jumper-configurable
- Inhibit fast charge by logic-level input



General Description

The DV2002L2 Development System provides a development environment for the bq2002 Fast Charge IC. The DV2002L2 incorporates a bq2002 and a linear regulator to provide fast charge control for 4 to 10 NiCd or NiMH cells.

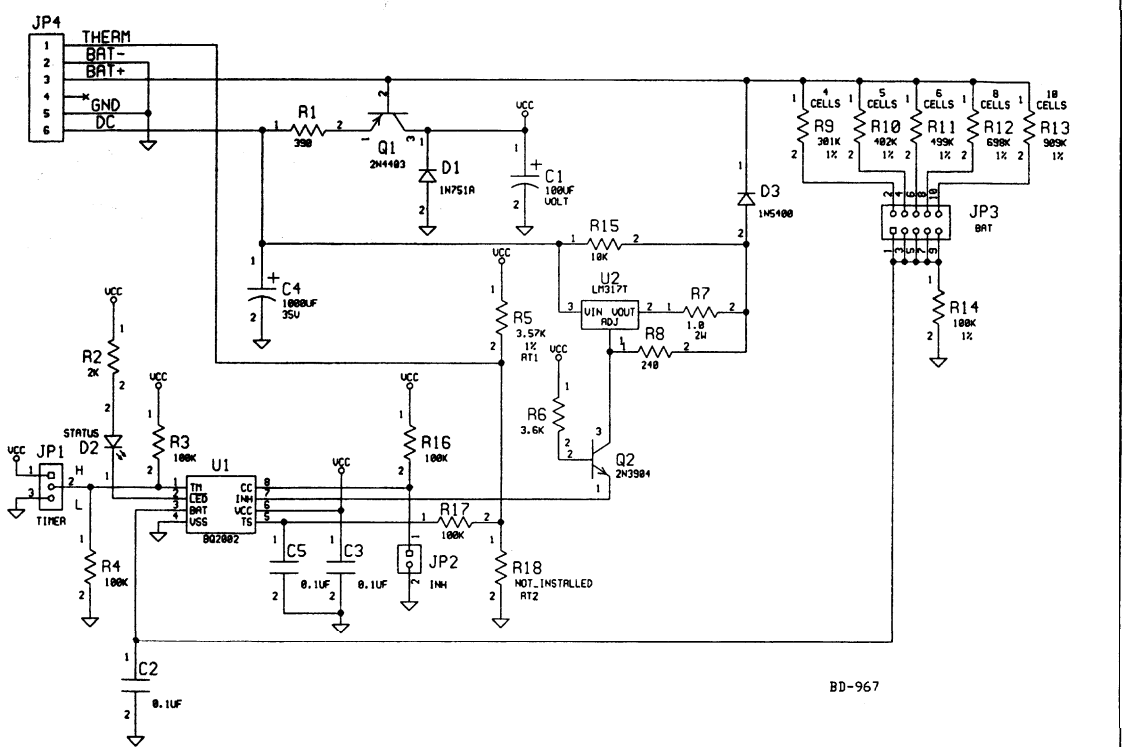
The fast charge is terminated by any of the following: -AV or peak voltage detect, maximum temperature, maximum time, and inhibit command. Jumper settings select the voltage termination mode, the hold-off, top-off, and maximum time limits.

The user provides a power supply and batteries. The user configures the DV2002L2 for the number of cells, voltage, charge termination mode, and maximum charge time (with or without top-off).

Please review the bq2002 data sheet before using the DV2002L2 board.

A full data sheet for this product is available on our web site (http://www.benchmarq.com), or you can contact the factory for one.

DV2002L2/TL2 Board Schematic



bq2003

Fast Charge IC

Features

- Fast charge and conditioning of nickel cadmium or nickel-metal hydride batteries
- Flexible current regulation:
  - Frequency-modulated switching current regulator
  - Gating control for use with external regulator
- Easily integrated into systems or as a stand-alone charger
- Pre-charge checks for temperature and voltage faults
- Direct LED outputa display battery and charge status
- Fast charge termination by A temperature/Δ time, -ΔV, maximum temperature, maximum time, and maximum voltage
- Optional top-off charge

General Description

The bq2003 Fast *Charge* IC provides comprehensive fast charge control functions together with high-speed switching power control circuitry on a monolithic CMOS device.

Flexible control of constant-current or current-limited charging eupply allows the bq2003 to be the basis of a cost-effective solution for stand-alone and system-integrated chargers for batteries of one or more cells.

Switch-activated discharge-before-charge allows bq2003-based chargers to support battery conditioning and capacity determination.

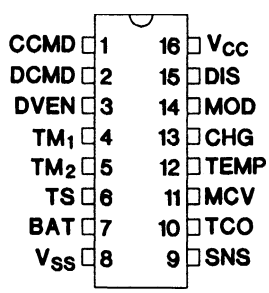
High-efficiency power conversion is accomplished using the bq2003 as a frequency-modulated controller for switched regulation of the charging current. The bq2003 may alternatively be used with a transistor or SCR to gate an external charging current.

Fast charge may begin on application of the charging supply, replacement of the battery, or switch depression. For safety, fast *charge* is inhibited until the battery temperature and voltage are within *configured* limits.

Temperature, voltage, and time are monitored throughout fast charge. Fast charge is terminated by any of the following:

- Delta temperature/delta time (ΔT/Δt)
- Negative delta voltage (-ΔV)
- Maximum temperature
- Maximum time
- Maximum voltage

Pin Connections



16-Pin DIP or SOIC

PN-31

Pin Names

CCMD	Charge command/select	SNS	Sense resistor input
DCMD	Discharge command	TCO	Temperature cutoff
DVEN	-ΔV enable/disable	MCV	Maximum voltage
TM_1	Tier mode select 1	TEMP	Temperature status output
TM_2	Tier mode select 2	CHG	Charging status output
TS	Temperature sense	MOD	Charge current control
BAT	Battery voltage	DIS	Discharge control
V_{SS}	System ground	V_{CC}	5.0V ±10% power

The bq2003 uses delta temperature/delta time (ΔT/Δt) and/or negative delta voltage (-ΔV) as primary decisions for fast charge cutoff. ΔT/Δt detection is very reliable for fast charge termination for NiCd and NiMH batteries and is compatible with varying current during charge. ΔT/Δt requires the use of a single thermistor to monitor the rate of temperature increase for contacted cells. Compared to the delta temperature method (using two sensors and comparing battery temperature to ambient temperature), the ΔT/Δt approach is relatively immune to corruption when the initial battery temperature and ambient temperature are significantly different.

-AV detection monitors the voltage across all of the cells and is very reliable as a primary charge terminator for NiCd batteries. -AV detection for the bq2003 may be disabled temporarily (for periods of time when the current fluctuates) or permanently.

To provide maximum safety for the battery and system, fast charging also terminates based on a hot-temperature cutoff threshold (TCO), a safety time period, and a maximum cell voltage threshold (MCV). To avoid possible premature fast charge termination when charging batteries after long periods of storage, the maximum voltage and -AV testa are disabled during a short "hold-off" period at the start of charge.

The bq2003 may be configured to have one, two, or three charge stages. With a two-stage fast charge configuration, the fast charge stage controlled by the bq2003 is preceded and followed by a continuous trickle charge at a rate controlled by a current-limiting resistor outside the bq2003.

With a three-stage charge configuration, the fast charge stage is followed by a "top-off" charge stage at 1/8 the fast charge rate. This allows the battery to be quickly and safely brought to a completely full charge state. Following "top-off," externally controlled trickle charge maintains the battery at a minimal charge-sustaining level (i.e., C/40 or C/50). The maximum top-off time period is the same as for the safety time period selected for fast charge, with TCO or MCV as backup terminations.

Discharge-before-charge may be switch-selected to discharge the battery to a nominal 1V per cell (V_{EDV}) and then automatically fast charge the battery. Discharge-before-charge on demand provides conditioning services (useful to correct or prevent the NiCd voltage depression, or "memory,' effect) and capacity-determining services (discharge to empty to calibrate battery capacity).

Charger status is indicated by readily distinguishable LED patterns showing:

- Charge pending
- Discharge
- Fast charge in progress
- Charge complete
- Battery removed or charge aborted

Cold or hot temperature faults are indicated by the temperature LED.

Figure 1 shows a block diagram of the bq2003 Fast Charge IC.

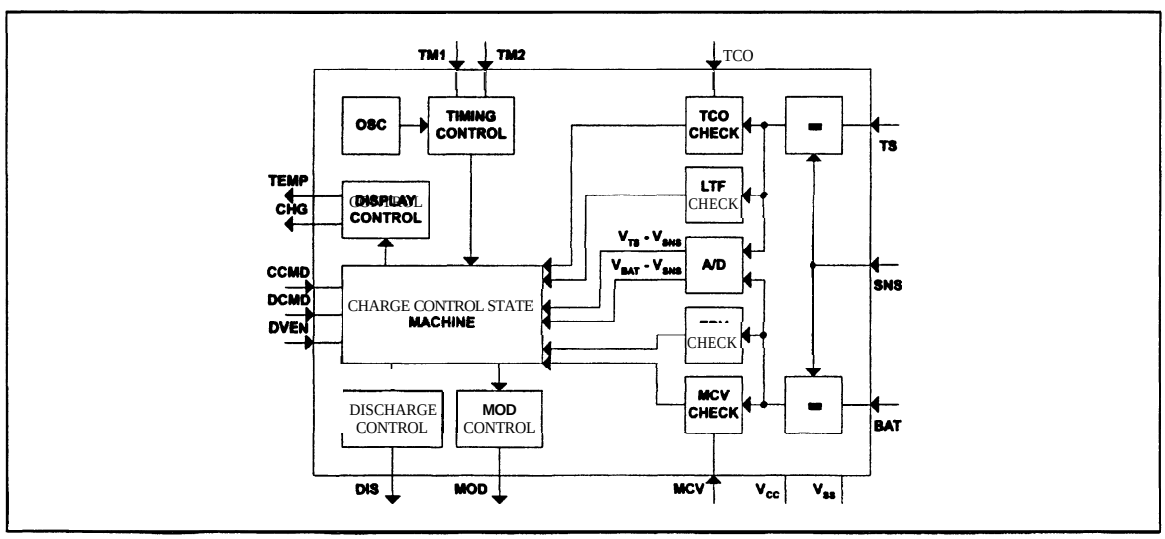


Figure 1. Block Diagram

Pin Descriptions

BAT Single-cell voltage input

Single-cell voltage referenced to SNS for the battery pack being charged. This is generally developed by a high-impedance resistor divider network connected between the positive and the negative terminals of the battery.

MCV Maximum-Cell-Voltage threshold input

Maximum single-cell voltage. If the difference in potential between BAT and SNS (pins 7 and 9) is greater than or equal to the voltage at the MCV input, then all charging activity is inhibited. (See Figure 3.)

Note: For valid device operation, the voltage level on MCV must not exceed 0.6 • Vcc.

TS Temperature sense input

Input referenced to SNS for external battery temperature monitoring thermistor. $\Delta T/\Delta t$ determination is valid only for $V_{TCO} \leq V_{TS} \leq V_{TCO} + 0.2V_{CC}$.

TCO Temperature cutoff threshold input

Maximum allowable battery temperature voltage. If the potential between TS and SNS (pins 6 and 9) is less than the voltage at the TCO input, then any fast charging or 'top-off" charging is terminated. (See Figure 3.)

CCMD, DCMD Charge initiation and discharge-before-charge control inputs

These two pine control charge initiation and discharge-before-charge. When both CCMD and DCMD pins are connected to Vcc or when both are connected to Vss, charge automatically initiates on battery replacement or when Vcc is applied. Charge is also initiated by (1) a rising edge to Vcc at CCMD if both CCMD and DCMD are connected to Vss, or (2) a falling edge to Vss at CCMD if both CCMD and DCMD are connected to Vcc.

Discharge-before-charge is initiated at any time by: (1) a rising edge to Vcc at DCMD if both DCMD and CCMD are connected to Vss, or (2) a negative-going pulse (from Vcc to Vss and then back to Vcc) at DCMD if both DCMD and CCMD are connected to Vcc.

DVEN -ΔV enable input

This input controls the -ΔV charge termination test. If DVEN is high, the -ΔV test is enabled. If DVEN is low, -ΔV test is disabled. DVEN may change state at any time.

DIS Discharge FET control output

Push-pull output used to control an external transistor to discharge the battery before charging. DIS is active high.

TEMP Temperature status output

Push-pull output indicating temperature status. TEMP is low if the temperature input voltage at the TS pin is not within the acceptable temperature window to initiate fast charging.

CHG Charging status output

Push-pull output indicating charging status. See Table 1, bq2003 Operational Summary, for output pattern details.

TM_1, TM2 Timer mode inputs

TM_1 and TM_2 are three-level inputs that control the settings for fast charge safety timer and "top-off" enable/disable. See Table 2 for details.

MOD Current-switching control output

MOD is a push/pull output that is used to control the charging current to the battery. MOD switches high to enable charging current flow and low to inhibit charging current flow.

SNS Charging current sense input

SNS controls the switching of MOD based on an external sense resistor. This provides the reference potentials for both the TS and BAT pins (pins 6 and 7).

If SNS is connected to Vss, MOD switches high at the beginning of charge and low at the end of charge.

Vcc Vcc supply input

5.0 V, ±10% power input.

Vss Ground

Functional Description

Figure 2 illustrates charge control and display status during a bq2003 charge cycle. Table 1 outlines the various bq2003 operational states and their associated conditions, which are described in detail in the following sections.

Charge Action Control

The bq2003 charge action is controlled by inputs from the CCMD, DCMD, and DVEN input pins and from the TM_1 and TM_2 programming input pins.

The bq2003 controls the initiation of a charge action, checks for acceptable battery temperature (between LTF—low temperature fault and HTF—high temperature fault) and voltage (between EDV-end-of-discharge voltage and MCV—maximum cell voltage), and performs any required discharge-before-charge operation prior to fast charging. Once fast charging is initiated, the bq2003 tests for the full charge conditions: delta temperature/delta time ($\Delta T/\Delta t$) and/or negative delta voltage ($-\Delta V$), with temperature cutoff (TCO), time, and voltage safety terminations.

Charge Status Indication

Charge status is indicated by the CHG output. The CHG output may be connected directly to an LED indicator. The various charge action states and associated CHG output patterns are described in Table 1.

Temperature status is indicated by the TEMP output. The TEMP output may be connected directly to an LED indicator. TEMP is in the high state whenever battery temperature is within the temperature window defined by the V_{LTF} and V_{HTF} temperature limits. When the

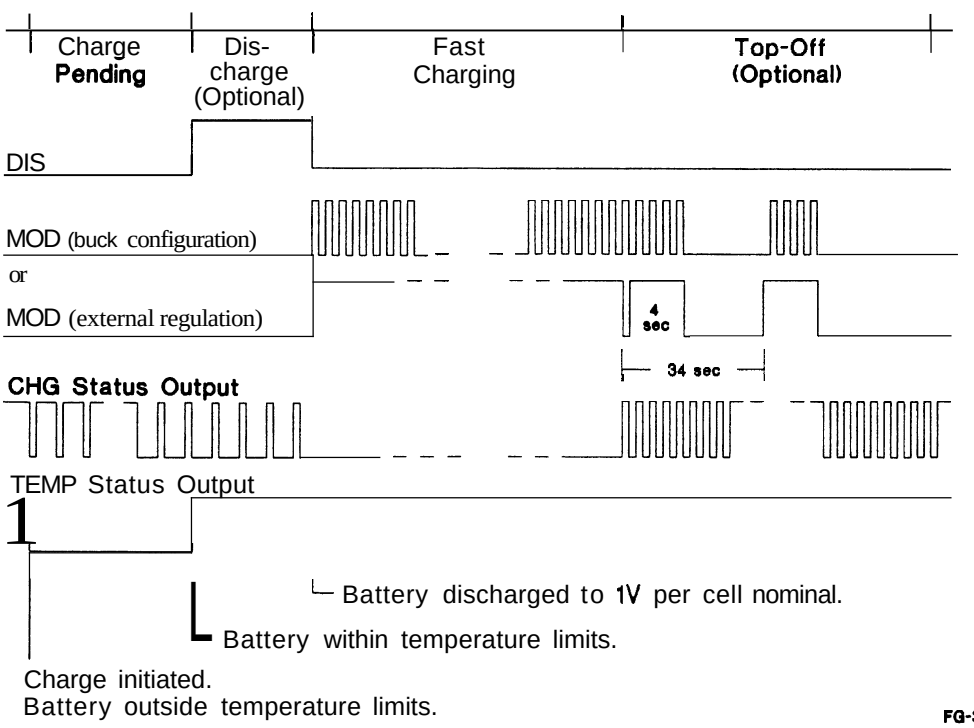


Figure 2. Example Charging Action Events

battery temperature is outside these limits, **TEMP** is in the low state, as indicated in Table 1.

In all cases, if the battery voltage at the BAT pin exceeds the voltage threshold at the MCV pin, both CHG and **TEMP** outputs are held high regardless of other conditions.

Table 1. bq2003 Operational Summary

Charge Action State	Conditions	MOD Output	DIS Output	CHG Status Output	
				Low	High
Battery absent/abort	V_{CELL}[1] ≥ V_{MCV}	Low	Low		Continuous
Charge initiation	(1) CCMD = V_{SS} and Vcc applied or V_{CEU} drops from ≥ V_{MCV} to < V_{MCV} (battery insertion) or (2) CCMD = V_{CC} and low-going pulse applied to CCMD	Low	Low		Continuous
Discharge-before-charge initiation (optional)	DCMD low-to-high transition	Low	Low	-	Continuous
Pending	Initiation occurred and V_{TEMP}[2] ≥ V_{LTF} or V_{TEMP} ≤ V_{HTF} or V_{CELL} < V_{EDV}	Low	Low	1/8 sec	1 3/8 sec
Discharging (optional)	Discharge-before-charge initiation and V_{HTF} < V_{TEMP} < V_{LTF} and V_{EDV} < V_{CELL} < V_{MCV}	Low	High	1 3/8 sec	1/8 sec
Fast charging	Initiation occurred and V_{HTF} < V_{TEMP} < V_{LTF} and V_{EDV} ≤ V_{CELL} < V_{MCV}	Law if V_{SNS} > 250mV, nominal; high if V_{SNS} < 220mV, nominal	Low	Continuous	
Charge complete	-ΔV ≥ 12mV nominal or $\Delta V_{TEMP}/\Delta T$ > 14mV/minute or V_{TEMP} < V_{TCO} or maximum time or maximum voltage	Low	Low	1/8 sec	1/8 sec
Top-off (optional; see Table 2)	Charge complete and top-off time not exceeded and V_{TEMP} > V_{TCO} and V_{CELL} < V_{MCV}	Activated per V_{SNS} (see fast charging state) for 4 sec of every 34 sec	Low	1/8 sec	1/8 sec
Temperature State	**Conditions**	**TEMP Status Output**			
Temp fault	V_{TEMP} ≤ V_{HTF} or V_{LTF} ≤ V_{TEMP} V_{CELL} < V_{MCV}	Low			
Temp OK	V_{HTF} < V_{TEMP} < V_{LTF}	High			

Notes:

1. $V_{CELL} = V_{BAT} - V_{SNS}$.
2. $V_{TEMP} = V_{TS} - V_{SNS}$.
3. The bq2003 cannot detect battery removal during the hold-off period (see Voltage Termination Hold-Off). If the battery is removed between the start of fast charge and the end of the hold-off period, then MOD may remain active and CHG remain high until the hold-off period expires.

Battery Voltage and Temperature Measurement

Battery voltage and temperature are monitored for maximum and minimum allowable values. The bq2003 requires that the thermistor used for temperature measurement have a negative temperature coefficient. See Figure 3.

The per-cell voltage for a battery containing N cells is defined by the resistor divider ratio:

$$\frac{R_1}{R_2} = N\text{-}1$$

where R_1 is the resietor connected to the positive battery terminal, and R_2 is the resistor connected to the negative battery terminal.

External Trickle Resistor

An external trickle resistor serves two purposes in the charging system. First, it supplies a high-voltage reference that allows the bq2003 to detect a battery insertion. Second, it supplies a small amount of trickle current to the battery that can be used to condition a deeply discharged battery for charging or maintain the charge state of a fully charged battery.

Temperature and Voltage Prequalifications

Discharge and charge are both prequalified by battery temperature and voltage. For discharge and charge to be performed, the battery temperature and voltage must fall within predetermined acceptable limits.

V_{CELL} (V_{BAT} - V_{SNS}) is compared to an internal low-voltage reference, V_{EDV} (0.2 • V_{CC}), which is the minimum acceptable battery voltage for fast charging.

V_{TEMP} voltage is compared to the internal low-temperature reference, V_{LTF} (0.4 • V_{CC}) and the internal hot-fault temperature reference, V_{HTF} [& * V_{LTF}) + (⅞ * V_{TCO})], where V_{TCO} is the cutoff temperature reference level on the TCO pin.

These limits establish the acceptable temperature sense voltage window for fast charge initiation. If the battery fails either of these two prequalifications for discharge or charge, the bq2003 enters a charge-pending mode, waiting for battery voltage and temperature to become acceptable.

In the case of a battery that is too warm or too cool, the charge action starts when the battery temperature becomes acceptable. In the case of deeply discharged batteries (voltage too low), the bq2003 waits until the battery voltage is an acceptable level before starting the charge action. In the case of a faulty battery, V_{BAT} may never reach an acceptable voltage level, causing the bq2003 to remain in the charge-pending state.

Initiating Charge Action and Discharge-Before-Charge

The CCMD and DCMD pins are described together in this section because these pine must be tied to the same potential for proper functionality.

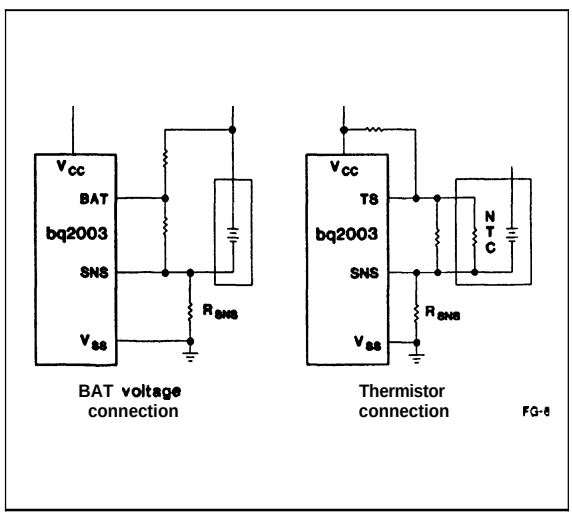


Figure 3. Voltage and Temperature Limit Measurement

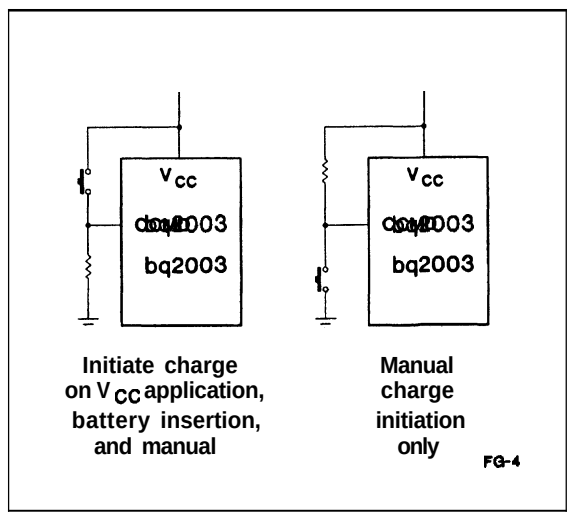


Figure 4. Charge Action Initiation

A battery charge action (prequalification, fast charge, and optional "top-off") is initiated under control of the CCMD pin. The DCMD pin supports automatic die-charge to V_{EDV} before charge to provide conditioning as well as capacity calibration.

Because the CCMD and DCMD pins must be tied to the same potential, these pins can be treated electrically in two ways. Both pins can be connected to V_{CC} or to V_{SS}. Either treatment allows for automatic *charge* initiation on battery replacement or when V_{CC} is applied. Battery replacement is recognized when the voltage at the BAT pin falls from above the MCV pin reference level to below that level.

Otherwise, charge is initiated by: (1) a rising edge to V_{CC} at CCMD if both CCMD and DCMD are connected to V_{SS}, or (2) a falling edge to V_{SS} at CCMD if both CCMD and DCMD are connected to V_{CC}.

Diecharge-before-charge is initiated at any time by: (1) a rising edge to V_{CC} at DCMD if both DCMD and CCMD are connected to V_{SS}, or (2) a negative-going pulse (from V_{CC} to V_{SS} and then back to V_{CC}) at DCMD if both DCMD and CCMD are connected to V_{CC}.

When the discharge begins, the DIS output goes high to activate an external transistor that connects a load to the battery. When discharge reaches $V_{CELL} = V_{EDV}$, DIS goes low and fast charge begins (provided the pre-charge qualifications are met).

Fast Charge

Once temperature and voltage prequalifications are met and any required discharging of the battery is completed, fast *charging* begins and continues until termination by one *or* more of the five possible termination conditions:

- Delta temperature/delta time ($\Delta T/\Delta t$)
- a Negative delta voltage ($-\Delta V$)
- a Maximum temperature
- Maximum charge time
- Maximum battery voltage

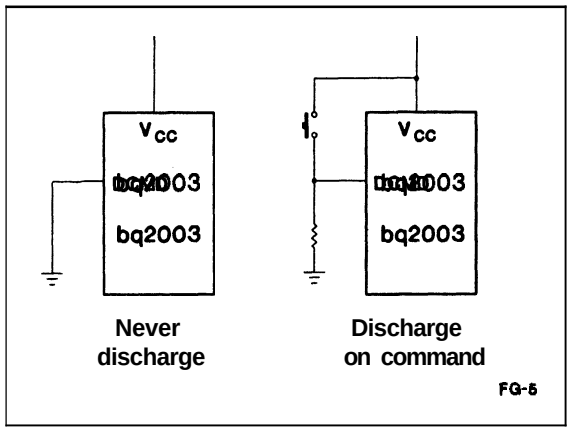


Figure 5. Discharge-Before-Charge

Voltage Termination Hold-Off

At the start of fast charging, there h a hold-off time during which -AV and maximum cell voltage (MCV) termination are disabled. (See Table 2) Once past the initial fast charge hold-off time, these terminations are re-enabled.

$\Delta T/\Delta t$ and maximum temperature terminations are not affected by the hold-off period.

-AV Fast Charge Termination

The bq2003 makes a termination decision based on negative delta voltage (-AV) every 34 seconds. If V_{CELL} is lower than any previously measured value by 12mV typical, the fast charge phase of the charge action is terminated.

The -ΔV test is valid only for $V_{MCV} - (0.2 \bullet V_{CC}) \le V_{CELL} \le V_{MCV}$. -$\Delta V$ detection may be enabled or disabled at any time using the DVEN pin.

$\Delta T/\Delta t$ Fast Charge Termination

The bq2003 makes a termination decision based on delta temperature/delta time ($\Delta T/\Delta t$) every 34 seconds based on temperature measurements over a 68-second time period. If V_{TEMP} + 16mV (typical) is less than the voltage measured 68 seconds previously, the fast charge phase of the charge action is terminated.

The $\Delta T/\Delta t$ test is valid only for $V_{TCO} \le V_{TEMP} \le V_{TCO} + 0.2 \bullet V_{CC}$.

Maximum Voltage, Maximum Time, and Maximum Temperature Safety Terminations

The bq2003 also terminates fast charge for maximum temperature (TCO), maximum time, and maximum voltage (MCV).

MCV and TCO reference levels provide the maximum limits for battery voltage and temperature during fast charging. If either of these limits is exceeded, both fast charging and *any* optional top-off charge are terminated.

Table 2. Fast Charge Safety Time/Hold-Off/Top-Off Table

Corresponding Fast Charge Rate	TM1	TM2	Fast Charge Safety Time (minutes) Typical	-ΔV/MCV Hold-Off Time (seconds) Typical	Top Off R-ate
C/4	Low	Low	360	137	Disabled
C/2	Float	Low	180	820	Disabled
1C	High	Low	90	410	Disabled
2C	Low	Float	45	200	Disabled
4C	Float	Float	23	100	Disabled
C/2	High	Float	180	820	C/16
1C	Low	High	90	410	C/8
2C	Float	High	45	200	C/4
4C	High	High	23	100	C/2

Note: $T_A = 25°C$, $V_{CC} = 5.0V$.

Maximum time selection is programmed using the TM_1 and TM_2 pins (see Table 1). Time settings are available for corresponding charge rates ranging from C/4 to 4C.

Temperature Monitoring

Temperature is represented as a voltage input to the bq2003 at the TS pin. Generally, this voltage is developed from a thermistor. The bq2003 recognizes an internal voltage level of $V_{LTF} = 0.4 \cdot V_{CC}$ as the Low-Temperature Fault (LTF) level. If $V_{TEMP} \geq V_{LTF}$, charging is inhibited ($V_{TEMP} = V_{TS} \cdot V_{SNS}$). Similarly, the external reference voltage level presented at the TCO pin represents the temperature cutoff point at which fast charging is terminated.

All temperature prequalifications and ΔT/Δt termination may be disabled by connecting TCO to Vss and fixing the TS pin level at $0.1 \cdot V_{CC}$.

Top-Off Charge

An optional top-off charge phase is selectable to follow fast charge termination for charge rates from C/2 to 4C. This option is selected through the TM_1/TM_2 programming pins. (See Table 2.) If selected, the bq2003 'tops off the battery at a pulsed rate. The charge control cycle is modified so that MOD is activated for only 4 seconds of every 34 seconds. This results in a rate 1/8th that of fast charging. Top-off charge proceeds for a time equal to the fast charge safety time (see Table 2). Temperature (TCO) and voltage (MCV) terminations are the only termination methods enabled during 'top off.'

Charge Current Control

The bq2003 controls charge current through the MOD output pin. The current control is designed to support implementation of a constant-current switching regulator. See Figure 6.

Nominal regulated current is:

$$I_{REG} = 0.235V/R_{SNS}$$

When used in this configuration, the charge current is monitored at the SNS input by the voltage drop acmes a resistor, R_{SNS}. R_{SNS} can be chosen to provide a variety of charging currents.

The MOD pin is switched high or low depending on the voltage input to the SNS pin. If the voltage at the SNS pin is less than V_{SNSLO} (0.220V nominal), the MOD output is switched high to gate charge current through the inductor to the battery.

When the SNS voltage is greater than V_{SNSHI} (0.250V nominal), the MOD output is switched low--shutting off current from the supply.

The MOD pin can be used to gate an external charging current source. When an external current source is used, no sense resistor is required, and the SNS pin is connected to Vss.

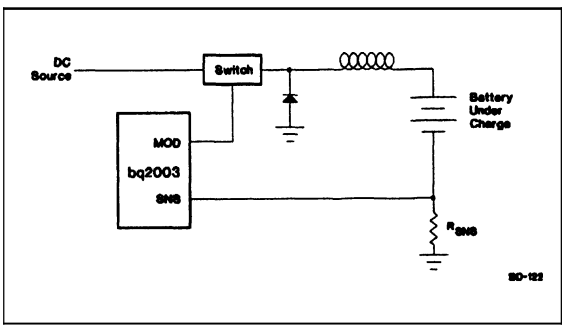


Figure 6. Constant-Current Regulation

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	V_{CC} relative to V_{SS}	-0.3	+7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to Vss	-0.3	+7.0	V	
T_{OPR}	Operating ambient temperature	0	+70	°C	Commercial
		-40	+85	°C	Industrial "N"
T_{STG}	Storage temperature	-55	+125	"C	
T_{SOLDER}	Soldering temperature		+260	°C	10 sec max.
T_{BIAS}	Temperature under bias	-40	+85	°C	

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds ($T_A = T_{OPR}$; V_{CC} ±10%)

Symbol	Parameter	Rating	Tolerance	Unit	Notes
V_{SNSHI}	High threshold at SNS resulting in MOD = Low	0.05 • V_{CC}	M.026	V	Tolerance is common mode deviation.
V_{SNSLO}	Low threshold at SNS resulting in MOD = High	0.044 • V_{CC}	±0.025	V	Tolerance is common mode deviation.
V_{LTF}	Low-temperature fault	0.4 • Vcc	t0.030	V	$V_{TEMP} \geq V_{LTF}$ inhibits charge
V_{HTF}	High-temperature fault	(⅛ • V_{LTF}) + (⅞ • V_{TCO})	M.030	V	$V_{TEMP} \leq V_{HTF}$ inhibits charge
V_{EDV}	End-of-discharge voltage	0.2 • vcc	±0.030	V	$V_{CELL} < V_{EDV}$ inhibits charge

Recommended DC Operating Conditions (T_A = 0 to +70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	
V_{CELL}	BAT voltage potential	0	-	V_{CC}	V	V_{BAT} - V_{SNS}
V_{BAT}	Battery input	0	-	V_{CC}	V	
V_{TEMP}	TS voltage potential	0	-	V_{CC}	V	V_{TS} - V_{SNS}
V_{TS}	Thermistor input	0	-	V_{CC}	V	
V_{MCV}	Maximum cell voltage	V_{EDV}	-	V_{EDV} + (0.2 • V_{CC})	V	
V_{TCO}	Temperature cutoff	V_{LTF} - (0.2 • V_{CC})	-	V_{LTF}	V	
V_{IH}	Logic input high	V_{CC} - 1.0	-	-	V	CCMD, DCMD, DVEN
	Logic input high	V_{CC} - 0.3	-	-	V	TM_1, TM_2
V_{IL}	Logic input low	-	-	1.0	V	CCMD, DCMD, DVEN
	Logic input low	-	-	0.3	V	TM_1, TM_2
V_{OH}	Logic output high	V_{CC} - 0.5	-	-	V	DIS, TEMP, CHG, MOD, $I_{OH} \leq$ -5mA
V_{OL}	Logic output low	-	-	0.5	V	DIS, TEMP, CHG, MOD, $I_{OL} \leq$ 5mA
I_{CC}	Supply current	-	0.75	2.2	mA	Outputs unloaded
I_{OH}	DIS, TEMP, MOD, CHG source	-5.0	-	-	mA	@V_{OH} = V_{CC} - 0.5V
I_{OL}	DIS, TEMP, MOD, CHG sink	5.0	-	-	mA	@V_{OL} = V_{SS} + 0.5V
I_{IL}	Input leakage	-	-	±1	µA	CCMD, DCMD, DVEN, V = V_{SS} to V_{CC}
	Logic input low source			70	µA	TM_1, TM_2, V = V_{SS} to V_{SS} + 0.3V
I_{IH}	Logic input high source	-70			µA	TM_1, TM_2, V = V_{CC} - 0.3V to V_{CC}
I_{IZ}	TM_1, TM_2 tri-state open detection	-2.0		2.0	µA	TM_1, TM_2 may be left disconnected (float: logic input state
V_{THERM}	Thermistor input resolution for $\Delta T/\Delta t$		16 ± 4		mV	V_{CC} = 5.0V, T_A = 2
-ΔV	Negative delta voltage		12 ± 4		mV	V_{CC} = 5.0V, T_A = 25'

Note: All voltages relative to V_{SS}.

Impedance

Symbol	Parameter	Minimum	Typical	Maximum	Unit
R_{BAT}	Battery input impedance	60			MQ
R_{MCV}	MCV input impedance	50			MΩ
R_{TCO}	TCO input impedance	60			MΩ
R_{SNS}	SNS input impedance	*50*			MQ
R_{TS}	TS input impedance	*50*			MΩ

Timing (T_A = 0 to +70°C; VCC ±10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{PW}	Pulse width for CCMD, DCMD pulse commands	1			µs	Pulse start for charge or discharge-before-charge
d_{FCV}	Fast charge safety time variation	0.84	1.0	1.16	•	V_{CC} = 4.5V to 5.5V; see Table 2.
t_{REG}	MOD output regulation frequency			100	kHz	Typical regulation capability; V_{CC} = 5.0V
t_{MCV}	$V_{CELL} \geq V_{MCV}$ valid period	200	250	300	ms	If $V_{CELL} \geq V_{MCV}$ for t_{MCV}, then a transition of $V_{CELL} < V_{MCV}$ is recognized as battery replaced. Otherwise, $V_{CELL} < V_{MCV}$ is ignored.

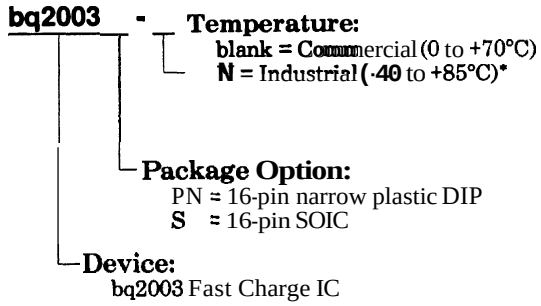
Note: Typical is at T_A = 25°C, V_{CC} = 5.0V.

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	7	DCMD transition to initiate discharge-before-charge	Was low-to-high; is pulse with period t_{PW}.
1	8	Table 2 C/4 charge rate -ΔV/MCV hold-off time changed	Was 1640 seconds; is 137 seconds.
1	10	Changed MCV allowable voltage range	Was 0.2 • V_{CC} min and 0.6 • V_{CC} max; is V_{EDV} min and V_{EDV} + (0.2 • V_{CC}) max.
2	10	Added tolerance to -AV typical value	Was 12 typ; is 12 ±4 typ.
2	11	Changed impedance parameters	Were 50 typ; are 50 min.
2	11	Changed t_{REG} value	Was 100 typ; is 100 max.
3	3, 6, 7	CCMD and DCMD pins must be tied together	Clarification
4	2	Changed description of -AV fast charge termination from "If V_{CELL} is lower than the previous measured value..." to "If V_{CELL} is lower than any previous measured value..."	Clarification
4	11	Added TS input impedance	Additional specification
5	2	Changed block diagram	Changed diagram
5	8	Added Top-Off values to Table 2	Added values

Note: Change 1 = Aug. 1992 B changes from Apr. 1992 A.
Change 2 = Oct. 1992 C "Final" changes from Aug. 1992 B "Preliminary."
Change 3 = Dec. 1992 D changes from Oct. 1992 C.
Change 4 = Oct. 1993 E changes from Dec. 1992 D.
Change 5 = Sept. 1996 F changes from Oct. 1993 E.

Ordering Information



* Contact factory for availability.

BENCHMARQ

Product Brief **DV2003L1**

Fast Charge Development System

Control of On-Board Linear Current Regulator or External Current Source

Features

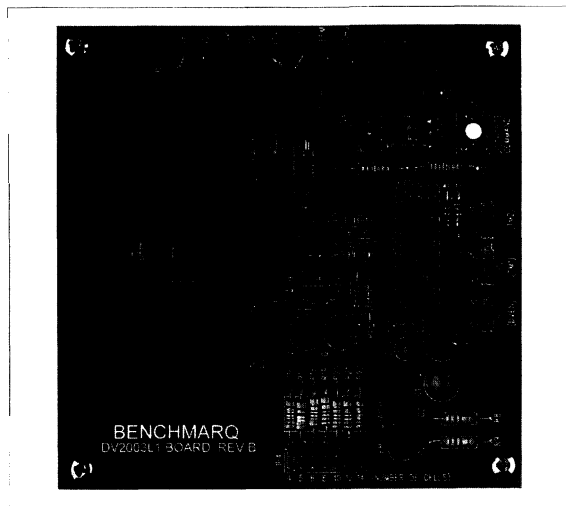
- bq2003 fast charge control evaluation and development
- Charge current sourced from an on-board linear regulator (1.25A, modifiable for 0.1 to 1.5 A) or an external current source
- Fast charge of 4 to 14 NiCd or NiMH cells
- Fast charge termination by $\Delta T/\Delta t$, $-\Delta V$, maximum temperature, time, and voltage
- -AV enable, hold-off, top-off, maximum time, number of cells, and off-board current source control are jumper-configurable
- ➤ Charging status displayed on charge and temperature LEDs
- Discharge-before-charge control with push-button switch
- Inhibit fast charge by external logic-level input

General Description

The DV2003L1 Development System provides a development environment for the bq2003 Fast Charge IC. The DV2003L1 incorporates a bq2003 and an LM317 linear regulator to provide fast charge control for 4 to 14 NiCd or NiMH cells. The DV2003L1 also supports on/off control of an external current source.

The fast charge is terminated by any of the following: $\Delta T/\Delta t$, $-\Delta V$, maximum temperature, maximum time, maximum voltage, and external inhibit command.

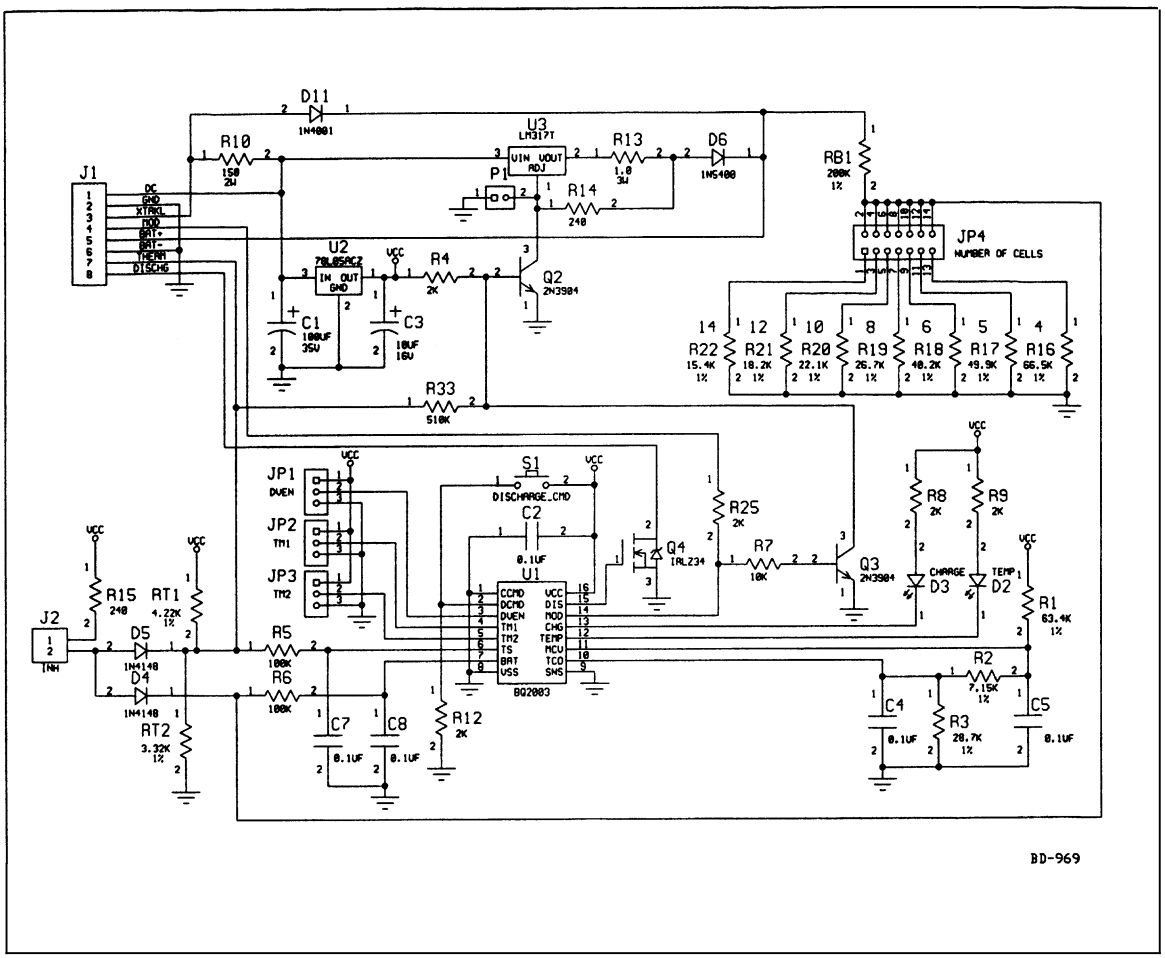
Jumper settings select the $-\Delta V$ enabled state, select the hold-off, top-off, and maximum time limits, and enable the use of an external current source.



The user provides a power supply and batteries. If the on-board 1.25A linear regulator is disabled, the external current source must have an appropriate digitally controlled switch (active high). The user configures the DV2003L1 for the number of cells, $-\Delta V$, charge termination enabled or disabled, and maximum charge time (with or without top-off), and commands discharge-before-charge with a push-button switch.

A full data sheet for this product is available on our web site (http:/lwww.benchmarq.com), or you may contact the factory for one.

DV2003L1 Board Schematic

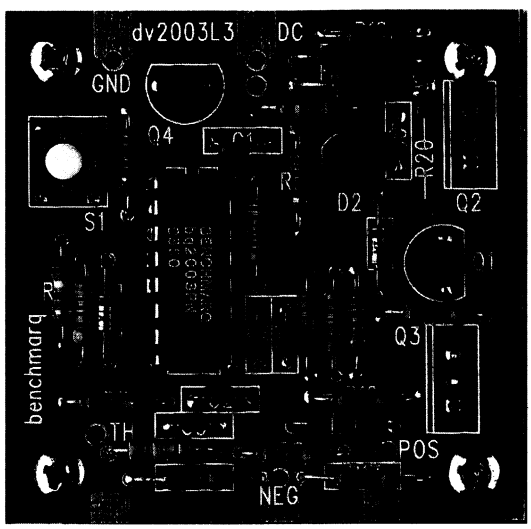


Fast Charge Development System

Control of Frequency-Modulated Linear Regulator

Features

- ➤ bq2003 fast charge control evaluation and development
- ➤ Charge current controlled with frequency-modulated linear design
- ● Fast charge of 2 to 12 NiCd and/or NiMH cells
- ● Fast charge termination by -ΔV, ΔT/Δt, maximum temperature, time, and voltage
- ● Discharge-before-charge option



General Description

The bq2003L3 Development System provides a cost-effective component-reduced development environment for the bq2003 Fast Charge IC. The DV2003L3 incorporates a frequency-modulated linear regulator for fast charge control of NiCd and/or NiMH cells.

A full data sheet for this product is available on our web site (http://www.benchmarq.com), or you may contact the factory for one.

DV2003L3 Configuration—Complete Before Ordering

Customer Name: _____

Contact: _____ Phone: _____

Address: _____

_____

Sales Contact: _____ Phone, _____

DC input voltage (V) _____

-AV enabled (yes/no) _____

ΔT/Δt enabled (yes/no) _____

Number of battery cells (2—12) _____

Charge current (A) (1.5A rnax.) _____

Battery capacity (mAh) _____

Battery type (NiCd and/or NiMH) _____

Top-off (yes/no) _____

Discharge-before-charge (yes/no) _____

Discharge current (mA) _____

Oct. 1994

DV2003L3 Board Schematic

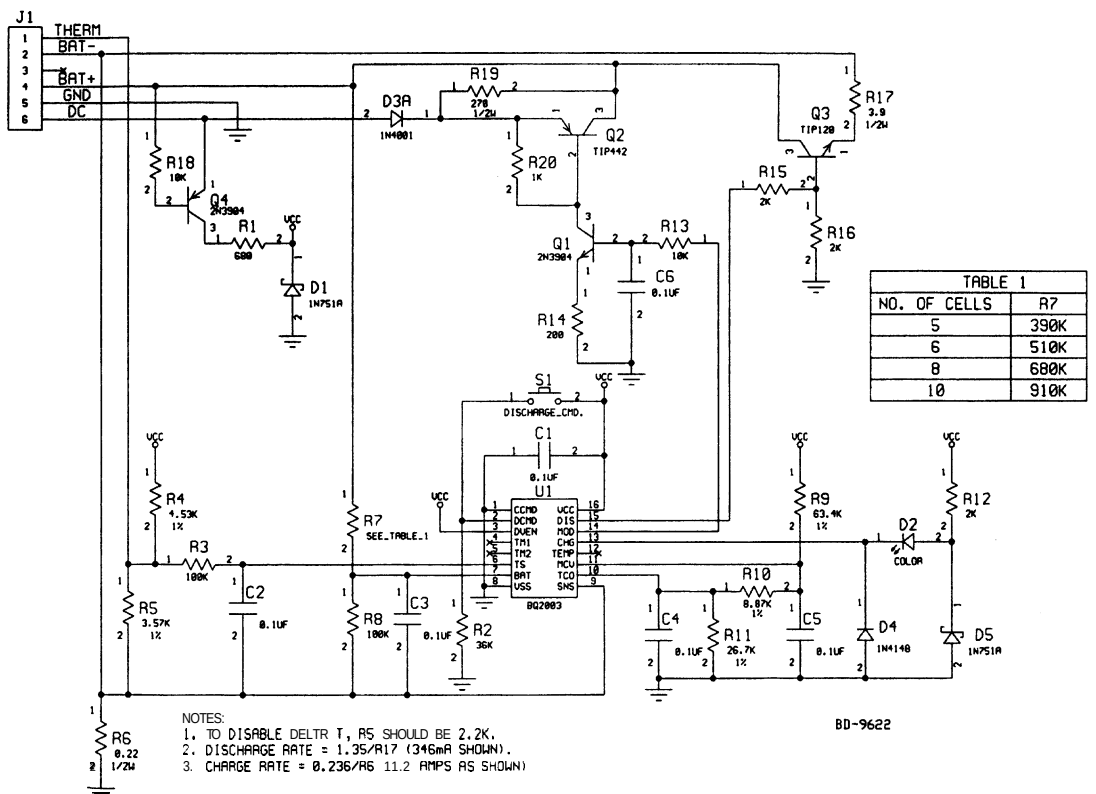


TABLE 1	
NO. OF CELLS	R7
5	390K
6	510K
8	680K
10	910K

BENCHMARQ

Product Brief **DV2003S1**

Fast Charge Development System

1

Control of On-Board p-FET Switch-Mode Regulator

Features

- bq2003 fast charge control evaluation and development

  Charge current sourced from an on-board switch-mode regulator (up to 3.0 **A)**
- Fast charge of 2 to 16 NiCd or NiMH cells
- Fast charge termination by delta temperature/delta time ($\Delta T/\Delta t$), negative delta voltage ($-\Delta V$), maximum temperature, maximum time, and maximum voltage

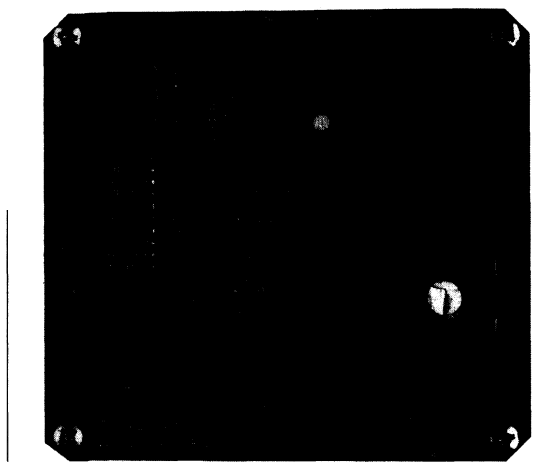
  -AV enable, hold-off, top-off, maximum time, and number of cells are jumper-configurable
- Charging status displayed on charge and temperature LEDs
- Discharge-before-charge control with push-button switch
- Inhibit fast charge by external logic-level input

General Description

The DV2003S1 Development System provides a development environment for the bq2003 Fast Charge IC. The DV2003S1 incorporates a bq2003 and a buck-type switch-mode regulator to provide fast charge control for 2 to 16 NiCd or NiMH cells.

Review the bq2003 data sheet and the application note, "Using the bq2003 to Control Fast Charge," before using the DV2003S1 board.

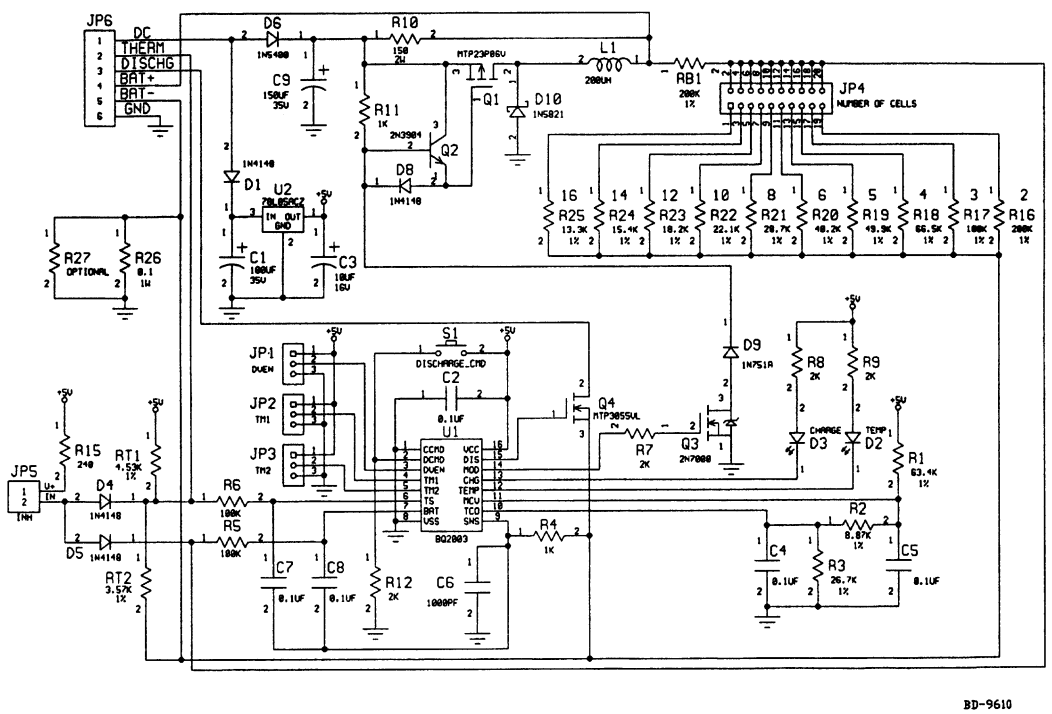
The fast charge is terminated by any of the following: $\Delta T/\Delta t$, $-\Delta V$, maximum temperature, maximum time, maximum voltage, and external inhibit command. Jumper settings select the $-\Delta V$ enabled state, select the hold-off, top-off, and maximum time limits.



The user provides a power supply and batteries. The user configures the DV2003S1 for the number of cells, -AV charge termination enabled or disabled, and maximum charge time (with or without top-off),and commands discharge-before-charge with push-button switch S1.

A full data sheet of this product is available on our web site (http://www.benchmarq.com), or you may contact the factory for one.

DV2003S1 Board Schematic



BENCHMARQ

Product Brief **DV2003S2**

Fast Charge Development System

Control of On-Board n-FET Switch-Mode Regulator

Features

- bq2003 fast charge control evaluation and development
- Charge current sourced from an on-board switch-mode regulator (up to 6.0 A)
- Fast charge of 2 to 16 NiCd or NiMH cells
- Fast charge termination by delta temperature/delta time ($\Delta T/\Delta t$), negative delta voltage ($-\Delta V$), maximum temperature, maximum time, and maximum voltage

  -AV enable, hold-off, top-off, maximum time, and number of cells are jumper-configurable

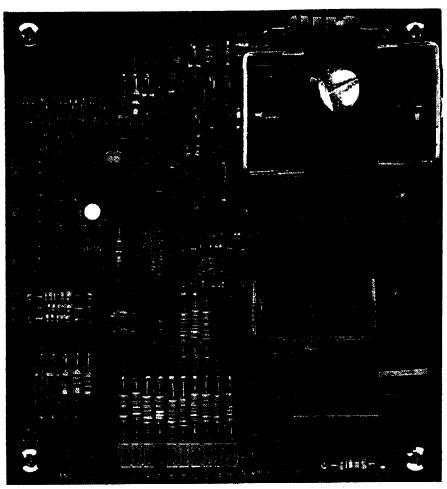
  Charging status displayed on charge and temperature LEDs

  Discharge-before-charge control with push-button switch
- Inhibit fast charge by external logic-level input

General Description

The DV2003S2 Development System provides a development environment for the bq2003 Fast Charge IC. The DV2003S2 incorporates a bq2003 and an n-FET buck-type switch-mode regulator to provide fast charge control for 2 to 16 NiCd or NiMH cells. The primary difference between the DV2003S2 and the DV2003S1 is in the switching FET Q1. The DV2003S1 uses a p-FET for battery charge currents of 3.0A or less, whereas the DV2003S2 uses an n-FET to support charge currents up to 6.0A.

Review the bq2003 data sheet and the application note, "Using the bq2003 to Control Fast Charge," before using the DV2003S2 board. Also review the application note, "Step-Down Switching Current Regulation Using the bq2003," for information concerning trade-offs between using p-FET and n-FET transistors for Q1.

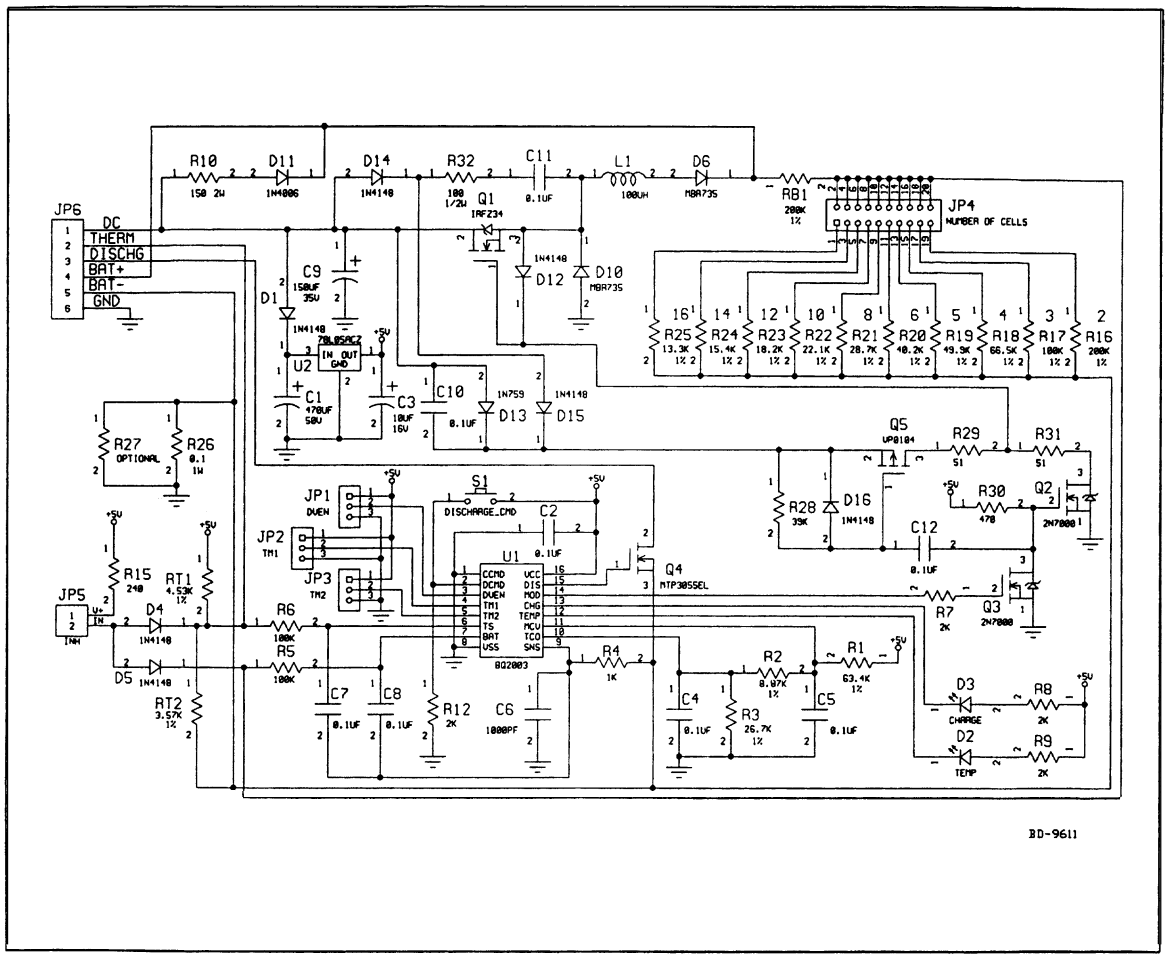


The fast charge is terminated by any of the following: $\Delta T/\Delta t$, $-\Delta V$, maximum temperature, maximum time, maximum voltage, and external inhibit command. Jumper settings select the -AV enabled state, select the hold-off, top-off, and maximum time limits.

The user provides a power supply and batteries. The user configures the DV2003S2 for the number of cells, -AV charge termination enabled or disabled, and maximum charge time (with or without top-off), and commands discharge-before-charge with push-button switch S1.

A full data sheet for this product is available on our web site (http:llwww.benchmarq.com), or you may contact the factory for one.

DV2003S2 Board Schematic



BENCHMARQ

Using the bq2003 to Control Fast Charge

1

Introduction

This application note describes the use and functions of the bq2003 gating a current source to fast charge NiCd or NiMH batteries. Examples describe the ease with which the bq2003 is incorporated into applications.

The bq2003 may also serve as the modulator for a switch-mode constant-current regulator to provide an efficient charge current source. This is discussed in the Application Note, "Step-Down Switching Current Regulation Using the bq2003 Fast Charge IC.'

Examples for additional applications are being developed. Please contact Benchmarq if your application is not supported by one of these examples.

The bq2003 is targeted for applications requiring state-of-the-art fast-charging performance at minimal cost. It provides sophisticated full-charge detection techniques such as ΔT/Δt (delta temperature/delta time) and -ΔV (negative delta voltage) that enable the user to take advantage of advanced battery technologies such as nickel metal-hydride (NiMH) and high-capacity fast-charge nickel cadmium (NiCd). Systems using the bq2003 can be easily upgraded from NiCd batteries to NiMH batteries without system redesign.

Background

A s cant advantage of the bq2003 over other fast-charge solutions is the use of ΔT/Δt and/or -ΔV as the primary decisions for fast-charge termination. ΔT/Δt detection is one of the most sensitive and reliable methods for fast-charge termination when charging NiMH and NiCd batteries. Near maximum charge acceptance, the temperature rise begins to accelerate at the same time that voltage rise accelerates. The ΔT/Δt decision typically precedes the peak voltage, allowing for minimal overcharge stress.

The ΔT/Δt method also tolerates varying rates of charge, which may be desirable when charging during system operation.

Compared to the AT method, which uses two sensors to monitor battery temperature and ambient temperature, the ΔT/Δt method uses a single thermistor to monitor the rate of temperature increase. This approach is more tolerant in cases when the initial battery temperature is significantly different from the ambient temperature.

bq2003 temperature monitoring may be permanently disabled without affecting other bq2003 charge-termination functions.

The bq2003 monitors the voltage across the battery to detect -ΔV, which is a very reliable *charge* terminator for NiCd batteries. -ΔV detection in the bq2003 may be temporarily disabled during periods when the *charge* current fluctuates greatly or during the beginning of a fast charge to eliminate false peaks. -ΔV may be permanently disabled without affecting other bq2003 charge-termination functions.

To ensure safety for the battery and system, fast charging also terminates based on a hot-temperature cutoff threshold (TCO), a safety time period, and a maximum cell voltage threshold (MCV). To avoid possible premature fast-charge termination when charging batteries after long periods of storage, the bq2003 disables MCV and -ΔV detection during a short 'hold-off period at the start of fast charge. This hold-off period is configured as described in the bq2003 data sheet.

The bq2003 may be configured to have one, two, or three charge stages. As a one-stage charger, the bq2003 controls charge with no trickle. In a two-stage configuration, the fast-charge stage controlled by the bq2003 is preceded and followed by a continuous trickle charge at a rate controlled by a current-limiting resistor outside of the bq2003. In a three-stage configuration, the fast *charge* is followed by a "top-off charge stage at 1/8 the fast *charge* rate. This allows the battery to be quickly and safely brought to a full charge state. Following top-off, an external resistor controls trickle charge to the battery at a minimal charge-sustaining rate, typically C/40 or C/50.

Basic Charge-Control Operation

Two detailed applications follow this section. One provides direct control of a linear regulator, and the other provides control of any external current source.

Gating Current

Figure 1 shows an example of external source gating. With SNS tied to chip ground, the bq2003 enables charge current to the battery by taking MOD high at the start of charging and maintaining this state until charging is terminated. In this example, R7, Q2, R15, and Q1 form the switching circuit. When MOD goes high, Q2 switches on—turning on Q1. When MOD goes low, the base current in Q1 collapses, breaking the charging path.

The current-handling capability of this circuit is limited by the product of the current gains of the transistors and by the 5mA drive capability of the MOD pin.

This limitation may be removed by replacing the PNP at Q1 with a pFET. See Table 1 for suggested transistors.

Table 1. Suggested Transistors (Q1)

Q1	Type	Package	Maximum Current	Maximum Voltage
IRFR9010	pFET	DPAK	5.3	-50
IRFR9022	pFET	DPAK	9.0	-50
IRFR9020	pFET	DPAK	9.9	-50
IRFD9014	pFET	HEXDIP	1.1	-60
IRFD9024	pFET	HEXDIP	1.6	-60
IRF9Z10	pFET	TO-220	4.7	-50
IRF9Z22	pFET	TO-220	8.9	-50
IRF9Z20	pFET	TO-220	9.7	-50
IRF9Z32	pFET	TO-220	15	-50
BD136	PNP	TO-225	1.5	-60
MJE171	PNP	TO-225	3.0	-60
TIP42A	PNP	TO-220	6.0	-60

Note: For very high currents, two paralleled pFETs or an nFET with a high-side driver circuit may be suitable.

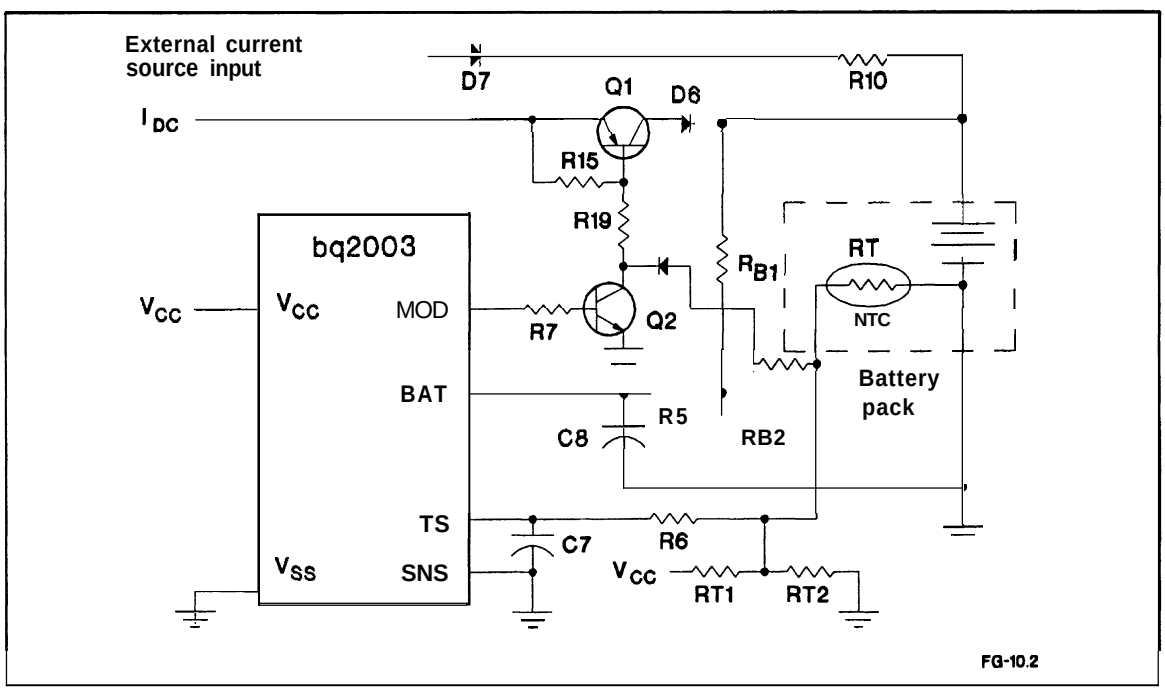


Figure 1. Gated External Source (Bipolar Switch Option)

Charge Status

The charge status of the bq2003 is indicated by two outputs. Each output may directly drive an LED. One LED uses distinctive flashing patterns to indicate the current charger status as:

Charge Action State	Charge Status Output	
	Low	High
Battery absent/abort	-	Continuous
Pending charge (waiting for proper temperature and/or voltage)	1/8 sec	1 3/8 sec
Discharging (optional)	1 3/8 sec	1/8 sec
Fast charging	Continuous	-
Charging complete	1/8 sec	1/8 sec
Top-off (optional)	1/8 sec	1/8 sec

A second LED indicates that the battery temperature detected by the bq2003 and associated thermistor is out of range for fast charging.

Charge Initiation

Charge may be initiated by power to the IC, battery replacement, or application of a digital signal. Configuration options are shown in Figure 2.

Charge initiation by application of power to the IC works as follows: When V_{CC} is applied, the bq2003 is held in reset for approximately one and one-half seconds. At the end of the reset period, the CCMD pin (pin 1) is sampled and, if CCMD and DCMD are low, a charge cycle initiates as soon as conditions allow.

Charge initiation on battery replacement relies on the BAT pin voltage being greater than MCV in the absence of a battery, and falling below MCV when the battery is connected. For example, in Figure 1 a resistor R10 is inserted between the positive battery terminal and I_{DC}. This resistor, in conjunction with RB1 and RB2, is sized to pull the BAT pin (pin 7) above the value programmed on MCV (pin 11, maximum cell voltage threshold) when the battery is removed.

When the battery is replaced in this case, the voltage on BAT should fall below MCV, at which time a charge cycle initiates as soon as conditions allow (if CCMD and DCMD are low).

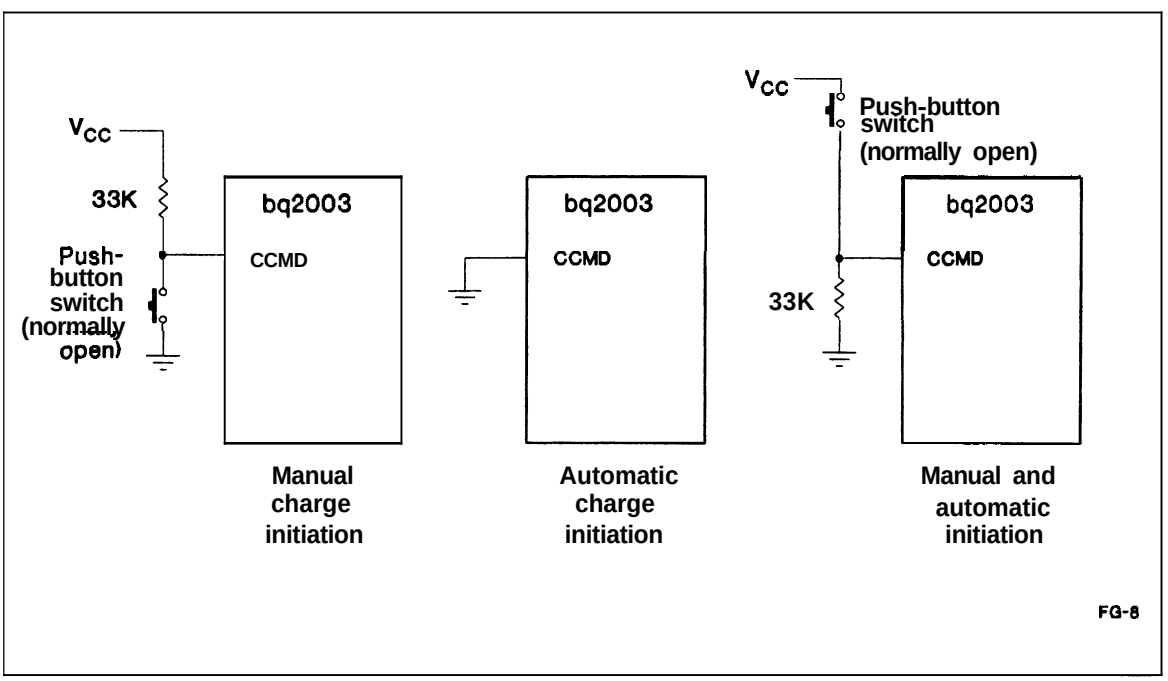


Figure 2. Charge Initiation Network

Charge initiation by digital signal occurs on the rising edge of CCMD with DCMD low. Digital charge initiation, which is simply a request to charge the battery, results in charging as soon as conditions allow.

The charge command may be issued at any time, but charging may be disqualified because the battery voltage or temperature is outside programmed limita. Fast charging remains pending until all charge qualifications become valid. When conditions allow, fast charging begins. A CCMD-initiated charge with battery absent remains pending until battery replacement.

Discharge-Before-Charge

It may be desirable in the application to allow the user to occasionally discharge the battery to a known voltage level prior to charge. The reason for this may either be to remedy a voltage-depression effect found in some NiCd batteriea or to determine the battery's charge capacity.

Figure 3 illustrates the implementation of this function. Discharge-before-charge is initiated on a positive strobe signal on DCMD. **This function takes precedence over a charge action and commences immediately when conditions warrant, forcing DIS to a high state until the voltage sensed on BAT falls below $V_{CC}/5$.** Charging begins as soon as conditions allow.

Care should be taken not to overheat the battery during this process; excessive temperature is not a condition that terminates discharge.

A strobe on CCMD terminates the discharge phase and initiates fast charging.

Unlike a CCMD-initiated charge, the discharge-before-charge function is ignored or terminated when $V_{BAT} - V_{SNS} > V_{MCV}$ (battery removed).

If the discharge-before-charge function is not desired, DCMD should be tied to V_{SS}.

Configuring the BAT Input

The bq2003 uses the battery voltage sense input on the BAT pin to control discharge-before-charge, qualify charge initiation, terminate charge at an absolute limit, and facilitate negative delta voltage (-ΔV) detection.

V_{BAT} may be derived from a simple passive network across the battery. As shown in Figure 1, resistors RB1 and RB2 are chosen to divide the battery voltage down to the optimal detection range, which is between V_{MCV} and $V_{MCV} - 1V$.

For NiCd and NiMH batteries, the battery terminal voltage is divided down to a per-cell potential. If, for example, the battery contains four NiCd cells, RB1 may be chosen as 562KΩ and RB2 as 187KΩ.

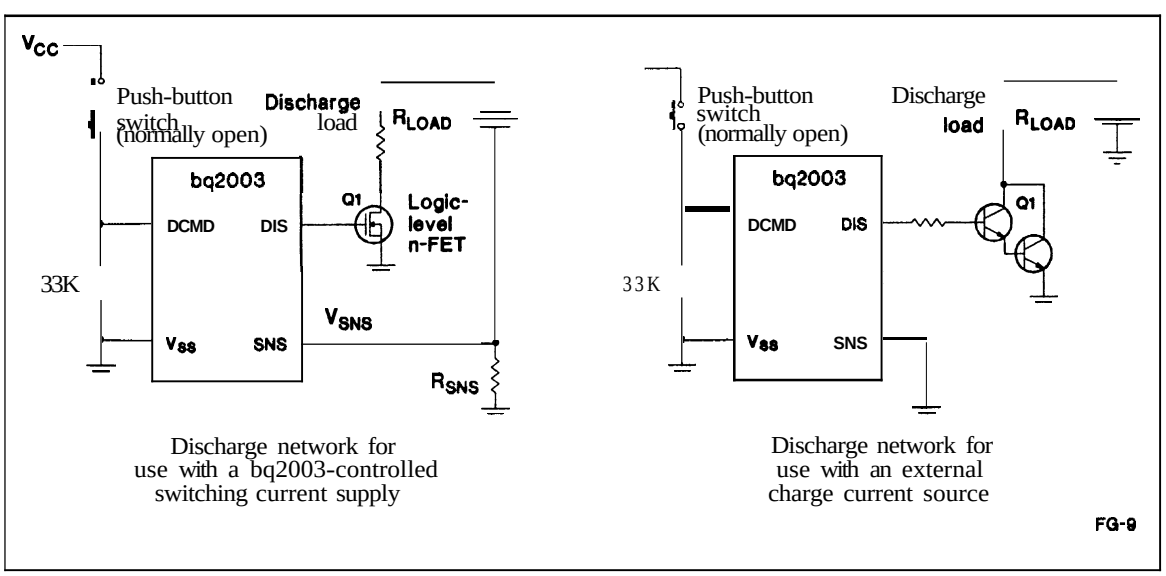


Figure 3. Battery Conditioning Network

Although virtually any value may be chosen for RB1 and RB2 due to the high input impedance of the BAT pin, the values selected must not be so low as to appreciably drain the battery nor so large as to degrade the circuit's noise performance. Constraining the source resistance as seen from BAT between 20KΩ and 1MΩ is acceptable over the bq2003 operating range. Total impedance between the battery terminal and Vss should typically be about 300KΩ to 1MΩ. See Table 2.

Notes: (1) Because V_{SNS} may be positive in bq2003 switching regulation applications, the actual internal comparison uses $V_{BAT} - V_{SNS}$, or V_{CELL}. This internal value V_{CELL} maintains a representative single-cell voltage independent of any current through R_{SNS}.

(2) The R-C time delay in the presentation of V_{BAT} must be shorter than 200ms (t_{MCV}). A longer delay may result in a failure to determine "battery replaced.'

Table 2. Suggested RB1 and RB2 Values for NiCd and NiMH Cells

Number of Cells (V_{BAT} Divisor)	RB1	RB2
4	562 KΩ	187 KΩ
5	649 KΩ	162 KΩ
6	590 KΩ	118 KΩ
8	931 KΩ	133 KΩ
10	953 KΩ	105 KΩ
12	374 KΩ	34 KΩ
14	649 KΩ	49.9 KΩ
16	750 KΩ	49.9 KΩ

Configuring the MCV Input

Battery over-voltage protection is accomplished by comparing V_{CELL} to the voltage on the MCV input pin. If V_{CELL} becomes greater than V_{MCV}, both charging and top-offterminate.

A typical MCV value is 1.8V for NiCd and NiMH batteries. The MCV voltage is derived from either of the networks shown in Figure 4. The combined network haa the advantage of fewer resistors in generating both the MCV and TCO thresholds, but loses the independence of threshold adjustment.

To detect the presence of a battery, the DC supply voltage must be larger than MCV * N + V_{LOSST}, where V_{LOSST} is defined as the trickle charging path voltage loss and N is the V_{BAT} divisor.

Temperature Sensing and the TCO Pin

The bq2003 uses the temperature sense input on the TS pin to qualify charge initiation and termination. A negative temperature coefficient (NTC) thermistor referenced to SNS and placed in close proximity to the battery may be used as a temperature-to-voltagetransducer as shown in Figure 1. This example shows a simple linearization network constituted by RT1 and RT2 in conjunction with the thermistor, RT. If this temperature sensor is to be used for charge control, it should be directly in contact with the cells.

Temperature-decision thresholds are defiied as LTF (low-temperature fault), HTF (hot-temperature fault), and TCO (temperature cutoff). Charge action initiation is inhibited if the temperature is outside the LTF-to-HTF range. In this case, the temperature fault indicator on TEMP is driven low, and charging does not initiate until the battery temperature is within range.

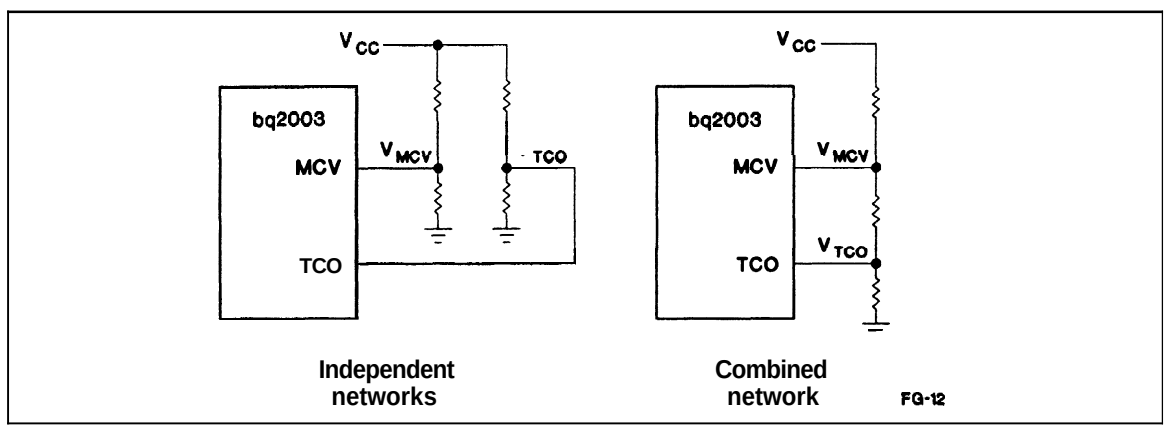


Figure 4. Threshold Networks

Once initiated, charging terminates if the temperature is either less than LTF or greater than TCO. The bq2003 interprets the reference points V_{LTF}, V_{HTF}, and V_{TCO} as V_{SS}-referenced voltages, with V_{LTF} fixed at 2/5 V_{CC} and V_{TCO} equal to the voltage presented on the TCO pin. See Figure 5. Note that since the voltage on pin TS decreases as temperature increases, V_{TCO} should always be less than 2/5 V_{CC}. V_{HTF} is set internally 7/8 of the way from V_{LTF} to V_{TCO}. The resistive dividers shown in Figure 4 may be used to generate the desired V_{TCO}.

Note: HTF is not meaningful for bq2003 switching current regulation chargers. See the Application Note, 'Step-Down Switching Current Regulation Using the bq2003 Fast Charge IC.'

ΔT/Δt detection adds an additional constraint on the selection of temperature sense components. Detection occurs when the voltage TS − SNS declines at a rate between 0.0024 V_{CC} and 0.0040 V_{CC} per 68 seconds, with a nominal 5V V_{CC} producing a nominal detection rate of 14mV/min (16mV/68sec). For example, assuming a 1°C/min desired average ΔT/Δt detection rate ($T_{\Delta T}$), and minimum and maximum charge temperatures of 0" and 40°C, respectively, V_{TCO} equals:

$$V_{TCO} = (2 \bullet V_{CC}/5) - (0.0028 \bullet V_{CC} \bullet (T_{TCO} - T_{LTF}))$$

$$= 2 - (0.014 \bullet (40 - 0))$$

$$= 1.44V$$

Table 3 shows the temperature control values that apply for Application Examples 1 and 2, assuming the Fenwal part number 197-103LA6-A01 thermistor. Appendix A explains the derivation of such component values.

New ΔT/Δt samples are processed every 34 seconds. To minimize the risk of premature termination, the design

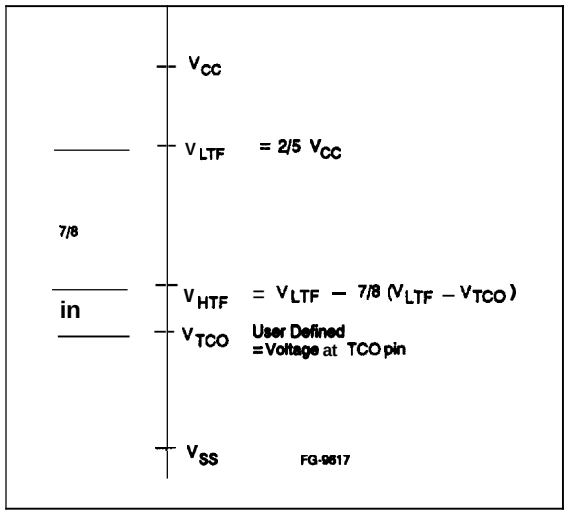


Figure 5. Temperature Reference Points

should be co gured assuming a minimum charge cutoff rate of 0.0024 • V_{CC}, or 10.6mV per minute (at 25°C; V_{CC} = 5V). This is the lowest signal that may be recognized as meeting the decision threshold. Repeating samples cause a decision quickly as the voltage ramps between this minimum threshold and the nominal 14mV per minute. The system is self-compensating in that the thermistor provides increasingly overstated negative voltage change with increasing temperature, making the measurement more sensitive at higher temperatures. The last three columns of Table 3 are an example of this relationship.

Table 3. Example Values, Temperature Sense Network

LTF (°C)	HTF (°C)	TCO	V_{TCO} (V)	RT1 (KΩ)	RT2 (KΩ)	$T_{\Delta T}$ (°C/min)	Minimum-to-Nominal ΔT/Δt Rate (°C/min) @ 25°C	@ 35°C	@ 45°C
10	47	50	1.50	3.65	2.80	1.04	0.94–1.26	0.75–1.00	0.64–0.85

Notes: 1. V_{SR} = OV.
2. Temperature control and qualification may be disabled by tying pin TCO to V_{SS} and fixing the voltage on pin TS to 0.1 • Vcc.

Vcc Supply

The Vcc apply provides both power and voltage reference to the bq2003. This reference directly affects BAT voltage and internal time-base voltage measurements.

A 5% or tighter tolerance on Vcc is recommended to minimize the error regarding MCV. For example, if MCV nominal is set to be 1.8V per cell, a 5% error on Vcc results in MCV = 1.71V to 1.89V. This range is acceptable from the perspective that an MCV charge termination represents a faulty battery. The minimum MCV must be safely above a "healthy" charging voltage. The maximum MCV must satisfy the requirement to recognize battery removed/replaced (see the section, "Configuring the MCV Input').

The time-base is trimmed during manufacturing to within 5 percent of the typical value with Vcc = 5V. The oscillator varies directly with Vcc. If, for example, a 6% regulator supplies Vcc, the time-base could be in error by as much as 10%.

Trickle Resistor

The trickle resistor, R10, is sized to limit the constant trickle current, IT.

$$R10 = (V_{DC} - V_{BAT}) / I_T$$

The resistance of R10 is calculated using IT = charge current desired after full (typically a C/20 to C/50 rate, possibly lees) and the voltage for a fully charged battery (number of cells • 1.4V).

The wattage rating of R10 must accommodate periods of higher IT when V_{BAT} is at a lower voltage (no fast-charge pending charge qualification).

A very low trickle current contributes to longer battery life, and is particularly critical for NiMH cells.

Top-Off Charge

The top-off charge option allows for the self-discharge replacement trickle current to be very low, but still provides for filling up the last fraction of capacity after the fast-charge phase has terminated. Top-off occurs at a 1/8 pulsed rate to prevent excess heat generation, and terminates after a period equal to the safety time-out. It also terminates if TCO or MCV is detected

Top-off is not recommended in applications where a battery charge is re-initiated with extremely high frequency (many times per day); for example, when the unit is returned to the charge cradle after each short period of use.

Negative Delta Voltage Fast-Charge Detection

-AV full-charge detection may operate in parallel with the A t detection. If temperature control is disabled by design, then -AV should be enabled (DVEN to Vcc). If -ΔV is enabled, a constant-current charging source is required. Otherwise a drop in current may cause a false -ΔV determination. DVEN may change state at any time.

Mode Selection Pins TM1 and TM2

These two pins are used to select the safety time-out (5 selections, 23 to 360 minutes) and optional top-off charge (4 selections, 23 to 180 minutes, equal to the safety time selection).

The safety time-out should be selected to be longer than any reasonably expected charge time. The nominal charge time (Ahr capacity/charge rate) must be factored up to allow for both charge inefficiency and the fact that many batteries hold more than the rated charge. A safety time-out 1.3–1.5 times the nominal time is normally adequate (i.e., 90 minutes for a 1C charge). The safety time-out may be far in excess of the nominal charge time if the temperature monitor is enabled.

Note: If the charge rate varies (such as fast charging during system operation using ΔT/Δt termination), then the safety time-out selection should allow for the slowest charges that may occur. The 180- or 360-minute selection may be appropriate.

System-Controlled Charge Inhibition

Some in-system chargers may require the ability to block fast charge activity when the system is on.

Two small 1N4148-type diodes—with cathodes connected outside the R-C filter—control the bq2003 BAT and TS inputs to provide this capability. A high signal (INHIBIT) applied to anodes of theae diodes blocks charge activity. See Figure 8.

With a high signal applied to BAT and TS, charge is inhibited and both LEDs are off. INHIBIT must be high for longer than t_{MCV} max (300ms) if a subsequent low state is to initiate charge.

INHIBIT muld be the system V_{CC}, blocking fast charge at all times the system is ON. This may be needed if -AV termination is to be used and the charge supply cannot simultaneously support fast charge and peak system loads.

INHIBIT might also be CPU-controlled, allowing the charger to be inhibited as required by specific situations.

Power Supply Selection

The DC supply voltage, V_{DC}, muet satisfy two requirements:

1. To support the bq2003 V_{CC} supply, V_{DC} muet be adequate to provide for 5V regulation after the losses in the regulator and across D1 ($V_{DC} \geq 7.7V$ using the 78L05).
2. To support the charge operation, $V_{DC} >$ (number of cells • MCV_{MAX}) + V_{LOSS} in the charging path. (MCV_{MAX} is the maximum cell voltage threshold with the maximum bq2003 V_{CC}.)

Polarity Reversal Protection

If the DC input has any risk of being accidentally connected with power (+) and ground (–) reversed, then the system input should include either a protection diode to protect against circuit damage or a diode bridge to provide both protection and operation. This also increases minimum input voltage for charger operation by approximately 1V to 2V.

Layout Guidelines

PCB layout to minimize the impact of system noise on the bq2003 is important when the bq2003 is used as a switching modulator, with a separate nearby switching regulator, or close to any other significant noise source.

1. Avoid mixing signal and power grounds by using a single-point ground technique incorporating both a small signal ground path and a power ground path.
2. The charging path components and associated traces should be kept relatively isolated from the bq2003 and its supporting components.
3. 0.1µF and 10µF decoupling capacitors should be placed close together and very close to the Vcc pin.
4. 0.1µF capacitors and resistors forming R-C filters connected to pins BAT, TS, TCO, and MCV should be as close as possible to their associated pins.
5. Because the bq2003 uses Vcc for its reference, additional loading on Vcc is not recommended.
6. Diode D1 (1N4148) is recommended for rectification and firing.
7. If the DCMD input is electronically controlled, care should be taken to prevent noise-induced false transitions.
8. For bq2003-modulated switching applications:
   - A 2KR resistor is required between the MOD pin and the transistor.
   - A 1000pF capacitor/1KΩ resistor R-C filter should be as close as possible to the SNS pin.
   - The 0.1µF capacitors for BAT and TS should be routed directly to SNS and not to ground.

Figures 6 and 7 show an example layout of the non-power path circuits in the "kernel board' available from Benchmarq. Figure 8 is a schematic of the board. Table 4 contains the parts list for the board. A comparable layout is recommended.

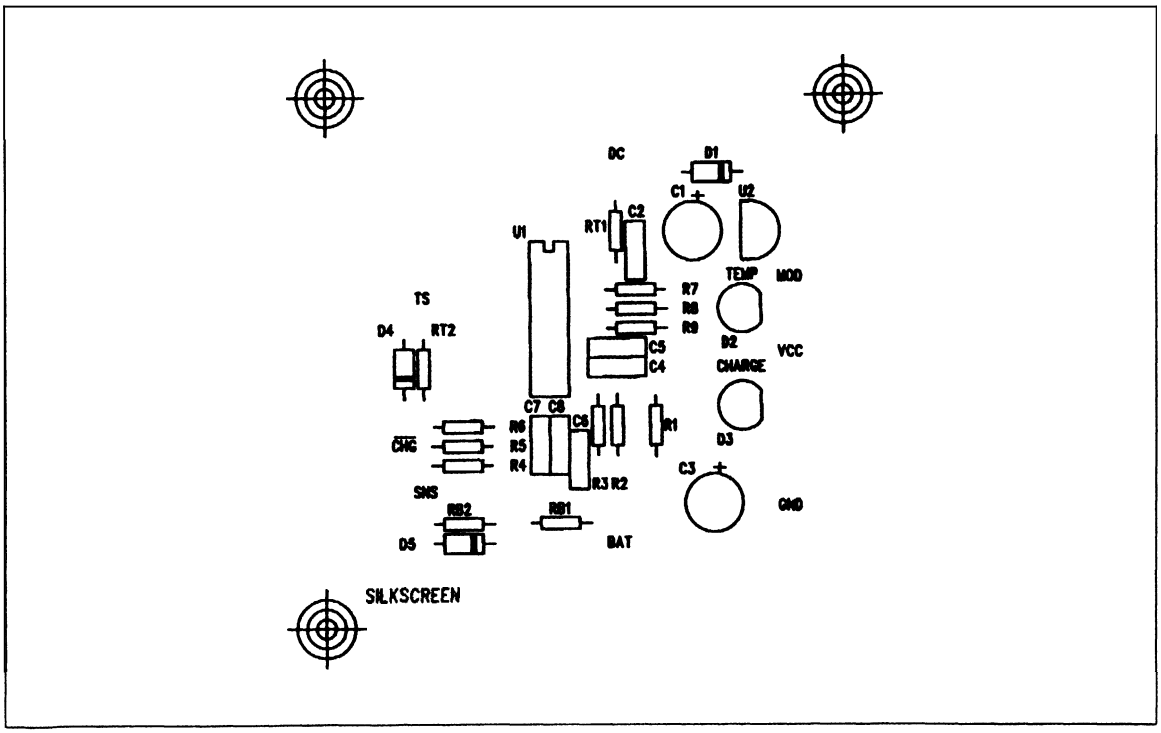


Figure 6. bq2003 Kernel Board Layout, Component Placement

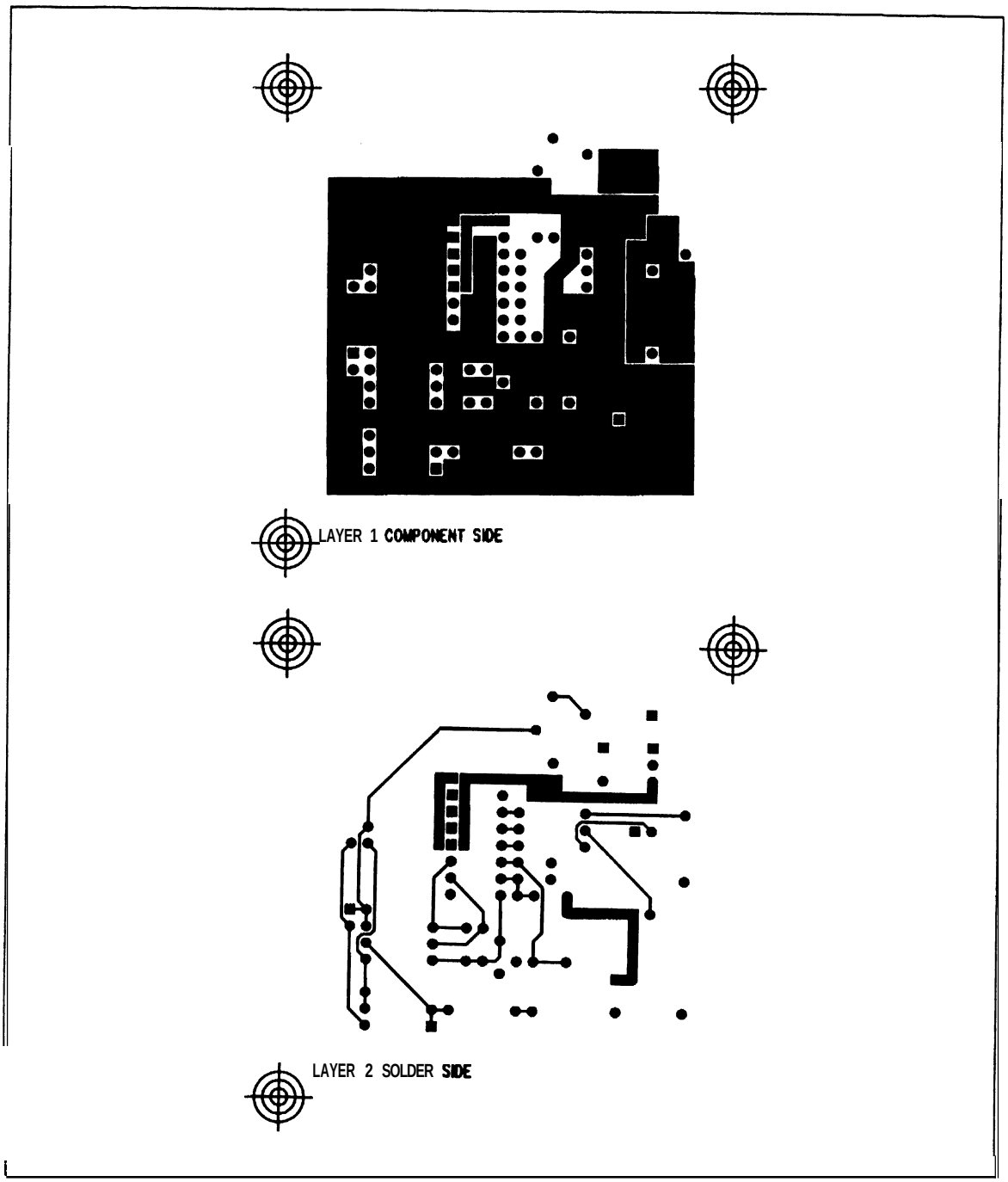


Figure 7. bq2003 Kernel Board Layout

Table 4. bq2003 Kernel Board Parts List

Component Name	Component Description
C1	10µF 50V electrolytic
C2, C4, C5, C7, C8	0.1µF ceramic
C3	10µF 7V electrolytic
C6	1000pF ceramic
D1, D4, D5	1N4148
D2, D3	HLMP 4700 red LED
R1	User-defined 1% ¼W or ⅛W carbon film
R2	User-defined 1% ¼W or ⅛W carbon film
R3	User-defined 1% ¼W or ⅛W carbon film
R4, R7, R8, R9	1KΩ 5% ¼W or ⅛W carbon film
R5, R6	100KΩ 5% ¼W or ⅛W carbon film
RB1	User-defined 1% ¼W or ⅛W carbon film
RB2	User-defined 1% ¼W or ⅛W carbon film
RT1	Ueer-defined 1% ¼W or ⅛W carbon film
RT2	User-defined 1% ¼W or ⅛W carbon film
U1	bq2003
U2	LM78L05ACZ

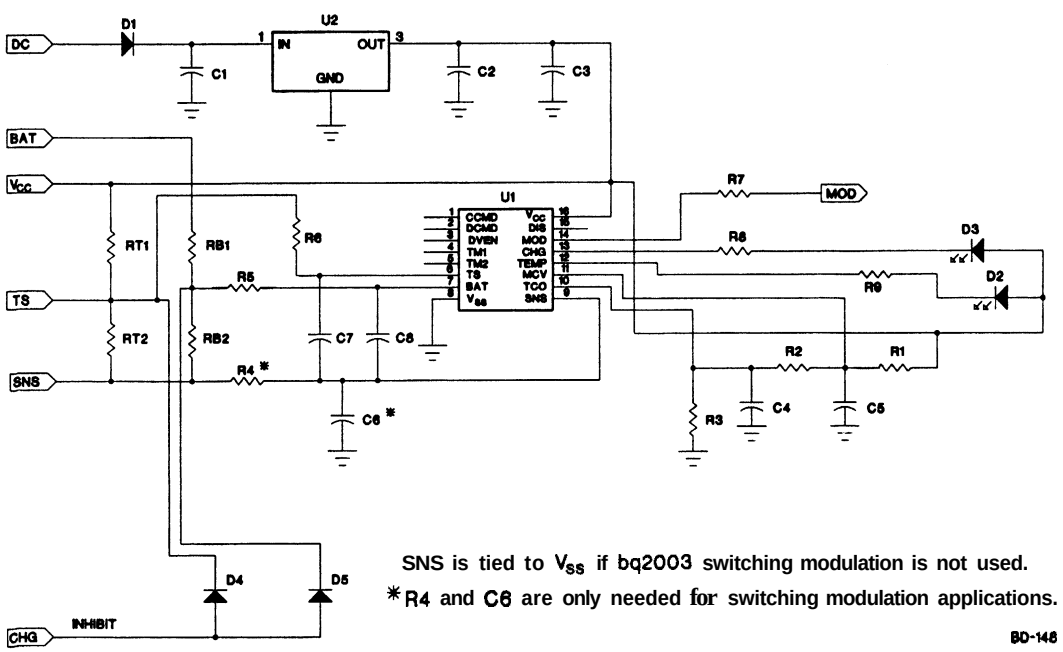


Figure 8. bq2003 Kernel Board Schematic

Application Example 1: Linear Regulator

In the example in Figure 9, the bq2003 is used to implement a linear regulator/charge controller that can charge 4 to 12 NiCd or NiMH cells with current regulated up to 1.5A. R_{16} determines the charge rate per the formula:

$$I = 1.25V / R_{16}$$

Charge is initiated on battery replaced or Vcc valid. -AV detection is enabled (DVEN high), and discharge control is disabled (DCMD low). MCV = 1.8V; LTF = 10°C; HTF = 47°C; TCO = 50°C; $T_{\Delta T}$ (average $\Delta T/\Delta t$) = 1.04°C/ minute. Timer-mode selection (see data sheet) and trickle resistor R10 selection (see page 7) are determined by the designer.

Components to complete this schematic may be selected from the preceding table:

- Table 2: BAT network RB1 and RB2 values

Table 5 contains the parts list for the board.

Notes: (1) Temperature control and qualification may be disabled by tying pin TCO to Vss and fixing the voltage on pin TS to 0.1 • Vcc.

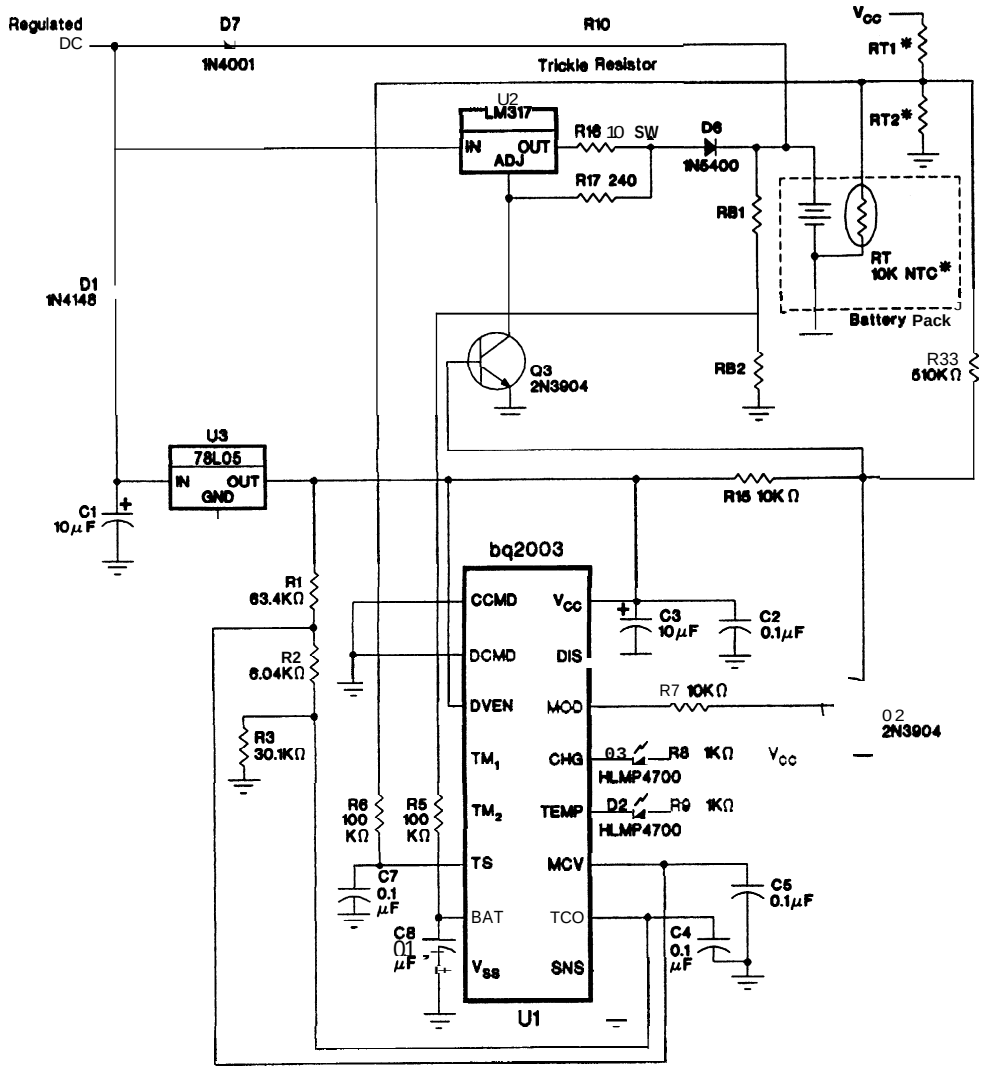
(2) The voltage drop (V_{LOSS}) across LM317, D6, and R16 is 4.25V minimum. The charging supply voltage must be greater than the following:

Number of cells • max. cell voltage + V_{LOSS}

The maximum allowable power loss across the LM317 depends on the heat sinking.

Table 5. Linear Regulator/Charge Controller Board Parts List

Component Name	Component Description
C1	10µF 50V electrolytic
C2, C4, C5, C7, C8	0.1µF ceramic
C3	10µF 7V electrolytic
D1	1N4148 or equivalent
D2, D3	HLMP 4700 red LED
D6	1N5400
D7	1N4001
Q2, Q3	2N3904
R1	63.4KΩ 1% ¼W or ⅛W carbon film
R2	6.04KΩ 1% ¼W or ⅛W carbon film
R3	30.1KΩ 1% ¼W or ⅛W carbon film
R5, R6	100KΩ 5% ¼W or ⅛W carbon film
R7, R15	10KΩ 5% ¼W or ⅛W carbon film
R8, R9	1.0KΩ 5% ¼W or ⅛W carbon film
R10	User-defined 5% carbon film
R16	1Ω 1% 3W carbon film
R17	240Ω 5% ¼W or ⅛W carbon film
R33	510KΩ 5% ¼W or ⅛W carbon film
RB1	User-defined 1% ¼W or ⅛W carbon film
RB2	User-defined 1% ¼W or ⅛W carbon film
RT	Negative temperature coefficient (NTC) thermistor (see Figure 9)
RT1	1% ¼W or ⅛W carbon film (see Figure 9)
RT2	1% ¼W or ⅛W carbon film (see Figure 9)
U1	bq2003
U2	LM317T
U3	LM78L05ACZ



TM1, TM2: To V_{CC}, V_{SS}, or float as required. DIS: No connect.

The R-C filters on MCV and TCO are recommended in noisy environments.

* NTC, **RT1,** and RT2:

Thermistor	RT1	RT2
Keystone RL0703-5744-103-SI	3.57K	2.67K
Philips 2322-640-63103	3.65K	2.80K
Fenwal Type 16, 197-103LA6-A01	3.65K	2.80K

BD-135.2

Figure 9. Linear Regulator/Charge Controller

Application Example 2: Gated External Current Source

In the example in Figure 10, the bq2003 is used to gate an external current-limited or regulated charge source that can charge NiCd or NiMH cells.

Charge is initiated on battery replaced or Vcc valid. -ΔV detection is enabled (DVEN high), and discharge control is disabled (DCMD low). MCV = 1.8V; LTF = 10°C; HTF = 47°C; TCO = 50°C; $T_{\Delta T}$ (average $\Delta T/\Delta t$) = 1.04°C/ minute. Timer-mode selection (see data sheet) and trickle resistor R10 selection (see page 7) are determined by the designer.

Components to complete this schematic may be selected from these preceding tables:

- Table 1: Power switch Q1
- Table 2: BAT network RB1 and RB2 values

Table 5 contains the parts list for the board.

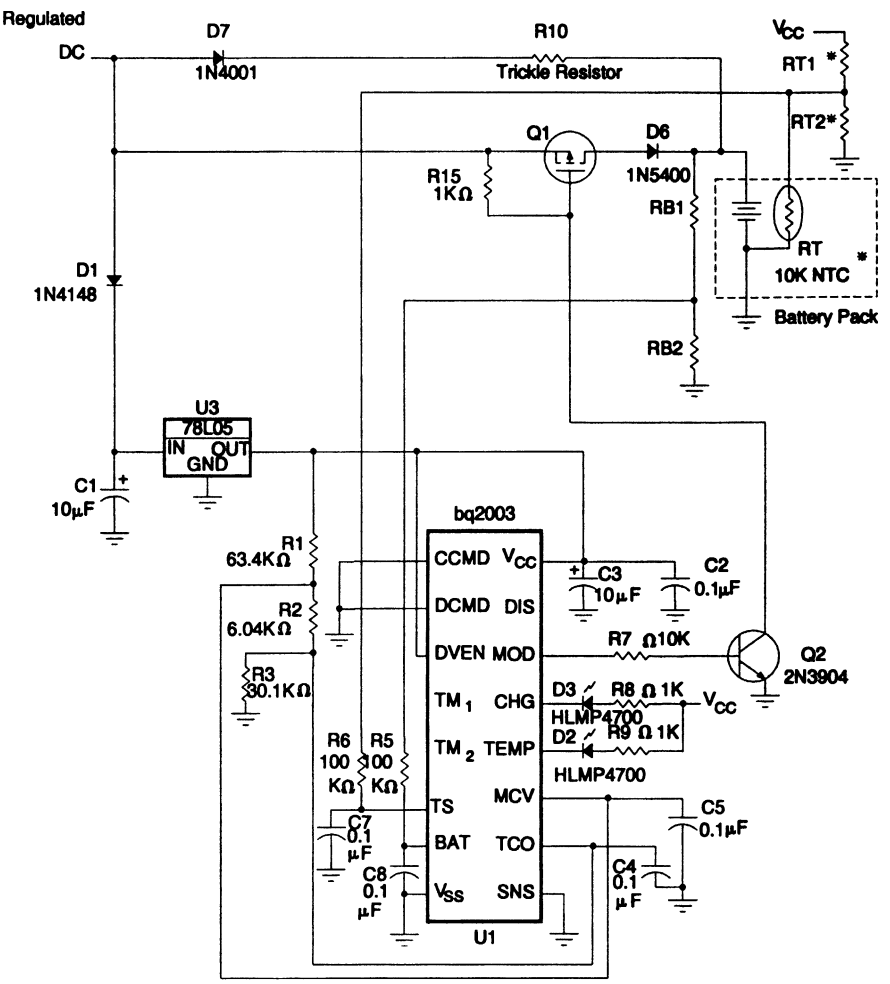
Notes: (1) Temperature control and qualification may be disabled by tying pin TCO to V_{SS} and fixing the voltage on pin TS to 0.1 * V_{CC}.

(2) The charging supply voltage must be greater than the following:

Number of cells * max. cell voltage + V_{LOSS}

Table 6. Gated External Current Source Board Parts List

Component Name	Component Description
C1	10µF 50V electrolytic
C2, C4, C5, C7, C8	0.1µF ceramic
C3	10µF 7V electrolytic
D1	1N4148 or equivalent
D2, D3	HLMP 4700 red LED
D6	
D7	1N4001
Q1	User-defined pFET
Q2	2N3904
R1	63.4kΩ 1% ¼W or ⅛W carbon film
R2	6.04kΩ 1% ¼W or ⅛W carbon film
R3	30.1kΩ 1% ¼W or ⅛W carbon film
R5, R6	100kΩ 5% ¼W or ⅛W carbon film
R7	10kΩ 5% ¼W or ⅛W carbon film
R8, R9, R15	1kΩ 5% ¼W or ⅛W carbon film
R10	User-defined 5% carbon film
RB1	User-defined 1% ¼W or ⅛W carbon film
RB2	User-defined 1% ¼W or ⅛W carbon film
RT	Negative temperature coefficient (NTC) thermistor (see Figure 10)
RT1	1% ¼W or ⅛W carbon film (see Figure 10)
RT2	1% ¼W or ⅛W carbon film (see Figure 10)
U1	bq2003
U3	LM78L05ACZ



TM1, TM2: To V_{CC}, V_{SS}, or float as required. DIS: No *connect*

The R-C filters on MCV and TCO are recommended in noisy environments.

* NTC, RT1, and RT2:

Thermistor	RT1	RT2
Keystone RL0703-5744-103-S1	3.57K	2.67K
Philips 2322-640-63103	3.65K	2.80K
Fenwal Type 16; 197-103LA6-A01	3.65K	2.80K

BD-137

Figure 10. Gating External Current Source

Appendix A
Determining Temperature-Control Component Values

The bq2003 uses a negative temperature coefficient (NTC) thermistor to determine temperature. The ΔT/Δt sensitivity can be adjusted using different resistor values (RT1 and RT2 in Figure 1 and Application Example 1 and 2) and a different high-temperature cutoff voltage. Table A-1 lists various thermistor manufacturers, with the appropriate part numbers.

Follow these steps to determine temperature-control component values (see Figure 5 on page 6):

1a. The low-temperature fault (LTF) limit for charging must be established. LTF for charging is determined by the battery specification and the charge rate used. A typical value for the low-temperature limit is 10°C.

b. V_{LTF} is set within the bq2003 at 0.4 • Vcc.

2a. The high-temperature cutoff (TCO) for charging must be established. TCO for charging is determined by the battery specification, the charge rate, and the heat dissipation of the system. Typical values range from 40°C to 50°C, although values outside this range may be applicable.

b. The average ΔT/Δt sensitivity from LTF to TCO ($T_{\Delta T}$, expressed as °C/minute) for termination must be established. As mentioned in this application note, the bq2003 provides a typical ΔT/Δt charge termination of 14 mV per minute. The TAT value is determined by the battery specification, the charge rate, and the heat dissipation of the system. Typical nominal values for TAT range from 0.75°C/min to 1.5°C/min.

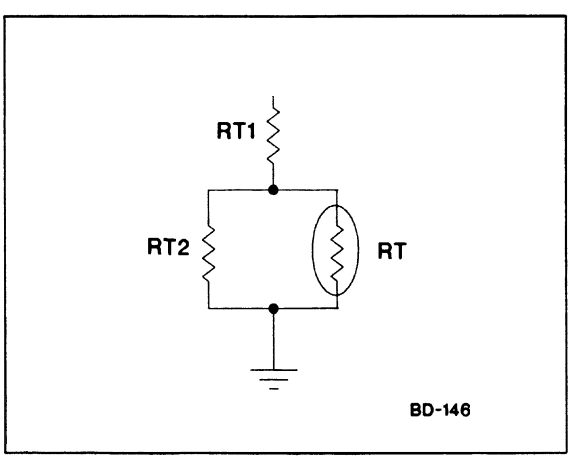


Figure A-1. Resistor Network

Relative to the average value TAT, the minimum-to-maximum range of ΔT/Δt at a specific temperature depends on two parameters:

- The measurement resolution of the bq2003, which contributes a ± 25% error.
- The non-linearity of the thermistor between LTF and TCO. As the temperature nears LTF, the expected ΔT/Δt is less than $T_{\Delta T}$ (less sensitive), and as the temperature nears TCO, the expected ΔT/Δt is more than $T_{\Delta T}$ (more sensitive).

The ΔT/Δt range should be considered in determining the nominal TAT. Nominal TAT should be selected so that its minimum value represents an acceptable (non-premature) termination threshold. Thus a fist bq2003 sample does not cause a premature termination. Multiple sampling ensures that the termination occurs well before the TAT max.

c. The high-temperature cutoff voltage, V_{TCO}, must be established. This V_{TCO} limit is determined by the TAT and may be calculated by:

$$V_{TCO} = 2 \cdot V_{CC}/5 - 0.0028 \cdot V_{CC} \cdot (TCO - LTF)/T_{\Delta T}$$

V_{TCO} is provided at the TCO pin by a resistor-divider network as shown in Figures 9 and 10: $V_{TCO} = V_{CC} \cdot R3/(R1 + R2 + R3)$. In this arrangement, R1 and R2 are selected such that MCV = Vcc • (R2 + R3)/(R1 + R2 + R3).

4. Select the thermistor to be used. If it is not from Table A-1, the thermistor sensitivity at 25°C should be at least 4%/°C and the ΔR steps between 30°C and 50°C should be comparable to or greater than those in Table A-1 to obtain the appropriate accuracy. Lower values affect the linearity of the ΔT/Δt.

5. Determine the thermistor resistance at LTF and TCO (R_{LTF} and R_{TCO}, respectively). This may be done using the thermistor temperature versus resistance conversion table provided with the thermistor specification. These tables are usually in 5°C increments.

6. The values for RT1 and RT2 may be calculated by:

$$T1 = R_{LTF} \cdot (1 - (2/V_{CC}))/(2/V_{CC})$$

$$T2 = R_{TCO} \cdot (1 - (V_{TCO}/(V_{CC} - V_{SNS})))/(V_{TCO}/(V_{CC} - V_{SNS}))$$

$$RT2 = ((T2 \cdot R_{LTF}) - (T1 \cdot R_{TCO}))/(T1 - T2)$$

$$RT1 = (RT2 \cdot T1)/(R_{LTF} + RT2)$$

Table A-1. 10K NTC Thermistor Types and Resistance Values

Temperature (°C)	Nominal Resistance (Ω) at Temperature			
	Keystone Carbon Co. RL0703-5744-103-S1 (Tel: 814/781-1591)	Philips Components 232284063103 (Tel: 407/743-2112)	Fenwal Electronics Type 16; 197-103LA6-A01 (Tel: 508/478-6000)	Thermometrics C100Y103J (Tel: 908/287-2870)
-30	188172	173900	177000	-
-25	138043	128500	-	-
-20	102263	95890	970700	-
-15	76461	72230	-	-
-10	57672	54890	55330	-
-5	43864	42070	-	-
0	33630	32510	32650	29588
5	25988	25310	-	23515
10	20243	19860	19900	18813
15	15889	15690	-	15148
20	12562	12490	12490	12271
25	10000	10000	10000	10000
30	8013	8060	8057	8195
35	6461	6536	-	6752
40	5241	5331	5327	5593
45	4276	4373	-	4656
50	3507	3606	3603	3894
55	2894	2989	-	3273
60	2400	2490	2488	2762
65	2001	2085	-	2342
70	1677	1753	1752	1993.7
75	1412	1481	-	1704.0
80	1194	1256	1258	1462.0
85	1014	1070	-	1259.1
90	865.2	915.5	917.7	1088.3
95	741.0	786.1	-	943.9
100	636.9	677.5	680.0	821.4

Application Note Revision History

Change No.	Page No.	Description	Nature of Change
1	13, 15	Changed thermistor values on Figures 9 and 10	Correction
1	12-15	Added component R33 to Figure 9 and Table 5 and R33 and D17 to Figure 10 and Table 6	Correction for cold temperature charge initiation
1	15	Corrected R1 value	Was 6.34K; is 63.4K

Note: Change 1 = Dec. 1992 B changes from Oct. 1992 A.

BENCHMARQ

Step-Down Switching Current Regulation Using the bq2003 Fast Charge IC

1

Introduction

This application note describes the use of the bq2003 Fast Charge IC as the modulator in a buck-type switch-mode regulator to fast charge NiCd and NiMH batteries. Please refer to the application note entitled "Using the bq2003 to Control Fast Charge' for a discussion of bq2003 charge control operation and for descriptions of non-switch-mode applications that gate current-limited sources to control battery charging.

Examples for additional applications are being developed. Please contact Benchmarq if your application is not supported by one of these examples.

The bq2003 is targeted for applications requiring state-of-the-& fast-charging performance at minimal cost. It provides sophisticated full-charge detection techniques such as ΔT/Δt (delta temperature/delta time) and -ΔV (negative delta voltage) that enable the user to take advantage of advanced battery technologies such as nickel metal-hydride (NiMH) and high-capacity fast-charge nickel cadmium (NiCd). Systems using the bq2003 can be easily upgraded from NiCd batteries to NiMH batteries without system redesign.

Background

The bq2003 may serve as a controller to provide a switch-mode current source configuration for battery charging. Switch-mode current source regulation is much more efficient than linear current-limited regulators.

The electrical and thermal requirements of the application determine the configuration used with the bq2003. If the charge supply is either current- or power-limited at a level compatible with fast charging the battery, switch-mode operation may not be needed. The use of a gated current configuration as described in "Using the bq2003 to Control Fast Charge' is most likely more economical.

If the charge current in a switch-mode application is less than 3A, a p-channel MOSFET buck-type power stage is generally recommended. This is desirable because of the minimal number of support components required for the bq2003. If the switch-mode charge current is above 3A, using an n-channel FET may be more economical. Several small signal support components must be added for gate drive of the n-channel MOSFET.

Thermal packaging requirements are often the practical limits in electronic design. Basic thermal management or component thermal stress/reliability issues can affect an otherwise successful product. The use of switching power-conversion techniques results in dramatically less heat being generated in the product.

A comparison of power loss demonstrates the advantage of switch-mode control versus linear control. Either may be used to charge a four-C-cell NiCd battery pack from a 12V DC source at a rate of 2A. Loss in the switch-mode circuit may be held below 2W, whereaa loss in the linear circuit can be above 12W.

Operational Aspects

In Figures 1 and 2, the bq2003 MOD pin controls the switching transistor Q1. In the switch-mode operation, the SNS pin is driven by the high side of the sense resistor R26. The current waveform of the inductor ie represented by a voltage waveform across R26. MOD transitions from high to low after SNS ramps up to 0.250V and from low to high after SNS ramps down to 0.220V. This action sustains a self-referenced oscillation about these two thresholds.

Both V_{TS} and V_{BAT} are referenced to V_{SNS} by an internal A-to-D converter. For this reason, both the TS and BAT pine must be well-coupled to SNS using the associated capacitors (C7 and C8) and resistors (R5 and R6). If the waveforms at TS and BAT are viewed with an oscilloscope, the AC content found at SNS is seen at TS and BAT. This is normal.

A resistor (R7) is placed in series with the Q3 gate to drive a small signal-switching FET, Q3. Internal bq2003 noise is lowered with this resistor in place.

V_{LTF}, V_{HTF}, and V_{TCO} are voltage-reference points monitored on the TS pin to qualify charge initiation and termination on temperature. Operation of the bq2003 in a non-switch-mode application is described fully in the application note entitled "Using the bq2003 to Control Fast Charge.'

When the bq2003 is used as a switch-mode controller, the application of these reference points is somewhat different:

- Prior to charge initiation, $V_{SNS} = V_{SS}$.
- While charging, V_{SNS} (average) = 0.235V.

Because the bq2003 internal A-to-D converter measures differentially between V_{TS} and V_{SNS}, component selection for temperature qualification of charge initiation must be done assuming V_{SNS} = OV, and component selection for temperature qualification of charge termination must be done assuming V_{SNS} = 0.235V.

V_{TS} is the voltage at the node of RT1, RT2, and the thermistor. The voltage is derived from reference V_{CC} (5V) by RT1 connected to V_{CC} and RT2 in parallel with the thermistor connected to SNS. Prior to charging, the voltage being divided is V_{CC}. When switching regulation is active, the bottom side of RT2 and the thermistor is biased positively by 0.235V, reducing the reference voltage to 4.65V.

Because V_{TCO} and V_{LTF} are both referenced to Vcc, V_{TS} for a particular temperature represents a colder temperature when the switch-mode is inactive than when the switch-mode is active. This effect could negate the HTF charge initiation qualification threshold. V_{HTF} is $\frac{1}{8} \cdot V_{LTF} + \frac{7}{8} \cdot V_{TCO}$. V_{TCO} is a threshold selected for use when the switch-mode is active. V_{LTF} is internally fixed at 0.4 • V_{CC}. The values of RT1, RT2, and the thermistor that define the LTF temperature (charging off) also define the TCO temperature (switch mode on). The resulting HTF temperature with charging off approaches or may even be above the TCO temperature (switch mode on), limiting the uselfulness of HTF to qualify the start of charge.

The bq2003 bQuick™ design disk is available to optimize these component values and thresholds for specific application objectives.

P-Channel MOSFET Buck-Topology Switch-Mode Charger

In this example, the bq2003 is used to implement a switching regulator/charge controller that can charge 4 to 12 NiCd or NiMH cells with current regulated up to 3A.

Figure 1 is a standard configuration for a pFET switch-mode charger. MOD drives a small signal DMOS FET, Q3. When MOD is high, Q3 is on, turning on Q1 via the path through D8 and D9.

L1 inductor current ramps up linearly while MOD is high. L1 current is in series with the battery and R26. The resulting voltage across R26, V_{SNS}, is delivered via R4 to C6 at the SNS pin. The L1 inductor current ramps up linearly until V_{SNS} reaches 0.250V, at which time MOD goes low and Q1 turns off. A flux reversal occurs in L1, causing D10 to conduct. Charge is now being transferred from L1 into the battery. The L1 current ramps down linearly until V_{SNS} reaches 0.220V. At this point the cycle repeats with MOD going high.

For input voltages that are higher than the rated Q1 safe operating gate voltage, Zener diode D9 can be placed in series with the drain lead of Q3. The Zener voltage should be sized to allow full Q1 enhancement while Q3 is conducting. See Table 1.

Capacitor C9 is used to provide a low-impedance for the Q1 source lead. Without C9 in place, Q1 can be connected to an overly inductive voltage supply. D6 is a blocking diode that keeps the battery from discharging via U2 during removal of the DC power source input.

Table 1. Lookup Table for D9 Selection

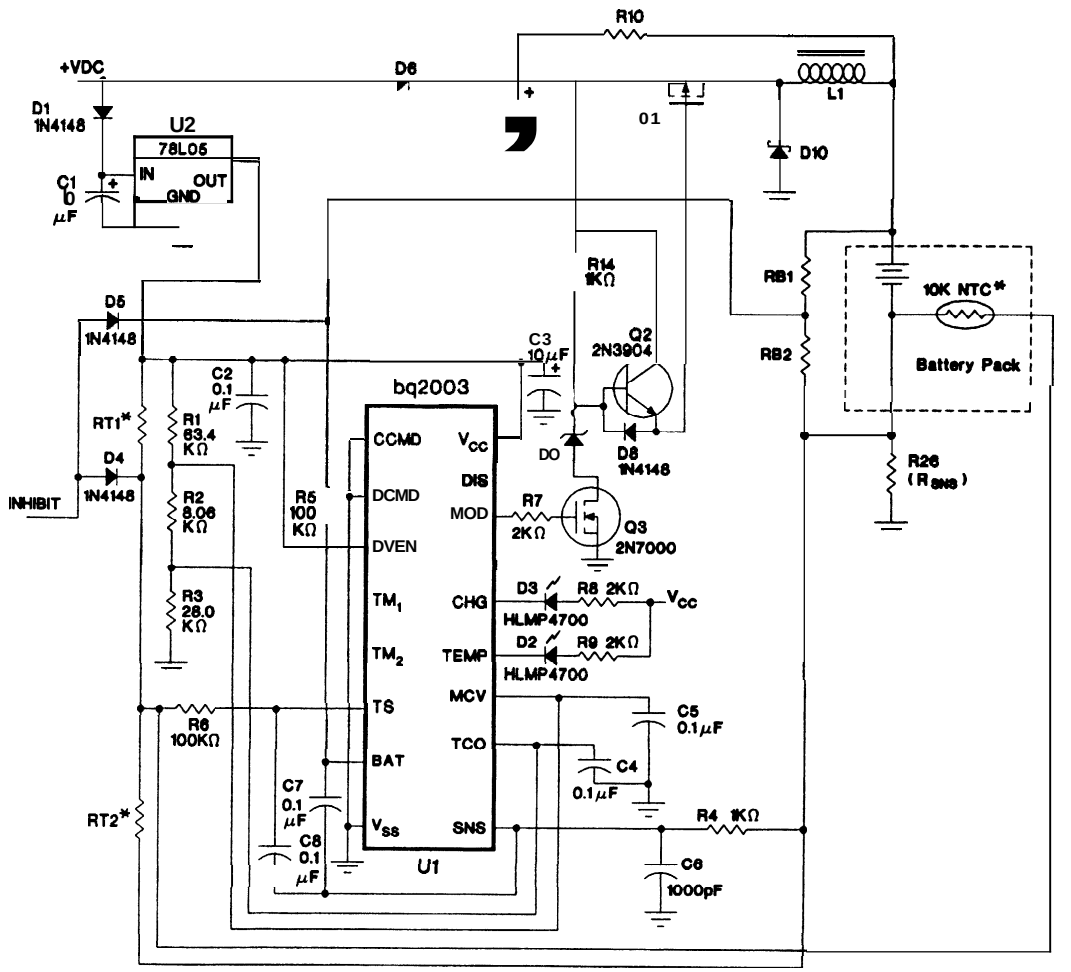
+VDC Input (Volts)	Motorola Part No.	Nominal Zener Voltage
Below 15	Shorted	0
15–18	1N749	4.3
18–21	1N755	7.5
21–24	1N758	10
24–27	1N964A	13
27–30	1N966A	16
30–32	1N967A	18
32–35	1N968A	20

Charge is initiated on battery replaced or V_{CC} valid. -AV detection is enabled (DVEN high), and discharge control is disabled (DCMD low). MCV = 1.8V; LTF = 10°C; TCO = 50°C; $\Delta T/\Delta t$ at 30°C = 0.82°C/min. (i.e., typical = 1.10°C/min.). Timer-mode selection (see data sheet) and trickle resistor R10 selection (see page 2-85 of the application note entitled "Using the bq2003 to Control Fast Charge") are determined by the designer. R26 is selected such that I_{CHG} • R26 = 0.235V.

The values of RB1 and RB2 to complete this schematic may be selected from Table 2 in the application note entitled "Using the bq2003 to Control Fast Charge."

Note: Temperature control and qualification may be disabled by tying the TCO pin to V_{SS} and fixing the voltage on the TS pin to 0.1 * V_{CC}.

Table 2 lists suggested components for different-rate chargers. Table 3 lists other components shown in Figure 1.



DIS: No connect.

* NTC, RT1, and RT2:

Thermistor	RT1	RT2
Keystone RL0703-5744-103-S1	3.83K	2.94K
Philips 2322-640-63103	4.02K	3.09K
Fenwal Type 16, 197-103LA6-A01	4.02K	3.09K

BD-169

Figure 1. P-Channel MOSFET Switching-Mode Charger

Table 2. Suggested Components—P-Channel MOSFET Charger

Suggested Max. Charging Current	Q1	D6	D10	C9	L1
1A	IRF9Z14	1N4001	1N5818	ECA-1VFQ390 39µF/35V/460mΩESR	30 turns, #26 AWG, wound on Magnetics, Inc., P/N 77040 core; nominal inductance 59µH; GFS Mfg., Inc., P/N 92-2156-1
2A	IRF9Z24	1N5821	1N5821	ECA-1VFQ560 56µF/35V/300mΩESR	37 turns, #22 AWG, wound on Magnetics, Inc., P/N 77120 core; nominal inductance 98µH; GFS Mfg., Inc., P/N 92-2157-1
3A	IRF9Z34	1N5821	1N5821	ECA-1VFQ121 120µF/35V/170mΩESR	
Source	International Rectifier	Motorola	Motorola	Panasonic	GFS Mfg., Inc. Dover, NH (603) 742-4375

Table 3. Other Components—P-Channel MOSFET Charger

Component Name	Component Description
C1	10µF 35V electrolytic
C2, C4, C5, C7, C8	0.1µF ceramic
C3	10µF 10V electrolytic
C6	1000pF ceramic
D1, D4, D5, D8	1N4148
D2, D3	HLMP 4700 red LED
Q2	2N3904
Q3	2N7000
R1, R2, R3	User-defined 1% ¼W or ⅛W
R4	1KΩ 5% ¼W
R5, R6	100KΩ 5% ¼W or ⅛W
R7, R8, R9	2KΩ 5% ¼W or ⅛W
R10, R26	User-defined
RB1	User-defined 1% ¼W or ⅛W
RB2	User-defined 1% ¼W or ⅛W
RT1	User-defined 1% ¼W or ⅛W
RT2	User-defined 1% ¼W or ⅛W
U1	bq2003
U2	LM78L05ACZ

N-Channel MOSFET Buck-Topology Switch-Mode Charger

The advantage of an n-FET buck topology is the price-versus-performance benefit of the n-FET family. The disadvantage is the number of additional components required to support it.

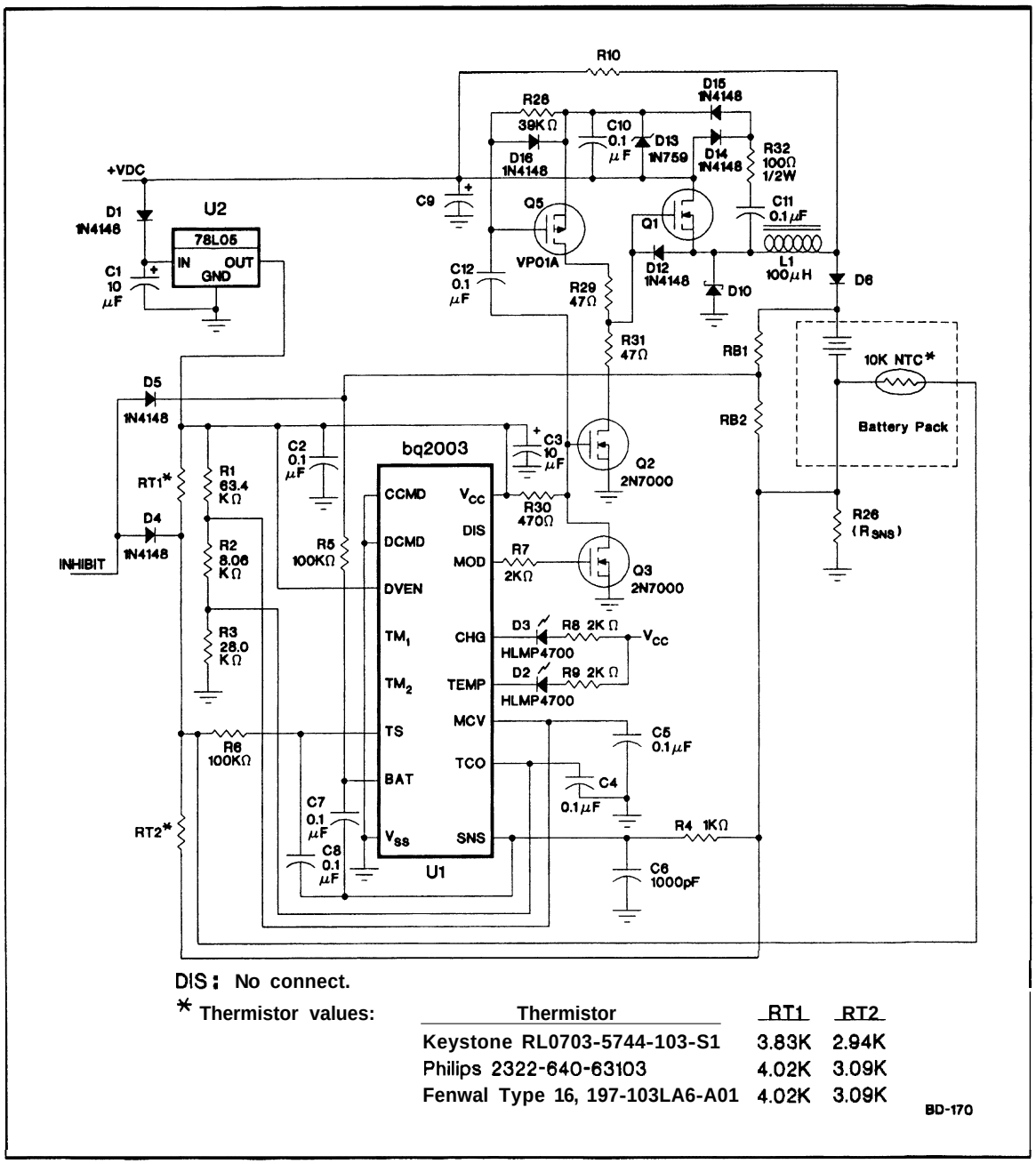
The schematic in *Figure* 2 is a standard configuration for an nFET switch-mode charger that can charge 4 to 12 NiCd or NiMH cells with current regulated up to 9A. The Q1 gate must be driven positive with respect to the drain in this application to provide full enhancement of the device. When catch diode D10 is conducting, C11 is charged. When Q1 is conducting, C11 is charging C10. This charge pump allows adequate voltage to drive Q1 into full enhancement via QS. As Q2 conducts, the Q1 gate charge is depleted, causing Q1 to turn off.

Charge is initiated on battery replaced or Vcc valid. -AV detection is disabled (DVEN low), and discharge control is disabled (DCMD low). MCV = 1.8V; LTF = 10°C; TCO = 50°C; $\Delta T/\Delta t$ at 30°C = 0.82°C/min. (i.e., typical = 1.10°C/min.). Timer-mode selection (see data sheet) and trickle resistor R10 selection (see page 2-85 of the application note entitled "Using the bq2003 to Control Fast Charge? are determined by the designer. R26 is selected such that $I_{CHG} \cdot R26 = 0.235V$.

The values for RB1 and RB2 to complete this schematic may be selected from Table 2 in the application note entitled "Using the bq2003 to Control Fast Charge."

Note: Temperature control and qualification may be disabled by tying the TCO pin to Vss and fixing the voltage on TS pin to 0.1 * Vcc.

Table 4 lists suggested components for different-rate chargers. Table 5 lists other components shown in Figure 2



DIS: No connect.

* Thermistor values:

Thermistor	RT1	RT2
Keystone RL0703-5744-103-S1	3.83K	2.94K
Philips 2322-640-63103	4.02K	3.09K
Fenwal Type 16, 197-103LA6-A01	4.02K	3.09K

BD-170

Figure 2. N-Channel MOSFET Switching-Mode Charger

Table 4. Suggested Components–N-Channel MOSFET Charger

Suggested Max. Charging Current	Q1	D6	D10	C9	L1
3A	IRFZ34	1N5821	1N5821	ECA-1VFQ121 120µF/35V/170mΩESR	37 turns, #22 AWG, wound on Magnetics, Inc., P/N 77120 core; nominal inductance 98µH; GFS Mfg.. Inc., P/N 92-2157-1
6A	IRFZ44	MBR735	MBR735	ECA-1VFQ391 390µF/35V/55mΩESR	33 turns, #18 AWG, wound on Magnetics, Inc., P/N 77310 core; nominal inductance 98µH; GFS Mfg., Inc., P/N 92-2158-1
9A	IRFZ48	MBR1035	MBR1035	ECA-1VFQ681 680µF/35V/34mΩESR	25 turns, #16 AWG, wound on Magnetics, Inc., P/N 77930 core; nominal inductance 98µH; GFS Mfg., Inc., P/N 92-2159-1
Source	International Rectifier	Motorola	Motorola	Panasonic	GFS Mfg., Inc. Dover, NH (603) 742-4375

Table 5. Other Components—N-Channel MOSFET Charger

Component Name	Component Description
C1	10µF 35V electrolytic
C2, C4, C5, C7, C8, C10, C11, C12	0.1µF ceramic
C3	10µF 10V electrolytic
C6	1000pF ceramic
D1, D12, D14, D15, D16	1N4148
D2, D3	HLMP 4700 red LED
D13	1N759 12V 500mW Zener
Q2, Q3	2N7000
Q5	VP01A
R1, R2, R3	User-defined 1% ¼W or ⅛W
R4	1KΩ 5% ¼W or ⅛W
R5, R6	100KΩ 5% ¼W or ⅛W
R7, R8, R9	2KΩ 5% ¼W or ⅛W
R10, R26	User-defined
R28	2.7KΩ 5% ¼W or ⅛W
R29, R31	47KΩ 5% ¼W or ⅛W
R30	470KΩ 5% ¼W or ⅛W
R32	100KΩ 5% ½W or ⅛W
RB1	User-defined 1% ¼W or ⅛W
RB2	User-defined 1% ¼W or ⅛W
RT1	User-defined 1% ¼W or ⅛W
RT2	User-defined 1% ¼W or ⅛W
U1	bq2003
U2	LM78L05ACZ

Operating Switching Frequency

During Q1 on-time, the L1 current ramps up linearly. During Q1 off-time (D10 conduction), the L1 current ramps down linearly. The rate of rise and fall (slew rate) of L1 current is determined by the inductance value of L1 and the DC voltage placed across L1. The slew rate is usually different between Q1 conduction time and D10 conduction time. This is because the DC voltage across L1 is usually different during these two timing intervals.

The sum of these two timing intervals equals the switching period. The switching period reciprocal equals the switching frequency.

Use the following equation to estimate the switching frequency.

$$F = \frac{1}{\frac{L\left(\frac{0.030V}{R_{SNS}}\right)}{V_{DC}-(V_{BAT}+V_{SNS}+D6_{VF}+Q1_{DROP})} + \frac{L\left(\frac{0.030V}{R_{SNS}}\right)}{V_{BAT}+V_{SNS}+D10_{VF}}}$$

where:

F = Frequency in Hertz

L = L1 inductance in Henrys

$D6_{VF}$ = D6 average forward voltage drop

$D10_{VF}$ = D10 average forward voltage drop

R_{SNS} = R26 value in ohms

$Q1_{DROP}$ = Charge current times Q1 on-state-resistance

$= (^{0.235V}/_{R_{SNS}})\, Q1_{RDSON}$

V_{DC} = Input DC voltage

V_{BAT} = Battery pack instantaneous voltage

Charge Current Regulation With Varying System Loads

Systems with an integrated charger and a constant-power external supply may not be capable of fast charging the batteries while simultaneously supporting system operation. In such cases the system operation takes priority, and the peak system energy demand must be supported.

In this situation, the charger designer has two options regarding charge during system operation:

1. The battery charging current may be held constant at a low level that is supportable during peak system operation loads. During periods of low system power demand, available power is not used. The charge time during system operation is typically quite long.
2. The battery charging current may be allowed to vary inversely with the system load. As the system power demand decreases, the charge rate increases and vice versa. For portable systems with varying load requirements (such as those using 'power management'), this allows any surplus power during low system activity to be used for battery charging. The charge time during system operation depends on the average system power requirement, not the peak requirement.

Option 1 may be implemented when using the bq2003 as the charge current regulator by using the system Vcc as an "INHIBIT" signal to pull pins BAT and TS high when the system is on. (See Figures 1 and 2 and the System-Controlled Charge Inhibition discussion in 'Using the bq2003 to Control Fast Charge.? When the system is on, fast charge is inhibited. The only charge path is the trickle resistor.

Option 2A may be implemented using the bq2003 as the charge current regulator with the system load return at the high end of the sense resistor R26 (Figure 3). $\Delta T/\Delta t$ charge termination is enabled and -AV termination is disabled.

With a battery pack cell voltage ≥ 1V per cell, the system load always receives its required current. The system load current flows through R26 along with the battery charge current. The battery receives any difference between the programmed charge current and the system load current. If the system load current exceeds the programmed charge current, then no charge current will be delivered to the battery. The system load current biases the SNS voltage via R26, which limits the buck regulator's current delivered to the battery. The total

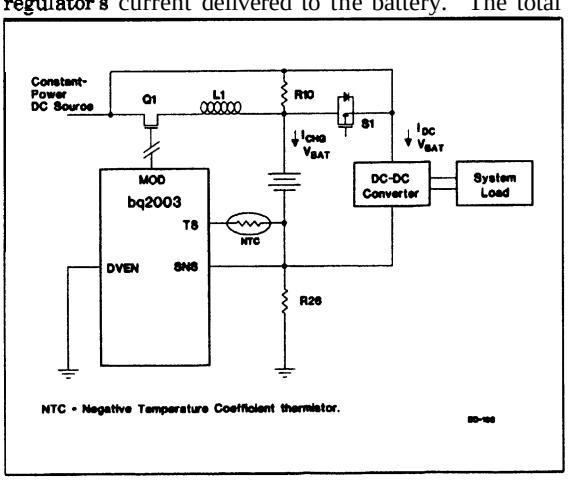


Figure 3. Option 2A

available power may be allocated between the battery charge and system operation such that power used = (I_{CHG} + I_{DC}) • V_{BAT}.

Using this method, the sense resistor R26 and its associated energy penalty are not in the battery discharge path The charge current is regulated in a variable fashion such that R26 • (I_{CHG} + I_{DC}) = 0.235V.

Charge current regulation may occur until I_{DC} • R26 ≥ 0.250V. Above this point, the MOD output is held low (off). When actively switching, the MOD frequency remains very nearly constant.

If the battery voltage is extremely low, the bq2003 does not begin charging until the battery trickle charges to 1V per cell. This protects the system voltage from being pulled down to an inoperable range by a very low battery.

-AV is disabled to prevent false terminations due to the varying charge current and the battery's internal impedance. Slight but significant voltage perturbations at V_{BAT} can cause a false -AV charge termination during variations in battery charge current in this configuration. $\Delta T/\Delta t$, however, is *not* affected by variations in charge current because the battery's physical mass has a relatively slow time constant that naturally integrate all variations.

Switch S1 is turned on for battery operation and off during charge. Switch S1 is driven by appropriate logic defined by the needs of the application. The presence or absence of an input DC power source could control this logic. A Schottky diode is a simpler alternative to S1, but the voltage drop may not be desirable.

Option 2B is another variable charge rate approach (*Figure* 4). This option may be preferred if the available power is considerably more than the maximum I_{CHG} • V_{BAT} (ignoring voltage loss). In the first approach, the system load return is to the high end of the sense resistor R26, limiting the power used to approximately (I_{CHG} + I_{DC}) • V_{BAT}, with I_{CHG} = 0 when I_{DC} ≥ maximum I_{CHG}.

For this second approach to use all the available power, the system load return is at the low end of the sense resistor. This accomplishes the fastest possible charge during system operation, but carries a penalty during battery operation because of the energy and voltage loss from discharge through the sense resistor (or the cost and impedance of a switch to bypass the sense resistor).

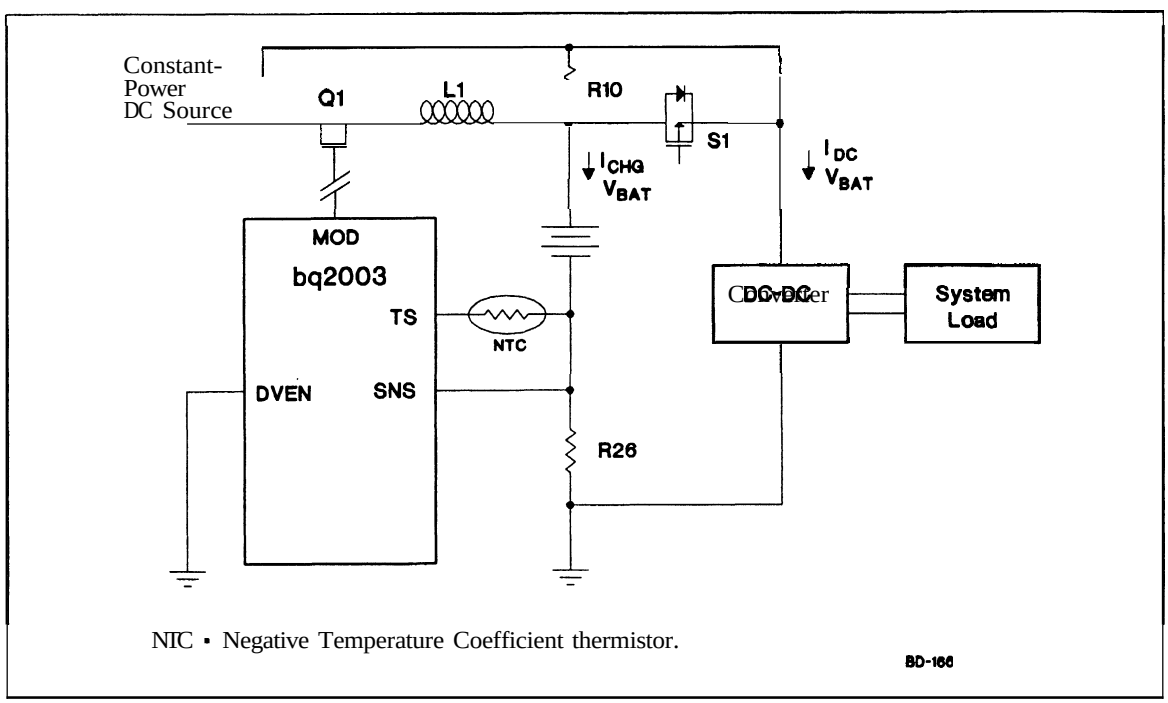


Figure 4. Option 2B

Layout and EMI Considerations

The beat approach to PC board layout follows the strict rule of a single-point ground return. Sharing high current ground with small signal ground causes undesirable noise on the small signal nodes. Referencing Figures 1 and 2, C2 and C3 should be placed as close as possible to the V_{CC} pin. C6 should be placed at the SNS pin. C7 and C8 should be associated between the TS/SNS and the BAT/SNS pins, respectively, with short leads. Isolation resistors R5 and R6 should be placed close to the BAT and TS pins.

Layout of power components C9, D10, L1, Q1, and R26 should reduce lead-length paths between these components to an absolute minimum.

If a dual-layer PC board is used, route signal lines on the solder side. This leavea the component side to be used as a ground plate. This technique reduces noise on adjacent nodes within the circuit and helps reduce EMI by giving the high-energy fields a ground plane to work against.

pFET and nFET Layout Examples

Figures 5–7 illustrate the layout of the p-channel MOSFET switch-mode charger board, and Figures 8–10 illustrate the layout of the n-channel MOSFET switch-mode charger board.

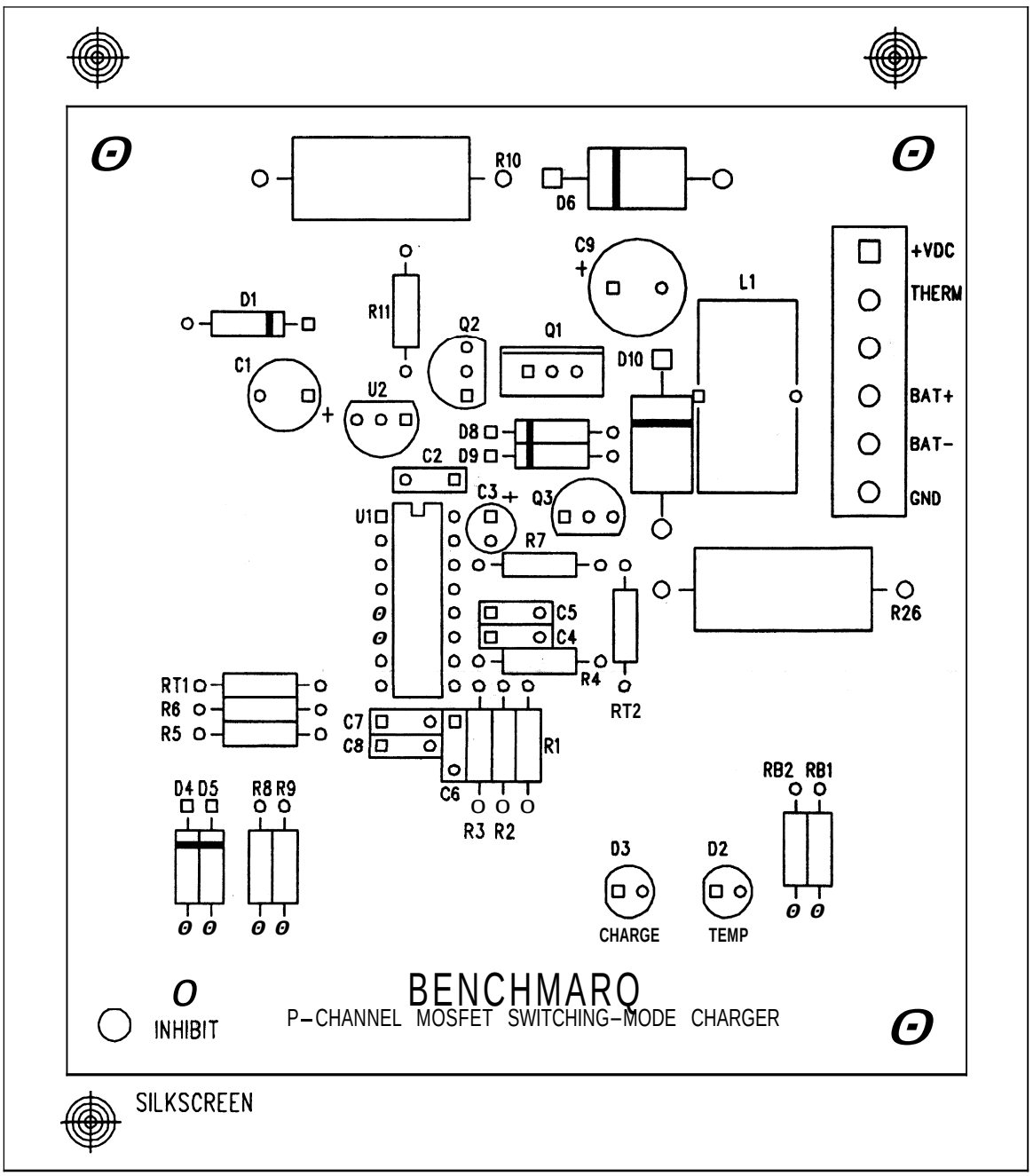


Figure 5. P-Channel MOSFET Switching Charger—Silkscreen

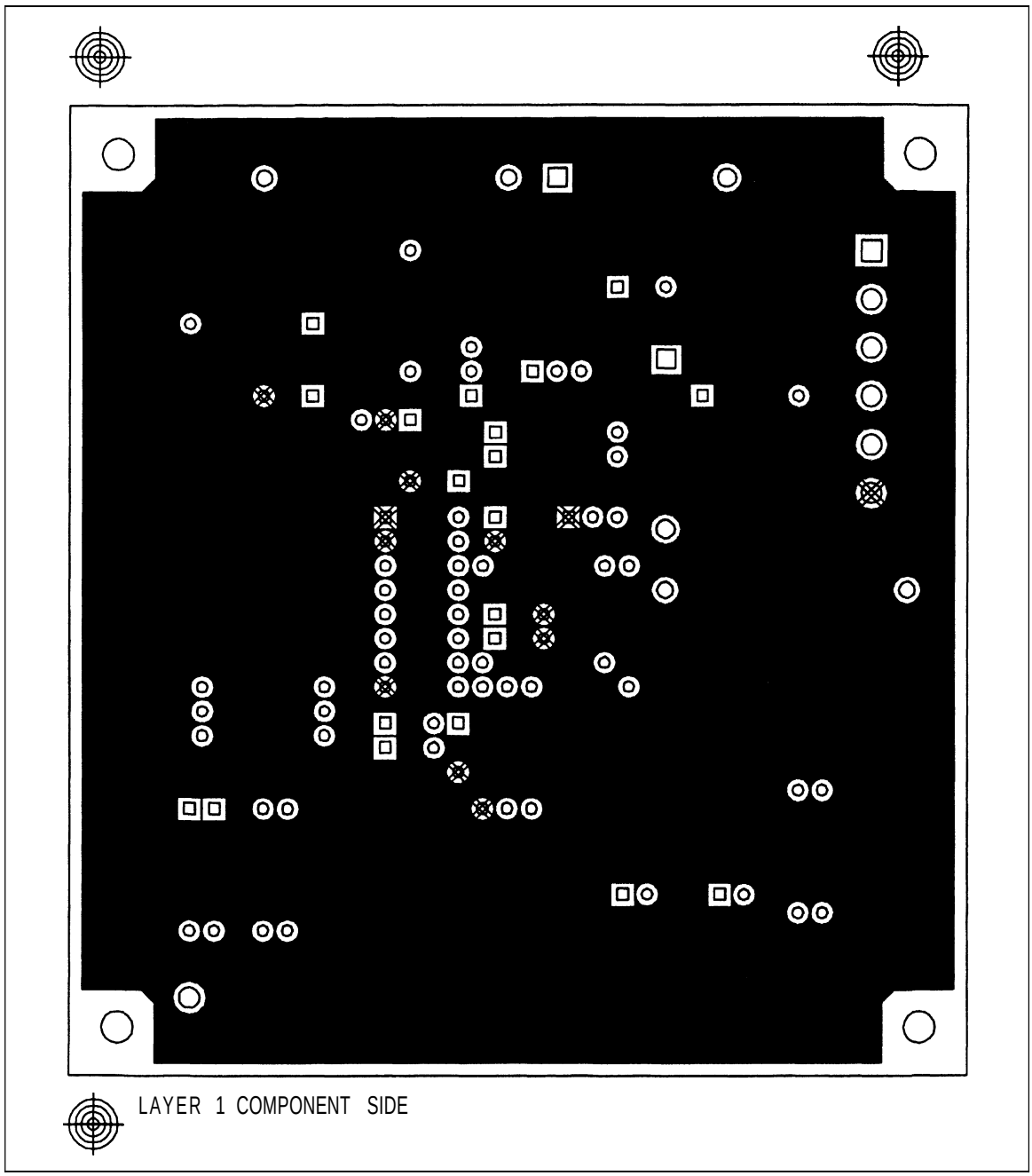


Figure 6. P-Channel MOSFET Switching Charger--Component Side

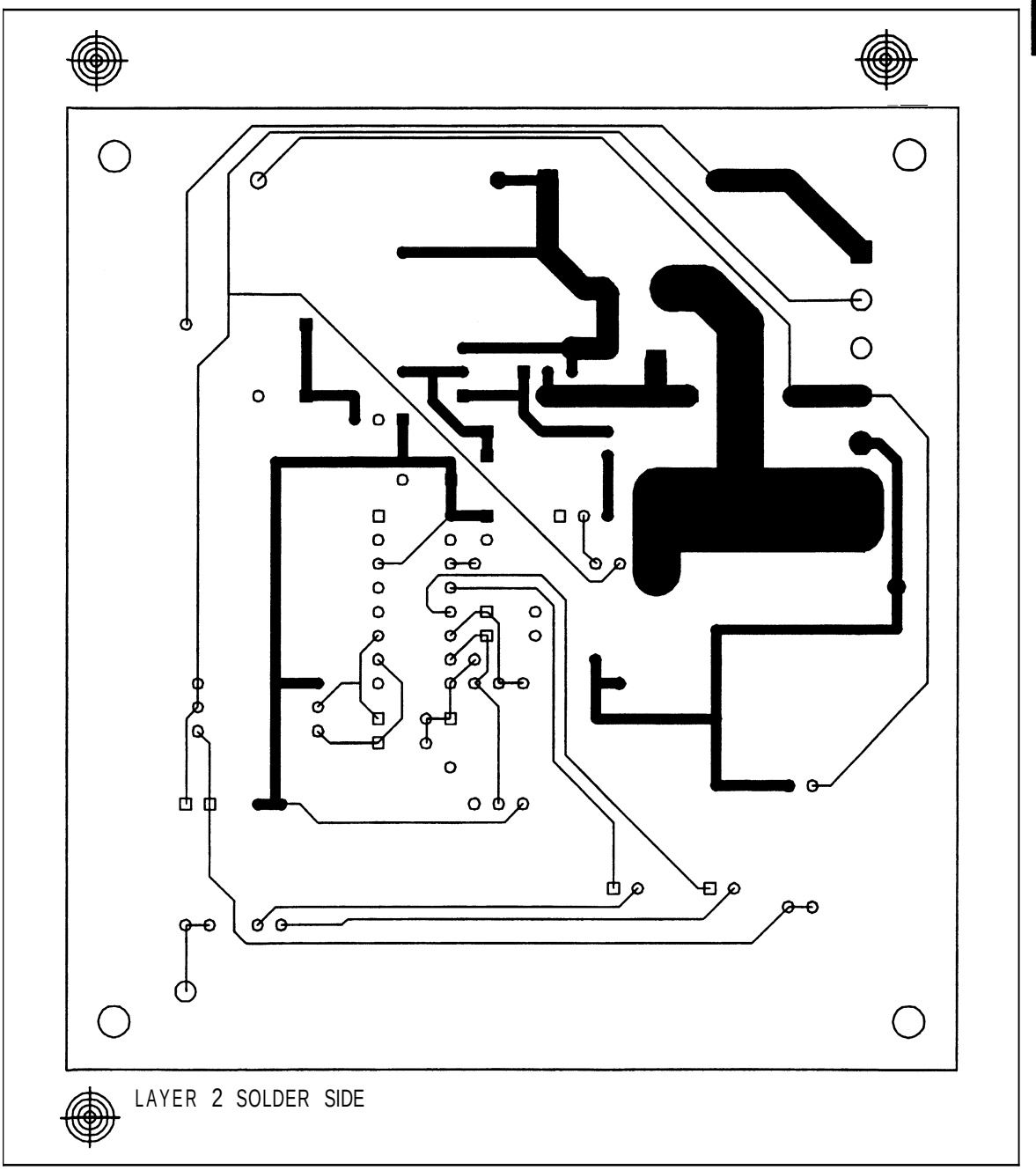


Figure 7. P-Channel MOSFET Switching Charger—Solder Side

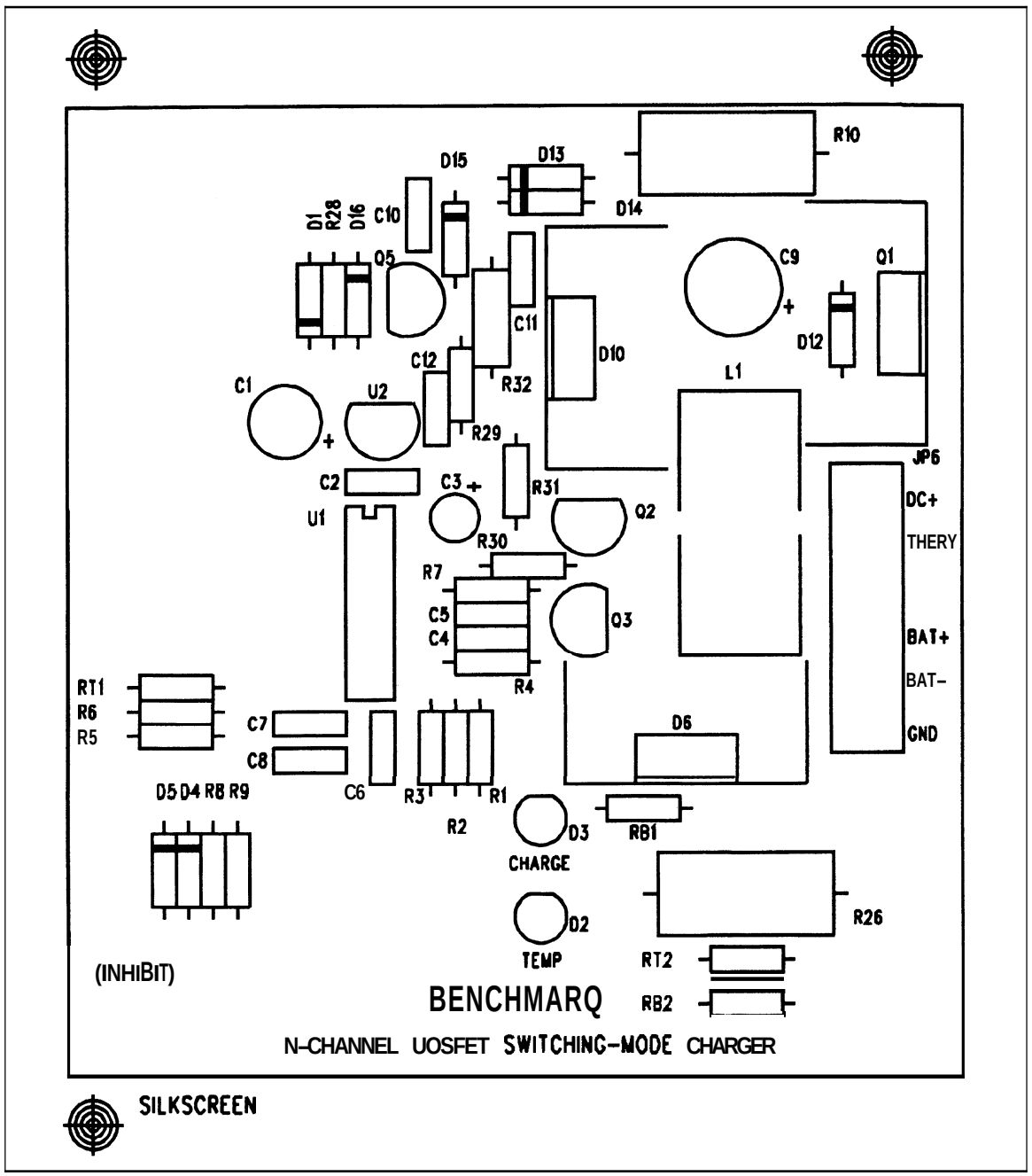


Figure 8. N-Channel MOSFET Switching Charger—Silkscreen

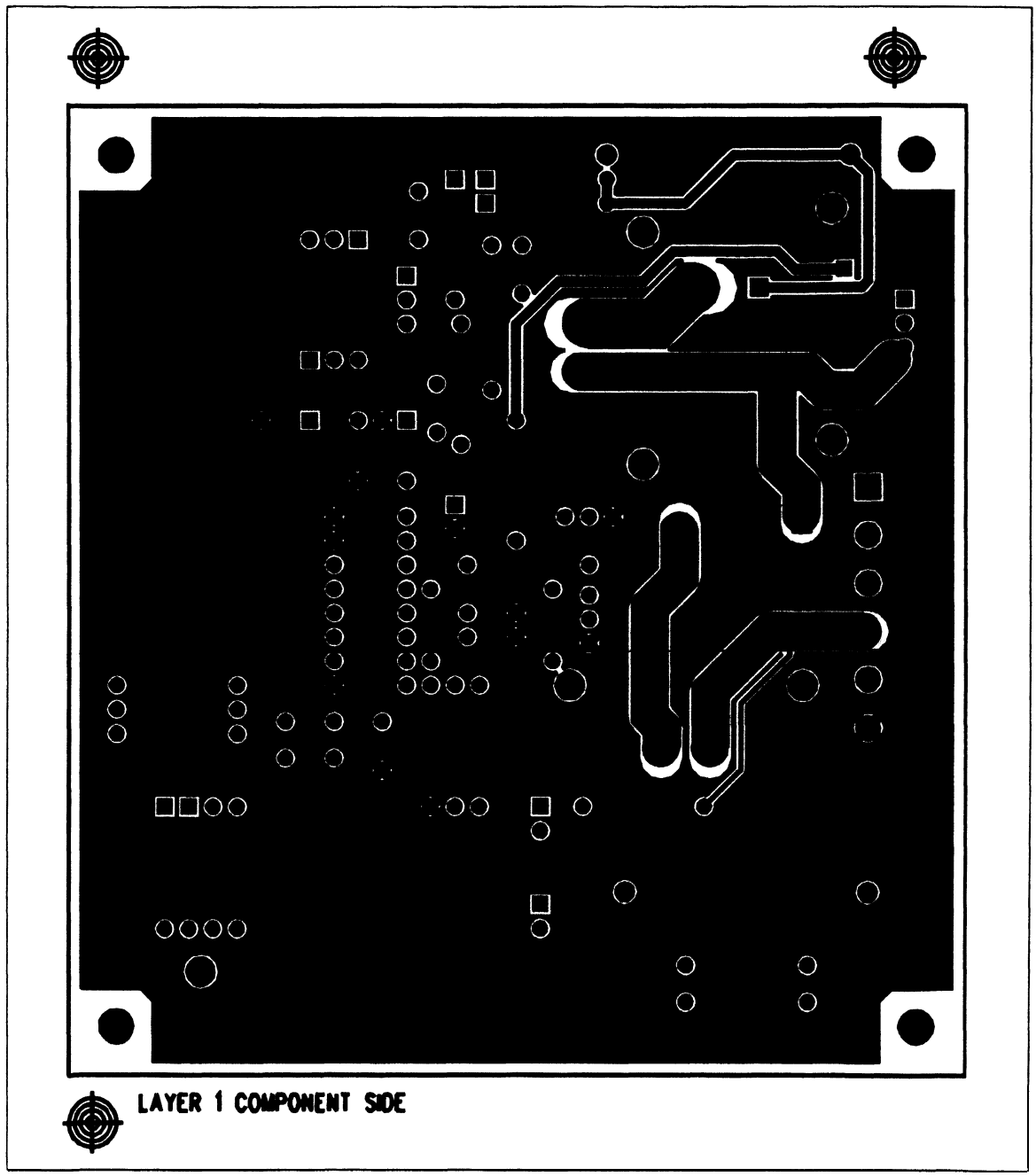


Figure 9. N-Channel MOSFET Switching Charger--Component Side

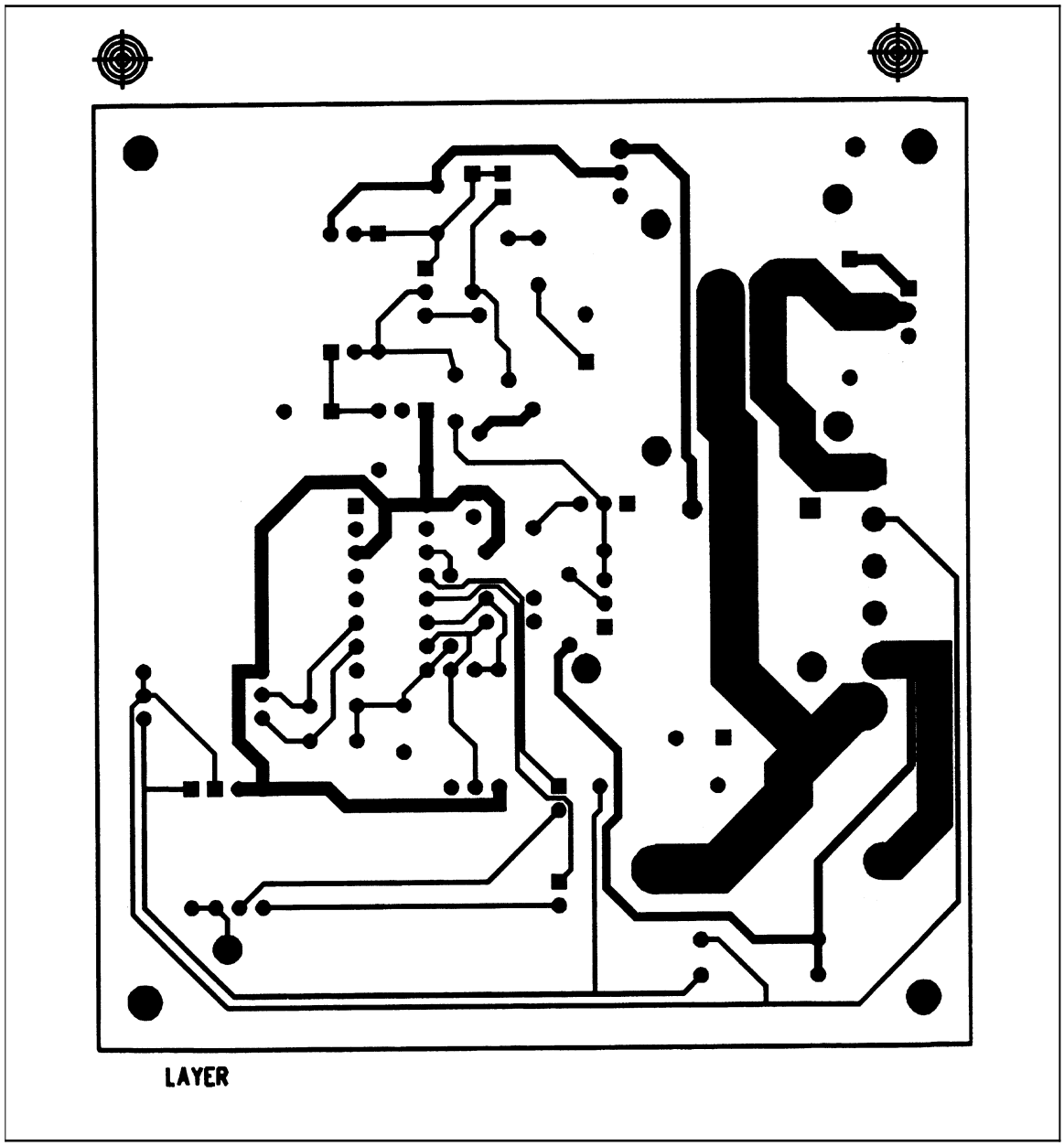


Figure 10. N-Channel MOSFET Switching Charger—Solder Side

BENCHMARQ

Using the bq2003

With High-Side Current Sensing In a Switch-Mode Charger

1

Introduction

This application note describes the use of the bq2003 in special applications that require high-side current sensing. Some system flexibility is gained with high-side current sensing. The DC source, the minus side of the battery, and the system load are all one common ground point. This simplifies the power-grounding architecture in applications such as automotive chargers for radio products.

Such applications may not allow for the standard low-side current sensing as referenced in the application note, "Step-Down Switching Current Regulation Using the bq2003 Fast Charge IC."

The Circuit

The circuit shown in Figure 1 is similar to the circuit described in Figure 1 of the application note, "Step-Down Switching Current Regulation Using the bq2003 Fast Charge IC," with the following exceptions.

The switching element and its associated drive circuitry have been changed to illustrate a high efficiency PNP transistor implementation. You can find a discussion of this circuit in application example 2 for the bq2005. Also note that the 78L05 has been replaced with a simple zener diode plus resistor combination. These two points are unrelated to the use of the bq2003 in a high-side sense mode, but they are important in avoiding confusion over the function of the circuit.

The salient differences between the function of this circuit and that of a normal low-side sense circuit include the following. The sense resietor lies between the inductive element and the positive battery terminal. The negative battery terminal connects to ground. The current signal is translated down to the level required at the SNS input by two small signal transistors forming a "voltagemirror." This "voltage mirror" reflects the voltage across the low ohmic value of the sense resistor onto the much larger 1K resistor in the emittter of a PNP transistor. The transistor pair is biased by a current sink formed by an NPN transistor, the base of which is V_{CC} and the emitter of which connects to ground through an 18K resistor. This arrangement assures that the battery will not be loaded by the bias network when power is not applied and that the best voltage compliance will occur at the regulation current. The collector of the PNP transistor in the "mirror"network will now source the current to pass through a 1K resistor referenced to ground to create the signal required at the SNS input.

Both BAT and TS inputs must be translated up by this same voltage to achieve the proper signal levels for normal operation. Accomplish this action at the BAT input by connecting the battery voltage divider between the more poeitive side of the sense resistor and the 1K termination resietor at the SNS input. Take care to ensure that the total bias current of the battery divider network does not significantly disturb the current regulator operating point (a bias current of 10µA or less would contribute leas than a 4.3% error). Use a voltage translator at the TS input so that the temperature signal tracks the current signal at the SNS input. This action is accomplished by intercepting the sense current signal on its way to the SNS input with the emitter of another PNP transistor, the base of which is biased to the thermistor connection point.

The connection of a 1K resietor in the emitter of this transistor has the effect of translating the TS signal up by the base-emitter drop in the transistor plus the senese current signal voltage. Buffering this point with a complementary NPN transistor subtracts out ı ɛ ter drop, leaving the proper signal to be applied t the TS input. The NPN emitter requires a load resistor which is fulfilled in thie example by a 10K resistor. The PNP transistor can now pass on the current signal to the SNS input of the bq2003 through its collector.

Earlier data books illustrated the way in which to perform this function using an operational amplifier, but the example limited the applicability to certain specific voltage configurations. This circuit is more univerally applicable and can easily be extrapolated to the bq2004, bq2005, and the bq2007.

The nurent-sensing resistor (R12) is placed between the inductor (L1) and the positive side of the battery. To translate the voltage waveform across R12 to the bq2003 SNS pin, a differential amplifier must be used.

The differential amplifier (U3A) is configured with a gain factor of one. Thus, this equation still applies:

$$I_{CHG} = \frac{0.235}{R12}$$

Depending on the application, a protection method to limit the U3A supply voltage may be needed. The TLC272 has a maximum supply voltage of 18 VDC. A small-signal Zener diode (15V nominal, 1N965A) could

also be used to clamp this voltage to a eafe level with a series current-limitingresistor.

Note that the U3A input voltages must always be less than the U3A supply voltage. To help meet this requirement, the four equal-value support resistors associated with U3A provide the secondary function of dividing the input voltages by half.

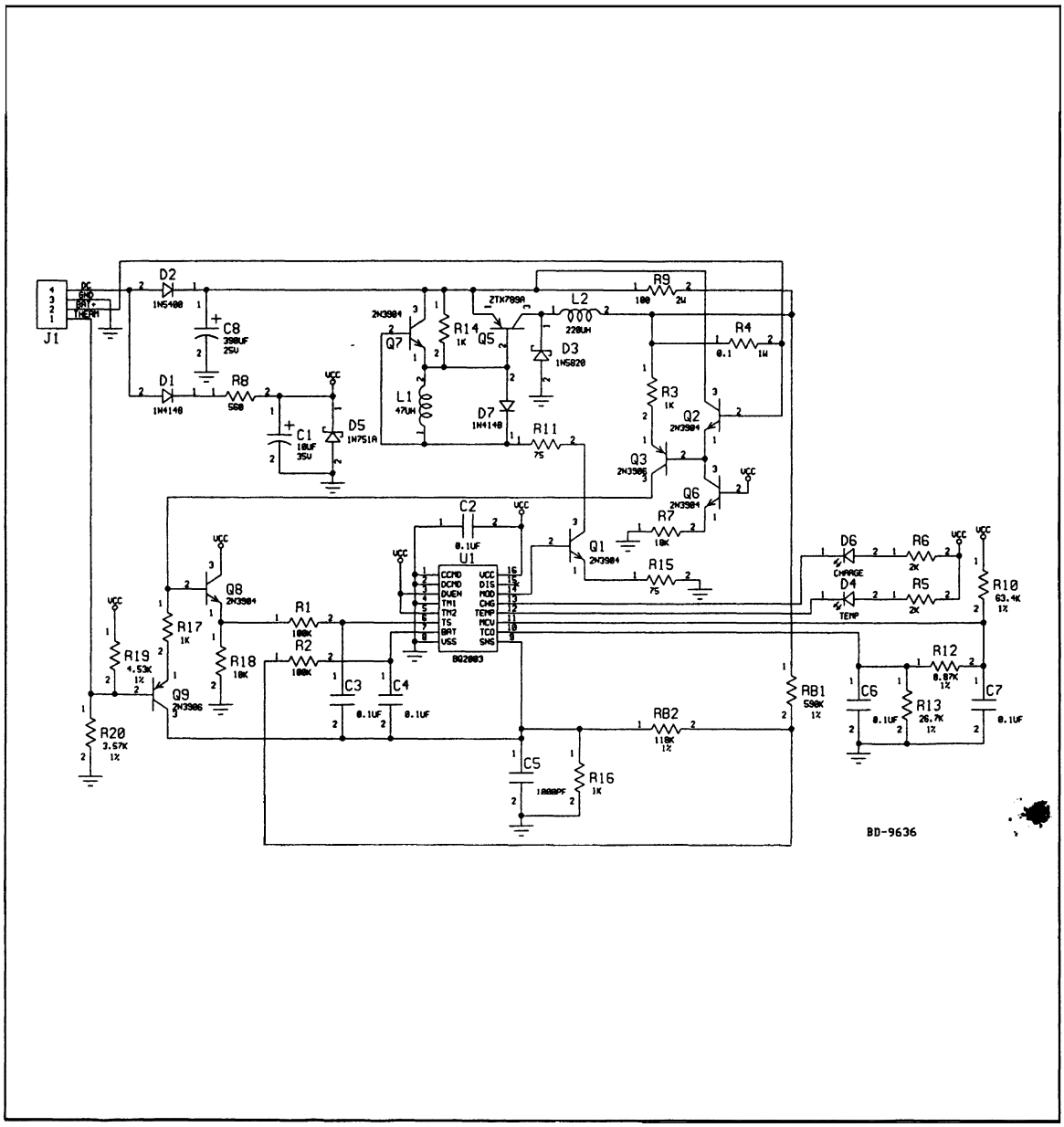


Figure 1. High-Side Sensed p-Channel Diagram

BENCHMARQ

bq2004

Fast Charge IC

Features

- Fast charge and conditioning of nickel cadmium or nickel-metal hydride batteries
- Supports logic-level-controlled low-power mode (< 5µA standby current)
- ➤ Optional peak voltage detect (PVD) fast-charge termination
- Flexible current regulation:
  - Frequency-modulated switching current regulator
  - Gating control for use with external regulator
- 150-mil SOIC is ideal for integration into portable systems
- Pre-charge qualification for temperature and voltage faults
- Programmable LED outputs display battery and charge status
- Fast charge termination by A temperature/Δ time, -ΔV or peak voltage, and maximum temperature, time, and voltage

General Description

The bq2004 Fast Charge IC provides comprehensive fast charge control functions together with high-speed switching power control circuitry on a monolithic CMOS device.

Flexible control of constant-current or current-limited charging supply allows the bq2004 to be the basis of a coat-effective system-integrated charger for batteries of two or more cells. High-efficiency switched constant-current regulation is accomplished using the bq2004 as a frequency-modulated controller. The bq2004 may alternatively be used with a transistor to gate an external charging current or in a cost-effective frequency-modulated linear regulator.

Switch-activated or automatic discharge-before-charge allows bq2004-based chargers to support battery conditioning and capacity determination.

Fast charge may begin on application of Vcc to the bq2004, replacement of the battery, or use of the $\overline{INH}$ pin. For safety, fast charge is inhibited until the battery temperature and voltage are within configured limits.

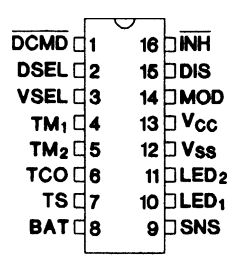
Temperature, voltage, and time are monitored throughout fast charge. Fast charge is terminated by any of the following:

- Delta temperature/delta time (ΔT/Δt)
- Negative delta voltage (-ΔV) or peak voltage detect
- Maximum temperature
- Maximum time

Maximum voltage

Followiug fast charge, the bq2004 proceeds with a pulsed top-off charge (if enabled) and a pulsed trickle charge. Figure 1 shows a block diagram of the bq2004 Fast Charge IC.

Pin Connections



16-Pin Narrow DIP
or Narrow SOIC

PN-47

Pin Names

$\overline{DCMD}$	Discharge command	SNS	Sense resistor input
DSEL	Display select	LED_1	Charge status output 1
VSEL	Voltage termination select	LED_2	Charge status output 2
TM_1	Timer mode select 1	Vss	System ground
TM_2	Timer mode select 2	Vcc	5.0V ±10% power
TCO	Temperature cutoff	MOD	Charge current control
TS	Temperature sense	DIS	Discharge control output
BAT	Battery voltage	$\overline{INH}$	Charge inhibit input

Pin Descriptions

$\overline{DCMD}$ **Discharge-before-charge** control **input**

$\overline{DCMD}$ controls the discharge-before-charge function of the bq2004. A negative-going pulse on $\overline{DCMD}$ initiates a discharge to EDV (0.4 • V_{CC}) followed by a charge if conditions allow. By tying $\overline{DCMD}$ to ground, automatic discharge-before-charge is enabled by the application of power, by battery replacement, or by a low-to-high transition on the $\overline{INH}$ pin. $\overline{DCMD}$ is pulled up internally.

DSEL Display select input

This three-level input controls the $LED_{1,2}$ charge status indication. See Table 2 for details.

VSEL Voltage termination select **input**

This three-level input controls the voltage-termination technique used by the bq2004.

TM_1, TM_2 Timer mode **inputs** ($TM_{1,2}$)

TM_1 and TM_2 are three-level inputs that control the settings for the fast charge safety timer and "top-off" trickle charge control. See Table 3 for details.

TCO Temperature cut-off threshold input

Minimum allowable battery temperature-sensor voltage. If the potential between TS and SNS is less than the voltage at the TCO input, then any fast charging or top-off charging is terminated.

TS Temperature sense input

Input for battery temperature monitoring negative temperature coefficient (NTC) thermistor.

SNS Charging current sense input

SNS controls the switching of MOD based on an external sense resistor network. This provides the reference potentials for both the TS and BAT pins. If SNS is connected to V_{SS}, then MOD switches high at the beginning of charge, and low at the end of charge. See Figure 2 and Table 1 for details.

BAT Battery voltage input

BAT is the battery voltage sense input. This potential is limited to between 0.4 • Vcc and 0.8 • V_{CC} and is generally developed by a high-impedance resistor-divider network connected between the positive and the negative terminals of the battery.

LED_1, LED_2 Charge statue outputs

Push-pull outputs indicating charging status. See Figure 2 and Table 2 for details.

VSS **Ground**

V_{CC} **V_{CC} supply input**

5.0V, ±10% power input.

MOD Charge current control output

MOD is a push-pull output that is used to control the charging current to the battery. MOD switches high to enable charging current to flow and low to inhibit charging current flow. See Figure 2 and Table 1 for details.

DIS Discharge control output

Push-pull output used to control an external transistor to discharge the battery before charging. DIS is active high.

$\overline{INH}$ Charge inhibit input

When low, the bq2004 suspends all charge actions, drives all outputs to high impedance, and assumes a low-power operational state. When transitioning from low to high, a charge cycle is initiated. See page 8 for details.

Functional Description

Figure 2 illustrates charge control and display status during a bq2004 charge cycle. Table 1 outlines the various bq2004 operational states and their associated conditions, which are described in detail in the following sections.

Charge Action Control

The bq2004 initiates a charge by the application of power on V_{CC}, by a battery replacement, or by a low-to-high transition on the $\overline{INH}$ pin. Control of the charge action is then determined by the inputs from $\overline{DCMD}$, VSEL, TS, BAT, and $TM_{1,2}$.

Following charge initiation, the bq2004 checks for acceptable battery temperature (between LTF—low-temperature fault and HTF—high-temperature fault) and battery voltage (between EDV—end-of-discharge voltage and MCV—maximum cell voltage). Fast charging begins when the voltage and temperature conditions are within these limits. Once the fast charging process begins, the bq2004 tests for the full-charge conditions: ΔT/Δt and/or -ΔV or peak voltage detect (PVD), with temperature, time, and voltage safety terminations.

Charge Status Indication

Table 1 outlines the various charge action states and the associated MOD and DIS output states. Table 2 describes the charge status indicated by the LED_1 and LED_2 outputs, which may be connected directly to an LED indicator. In all cases, if the battery voltage at the BAT pin exceeds the maximum cell voltage (0.8 • Vcc), the LED_1 and LED_2 outputs are held low.

Battery Voltage and Temperature Measurements

Battery voltage and temperature are monitored for maximum and minimum allowable values. The battery voltage sense input, BAT, for a battery pack should be divided to between 0.8 • Vcc and 0.4 • Vcc for proper operation. A resistor-divider ratio of:

$$\frac{R1}{R2} = \frac{N}{2} - 1$$

is recommended to maintain the battery voltage within the valid range, where N is the number of cab, R1 is the resistor connected to the positive battery terminal, and R2 is the resistor connected to the respective SNS pin. See Figure 3.

Note: The resistor-divider network impedance should be above 200KΩ to protect the bq2004.

The thermistor used for temperature measurement should have a negative temperature coefficient. The temperature sense voltage input at TS is developed using a resistor-thermistor network between Vcc and SNS. See Figure 3.

Battery Removal Detection

Battery removal is sensed by V_{CELL} (V_{BAT} - V_{SNS}) rising above V_{MCV} (0.8 • Vcc). An external resistor, R_{EXT}, between the battery positive lead and the charging supply input pulls V_{CELL} above V_{MCV} to detect battery removal.

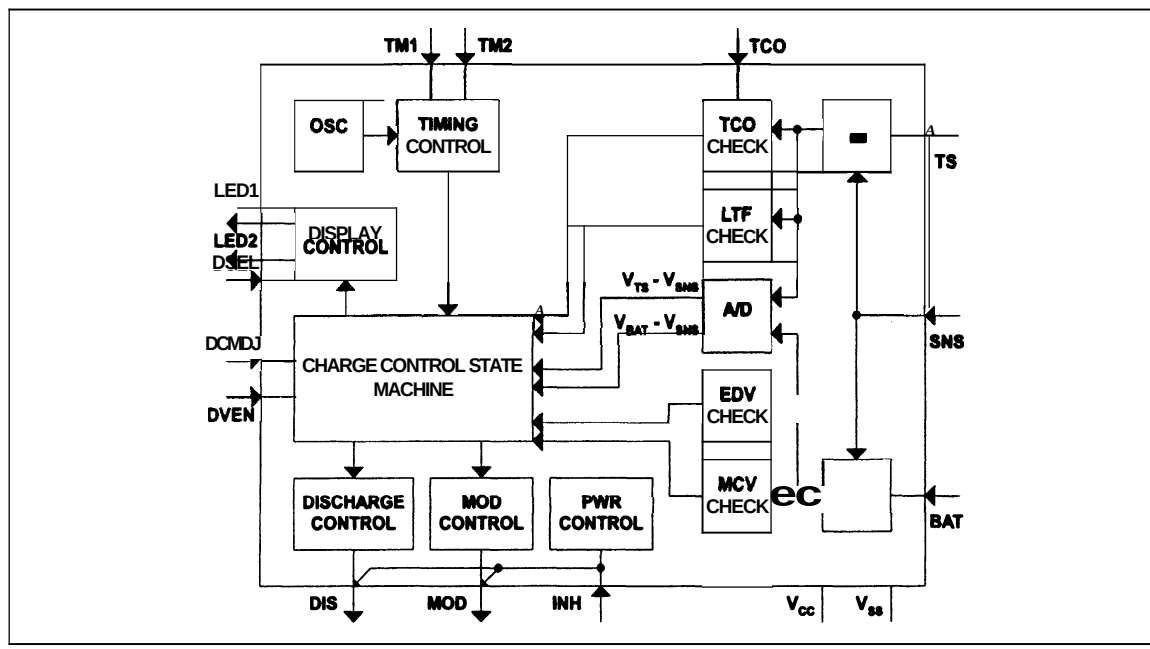


Figure 1. Block Diagram

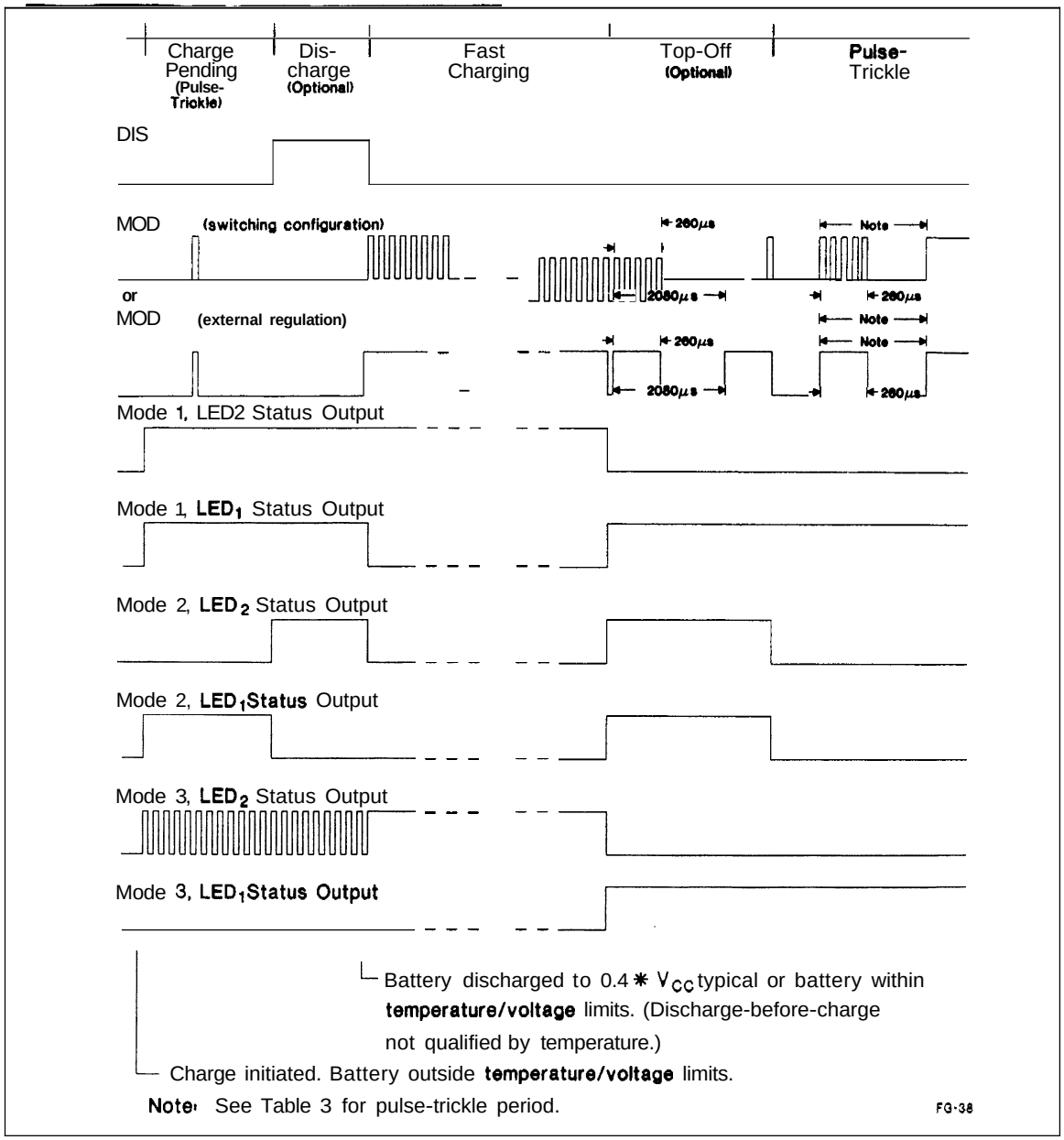


Figure 2. Example Charging Action Events

Initiating a Charge Action

A battery charge action is initiated with a battery insertion, application of V_{CC} to the bq2004, or a low-to-high transition on the $\overline{INH}$ pin. Battery insertion is recognized when the voltage at the BAT pin falls from above the internal V_{MCV} reference level to below that level. When V_{CC} is applied to the bq2004 or when $\overline{INH}$ transitions from low to high, a charge action begins after a brief reset period.

Temperature and Voltage Prequalification

Before fast charging can begin, the battery temperature and voltage must fall within predetermined acceptable limits.

V_{CELL} is compared to an internal low-voltage reference, V_{EDV} (0.4 • V_{CC}), which is the minimum acceptable battery voltage for fast charging. The V_{TEMP} (V_{TS} - V_{SNS}) voltage is compared to an internal hot-temperature fault reference, V_{HTF} ((44 • V_{LTF}) + (¾ • V_{TCO})) and optionally

Table 1. bq2004 Operational Summary

Charge Action State	Conditions	MOD Output	DIS Output
Battery absent	$V_{CELL} \geq V_{MCV}$	Trickle charge activated per V_{SNS} for period specified in Table 3	Low
Charge initiation	V_{CC} applied, V_{CELL} drops from $\geq V_{MCV}$ to $< V_{MCV}$ (battery insertion), or $\overline{INH}$ transitions low to high with battery inserted		–
Discharge-before-charge (optional)	$\overline{DCMD}$ high-to-low pulse or tied to V_{SS} on charge initiation; $V_{EDV} < V_{CELL} < V_{MCV}$	Low	High
Pending	Charge initiation occurred and $V_{TEMP} \geq V_{LTF}$[1] or $V_{TEMP} \leq V_{HTF}$ or $V_{CELL} < V_{EDV}$	Trickle charge activated per V_{SNS} for period specified in Table 3	Low
Fast charging	Charge initiation occurred and $V_{HTF} < V_{TEMP} < V_{LTF}$[1] and $V_{EDV} \leq V_{CELL} < V_{MCV}$	Low if $V_{SNS} > 250mV$, nominal; high if $V_{SNS} < 200mV$, nominal	Low
Charge complete	$-\Delta V \geq 6mV$/cell or PVD ≥ 0 to 3mV/cell or $\Delta V_{TEMP}/\Delta T > 14mV$/minute or $V_{TEMP} < V_{TCO}$ or $V_{TEMP} > V_{LTF}$[1] or maximum time or voltage		–
Top-off (optional; see Table 3)	Charge complete and top-off time not exceeded and $V_{TEMP} > V_{TCO}$ and $V_{CELL} < V_{MCV}$	Activated per V_{SNS} (see fast charging state) for 260µs of every 2080µs	Low
Trickle	Charge complete and top-off disabled or top-off complete	Trickle charge activated per V_{SNS} for period specified in Table 3	Low
Charge inhibit	$\overline{INH}$ low	Z	Z

Definitions: $V_{CELL} = V_{BAT} - V_{SNS}$; $V_{MCV} = 0.8 \bullet V_{CC}$; $V_{EDV} = 0.4 \bullet V_{CC}$;
$V_{TEMP} = V_{TS} - V_{SNS}$; $V_{LTF} = 0.4 \bullet V_{CC}$; $V_{HTF} = ((¼ \bullet V_{LTF}) + (¾ \bullet V_{TCO}))$.

Note: 1. The low-temperature fault is not considered when PVD is enabled.

Table 2. bq2004 LED Output Summary

Mode 1	Charge Action State	LED_1	LED_2
DSEL = V_{SS}	Battery absent	Low	Law
	Fast charge pending or a discharge-before-charge in progress	High	High
	Fast charging	Low	High
	Charge complete, top-off, and/or trickle	High	Low
Mode 2	**Charge Action State**	**LED_1**	**LED2**
DSEL = Floating	Battery absent, fast charge in progress or complete	Low	Low
	Fast charge pending	High	Low
	Discharge in progress	Low	High
	Top-off pending or in progress	High	High
Mode 3	**Charge Action State**	**LED_1**	**LED_2**
DSEL = V_{CC}	Battery absent	Low	Low
	Fast charge pending or diecharge-before-charge in progress	Low	1/8 second high 1/8 second low
	Fast charge in progress	Low	High
	Fast charge complete, top-off, and/or trickle	High	Low

to an internal low-temperature fault reference, V_{LTF} (0.4 • Vcc). These limits establish the acceptable battery and temperature sense voltage window for fast charge initiation. If the battery fails either of these two pre-qualifications for charge, the bq2004 enters a charge-pending mode, waiting for the battery voltage and temperature to become acceptable.

In the case of a battery that is too warm or too cold, the charge action starts when the battery temperature becomes acceptable. In the case of deeply discharged batteries (voltage too low), the bq2004 waits until the battery voltage is at an acceptable level before starting fast charge. In the case of a faulty battery, V_{BAT} may never reach an acceptable voltage level, causing the bq2004 to remain in the charge-pending state. The bq2004 continues to trickle charge (if enabled) the battery until the fast charge conditions are met.

Discharge-Before-Charge

The bq2004 supports discharge-before-charge on the battery, providing conditioning as well as capacity calibration. Once activated, the DIS pin goes active high until V_{CELL} falls below V_{EDV}, at which time fast charge qualification begins.

If $\overline{DCMD}$ is directly connected to Vss, automatic discharge-before-charge is enabled with the application of power to the bq2004, by battery replacement, or by a low-to-high transition on the $\overline{INH}$ pin. A negative-going pulse on $\overline{DCMD}$ causes the bq2004 to initiate a discharge-before-charge action on the battery regardless of charging activity. The $\overline{DCMD}$ pin is internally pulled up to V_{CC}; therefore, not connecting this pin results in disabling the discharge-before-charge function. See Figure 4.

TM_1 and TM2 Pins

The TM_1 and TM_2 pins are three-level input pine used to select the various charge, top-off, and trickle rates, maximum safety times, and -ΔV/PVD holdoff period. Table 3 describes the various states selected by the TM_1 and TM_2 pins.

Fast Charge

Once temperature and voltage prequalifications are met and any requested discharging of the battery is completed, fast charging begins and continues until termination by one or more of the five possible conditions:

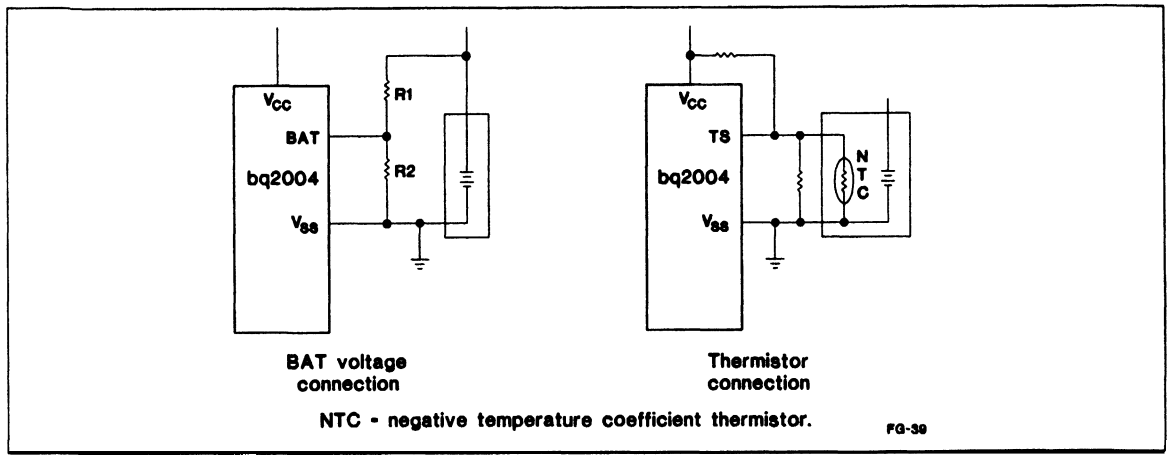


Figure 3. Voltage and Temperature Limit Measurement

- Delta temperature/delta time (ΔT/Δt)
- Negative delta voltage (-ΔV) or peak voltage detect (PVD)
- Maximum temperature
- Maximum charge time
- Maximum battery voltage

Voltage Termination Hold-off

At the start of fast charging, there is a hold-off time during which the -AV and PVD terminations are disabled (see Table 3). Once past the initial fast charge hold-off time, -ΔV or PVD termination is re-enabled. ΔT/Δt, maximum cell voltage (MCV), and maximum temperature (TCO) terminations are not *affected* by the hold-off period.

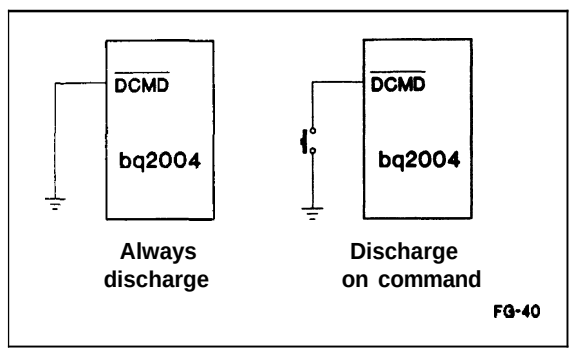


Figure 4. Discharge-Before-Charge

VSEL	Termination
Low	PVD
Float	-ΔV
High	Disabled

-ΔV or Peak Voltage Detect Termination

The bq2004 has two modes for voltage termination, depending on the state of the VSEL pin. VSEL high enables peak voltage detection; VSEL floating enables -ΔV detection; and VSEL low disables -AV and PVD terminations. -ΔV and PVD may be enabled or disabled at any time during the charge cycle. The bq2004 makes a termination decision every 34 seconds. For -ΔV, if V_{BAT} is lower than any previously measured value by 12mV typical, the fast charge phase of the charge action is terminated. This equates to a -AV termination of -6mV per cell typical.

The -ΔV test is valid only for:

$$0.4 \cdot V_{CC} \le V_{CELL} \le 0.8 \cdot V_{CC}$$

For peak voltage detect, the fast charge phase of the charge action is terminated when V_{CELL} is lower than the previously measured values by 0 to -3mV per cell (-6mV at the BAT pin).

ΔT/Δt Fast Charge Termination

The bq2004 makes a termination decision based on delta temperature/delta time (ΔT/Δt) every 34 seconds. If V_{TEMP} is 16mV (typical) less than the voltage measured 68 seconds previously, the fast charge phaee of the charge is terminated.

The ΔT/Δt test is valid only for:

$$0.2 \cdot V_{CC} \leq V_{TEMP} \leq 0.4 \cdot V_{CC}$$

Maximum Voltage, Time, and Temperature Safety Terminations

The bq2004 also terminates fast charge for maximum temperature (TCO), maximum time, and maximum voltage (MCV). MCV and TCO reference levels provide the maximum limits for battery voltage and temperature during faet charging. If either of these limits is exceeded, then fast charging or optional top-off charge is terminated. MCV is treated as a fault, so LED_1 and LED_2 are switched low with this condition.

Maximum time selection is programmed using the TM_1 and TM_2 pins (see Table 3). Time settings are available for corresponding charge rates ranging from C/4 to 4C.

Temperature Monitoring

Temperature is represented as a voltage input on the bq2004 at the TS pin. Generally this voltage is developed from an NTC (negative temperature coefficient) thermistor referenced to the negative battery terminal. The bq2004 recognizes an internal voltage level of $V_{LTF} = 0.4 \cdot V_{CC}$ as the low-temperature fault (LTF) level.

Note: If $V_{TEMP} \geq V_{LTF}$, charging is inhibited (if a cycle has not yet started) or terminated (if a cycle is in progress) except for the peak voltage detection (VSEL = high) mode. In this mode, LTF is not used to qualify charge or terminate *charge*.

Similarly, the external reference voltage level presented at the TCO pin represents the high-temperature cut-off point at which fast charging is terminated. V_{TCO} should always be less than V_{LTF} to ensure proper device operation.

All temperature prequalifications and ΔT/Δt termination may be disabled by connecting TCO to V_{SS} and fixing the TS pin level to 0.2 • V_{CC} with respect to SNS. ΔT/Δt termination sensitivity is user-adjustable, depending on the values of the external mistor-divider network.

Top-Off Charge

An optional top-off *charge* phase is selected to follow fast charge termination for charge rates from C/2 to 4C. This option is selected through the TM_1/TM_2 programming pins (see Table 3). The *charge* control cycle is modified so that the MOD pin is activated for 260µs of every 2080µs. This results in a rate 1/8th that of fast charging. Top-off charge proceeds for a time equal to the fast charge safety time. Maximum time, temperature (TCO), and voltage (MCV) terminations are the only termination methods enabled *during* top-off. If the fast-charge phase of a *charge* terminates due to TCO, top-off *charge* pends until the temperature falls below HTF.

Table 3. Fast Charge Safety Timemold-Offpop-OffTable

Corresponding Fast Charge Rate	TM1	TM2	Fast Charge Safety Time (minutes) Typical	PVD,-ΔV Hold-Off Time (seconds) Typical	Top-Off Rate	Pulse-Trickle Rate	Pulse-Trickle Period (Hz)
C/4	Low	Low	360	137	Disabled	Disabled	Disabled
C/2	Float	Low	180	820	Disabled	C/32	240
1C	High	Low	90	410	Disabled	C/32	120
2C	Low	Float	45	200	Disabled	C/32	60
4C	Float	Float	23	100	Disabled	C/32	30
C/2	High	Float	180	820	C/16	C/64	120
1C	Low	High	90	410	C/8	C/64	60
2C	Float	High	45	200	C/4	C/64	30
4C	High	High	23	100	C/2	C/64	15

Note: $T_A = 25°C$, $V_{CC} = 5.0V$.

Pulse-Trickle Charge

Pulse-trickle charge is used to compensate for self discharge of the battery while idle in the charger, and to bring a depleted battery to a valid charge voltage prior to fast charge. The battery pulse-trickles at the end of fast charge and top-off, and prior to charge (see Table 1).

In the pulse-trickle state, MOD is active for 260µs of a period specified by the state of TM_1 and TM_2 pins. The resulting trickle rate is 1/64 when top-off is enabled and 1/32 when top-off is disabled. Pulse-trickle and top-off can be disabled by tying TM_1 and TM2 to Vsa

Charge Inhibit

Fast charge, top-off, and pulse trickle may be inhibited by wiing the $\overline{INH}$ input pin. When low, the bq2004 suspends all charge activity, drives all outputs to high impedance, and assumes a low-power operational state. When $\overline{INH}$ returns high, a fast-charge cycle is qualified and begins as soon as conditions allow.

Charge Current Control

The bq2004 controls the charge current through the MOD output pin. The current control is designed to support implementation of a constant-current regulator. See Figure 5. Nominal regulated current is:

$$I_{REG} = 0.225V / R_{SNS}$$

When used in this configuration, the charge current is monitored at the SNS input by the voltage drop across a resistor, R_{SNS}. R_{SNS} may be chosen to provide a variety of charging currents.

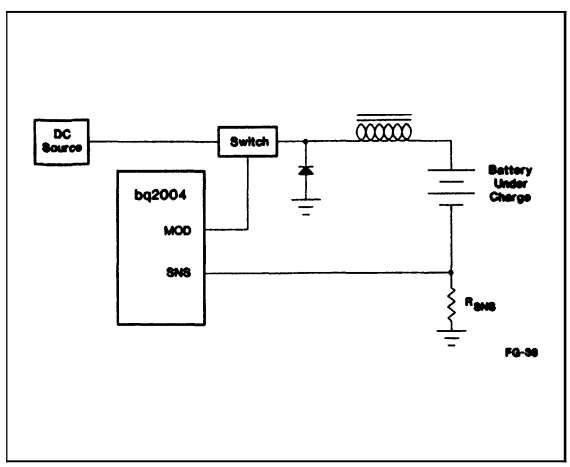


Figure 5. Constant-Current Switching Regulation

The MOD pin is switched high or low depending on the voltage input to the SNS pin. If the voltage at the SNS pin is less than V_{SNSLO} (0.2V typical), the MOD output is switched high to gate charge current. When the SNS voltage is greater than V_{SNSHI} (0.25V typical), the MOD output is switched low--+hutting off current from the supply.

The MOD pin can also be used to gate an external charging current source. When an external current source is used, a sense resistor is not required, and the SNS pin h connected to Vss. See Figure 6.

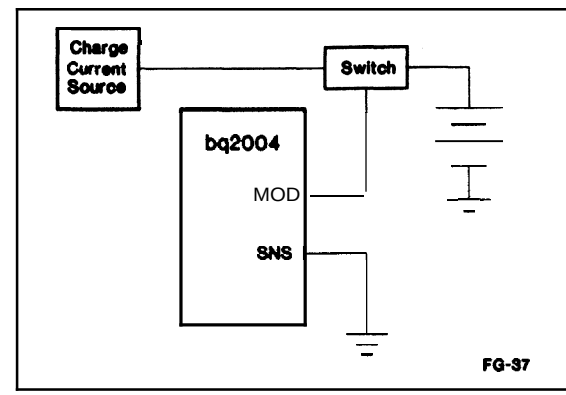


Figure 6. External Current Regulation

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Vcc relative to Vss	-0.3	+7.0	V	
VT	DC voltage applied on any pin excluding Vcc relative to Vss	-0.3	+7.0	V	
T_{OPR}	Operating ambient temperature	-20	+70	°C	Commercial
		-40	+85	°C	Industrial "N"
T_{STG}	Storage temperature	-55	+125	°C	
T_{SOLDER}	Soldering temperature		+260	°C	10 sec max.
T_{BIAS}	Temperature under bias	-40	+85	°C	

Note: Permanent device damage may occur if Absolute **Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds (TA = TOPR; VCC ±10%)

Symbol	Parameter	Ratina	Tolerance	Unit	Notes
V_{SNSHI}	High threshold at SNS resullg in MOD = Low	0.05 • Vcc	i0.025	V	
V_{SNSLO}	Low threshold at SNS resulting in MOD = High	0.04 • V_{CC}	±0.010	V	
V_{LTF}	Low-temperature fault	0.4 • Vcc	±0.030	V	$V_{TEMP} \geq V_{LTF}$ inhibit4 terminates charge[1]
V_{HTF}	High-temperature fault	(¼ • V_{LTF}) + (¾ • V_{TCO})	±0.030	V	$V_{TEMP} \leq V_{HTF}$ inhibits charge
V_{EDV}	End-of-discharge voltage	0.4 • Vcc	±0.030	V	~CEL ≤ V_{EDV} inhibits fast charge
V_{MCV}	Maximum cell voltage	0.8 • Vcc			$V_{CELL} > V_{MCV}$ inhibit4 terminates charge

Note: $V_{CELL} = V_{RAT} - V_{SNS}$. $V_{TEMP} = V_{TS} - V_{SNS}$.

1. VSEL = high disables low-temperature fault charge qualification.

1

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Condition	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	
V_{CELL}	BAT voltage potential	0		V_{CC}	V	$V_{BAT} - V_{SNS}$
V_{BAT}	Battery input	0		V_{CC}	V	
V_{TEMP}	TS voltage potential	0		V_{CC}	V	$V_{TS} - V_{SNS}$
V_{TS}	Thermistor input	0		V_{CC}	V	
V_{TCO}	Temperature cutoff	0.2 • V_{CC}		0.4 • V_{CC}	V	Valid $\Delta T/\Delta t$ range
V_{IH}	Logic input high	2.0			V	$\overline{DCMD}$, $\overline{INH}$
	Logic input high	V_{CC} - 0.3			V	TM_1, TM_2, DSEL, VSEL
V_{IL}	Logic input low			0.8	V	$\overline{DCMD}$, $\overline{INH}$
	Logic input low			0.3	V	TM_1, TM_2, DSEL, VSEL
V_{OH}	Logic output high	V_{CC} - 0.8			V	DIS, MOD, LED_1, LED_2, $I_{OH} \le -10mA$
V_{OL}	Logic output low			0.8	V	DIS, MOD, LED_1, LED_2, $I_{OL} \le 10mA$
I_{CC}	Supply current		1	3	mA	Outputs unloaded
I_{SB}	Standby current			1	µA	$\overline{INH} = V_{IL}$
I_{OH}	DIS, LED_1, LED_2, MOD source	-10			mA	@$V_{OH} = V_{CC}$ - 0.8V
I_{OL}	DIS, LED_1, LED_2, MOD sink	10			mA	@$V_{OL} = V_{SS}$ + 0.8V
I_L	Input leakage			±1	µA	$\overline{INH}$, BAT, V = V_{SS} to V_{CC}
	Input leakage	50		400	µA	$\overline{DCMD}$, V = V_{SS} to V_{CC}
I_{IL}	Logic input low source			70	µA	TM_1, TM_2, DSEL, VSEL, V = V_{SS} to V_{SS} + 0.3V
I_{IH}	Logic input high source	-70			µA	TM_1, TM_2, DSEL, VSEL, V = V_{CC} - 0.3V to V_{CC}
I_{IZ}	Tri-state	-2		2	µA	TM_1, TM_2, DSEL, and VSEL should be left disconnected (floating) for Z logic input state

Note: All voltages relative to Vss.

Impedance

Symbol	Parameter	Minimum	Typical	Maximum	Unit
R_{BAT}	Battery input impedance	50			MΩ
R_{TS}	TS input impedance	50			MΩ
R_{TCO}	TCO input impedance	50	-	-	MΩ
R_{SNS}	SNS input impedance	50			MΩ

Timing (TA = 0 to +70°C; VCC ±10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{PW}	Pulse width for $\overline{DCMD}$ and $\overline{INH}$ pulse command	1			µs	
d_{FCV}	Fast charge safety time variation	0.84	1.0	1.16	-	V_{CC} = 4.75V to 5.25V; T_A = 0 to 60°C; see Table 3.
t_{REG}	MOD output regulation frequency	-		300	kHz	Typical regulation capability; V_{CC} = 5.0V
t_{MCV}	$V_{CELL} \geq V_{MCV}$ valid period	1		2	sec	If $V_{CELL} \geq V_{MCV}$ for t_{MCV} during charge or top-off, then a transition of $V_{CELL} < V_{MCV}$ is recognized as battery replaced. Otherwise, $V_{CELL} < V_{MCV}$ is ignored.

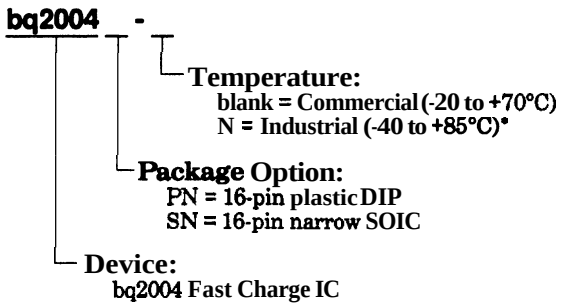
Note: Typical is at T_A = 25°C, V_{CC} = 5.0V.

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	10	Standby current I_{SB}	Was 5 µA max; is 1 µA max
2	9	V_{SNSLO} Rating	Was: V_{SNSHI} - (0.01 * V_{CC}) Is: 0.04 * V_{CC}
2	7	Correction in Peak Voltage Detect Termination section	Was: V_{CELL} Is: V_{BAT}
2	3	Added block diagram	Diagram insertion
2	7	Added VSEL/termination table	Table insertion
2	8	Added values to Table 3	Top-Off rate values

Note: Change 1 = Apr. 1994 B "Final" changes from Dec. 1993 A "Preliminary."
Change 2 = Sept. 1996 C from Apr. 1994 B.

Ordering Information



* Contact factory for availability.

BENCHMARQ

Product Brief **DV2004L1**

Fast Charge Development System

Control of PNP Power Transistor

Features

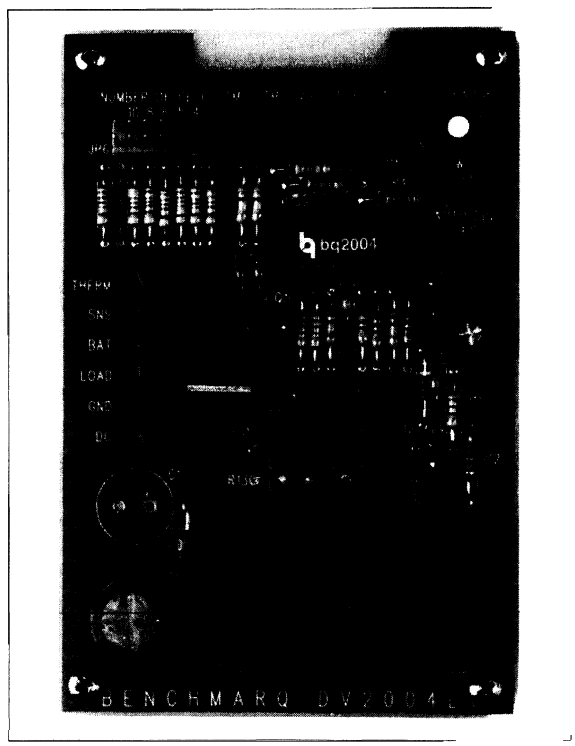
- bq2004 fast charge control evaluation and development
- Charge current sourced from an on-board frequency-modulated linear regulator (up to 3.0 A)
- Fast charge of 4 to 10 NiCd or NiMH cells and one user-defined selection
- Fast charge termination by delta temperature/delta time ($\Delta T/\Delta t$), negative delta voltage ($-\Delta V$) or peak voltage detect, maximum temperature, maximum time, and maximum voltage
- $-\Delta V$/peak voltage detect, hold-off, top-off, maximum time, and number of cells are jumper-configurable
- Programmable charge status display
- Discharge-before-charge control with push-button switch or auto discharge-before-charge with jumper
- Inhibit fast charge by logic-level input

General Description

The DV2004L1 Development System provides a development environment for the bq2004 Fast Charge IC. The DV2004L1 incorporates a bq2004 and a frequency-modulated linear regulator to provide fast charge control for 4 to 10 NiCd or NiMH cells.

The fast charge is terminated by any of the following: $\Delta T/\Delta t$, $-\Delta V$ or peak voltage detect, maximum temperature, maximum time, maximum voltage, and inhibit command. Jumper settings select the voltage termination mode, the hold-off, top-off, and maximum time limits, and automatic discharge-before-charge.

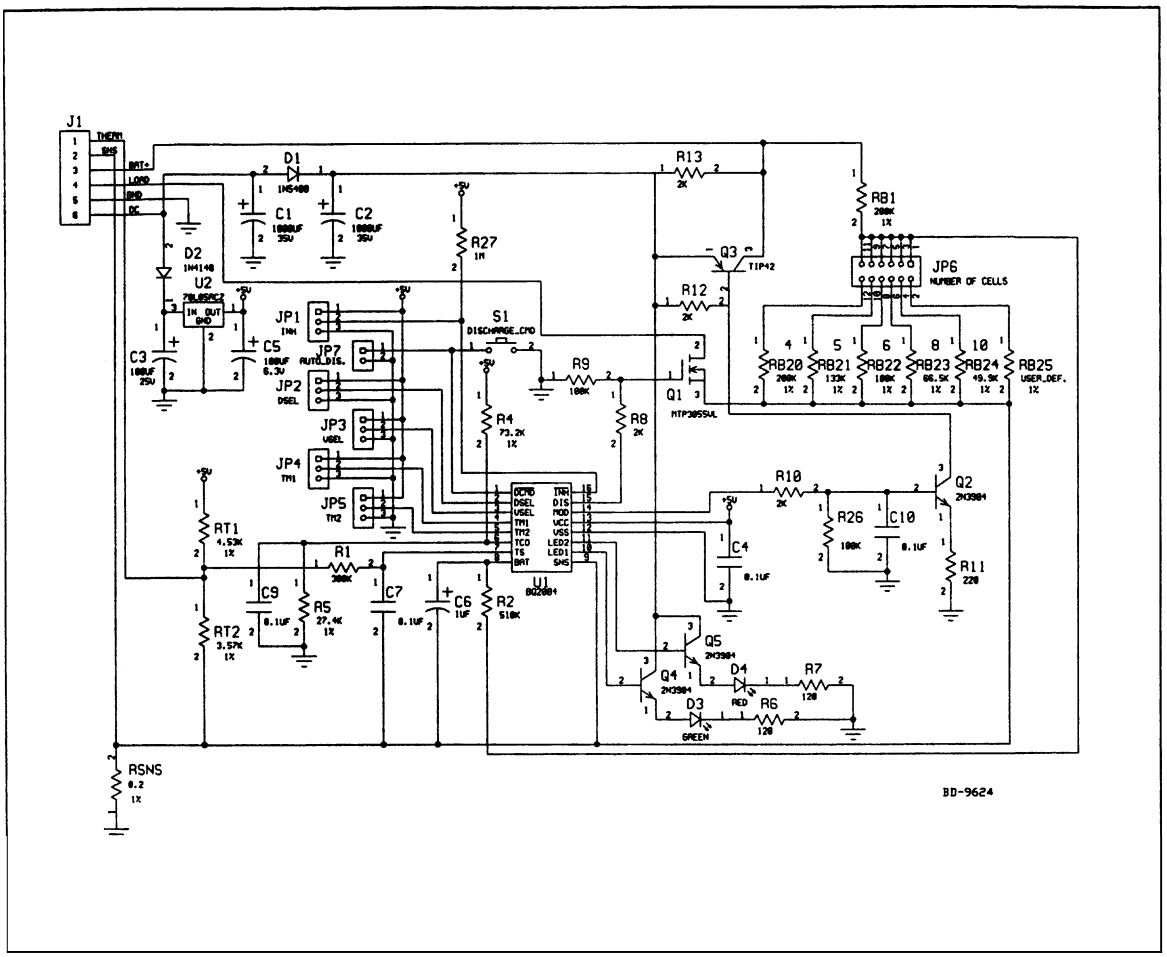
The user provides a power supply and batteries. The user configures the DV2004L1 for the number of cells, voltage, charge termination mode, and maximum charge time (with or without top-off), and commands discharge-before-charge with push-button switch S1.



Please review the bq2004 data sheet before using the DV2004L1 board.

A full data sheet for this product is available on our web site (http://www.benchmarq.com),or you may contact the factory for one.

DV2004L1 Board Schematic



Fast Charge Development System

Control of Frequency-Modulated Linear Regulator

Features

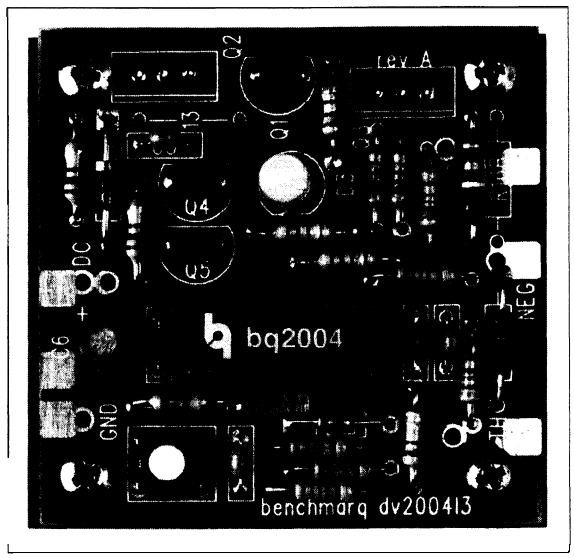
- bq2004 fast charge control evaluation and development
- Charge current controlled with frequency-modulated linear design
- Fast charge of 2 to 12 NiCd and/or NiMH cells
- Fast charge termination by -ΔV, PVD, ΔT/Δt, maximum temperature, time, and voltage
- Discharge-before-charge option

General Description

The bq2004L3 Development System provides a cost-effective component-reduced development environment for the bq2004 Fast Charge IC. The DV2004L3 incorporates a frequency-modulated linear regulator for fast charge control of NiCd and/or NiMH cells.

The bq2004 MOD output drives a transistor that switches the bipolar transistor Q2. The switching frequency of the MOD output depands on the voltage of the SNS pin. The bq2004 switches MOD to maintain a nominal 0.225V across resistor R7. The charge current can easily be adjusted by modifying the value of R7.

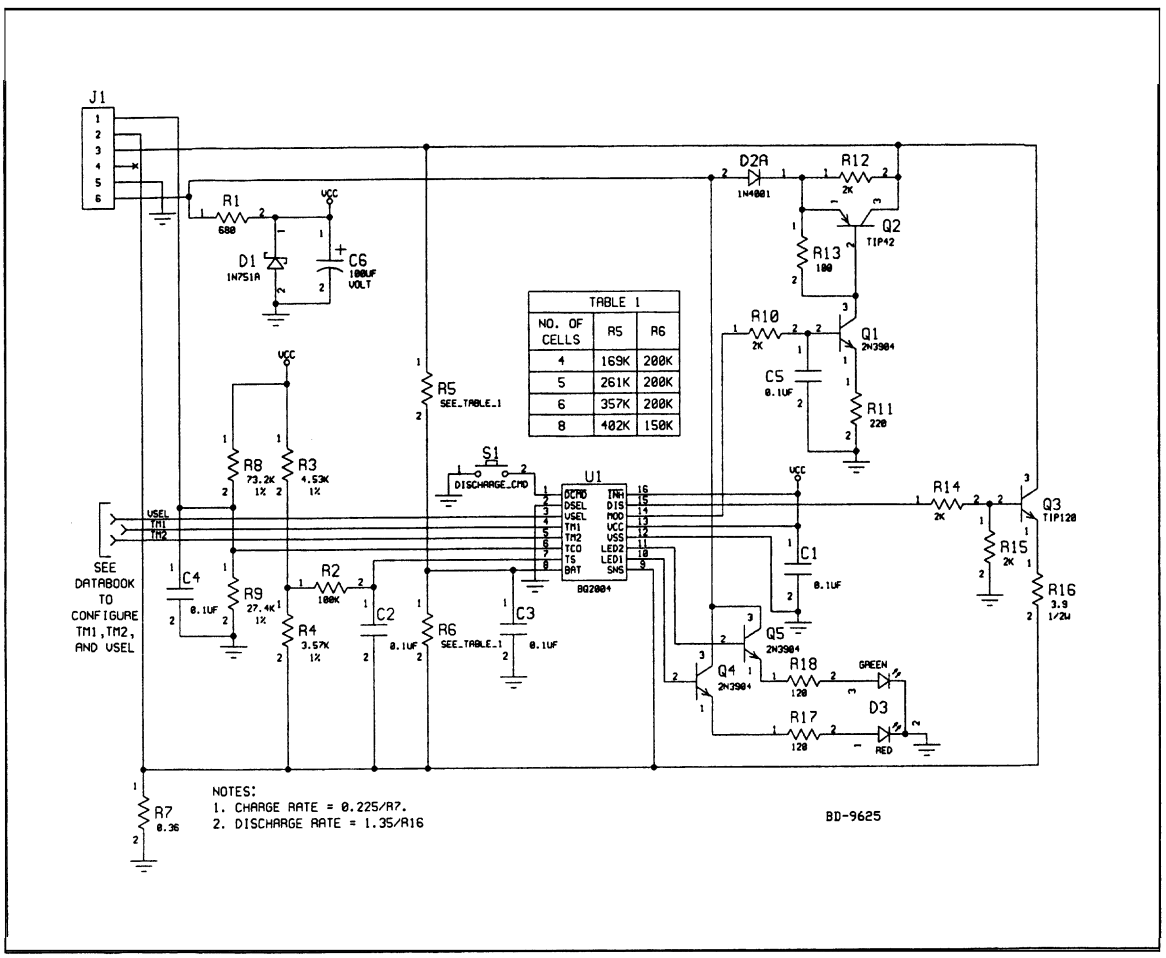
Fast charge is terminated by any of the following: -ΔV or peak voltage detect (PVD), ΔT/Δt, maximum time, and maximum voltage. Jumper settings select the -AV enabled state, select the hold-off, top-off, and maximum time limits.



The user provides a power supply and batteries.

A full data sheet for this product is available on our web site (http://www.benchmarq.com), or you may contact the factory for one.

DV2004L3 Board Schematic



Product Brief DV2004S1

Fast Charge Development System

Control of On-Board p-FET Switch-Mode Regulator

Features

- ➤ bq2004 fast charge control evaluation and development
- ● Charge current sourced from an on-board switch-mode regulator (up to 3.0 A)

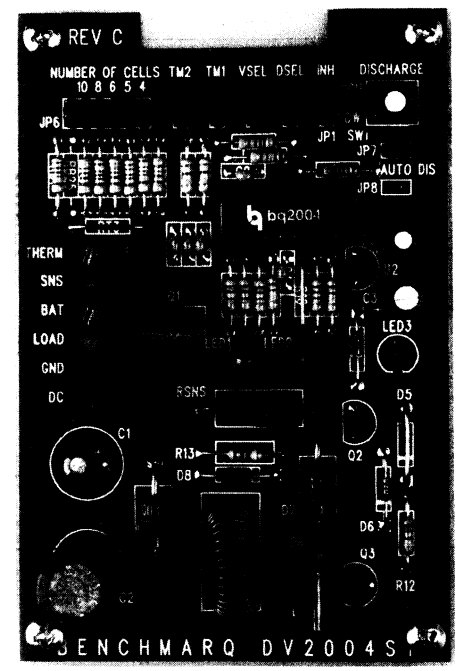
  Fast charge of 4 to 10 NiCd or NiMH cells and one user-defined selection
- ➤ Fast charge termination by delta temperature/delta time ($\Delta T/\Delta t$), negative delta voltage ($-\Delta V$) or peak voltage detect, maximum temperature, maximum time, and maximum voltage
- ● $-\Delta V$/peak voltage detect, hold-off, top-off, maximum time, and number of cells are jumper-configurable
- ● Programmable charge status display
- ● Discharge-before-charge control with push-button switch or auto discharge-before-charge with jumper
- ● Inhibit fast charge by logic-level input

General Description

The DV2004S1 Development System provides a development environment for the bq2004 Fast Charge IC. The DV2004S1 incorporates a bq2004 and a buck-type switch-mode regulator to provide fast charge control for 4 to 10 NiCd or NiMH cells.

The fast charge is terminated by any of the following: $\Delta T/\Delta t$, $-\Delta V$ or peak voltage detect, maximum temperature, maximum time, maximum voltage, and inhibit command. Jumper settings select the voltage termination mode, the hold-off, top-off, and maximum time limits, and automatic discharge-before-charge.

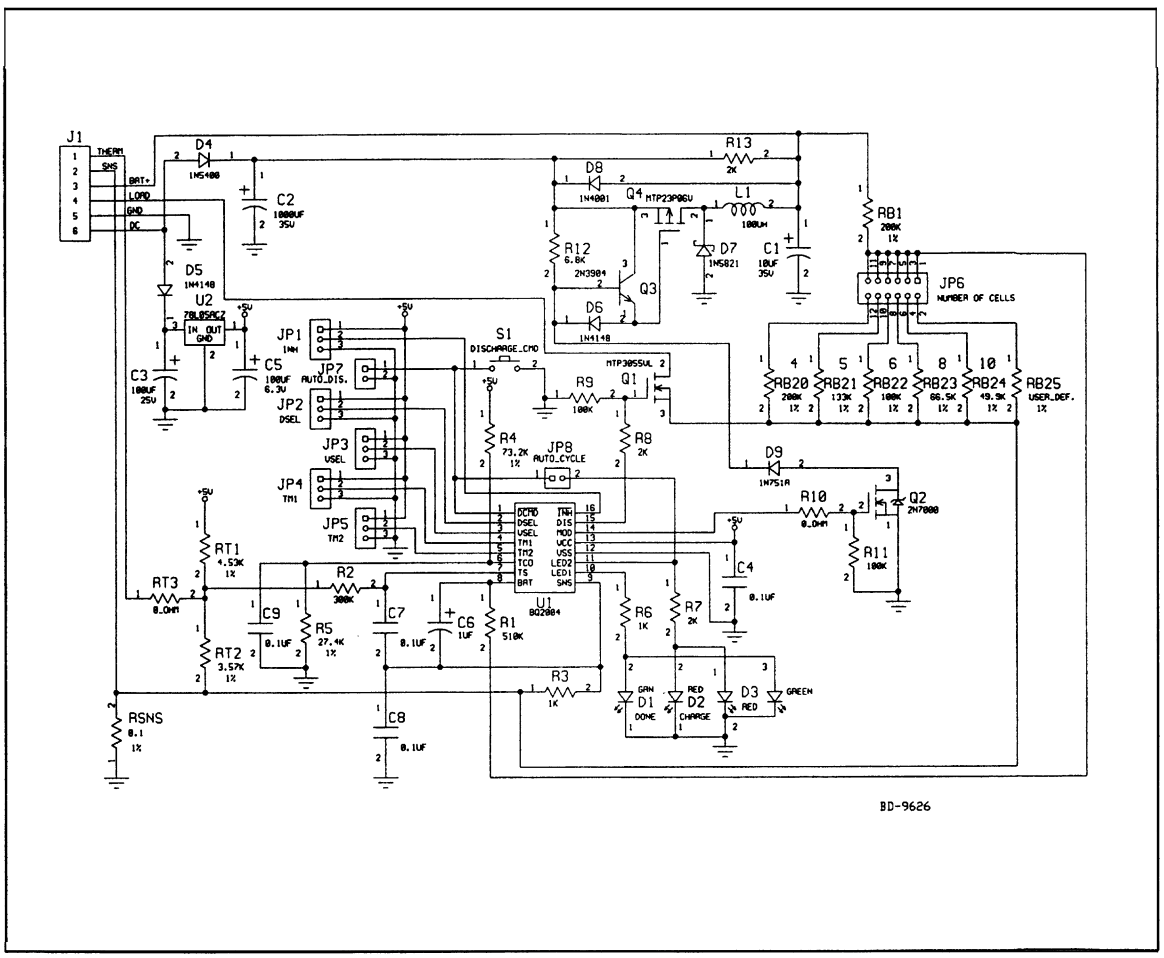
The user provides a power supply and batteries. The user configures the DV2004S1 for the number of cells, voltage, charge termination mode, and maximum charge time (with or without top-off), and commands discharge-before-charge with push-button switch S1.



Please review the bq2004 data sheet before using the DV2004S1 board.

A full data sheet for this product is available on our web site (http://www.benchmarq.com), or you may contact the factory for one.

DV2004S1 Board Schematic



BENCHMARQ

Product Brief **DV2004S3**

Nickel/Li-Ion Development System

1

Control of On-Board p-FET Switch-Mode Regulator

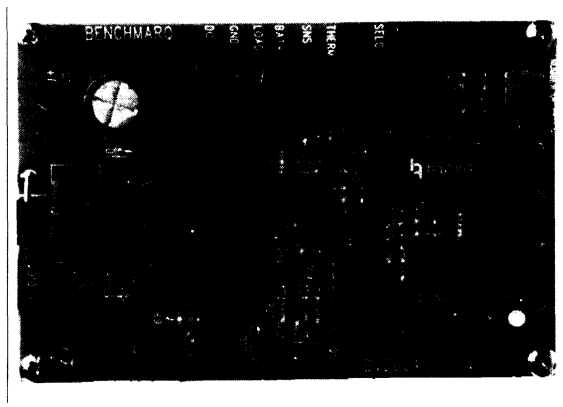
Features

- ➤ bq2004 fast charge control evaluation and development for NiMH, NiCd, and Li-Ion chemistries
- ➤ Charge current sourced from an on-board switch-mode regulator (up to 2.0 A)
- ➤ Fast charge of 3, 6, or 9 NiCd or NiMH cells and 1, 2, or 3 Li-Ion cells
- ➤ Fast charge termination by delta temperature/delta time ($\Delta T/\Delta t$), negative delta voltage ($-\Delta V$) or peak voltage detect, maximum temperature, maximum time, and maximum voltage for nickel-based and constant-current to constant-voltage for Li-Ion
- ➤ $-\Delta V$/peak voltage detect, hold-off, top-off, maximum time, and number of cells are jumper-configurable
- ● Programmable charge status display
- ● Discharge-before-charge control with push-button switch or auto discharge-before-charge with jumper
- ● Inhibit fast charge by logic-level input

General Description

The DV2004S3 Development System provides a dual-chemistry development environment for the bq2004 Fast Charge IC. The DV2004S3 incorporates a bq2004 and a buck-type switch-mode regulator to provide fast charge control for 3, 6, or 9 NiCd or NiMH cells and 1, 2, or 3 Li-Ion cells.

The fast charge is terminated by any of the following: $\Delta T/\Delta t$, -AV or peak voltage detect, maximum temperature, maximum time, maximum voltage, and inhibit command. Jumper settings select the voltage termination mode, the hold-off, top-off, and maximum time limits, and automatic discharge-before-charge.



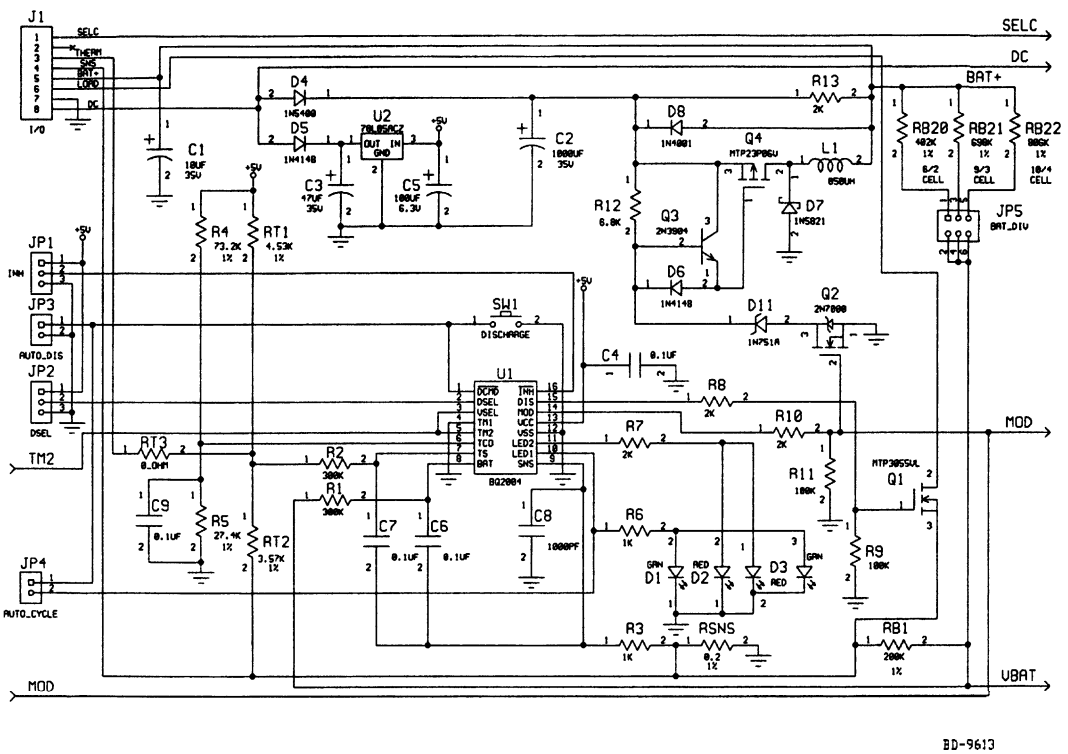
Fast charge for Li-Ion transitions from a constant-current to constant-voltage regulation. Voltage is regulated to within 1%. Charge complete is indicated at the maximum charge time.

The user provides a power supply and batteries. The user configures the DV2004S3 for the number of cells and charge termination mode, and commands discharge-before-charge with push-button switch S1.

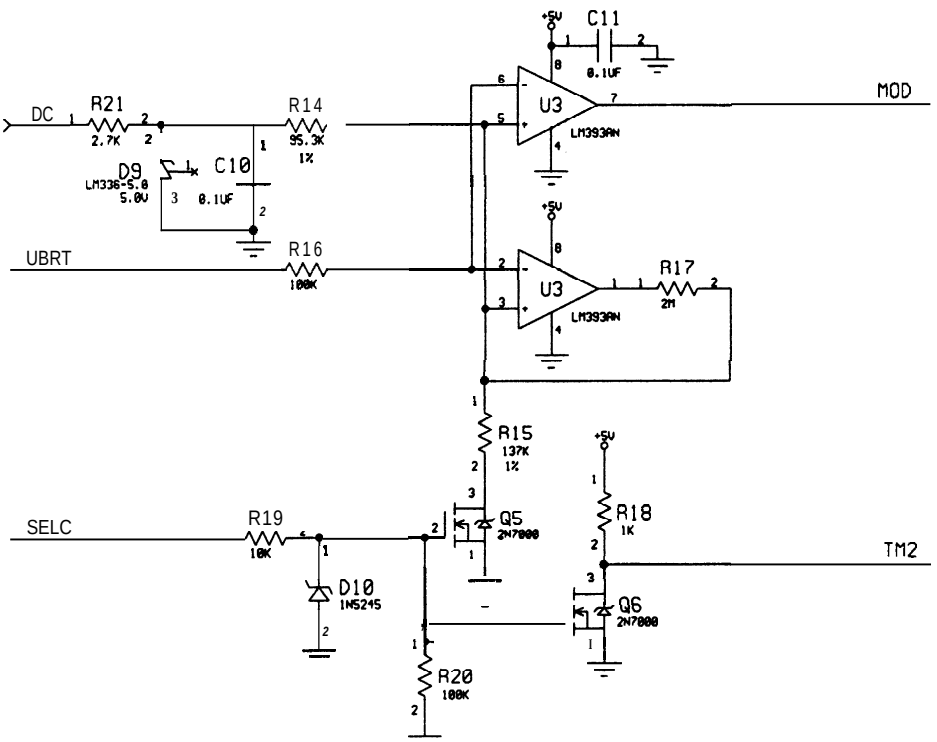
Please review the bq2004 data sheet and application note entitled "Using NiMH and Li-Ion Batteries in Portable Applications," before using the DV2004S3 board.

A full data sheet for this product is available on our web site (http://www.benchmarq.com),or you may contact the factory for one.

DV2004S3 Board Schematic



DV2004S3 Board Schematic (Continued)



Notes

bq2004E

Fast Charge IC

Features

- Supports fast charge and conditioning of nickel cadmium, nickel-metal hydride, and lithium-ion batteries
- Supports logic-level-controlled low-power mode (< 1 µA standby current)
- Optional peak voltage detect (PVD) fast-charge termination
- Flexible current regulation:
  - Frequency-modulated switching current regulator
  - Gating control for use with external regulator
- 150-mil SOIC is ideal for integration into portable systems
- Pre-charge qualification for temperature and voltage faults
- Programmable LED outputs display battery and charge status
- Fast charge termination by A temperature/Δ time, -AV or peak voltage, and maximum temperature, time, and voltage

General Description

The bq2004E Fast Charge IC provides comprehensive fast charge control **functions** together with high-speed **switching** power **control circuitry for** nickel and **lithium-ion-based rechargeable chemistries.**

Flexible control of **constant-current** or **constant-voltage** charging mpply allows the **bq2004E** to be the **basis of** a cost-effective **system-integrated** charger for **batteries.** High-efficiency switched constant-current or **con**etant-voltage regulation **is** accomplished using the **bq2004E** ae a frequency-modulated controller. The **bq2004E** may alternatively be used with a transistor to **gate** an external **charging current or in a cost-effective** frequency-modulated linear **regulator.**

Switch-activated or automatic **discharge-before-charge allows bq2004E-based** chargers to **support battery conditioning and capacity determination.**

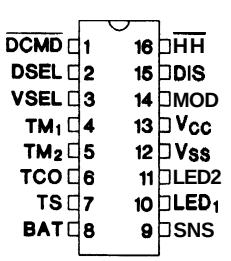
Fast charge may **begin** on application of Vcc to **the bq2004E, replacement** of **the battery, or use of the $\overline{INH}$ pin.** For **safety, fast** *charge* is inhibited **until the battery temperature** and **voltage are** within **configured limits.**

Temperature, voltage, and time are **monitored** throughout **fast** charge. Fast *charge* **is** terminated by any of the following:

- Delta **temperature/delta** time **(ΔT/Δt)**
- **Negative** delta voltage **(-ΔV)** or peak voltage detect
- **Maximum temperature**
- **Maximum time**
- Maximum voltage

Following fast charge, the **bq2004E proceeds** with an optional **pulsed top-off** and a **pulsed** trickle charge. **Figure 1 shows** a block diagram of the **bq2004E Fast** Charge IC.

Pin Connections



16-Pin Narrow DIP
or Narrow SOIC

PN-47

Pin Names

$\overline{DCMD}$	Discharge command	SNS	Sense resistor input
DSEL	Display select	LED_1	Charge status output 1
V S U	Voltage termination select	LED_2	Charge status output 2
TM_1	T i e r mode select 1	V_{SS}	System ground
TM_2	Timer mode select 2	V_{CC}	5.0V ±10% power
TCO	Temperature cutoff	MOD	Charge current control
TS	Temperature sense	DIS	Discharge control output
BAT	Battery voltage	$\overline{INH}$	Charge inhibit input

Pin Descriptions

$\overline{DCMD}$ **Discharge-before-charge** control input

$\overline{DCMD}$ controls the discharge-before-charge function of the **bq2004E.** A negative-going pulse on $\overline{DCMD}$ **initiates** a discharge to EDV (0.4 • **Vcc)** followed by a charge if conditions allow. By tying $\overline{DCMD}$ to ground, automatic discharge-before-charge is enabled by the application of power, by battery **replacement,** or by a low-to-high tramition on the $\overline{INH}$ **pin.** $\overline{DCMD}$ is pulled up internally.

DSEL Display select input

This three-level input controls the **$LED_{1,2}$** *charge* status indication. **See** Table 2 **for** details.

VSEL Voltage **termination** select **input**

This three-level input controls the **voltage**-termination technique **used** by the **bq2004E.**

TM_1, TM_2 Timer mode inputs **($TM_{1,2}$)**

TM_1 and **TM_2** are **three-level inputs** that control the settings for the fast charge safety timer and **"top-off"/trickle** charge control. ***See*** Table 3 for details.

TCO Temperature **cut-off** threshold input

Minimum allowable battery **temperature-sensor** voltage. If the potential between TS and SNS is **less** than the voltage at the **TCO input, then any** fast charging or top-off charging is terminated.

TS **Temperature sense** input

Input for battery temperature monitoring negative temperature coefficient **(NTC) thermistor.** TS > **Vcc - 0.5V** disables temperature sensing.

SNS **Charging** current sense input

SNS controls the switching of MOD based on an external sense resistor network. This provides the reference potentials for both the TS and BAT pins. If SNS is connected to **Vss,** then MOD switches high at the beginning of charge, and low at the end of charge. See Figure 2 and Table 1 for details.

BAT Battery voltage input

BAT is the **battery** voltage **sense** input. **This potential is** limited to between 0.4 • **Vcc** and 0.8 • **Vcc** and is generally **developed** by a high-impedance **resistor-divider** network **connected** between the **positive** and the negative terminals of the battery.

LED_1, LED_2 Charge status **outputs**

Push-pull outputa indicating charging **status.** ***See*** **Figure** 2 and Table 2 for details.

Vss **Ground**

Vcc **Vcc supply** input

5.0V, ±10% power input,

MOD Charge current control output

MOD is a push-pull output that is **used** to control the **charging** current to the battery. MOD **switches** high to enable charging current to flow and low to inhibit charging current flow. **See Figure** 2 and Table 1 for details.

DIS Discharge control output

Push-pull output used to control an external transistor to discharge the battery before charging. DIS is active high.

$\overline{INH}$ Charge inhibit input

When low, the **bq2004E** suspends all charge actions, drives all outputa to high impedance, and assumes a low-power operational state. When **transitioning from** low to high, a charge cycle is initiated. See page 8 for details.

Functional Description

Figure 2 **illustrates** charge control and display status during a **bq2004E** charge cycle. Table 1 outlines the various **bq2004E** operational states and their **associated** conditions, which are described in detail in the following sections.

Charge Action Control

The **bq2004E** initiates a charge by the application of power on **Vcc,** by a **battery replacement,** or by a low-to-high tramition on the $\overline{INH}$ **pin.** Control of the **charge** action is then determined by the **inputs from** $\overline{DCMD}$, VSEL, TS, BAT, and $TM_{1,2}$.

Following charge initiation, the bq2004E checks for acceptable battery temperature (between LTF—low-temperature fault and HTF—high-temperature fault) and battery voltage (between EDV—end-of-discharge voltage and MCV—maximum cell voltage). Fast charging begins when the voltage and temperature conditions are within these limits. Once the fast charging process begins, the bq2004E tests for the full-charge conditions: $\Delta T/\Delta t$ and/or -AV or peak voltage detect (PVD), with temperature, time, and voltage safety terminations.

Charge Status Indication

Table 1 outlines the various charge action states and the associated MOD and DIS output states. Table 2 describes the charge status indicated by the LED_1 and LED_2 outputs, which may be connected directly to an LED indicator. In all cases, if the battery voltage at the BAT pin exceeds the maximum cell voltage (0.8 • V_{CC}), the LED_1 and LED_2 outputs are held low.

Battery Voltage and Temperature Measurements

Battery voltage and temperature are monitored for maximum and minimum allowable values. The battery voltage sense input, BAT, for a battery pack should be divided to between 0.8 • V_{CC} and 0.4 • V_{CC} for proper operation. A resistor-divider ratio of:

$$\frac{R1}{R2} = \frac{N}{2} - 1$$

is recommended to maintain the battery voltage within the valid range, where N is the number of cells, R1 is the resistor connected to the positive battery terminal, and R2 is the resistor connected to the respective SNS pin. See Figure 3.

Note: The resistor-divider network impedance should be above 200KΩ to protect the bq2004E.

The thermistor used for temperature measurement should have a negative temperature coefficient. The temperature sense voltage input at TS is developed using a resistor-thermietor network between V_{CC} and SNS. See Figure 3.

Battery Removal Detection

Battery removal is sensed by V_{CELL} (V_{BAT} - V_{SNS}) rising above V_{MCV} (0.8 • V_{CC}). An external resistor, R_{EXT}, between the battery positive lead and the charging supply input pulls V_{CELL} above V_{MCV} to detect battery removal.

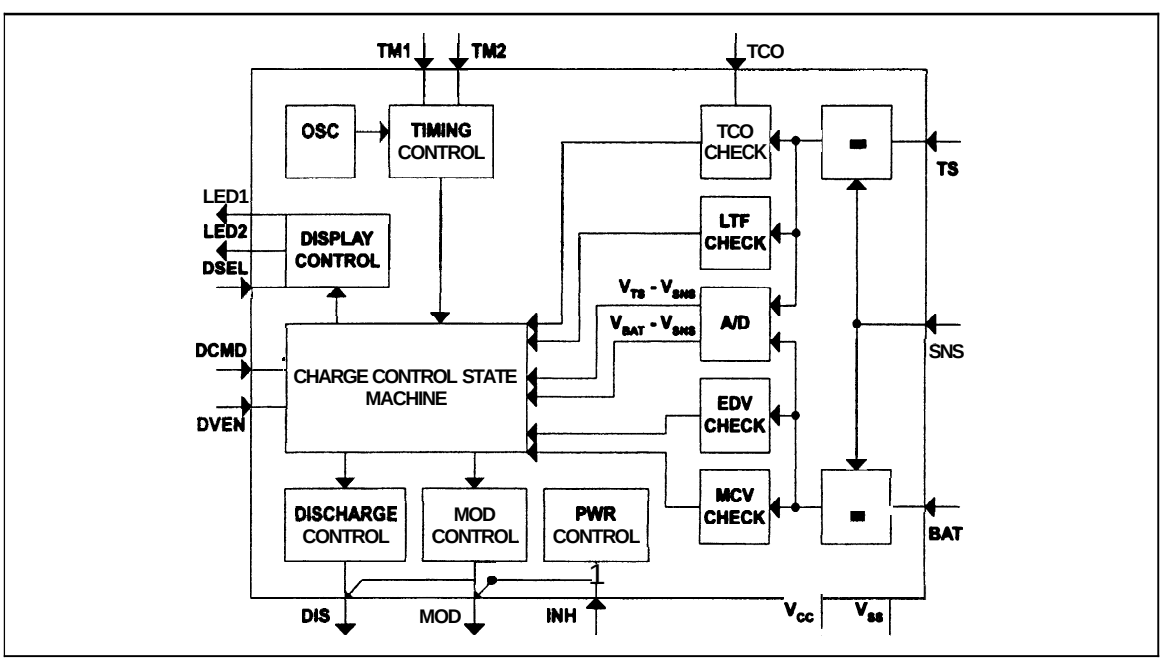


Figure 1. Block Diagram

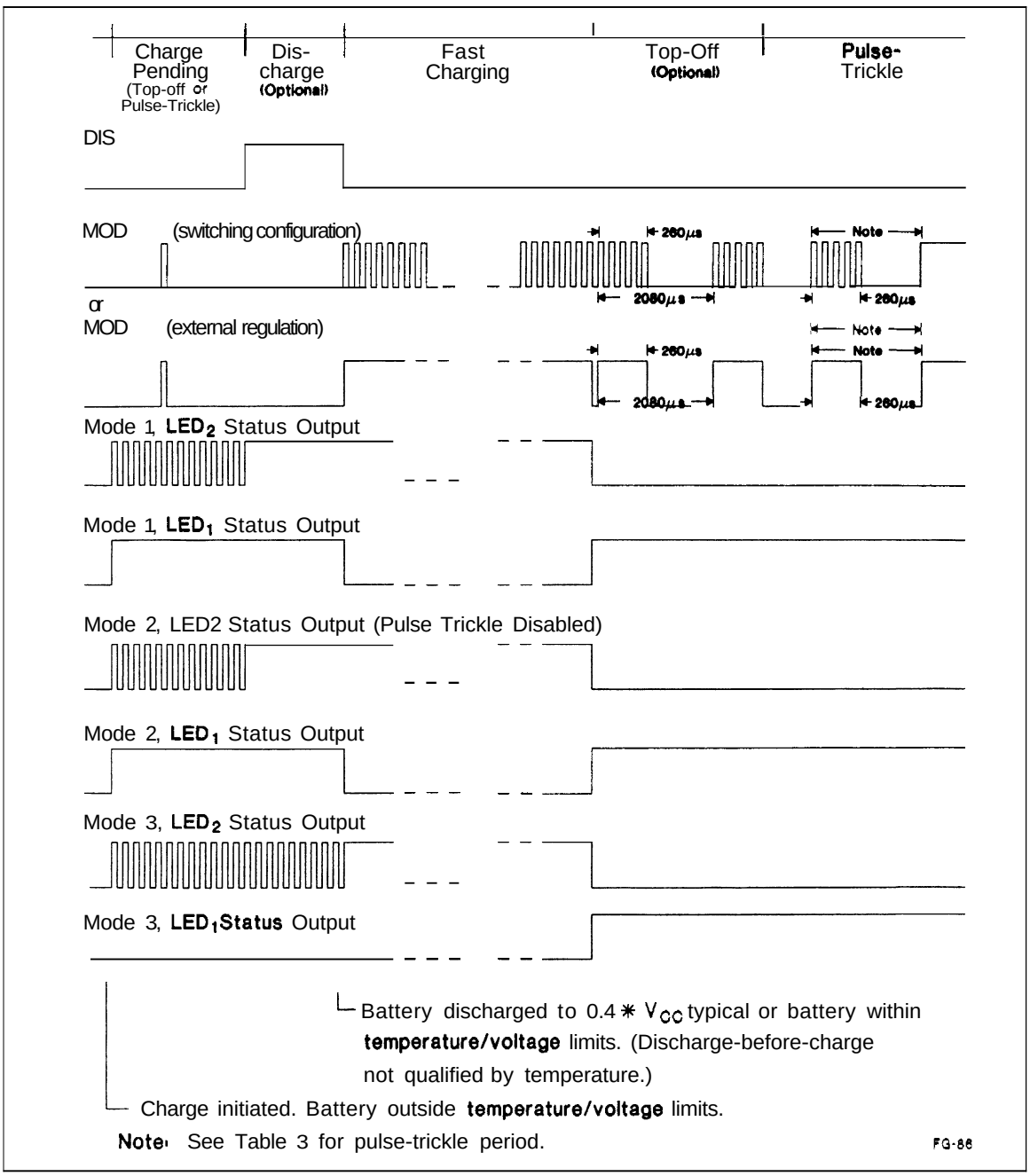


Figure 2. Example Charging Action Events

Initiating a Charge Action

A battery charge action is initiated with a battery insertion, an application of V_{CC} to the bq2004E, a a low-to-high transition on the $\overline{INH}$ pin. Battery insertion is recognized when the voltage at the BAT pin falls from above the internal V_{MCV} reference level to below that level. When V_{CC} is applied to the bq2004E or $\overline{INH}$ transitions from low to high, a charge action begins after a brief reset period.

Temperature and Voltage Prequalification

A charge action is prequalified by the battery temperature and voltage. Before fast charging can begin, the battery temperature and voltage must fall within predetermined acceptable limits.

V_{CELL} is compared to an internal low-voltage reference, V_{EDV} (0.4 • V_{CC}), which is the minimum acceptable battery voltage for fast charging. The V_{TEMP} (V_{TS} - V_{SNS}) voltage is compared to an internal hot-temperature fault

Table 1. bq2004E Operational Summary

Charge Action State	Conditions	MOD Output	DIS Output
Battery absent	$V_{CELL} \geq V_{MCV}$	Trickle charge activated per V_{SNS} for period specified in Table 3*	Low
Charge initiation	V_{CC} applied, V_{CELL} drops from $\geq V_{MCV}$ to $< V_{MCV}$ (battery insertion), or $\overline{INH}$ transitions low to high with battery inserted	–	–
Discharge-before-charge (optional)	$\overline{DCMD}$ high-to-low pulse or tied to V_{SS} on charge initiation; $V_{EDV} < V_{CELL} <$ V_{MCV}	Low	High
Pending	Charge initiation occurred and $V_{TEMP} \geq V_{LTF}$ or $V_{TEMP} \leq V_{HTF}$ or $V_{CELL} <$ Vmv	Activated per V_{SNS} for 260µs of every 2080 for top-off period; then trickle(see trickle state)	Low
Fast charging	Charge initiation occurred and $V_{HTF} < V_{TEMP} < V_{LTF}$ and $V_{EDV} \leq V_{CELL} < V_{MCV}$	Low if V_{SNS} > 250mV, nominal; high if V_{SNS} < 200mV, nominal	Low
Charge complete	-AV ≥ 6mV/cell or PVD ≥ 0 to 3mV/cell or $\Delta V_{TEMP}/\Delta T$ > 14mV/minute or $V_{TEMP} < V_{TCO}$ or $V_{TEMP} > V_{LTF}$ or maximum time or maximum voltage		–
Top-off (optional; see Table 3)	Charge complete and top-off time not exceeded and $V_{TEMP} > V_{TCO}$ and $V_{CELL} < V_{MCV}$	Activated per V_{SNS} (see fast state) for 260µs of every 2080µs	Low
Trickle (Optional; see Table 3)	Charge complete and top-off disabled or top-off complete	Trickle charge activated per V_{SNS} for period specified in Table 3 *	Low
Charge inhibit	$\overline{INH}$ low	Z	Z

Definitions: $V_{CELL} = V_{BAT} - V_{SNS}$; $V_{MCV} = 0.8 \cdot V_{CC}$; $V_{EDV} = 0.4 \cdot V_{CC}$;
$V_{TEMP} = V_{TS} - V_{SNS}$; $V_{LTF} = 0.4 \cdot V_{CC}$; $V_{HTF} = ((1/3 \cdot V_{LTF}) + (2/3 \cdot V_{TCO}))$.
*DSEL = Z also disables trickle.

Table 2. bq2004E LED Output Summary

Mode 1	Charge Action State	LED_1	LED_2
DSEL = V_{SS}	Battery absent	Low	Low
	Fast charge pending or a discharge-before-chargein progress	High	High
	Fast charging	Low	High
	Fast charge complete, top-off, and/or trickle	High	Low
Mode 2	**Charge Action State (See note)**	**LED_1**	**LED_2**
DSEL = Floating	Battery absent	Low	Low
	Fast charge pending or discharge-before-charge in progress	High	High
	Fast charging	Low	High
	Fast charge complete, top-off, and/or trickle	High	Low
Mode3	**Charge Action State**	**LED_1**	**LED_2**
DSEL = V_{CC}	Battery absent	Low	Low
	Fast charge pending or discharge-before-chargein progress	Low	1/8 second high 1/8 second low
	Fast charging	Low	High
	Fast charge complete, top-off, and/or trickle	High	Low

Note: Pulse trickle is inhibited in Mode 2.

reference, V_{HTF} ((1/3 • V_{LTF}) + (2/3 • V_{TCO})) and optionally to an internal low-temperature fault reference, V_{LTF} (0.4 • V_{CC}). These limits establish the acceptable battery and temperature sense voltage window for fast charge initiation. If the battery fails either of these two pre-qualifications for charge, the bq2004E enters a charge-pending mode, waiting for the battery voltage and temperature to become acceptable.

In the case of a battery that is too warm or too cold, the charge action starts when the battery temperature becomes acceptable. In the case of deeply discharged batteries (voltage too low), the bq2004E waits until the battery voltage is at an acceptable level before starting fast charge. In the case of a faulty battery, V_{BAT} may never reach an acceptable voltage level, causing the bq2004E to remain in the charge-pending state.

During the charge-pending mode, the bq2004E continues to pulse at 1/8 of the fast charge rate until the fast charge conditions are met or the top-off time-out period is exceeded. The bq2004E then trickle charges until the fast charge conditions are met.

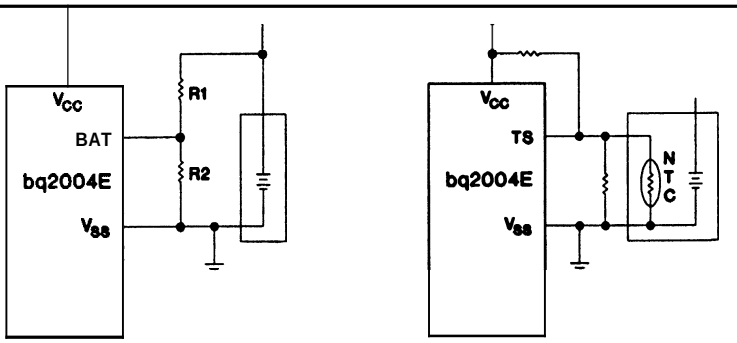
Discharge-Before-Charge

The bq2004E supports discharge-before-charge on the battery, providing conditioning as well as capacity calibration. Once activated, the DIS pin goes active high until V_{CELL} falls below V_{EDV}, at which time fast charge qualification begins.

If $\overline{DCMD}$ is directly connected to V_{SS}, automatic discharge-before-charge is enabled with the application of power to the bq2004E or by battery replacement. A negative-going pulse on $\overline{DCMD}$ causes the bq2004E to initiate a discharge-before-charge action on the battery regardless of charging activity. The $\overline{DCMD}$ pin is internally pulled up to V_{CC}; therefore, not connecting this pin results in disabling the discharge-before-chargefunction. See Figure 4.

TM_1 and TM_2 Pins

The TM_1 and TM_2 pins are three-level input pins used to select the various charge, top-off, and trickle rates, maximum safety times, and -ΔV/PVD holdoff period. Table 3 describes the various states selected by the TM_1 and TM_2 pins.



BAT voltage connection

Thermistor connection

NTC = negative temperature coefficient thermistor.

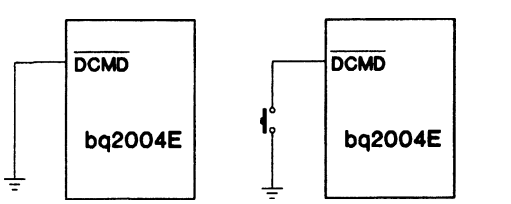
FG-72

Figure 3. Voltage and Temperature Limit Measurement

Fast Charge

Once temperature and voltage prequalifications are met and any requested discharging of the battery is completed, fast charging begins and continues until termination by one or more of the five possible termination conditions:

- Delta temperature/delta time (ΔT/Δt)
- Negative delta voltage (-ΔV) or peak voltage detect (PVD)
- Maximum temperature
- Maximum charge time
- Maximum battery voltage



Always discharge

Discharge on command

FG-73

Figure 4. Discharge-Before-Charge

Voltage Termination Hold-off

At the start of fast charging, there is a hold-off time during which the -ΔV, PVD, and ΔT/Δt t[redacted] are disabled (see Table 3). During hold-off, MOD is active for 1/8th of the charge rate. Once past the initial fast charge hold-off time, -ΔV, PVD, and ΔT/Δt terminations are re-enabled and MOD is active for fast charging per Table 1. Maximum cell voltage (MCV), and maximum temperature (TCO) terminations are not affected by the hold-off period. The hold-off time is not included in the Fast Charge Safety Time.

VSEL	Termination
Low	PVD
Float	-ΔV
High	Disabled

-ΔV or Peak Voltage Detect Termination

The bq2004E has two modes for voltage termination, depending on the state of the VSEL pin. VSEL high enables peak voltage detection; VSEL floating enables -AV detection; and VSEL low disables -AV and PVD terminations. -AV and PVD may be enabled or disabled at any time during the charge cycle. The bq2004E makes a termination decision every 17 seconds. For -ΔV, if V[redacted] ie lower than any previously measured value by 12mV typical, the fast charge phase of the charge action is terminated. This equates to a -ΔV termination of -6mV per cell typical. The -ΔV test is valid only for:

$$0.4 \cdot V_{CC} \le V_{CELL} \le 0.8 \cdot V_{CC}$$

For peak voltage detect, the fast charge phase of the charge action is terminated when V_{CELL} is lower than any previously measured value by 0 to -3mV per cell (-6mV at the BAT pin).

ΔT/Δt Fast Charge Termination

The bq2004E makes a termination decision based on delta temperature/delta time (ΔT/Δt) every 34 seconds. If V_{TEMP} is 16mV (typical) less than the voltage measured 68 seconds previously, the fast charge phase of the *charge* is terminated. The ΔT/Δt test is valid only for:

$$0.2 \cdot V_{CC} \le V_{TEMP} \le 0.4 \cdot V_{CC}$$

Maximum Voltage, Time, and Temperature Terminations

The bq2004E also terminates fast charge for maximum temperature (TCO), maximum time, and maximum voltage (MCV). MCV and TCO reference levels provide the maximum limits for battery voltage and temperature during fast charging. If either of these limits is exceeded, then fast charging or optional top-off charge is terminated. MCV is treated as a fault, so LED_1 and LED_2 are switched low with this condition.

Masimum time selection is programmed using the TM_1 and TM2 pins (see Table 3). Time settings are available for corresponding charge rates ranging from C/4 to 4C.

Temperature Monitoring

Temperature is represented as a voltage input on the bq2004E at the TS pin. Generally this voltage is developed from an NTC (negative temperature coefficient) thermistor referenced to the negative battery terminal. The bq2004E recognizes an internal voltage level of V_{LTF} = 0.4 • V_{CC} as the low-temperature fault (LTF) level.

Note: If $V_{TEMP} \ge V_{LTF}$, *charging* is inhibited (if a cycle has not yet started) or terminated (if a cycle is in progress).

Similarly, the external reference voltage level presented at the TCO pin represents the high-temperature cut-off point at which fast charging is terminated. V_{TCO} should always be less than V_{LTF} to ensure proper device operation.

All temperature prequalifications and ΔT/Δt termination may be disabled by connecting TCO to V_{SS} and tying the TS pin to V_{CC}. ΔT/Δt termination sensitivity is user-adjustable, depending on the values of the external resistor-divider network.

Top-Off Charge

An optional top-off charge phase is selected to follow fast charge termination for charge rates from C/2 to 4C. This option is selected through the TM_1/TM_2 programming pins (see Table 3). The charge control cycle is modified so that the MOD pin is activated for 260µs of every 2080µs. This results in a rate 1/8th that of fast charging. Top-off charge proceeds for a time equal to 4/17 of the fast charge safety time (0.235 • safety time).

Table 3. Fast Charge Safety Time/Hold-Off/Top-Off Table

Fast Charge Rate	Chemistry	TM1	TM2	Fast Charge Safety Time (minutes) Typical	PVD, -ΔV, and ΔT/Δt Hold-Off Time (seconds) Typical	Top-Off Rate	Pulse-Trickle Rate*	Pulse-Trickle Period (Hz)
C/4	Li-Ion	Low	Low	325	137	Disabled	Disabled	Disabled
C/2	NiCd	Float	Low	154	546	Disabled	C/512	15
1C	NiCd	High	Low	77	273	Disabled	C/512	7.5
2C	NiCd	Low	Float	39	137	Disabled	C/512	3.75
4C	NiCd	Float	Float	19	68	Disabled	C/512	1.88
C/2	NiMH	High	Float	154	546	C/16	C/512	15
1C	NiMH	Low	High	77	273	C/8	C/512	7.5
2C	NiMH	Float	High	39	137	C/4	C/512	3.75
4C	NiMH	High	High	19	68	C/2	C/512	1.88

Note: T_A = 25°C, V_{CC} = 5.0V.
*DSEL = Z disables pulse trickle

Maximum time, temperature (TCO), and voltage (MCV) terminations are the only termination methods enabled during top-off. If the fast-charge phase of a charge terminates due to TCO, top-off charge pends until the temperature falls below high temperature fault (HTF).

Pulse-Trickle Charge

Pulse-trickle charge is used to compensate for self-discharge of the battery while idle in the *charger.* The battery pulse-trickles at the end of fast charge and top-off (see Table 1).

In the pulse-trickle state, MOD is active for 260µs of a period specified by the state of TM_1 and TM_2 pine. The resulting trickle rate is C/512. Pulse-trickle and top-off can be disabled by tying TM_1 and TM2 to Vss. Pulse trickle can also be disabled when DSEL = Z.

For pre-charge qualification, MOD is active for 260µs of every 2080µs, resulting in a rate 1/8th that of the fast charge rate. MOD continues to pulse at a 1/8 the rate for the top-off time-out period and then pulse trickles until the fast charge conditions are met. This is useful for bringing up the voltage on a battery after long storage periods.

Charge Inhibit

Fast charge, top-off, and pulse trickle may be inhibited by using the $\overline{INH}$ input pin. When low, the bq2004E suspends all charge activity, drives all outputs to high impedance, and assumes a low-power operational state. When $\overline{INH}$ returns high, a fast-charge cycle is qualified and begins as soon as conditions allow.

Charge Current Control

The bq2004E controls the charge current through the MOD output pin. The current control is designed to support implementation of a constant-current regulator. See Figure 6. Nominal regulated current is:

$$I_{REG} = 0.225V / R_{SNS}$$

When used in this configuration, the *charge* current is monitored at the SNS input by the voltage drop across a resistor, R_{SNS}. R_{SNS} may be chosen to provide a variety of charging currents.

The MOD pin is switched high or low depending on the voltage input to the SNS pin. If the voltage at the SNS pin is less than V_{SNSLO} (0.2V typical), the MOD output is switched high to gate charge current. When the SNS voltage is greater than V_{SNSHI} (0.25V typical), the MOD output is switched low—shutting off current from the supply.

The MOD pin can also be used to regulate constant voltage. For Li-Ion charge control, the bq2004E provides current-limited voltage regulation and *charge* termination based on time and temperature. *See* Figure 6.

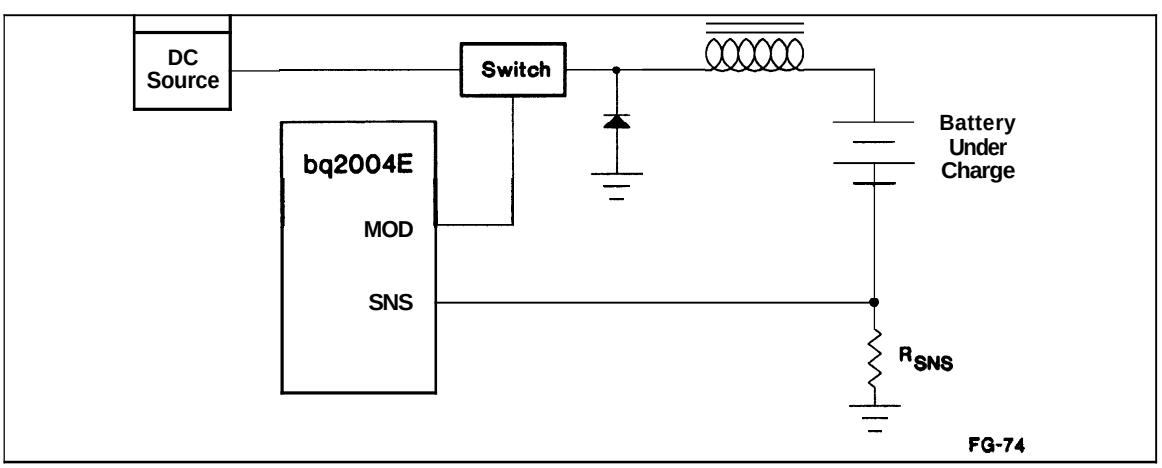


Figure 5. Constant-Current Switching Regulation

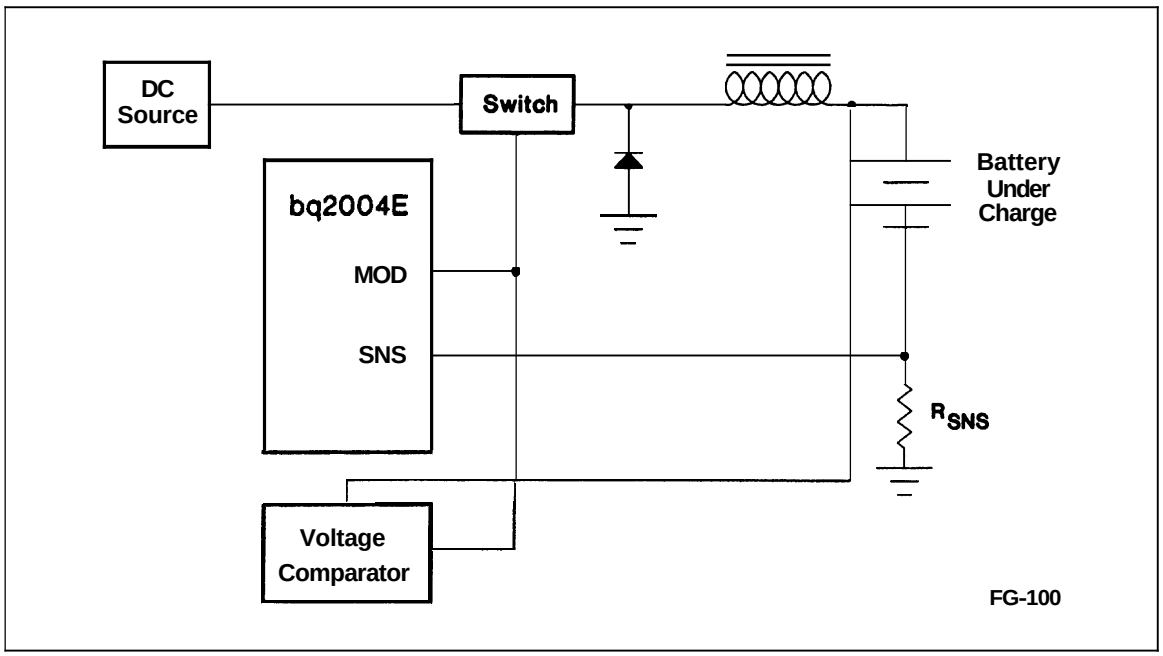


Figure 6. Constant-Voltage Regulation

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Vcc relative to V_{SS}	-0.3	+7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3	+7.0	V	
T_{OPR}	Operating ambient temperature	-20	+70	°C	Commercial
		-40	+85	°C	Industrial "N"
T_{STG}	Storage temperature	-55	+125	°C	
T_{SOLDER}	Soldering temperature		+260	°C	10 sec max.
T_{BIAS}	Temperature under bias	-40	+85	°C	

Note: Permanent device damage may occur if **Absolute Maximum Ratings are exceeded.** Functional operation **should** be limited to the Recommended DC **Operating Conditions** detailed in this data sheet. **Exposure** to conditions beyond the operational limits for extended **periods of** time may *affect* device reliability.

DC Thresholds ($T_A = T_{OPR}$; VCC ±10%)

Symbol	Parameter	Rating	Tolerance	Unit	Notes
V_{SNSHI}	High **threshold** at SNS resulting in MOD = Low	0.05 • Vcc	±0.025	V	
V_{SNSLO}	Low threehold at SNS resulting in MOD = High	0.04 • V_{CC}	±0.010	V	
V_{LTF}	Low-temperature fault	0.4 • V_{CC}	M.030	V	$V_{TEMP} \geq V_{LTF}$ inhibits/ terminates charge
V_{HTF}	High-temperature fault	(⅓ • V_{LTF}) + (⅔ • V_{TCO})	M.030	V	$V_{TEMP} \leq V_{HTF}$ inhibits charge
V_{EDV}	End-of-discharge voltage	0.4• Vcc	±0.030	V	$V_{CELL} < V_{EDV}$ inhibits fast charge
V_{MCV}	Maximum cell voltage	0.8• V_{CC}	±0.030	V	$V_{CELL} > V_{MCV}$ inhibits/ terminates charge

Note: $V_{CELL} = V_{BAT} - V_{SNS}$. $V_{TEMP} = V_{TS} - V_{SNS}$.

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	
V_{CELL}	BAT voltage potential	0		V_{CC}	V	$V_{BAT} - V_{SNS}$
V_{BAT}	Battery input	0	-	V_{CC}	V	
V_{TEMP}	TS voltage potential	0	-	V_{CC}	V	$V_{TS} - V_{SNS}$
V_{TS}	Thermistor input	0	-	V_{CC} - 1.5	V	Valid temperature sensing
		V_{CC} - 0.5		V_{CC}		Disable temperature sensing
V_{TCO}	Temperature cutoff	0.2 * V_{CC}	-	0.4 • V_{CC}	V	Valid $\Delta T/\Delta t$ range
V_{IH}	Logic input high	2.0			V	$\overline{DCMD}$, $\overline{INH}$
	Logic input high	V_{CC} - 0.3			V	TM_1, TM_2, DSEL, VSEL
V_{IL}	Logic input low			0.8	V	$\overline{DCMD}$, $\overline{INH}$
	Logic input low			0.3	V	TM_1, TM_2, DSEL, VSEL
Vow	Logic output high	V_{CC} - 0.8	-	-	V	DIS, MOD, LED_1, LED_2, $I_{OH} \leq -10mA$
V_{OL}	Logic output low			0.8	V	DIS, MOD, LED_1, LED_2, $I_{OL} \leq 10mA$
I_{CC}	Supply current		1	3	mA	Outputs unloaded
I_{SB}	Standby current			1	µA	$\overline{INH} = V_{IL}$
I_{OH}	DIS, LED_1, LED_2, MOD source	-10			mA	@V_{OH} = Vcc - 0.8V
I_{OL}	DIS, LED_1, LED_2, MOD sink	10			mA	@V_{OL} = Vss + 0.8V
I_L	Input leakage			±1	µA	$\overline{INH}$, BAT, V = Vss to Vcc
	Input leakage	50		400	µA	$\overline{DCMD}$, V = Vss to Vcc
I n	Logic input low source			70	µA	TM_1, TM2, DSEL, VSEL, V = Vss to Vss + 0.3V
I_{IH}	Logic input high source	-70			µA	TM_1, TM_2, DSEL, VSEL, V = Vcc - 0.3V to Vcc
I_{IZ}	Tri-state	-2	-	2	µA	TM_1, TM_2, DSEL, and VSEL should be left disconnected (floating) for Z logic input state

Note: All voltages relative to Vss.

Impedance

Symbol	Parameter	Minimum	Typical	Maximum	Unit
R_{BAT}	Battery input impedance	50			MΩ
R_{TS}	TS input impedance	50			MΩ
R_{TCO}	TCO input impedance	50			MΩ
R_{SNS}	SNS input impedance	50			MΩ

Timing (TA = 0 to +70°C; VCC ±10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Note8
t_{PW}	Pulse width for $\overline{DCMD}$ and $\overline{INH}$ pulse command	1			µs	
d_{FCV}	Fast charge safety time variation	0.84	1.0	1.16		V_{CC} = 4.75V to 5.25V; T_A = 0 to 60°C; see Table 3.
t_{REG}	MOD output regulation frequency			300	kHz	Typical regulation capability; V_{CC} = 5.0V
t_{MCV}	$V_{CELL} \geq V_{MCV}$ valid period	1		2	sec	If $V_{CELL} \geq V_{MCV}$ for t_{MCV} during charge or top-off, then a transition of $V_{CELL} < V_{MCV}$ is recognized as battery replaced. Otherwise, $V_{CELL} < V_{MCV}$ is ignored.

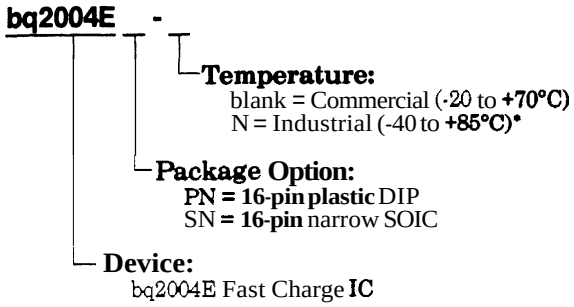
Note: Typical is at T_A = 25°C, V_{CC} = 5.0V.

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	3	Added block diagram	Diagram insertion
1	7	Added VSEL/termination table	Table insertion
1	8	Added values to Table 3	Top-Off rate values
1	11	Changed value for V_{SNSLO} rating	Was: V_{SNSHI} - (0.01 • V_{CC}) Is: 0.04 • V_{CC}

Note: Change 1 = Sept. 1996 B changes from Apr. 1995.

Ordering Information



* Contact factory for availability.

BENCHMARQ

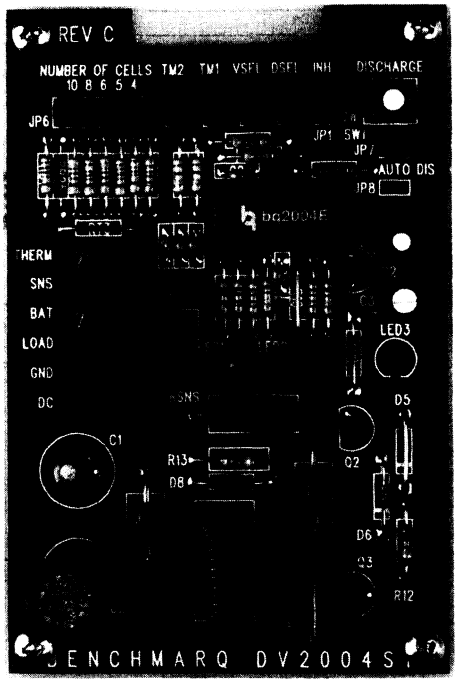
Product Brief **DV2004ES1**

Fast Charge Development System

Control of On-Board p-FET Switch-Mode Regulator

Features

- ➤ bq2004E fast charge control evaluation and development
- ● Charge current sourced from an on-board switch-mode regulator (up to 3.0 A)
- ➤ Fast charge of 4 to 10 NiCd or NiMH cells and one user-defined selection
- ● Fast charge termination by delta temperature/delta time ($\Delta T/\Delta t$), negative delta voltage ($-\Delta V$) or peak voltage detect, maximum temperature, maximum time, and maximum voltage
- ● $-\Delta V$/peak voltage detect, hold-off, top-off, maximum time, and number of cells are jumper-configurable
- ● Programmable charge status display
- ● Discharge-before-charge control with push-button switch or auto discharge-before-charge with jumper
- ● Inhibit fast charge by logic-level input



General Description

The DV2004ES1 Development System provides a development environment for the bq2004E Fast Charge IC. The DV2004ES1 incorporates a bq2004E and a buck-type switch-mode regulator to provide fast charge control for 4 to 10 NiCd or NiMH cells.

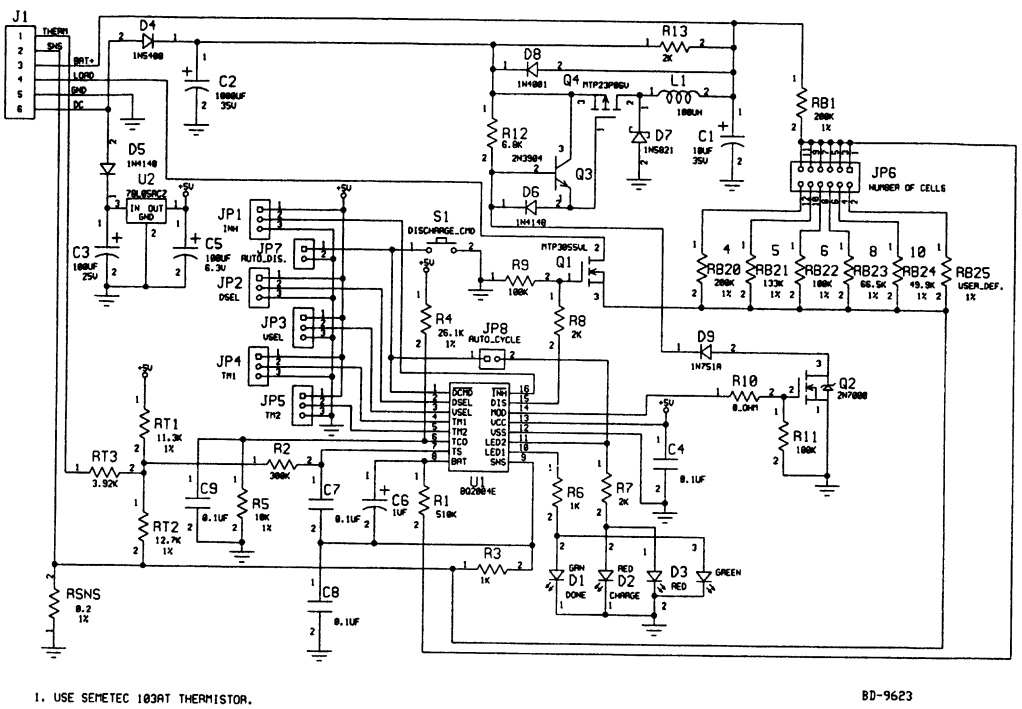
The fast charge is terminated by any of the following: $\Delta T/\Delta t$, $-\Delta V$ or peak voltage detect, maximum temperature, maximum time, maximum voltage, and inhibit command. Jumper settings select the voltage termination mode, the hold-off, top-off, and maximum time limits, and automatic discharge-before-charge.

The user provides a power supply and batteries. The user configures the DV2004ES1 for the number of cells, voltage, charge termination mode, and maximum charge time (with or without top-off), and commands discharge-before-charge with push-button switch S1.

Please review the bq2004E data sheet before using the DV2004ES1 board.

A full data sheet for this product is available on our web site (http://www.benchmarq.com), or you may contact the factory for one.

DV2004ES1 Board Schematic



Product Brief **DV2004ES3**

Nickel/Li-Ion Development System

Control of On-Board p-FET Switch-Mode Regulator

Features

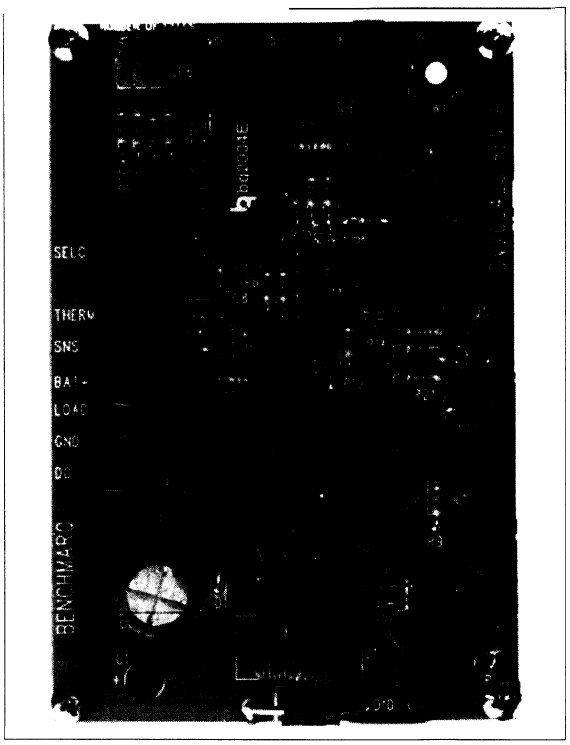
- ➤ bq2004E fast charge control evaluation and development for NiMH, NiCd and Li-Ion chemistries
- Charge current sourced from an on-board switch-mode regulator (up to 2.0 A)
- Fast charge of 3, 6, or 9 NiCd or NiMH cells and 1, 2, or 3 Li-Ion cells
- Fast charge termination by delta temperature/delta time ($\Delta T/\Delta t$), negative delta voltage ($-\Delta V$) or peak voltage detect, maximum temperature, maximum time, and maximum voltage for nickel-based and constant-current to constant-voltage for Li-Ion
- $-\Delta V$/peak voltage detect, hold-off, top-off, maximum time, and number of cells are jumper-configurable
- Programmable charge status display
- Discharge-before-charge control with push-button switch or auto discharge-before-charge with jumper
- Inhibit fast charge by logic-level input

General Description

The DV2004ES3 Development System provides a dual-chemistry development environment for the bq2004E Fast Charge IC. The DV2004ES3 incorporates a bq2004E and a buck-type switch-mode regulator to provide fast charge control for 3, 6, or 9 NiCd or NiMH cells and 1, 2, or 3 Li-Ion cells.

The fast charge is terminated by any of the following: $\Delta T/\Delta t$, -AV or peak voltage detect, maximum temperature, maximum time, maximum voltage, and inhibit command. Jumper settings select the voltage termination mode, the hold-off, top-off, and maximum time limits, and automatic discharge-before-charge.

Fast charge for Li-Ion transitions from a constant-current to constant-voltage regulation. Voltage is regulated to within 1%. Charge complete is indicated at the maximum charge time.

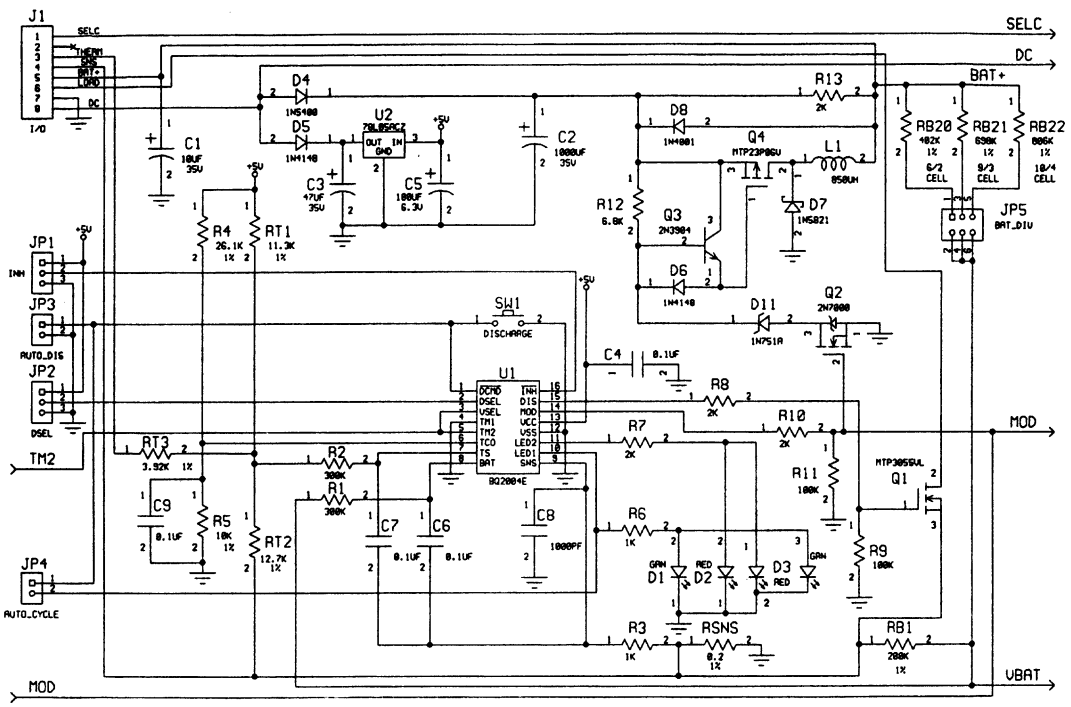


The user provides a power supply and batteries. The user configures the DV2004ES3 for the number of cells and charge termination mode, and commands discharge-before-charge with push-button switch S1.

Please review the bq2004E data sheet and application note: "Using NiMH and Li-Ion Batteries in Portable Applications", before using the DV2004ES3 board.

A full data sheet for this product is available on our web site (http://www.benchmarq.com), or you may contact the factory for one.

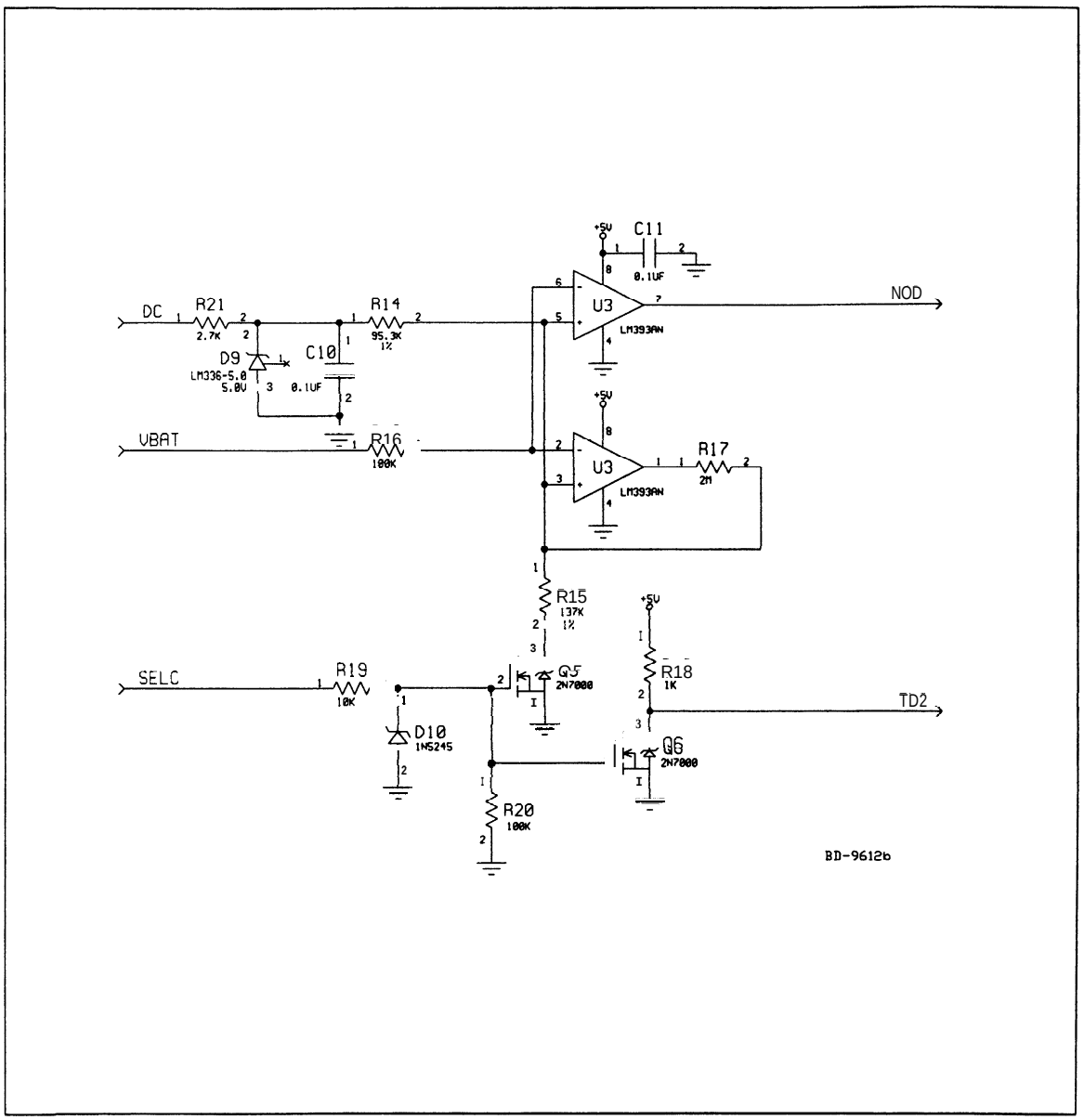
DV2004ES3 Board Schematic



1. USE SEMETEC 103AT THERVISTOR.

BD-9612

DV2004ES3 Board Schematic (Continued)



Notes

bq2005

Dual-Battery Fast Charge IC

Features

- Fast charge control and conditioning for one or two NiMH or NiCd batteries
- Flexible current regulation:
  - Integrated switching charge current controller
  - Gating control for use with external regulation
- Discharge-before-charge for battery conditioning
- Fast *charge* termination by: $\Delta T/\Delta t$, $-\Delta V$, maximum time, maximum temperature, and maximum voltage
- Selectable pulsed "top-off" and trickle charge
- Direct LED control outputa display battery and charge status
- 20-pin 300-mil PDIP or SOIC packages

General Description

The CMOS bq2005 Dual-Battery Fast Charge IC provides comprehensive fast charge control functions with high-*speed* switching power control circuitry for one or two independent battery-pack systems.

The bq2005 is the baeie of a cost-effective solution for sequentially charging two battery packs using flexible control of constant-current or current-limited charging supply. The bq2005 can be used as a frequency-modulated controller operating up to 300KHz far switched regulation of the charging current. The bq2005 may alternatively be used with a linear regulator or transistor to gate an external supply.

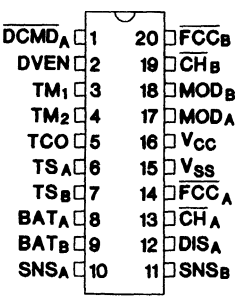
Switch-activated or automatic die-charge-before-chargefor one battery allows bq2005-based chargers to support battery conditioning, eliminating the voltage-depression effect found in some rechargeable battery chemistries.

Fast charge begins with the application of the charging supply or by replacement of the battery. For safety, charge is inhibited until the battery temperature and voltage are within configured limits. Temperature, voltage, and time are monitored throughout fast charge.

Charge is terminated by any of the following:

- Delta temperature/delta time ($\Delta T/\Delta t$)
- Negative delta voltage ($-\Delta V$)
- Maximum temperature
- Maximum time
- Masimumvoltage

Pin Connections



PO-Pin DIP or SOIC

PN-44

Pin Names

$\overline{DCMD_A}$	Discharge command input, battery A
DVEN	$-\Delta V$ enable
TM_1	Tier mode select 1
TM_2	Timer mode select 2
TCO	Temperature cut-off
TS_A, TS_B	Temperature sense input, battery A/B
BAT_A, BAT_B	Battery voltage input, battery A/B
DIS_A	Discharge control output, battery A
$\overline{CH_A}$, $\overline{CH_B}$	Charge status output, battery A/B
$\overline{FCC_A}$, $\overline{FCC_B}$	Fast charge complete output, battery A/B
V_{SS}	System ground
V_{CC}	5.0V ±10% power
MOD_A, MOD_B	Charge current control output, battery A/B
SNS_A, SNS_B	Charging current sense input, battery A/B

Pin Descriptions

$\overline{DCMD}_A$ **Discharge-before-charge** control **input, battery A**

$\overline{DCMD}_A$ **controls** the discharge-before-charge function of the bq2005. A negative-going pulse on $\overline{DCMD}_A$ initiates a discharge to EDV (0.475 • Vcc) followed by a charge if conditions allow. By tying $\overline{DCMD}_A$ to ground, automatic discharge-befom-charge is enable either by the application of power or by battery replaced.

DVEN **-ΔV** enable input

This input **controls** the **-ΔV** charge **termination** test. If DVEN is high, the -AV termination method is enabled. If DVEN is low, **-ΔV** is disabled. DVEN *may* change state at any time.

TM_1, TM2 Timer mode inputs **($TM_{1,2}$)**

TM_1 and TM_2 are three-level inputs that **control** the **settings** for fast charge safety timer and **"top-off"/trickle** charge control. See Table 3 for details.

TCO **Temperature cut-off** threshold input

Maximum allowable battery **temperature**-sensor voltage. If the potential between **TS_A** and **SNS_A** or **TS_B** and **SNS_B** is **less** than the voltage at the TCO input, then any fast charging or 'top off charging is terminated for the respective battery.

TS_A, TS_B Temperature sense **inputs,** battery A/B **($TS_{A,B}$)**[1]

Input for external battery temperature monitoring thermistor.

SNS_A, SNS_B Charging current sense **inputs,** battery **A/B ($SNS_{A,B}$)**[1]

$SNS_{A,B}$ controls the switching of **$MOD_{A,B}$** based on an **external sense** resistor network. This provides the reference **potentials** for both the **$TS_{A,B}$** and **$BAT_{A,B}$** pins. If **$SNS_{A,B}$ is connected to V_{SS},** then **$MOD_{A,B}$** switches high at the beginning of charge, and low at the end of charge. See **Figure 1** and Table 1 for details.

BAT_A, BAT_B Battery voltage inputs, battery **A/B ($BAT_{A,B}$)**[1]

BAT_A and **BAT_B** are the divided **input** voltages for battery A and battery B. This **potential** is limited to 0.96 • Vcc and 0.475 • Vcc and is **generally** developed by a high impedance **resistor**-divider network connected between the **positive** and the negative terminals of the battery.

DIS**A** **Discharge control** output

Push-pull output **used** to control an **external** transistor to **discharge** battery A before charging. **DIS_A** is active high.

$\overline{CH}_A$, $\overline{CH}_B$ Charge status outputs, **battery A/B ($\overline{CH}_{A,B}$)**[1]

Open-drain output indicating charging status. See **Figure 1** and Table 2 for details.

$\overline{FCC}_A$, $\overline{FCC}_B$ Fast charge complete outputs, **battery A/B ($\overline{FCC}_{A,B}$)**[1]

Open-drain output indicating fast charge complete. See Figure 1 and Table 2 for details.

MOD_A, MOD_B Charge current control **outputs,** battery A/B **($MOD_{A,B}$)**[1]

$MOD_{A,B}$ is a push-pull output that is used to control the charging current to the battery. **$MOD_{A,B}$** switches high to enable charging current to flow and low to inhibit charging current flow. **See Figure 1** and Table 1 for details.

VCC **V_{CC} supply input**

5.0V, ±10% power input.

Vss **Ground**

[1] Notation used in **text** for generic pin reference.

1

Functional Description

Figure 1 illustrates charge control and display status during a bq2005 charge cycle. Table 1 outlines the various bq2005 operational states and their associated conditions, which are described in detail in the following sections.

Charge Action Control

The bq2005 initiates a charge by either the application of power on V_{CC} or by a battery replacement. A charge action is controlled by the inputs from $\overline{DCMD}_A$, DVEN, $TS_{A,B}$, $BAT_{A,B}$, and $TM_{1,2}$.

The bq2005 is a sequential *charger*, initiating a charge action *on* either battery A or B. If both battery A and battery B are present when V_{CC} is applied to the bq2005, the charge action begins with battery B if conditions are acceptable. If A is present and B absent, the charge cycle begins on A and fast charge will complete before beginning on B. The bq2005 controls the initiation of a charge action and checks for acceptable battery temperature (between LTF—low-temperature fault and HTF—high-temperature fault) and voltage (between EDV—end-of-discharge voltage and MCV—maximum cell voltage) prior to fast charging. The fast charging process begins, and the bq2005 tests for the full-charge conditions: $\Delta T/\Delta t$ and/or $-\Delta V$, with temperature, time, and voltage safety terminations.

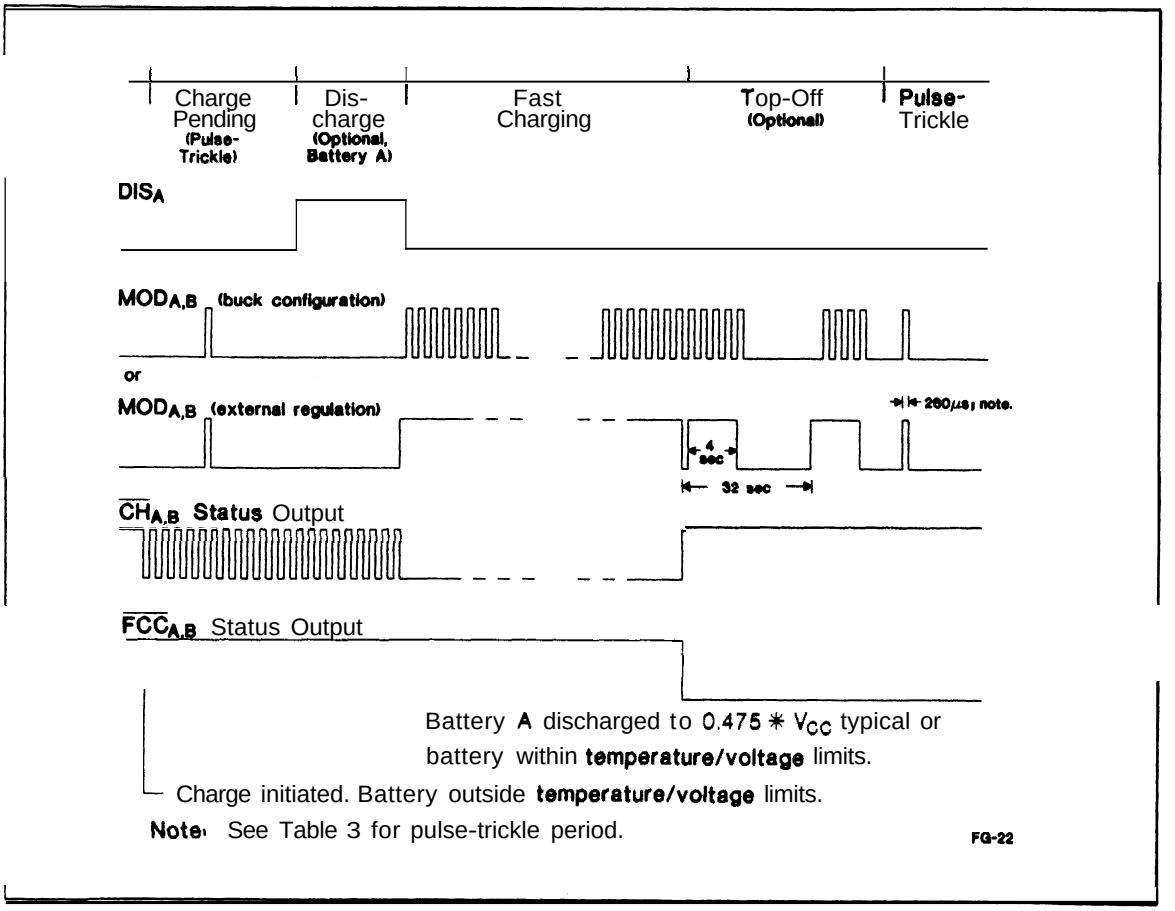


Figure 1. Example Charging Action Events

Charge Status Indication

Table 1 outlines the various charge action states and the associated $MOD_{A,B}$ and DIS_A output states. Table 2 describes the charge status indicated by the $\overline{CH}_{A,B}$ and $\overline{FCC}_{A,B}$ outputs, which may be connected to an LED indicator through a current-limiting resistor. In all cases, if the battery voltage at the BAT_A and/or BAT_B pins exceeds the maximum cell voltage (0.95 • V_{CC}), the $\overline{CH}_{A,B}$ and $\overline{FCC}_{A,B}$ outputs are held high

Table 1. bq2005 Operational Summary

Charge Action State	Conditions	$MOD_{A,B}$ Output	DIS_A Output
Battery absent	V_{CELL} 2 V_{MCV}	Trickle charge activated per V_{SNS} for period specified in Table 3. Output is inactive if other battery is fast charging or topping off.	Low
Charge initiation	V_{CC} applied or V_{CELL} drops from 2 V_{MCV} to < V_{MCV} (battery insertion)	-	-
Discharge-before-charge (optional, battery A)	$\overline{DCMD}_A$ high-to-low pulse or tied to V_{SS} when V_{CC} is applied; V_{EDV} < V_{CELL} < V_{MCV}	MOD_A low	High
Pending	Charge initiation occurred and V_{TEMP} ≥ V_{LTF} or V_{TEMP} ≤ V_{HTF} or V_{CELL} < V_{EDV}, or other battery fast charging	Trickle charge activated per V_{SNS} for period specified in Table 3. Output is inactive if other battery is fast charging or topping off.	Low
Fast charging	Charge initiation occurred and V_{HTF} < V_{TEMP} < V_{LTF} and V_{EDV} ≤ V_{CELL} < V_{MCV}	Low if V_{SNS} > 250mV, nominal; high if V_{SNS} < 200mV, nominal	Low
Charge complete	-ΔV ≥ 13mV typical or $\Delta V_{TEMP}/\Delta T$ > 14mV/minute or V_{TEMP} < V_{TCO} or V_{TEMP} > V_{LTF} or maximum time or maximum voltage	-	-
Top-off (optional; see Table 3)	Charge complete and top-off time not exceeded and V_{TEMP} > V_{TCO} and V_{CELL} < V_{MCV}	Activated per V_{SNS} (see fast charging state) for 4 of every 32 sec. Output is inactive if other battery is fast charging or topping off.	Low
Trickle	Charge complete and top-off disabled or top-off complete	Trickle charge activated per V_{SNS} for period specified in Table 3. Output is inactive if other battery is fast charging or topping off.	Low

Notes: $V_{CELL} = V_{BAT} - V_{SNS}$, $V_{MCV} = 0.95 \cdot V_{CC}$, $V_{EDV} = 0.475 \cdot V_{CC}$.
$V_{TEMP} = V_{TS} - V_{SNS}$, $V_{LTF} = 0.4 \cdot V_{CC}$, $V_{HTF} = ((1/4 \cdot V_{LTF}) + (3/4 \cdot V_{TCO}))$

1

Table 2. bq2005 LED Output Summary

Charge Action State	Note	$\overline{CH}_A$, $\overline{CH}_B$	$\overline{FCC}_A$, $\overline{FCC}_B$
Battery absent	Battery not inserted	High	High
Charge initiated and pending or battery A discharge-beforecharge	Fast charge conditions are not valid, or other battery is fast charging	1/8 sec high, 1/8 sec low	High
Fast charging		Low	High
Charge complete, top-off, and/or trickle		High	Low

Note: $\overline{CH}_A$ and $\overline{FCC}_A$ are related outputs, but are independent of the states of $\overline{CH}_B$ and $\overline{FCC}_B$, which are also related outputs.

Battery Voltage and Temperature Measurements

Battery voltage and temperature are monitored for maximum and minimum allowable valuea. The battery voltage sense input, $BAT_{A,B}$, for a battery pack must be divided to between 0.95 • V_{CC} and 0.475 • V_{CC} for proper operation. A resistor-dividerratio of:

$$\frac{R1}{R2} = \frac{N}{2.375} - 1$$

is recommended to maintain the battery voltage within the valid range, where R1 is the resistor connected to the positive battery terminal, and R2 is the resistor connected to the respective $SNS_{A,B}$ pins. See Figure 2.

Note: The resistor-divider network impedance should be above 200KΩ to protect the bq2005 if V_{CC} is removed with batteries inserted.

The bq2005 requires that the thermistors used for temperature measurements have a negative temperature coefficient. The temperature sense voltage inputs at $TS_{A,B}$ are developed using a resistor-thermistor network between V_{CC} and $SNS_{A,B}$. *See Figure* 2.

Battery Removal Detection

An external resistor, R_{EXT}, between the battery positive lead and the charging supply input is necessary to allow the bq2005 to detect battery insertion.

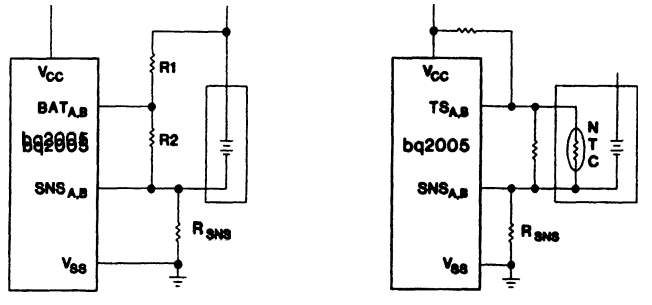


Figure 2. Voltage and Temperature Limit Measurement

Initiating a Charge Action

A battery charge action is initiated with either battery insertion or application of Vcc to the bq2005. Battery insertion is recognized when the voltage at either of the $BAT_{A,B}$ pins falls from above the internal V_{MCV} reference level to below that level. When Vcc is applied to the bq2005, a charge action begins after a brief power-on reset period.

Temperature and Voltage Prequalification

A charge action is prequalified by the battery temperature and voltage. Before fast charging can begin, the battery temperature and voltage must fall within predetermined acceptable limits.

V_{CELL} is compared to an internal low-voltage reference, V_{EDV}, which is the minimum acceptable battery voltage for fast charging. V_{TEMP} voltage is compared to an internal low-temperature fault reference, V_{LTF}, and the internal hot-temperature fault reference, V_{HTF}. These limits establish the acceptable battery and temperature sense voltage window for fast charge initiation. If the battery fails either of these two prequalifications for charge, the bq2005 enters a charge-pending mode, waiting for the battery voltage and temperature to become acceptable.

In the case of a battery that is too warm or too cold, the charge action starts when the battery temperature becomes acceptable. In the case of deeply discharged batteries (voltage too low), the bq2005 waits until the battery voltage is at an acceptable level before starting fast charge. In the case of a faulty battery, V_{BAT} may never reach an acceptable voltage level, causing the bq2005 to remain in the charge-pending state. The bq2005 continues to trickle charge (if enabled) the battery until the fast charge condition becomes acceptable.

Discharge-Before-Charge

The bq2005 supports discharge-before-charge on battery A, providing battery conditioning as well as capacity calibration. Once activated, the DIS_A pin goes active high until V_{CELL} falls below V_{EDV}, at which time the battery starts fast charge.

If $\overline{DCMD}_A$ is directly connected to V_{SS}, automatic discharge-before-charge is enabled with either the application of power to the bq2005 or by battery replaced. A negative-going pulse on $\overline{DCMD}_A$ causes the bq2005 to initiate a discharge-before-charge action on BAT_A regardless of its current charging activity. The $\overline{DCMD}_A$ pin is internally pulled up to Vcc; therefore, not connecting this pin results in disabling the discharge-before-charge function. See Figure 3.

Fast charging, top-off, and trickle charge of battery B are not affected during the discharge of battery A.

Fast Charge: TM_1 and TM2 Pins

When fast charge begins on either of the batteries, the other battery remains in a pending state until the first battery terminates fast charge. At this time, fast charging begins on the second battery. When fast charge of the second battery terminates, optional top-off sequentially proceeds if enabled (program pine TM_1 and TM_2). A pulse-trickle begins on both batteries at the end of top-off or fast charge. Fast charge and optional top-off of battery B always take precedence over battery A when both batteries are present.

The TM_1 and TM_2 pine are three-level input pine used to select the various charge and top-off rates, maximum safety times, and -AV hold-off period. Table 3 describes the varioue states selected by the TM_1 and TM_2 pine.

Once temperature and voltage prequalifications are met and any *requested* discharging of the battery is completed, fast charging begins and continues until termination by one or more of the five possible termination conditions:

- Delta temperature/delta time (AT/&)
- Negative delta voltage (-ΔV)
- Maximum temperature
- Maximum charge time
- Maximum battery voltage

Voltage Termination Hold-off

At the start of fast charging, there is a hold-off time during which the -ΔV termination is disabled (see Table 3). Once past the initial fast charge hold-off time, -AV termination is re-enabled. AT/&, maximum cell voltage (MCV), and maximum temperature (TCO) terminations are not affected by the hold-off period.

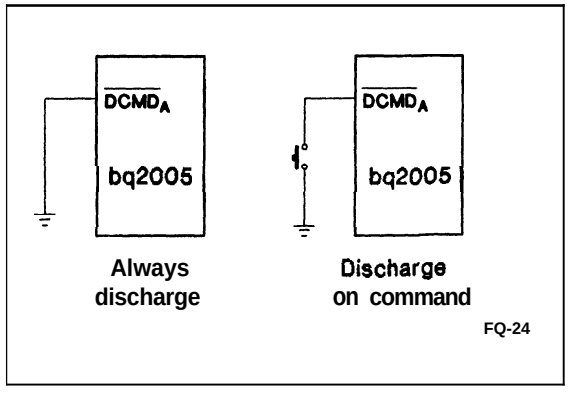


Figure 3. Discharge-Before-Charge

-AV Termination

The bq2005 makes a termination decision based on negative delta voltage every 32 seconds. If V_{CELL} is lower than any previously measured value by 13mV typical, the fast charge phase of the charge action is terminated. This equates to a -AV termination of -6mV per cell typical. The -AV test is valid only for:

$$0.475 \cdot V_{CC} \le V_{CELL} \le 0.95 \cdot V_{CC}$$

-AV detection may be enabled or disabled at any time using the DVEN pin.

ΔT/Δt Fast Charge Termination

The bq2005 makes a termination decision based on delta temperature/delta time (ΔT/Δt) every 32 seconds. If V_{TEMP} is 16mV (typical) less than the voltage measured 64 seconds previously, the fast charge phase of the charge is terminated.

The ΔT/Δt test is valid only for:

$$0.2 \cdot V_{CC} \le V_{TEMP} \le 0.4 \cdot V_{CC}$$

Maximum Voltage, Maximum Time, and Maximum Temperature Safety Terminations

The bq2005 also terminates fast charge for maximum temperature (TCO), maximum time, and maximum voltage (MCV). MCV and TCO reference levels provide the maximum limits for battery voltage and temperature during fast charging. If either of these limits is exceeded, both fast charging and optional top-off charge are terminated. MCV is treated as a fault, so $\overline{FCC}_{A,B}$ and $\overline{CH}_{A,B}$ become inactive with this condition

Maximum time selection is programmed using the TM_1 and TM_2 pins (see Table 3). Time settings are available for corresponding charge r a t . ranging from C/4 to 4C.

Temperature Monitoring

Temperature is represented as a voltage input on the bq2005 at the TS_A and TS_B pins. Generally this voltage is developed from an NTC (negative temperature coefficient) thermistor referenced to the negative battery terminal. The bq2005 recognizes an internal voltage level of $V_{LTF} = 0.4 \cdot V_{CC}$ as the low-temperature fault (LTF) level. If $V_{TEMP} \ge V_{LTF}$, charging is inhibited or terminated.

Table 3. Fast Charge Safety Time/Hold-Off/Top-Off Table

Corresponding Fast Charge Rate	TM_1	TM_2	Fast Charge Safety (minutes)	-ΔV Hold-Off Time (seconds)	Top-Off Rate	Pulse-Trickle Rate	Pulse-Trickle Period (Hz)
			Typical	Typical			
C/4	Low	Law	360	137	Disabled	Dieabled	Disabled
C/2	Float	Law	180	820	Disabled	C/32	240
1C	High	Low	90	410	Disabled	C/32	120
2C	Low	Float	45	200	Disabled	C/32	60
4C	Float	Float	23	100	Disabled	C/32	30
C/2	High	Float	180	820	C/16	C/64	120
1C	Low	High	90	410	C/8	C/64	60
2C	Float	High	45	200	C/4	C/64	30
4C	High	High	23	100	C/2	C/64	15

Note: T_A = 25°C, V_{CC} = 5.0V.

Similarly, the external reference voltage level presented at the TCO pin represents the high-temperature cut-off point at which fast charging is terminated. V_{TCO} should always be less than V_{LTF} to ensure proper device operation.

All temperature prequalifications and $\Delta T/\Delta t$ termination may be disabled by connecting TCO to V_{SS} and fixing the $TS_{A,B}$ pin level to 0.2 • V_{CC}. $\Delta T/\Delta t$ termination sensitivity is user-adjuetable, depending on the values of the external resistor-divider network.

Top-Off Charge

An optional top-off charge phase is selected to follow fast charge termination for charge rates from C/2 to 4C. This option is selected through the TM_1/TM_2 programming pins (see Table 3).

If selected, the bq2005 "tops off the battery at the pulsed rate. The charge control cycle is modified so that $MOD_{A,B}$ pins are activated for only 4 of every 32 seconds. This results in a rate 1/8th that of fast charging. Top-off charge proceeds for a time equal to the fast charge safety time. Temperature (TCO) and voltage (MCV) terminations are the only termination methods enabled during "top-off." Any fast charge initiation immediately terminates a top-off charge in progress.

Pulse-Trickle Charge

Pulse-trickle charge is used to compensate for self discharge of the battery while idle in the charger, and to bring a depleted battery to a valid charge voltage prior to fast charge. Both batteries pule-trickle at the end of fast charge and top-off, and prior to charge (see Table 1).

In the pulse-trickle state, MOD_A and MOD_B are separately active for 260µs of a period specified by the state of TM_1 and TM_2 pine. The resulting trickle rate is C/64 when top-off is enabled and C/32 when top-off is disabled. Pulse-trickle and top-off can be dieabled by tying TM_1 and TM_2 to V_{SS}. Fast charge or top-off of either battery suspends pulse-trickle.

Charge Current Control

The bq2005 controls charge current through the $MOD_{A,B}$ output pins. The current control is designed to support implementation of a constant-current switching regulator. See Figure 4. Nominal regulated current is:

$$I_{REG} = 0.225V / R_{SNS}$$

When ueed in this configuration, the charge current is monitored at the $SNS_{A,B}$ input by the voltage drop across a resistor, R_{SNS}. R_{SNS} may be chosen to provide a variety of charging currents and may differ between slots A and B.

The $MOD_{A,B}$ pine are switched high or low depending on the voltage input to the $SNS_{A,B}$ pine. If the voltage at the $SNS_{A,B}$ pine is lees than V_{SNSLO} (0.2V typical), the MOD outputs are switched high to gate charge current through the inductor to the battery. When the SNS voltage is greater than V_{SNSHI} (0.25V typical), the MOD outputs are switched low--shutting off current from the supply.

The $MOD_{A,B}$ pins can also be used to gate an external charging current source. When an external current source is used, a sense resistor is not required, and the $SNS_{A,B}$ pins are connected to V_{SS}. See Figure 5.

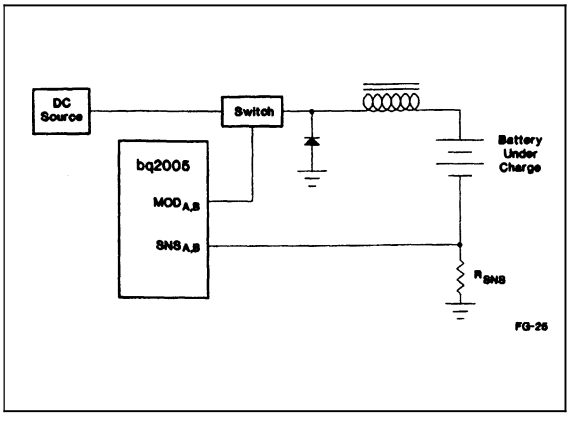


Figure 4. Constant-Current Switching Regulation

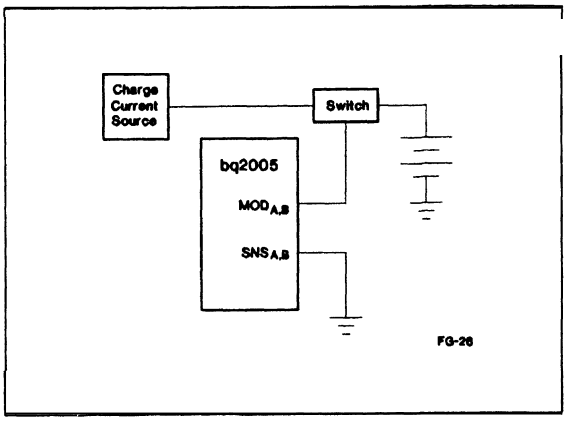


Figure 5. External Current Regulation

1

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	V_{CC} relative to V_{SS}	-0.3	+7.0	V	
VT	DC voltage applied on *any* pin excluding V_{CC} relative to V_{SS}	-0.3	+7.0	V	
T_{OPR}	Operating ambient temperature	-20	t70	°C	Commercial
		-40	+85	°C	Industrial "N"
T_{STG}	Storage temperature	-55	+125	°C	
T_{SOLDER}	Soldering temperature		+260	"C	10 sec max.
T_{BIAS}	Temperature under bias	-40	+85	"C	

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds ($T_A = T_{OPR}$; V_{CC} ±10%)

Symbol	Parameter	Rating	Tolerance	Unit	Notes
V_{SNSHI}	High threshold at $SNS_{A,B}$ resulting in $MOD_{A,B}$ = Low	0.05 • V_{CC}	d.025	V	
V_{SNSLO}	Low threshold at $SNS_{A,B}$ resulting in $MOD_{A,B}$ = High	0.04 • V_{CC}	±0.010	V	
V_{LTF}	Low-temperature fault	0.4 • V_{CC}	±0.030	V	V_{TEMP} 2 V_{LTF} inhibits/ terminates charge
V_{HTF}	High-temperatwe fault	(¼ • V_{LTF}) + (¾ • V_{TCO})	±0.030	V	$V_{TEMP} \leq V_{HTF}$ inhibits charge
V_{EDV}	End-of-discharge voltage	0.475 • V_{CC}	±0.030	V	$V_{CELL} < V_{EDV}$ inhibits fast charge
V_{MCV}	Maximum œll voltage	0.95• V_{CC}	±0.030	V	$V_{CELL} > V_{MCV}$ inhibits/ terminates charge

Note: $V_{CELL} = V_{BAT} - V_{SNS}$.

$V_{TEMP} = V_{TS} - V_{SNS}$.

Recommended DC Operating Conditions (T_A = 0 to +70°C)

Symbol	Parameter	Inimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	
V_{CELL}	BAT voltage potential	0	-	V_{CC}	V	V_{BAT} - V_{SNS}
V_{BAT}	Battery input	0	-	V_{CC}	V	
V_{TEMP}	TS voltage potential	0	-	V_{CC}	V	V_{TS} - V_{SNS}
V_{TS}	Thermistor input	0	-	V_{CC}	V	
V_{TCO}	Temperature cutoff	0.2 • V_{CC}	-	0.4 • V_{CC}	V	
V_{IH}	Logic input high	2.0	-	-	V	$\overline{DCMD}_A$, DVEN
	Logic input high	V_{CC} - 0.3	-	-	V	TM_1, TM_2
V_{IL}	Logic input low	-	-	0.8	V	$\overline{DCMD}_A$, DVEN
	Logic input low	-	-	0.3	V	TM_1, TM_2
V_{OH}	Logic output high	V_{CC} - 0.5	-	-	V	DIS_A, $MOD_{A,B}$, $I_{OH} \leq$ -5mA
V_{OL}	Logic output low	-	-	0.5	V	DIS_A, $\overline{FCC}_{A,B}$, $\overline{CH}_{A,B}$, $MOD_{A,B}$, $I_{OL} \leq$ 5mA
I_{CC}	Supply current	-	1.0	3.0	mA	Outputs unloaded
I_{OH}	DIS_A, $MOD_{A,B}$ source	-5.0	-	-	mA	@V_{OH} = V_{CC} - 0.5V
I_{OL}	$\overline{DIS}_A$, $\overline{FCC}_{A,B}$, $MOD_{A,B}$, $\overline{CH}_{A,B}$ sink	5.0	-	-	mA	@V_{OL} = V_{SS} + 0.5V
I_L	Input leakage	-	-	±1	µA	DVEN, V = V_{SS} to V_{CC}
		-	-	-400	µA	$\overline{DCMD}_A$, V = V_{SS}
I_{IL}	Logic input low source	-	-	70.0	µA	TM_1, TM_2, V = V_{SS} to V_{SS} + 0.3V
I_{IH}	Logic input high source	-70.0	-	-	µA	TM_1, TM_2, V = V_{CC} - 0.3V to V_{CC}
I_{IZ}	TM_1, TM_2 tri-state open detection	-2.0	-	2.0	µA	TM_1, TM_2 should be left disconnected (floating) for Z logic input state
I_{BAT}	Input current to $BAT_{A,B}$ when battery is removed	-	-	-20	µA	V_{CC} = 5.0V; T_A = 25°C; input should be limited to this current when input exceeds V_{CC}.
V_{THERM}	$\Delta T/\Delta t$ detection threshold from $TS_{A,B}$		16 ± 4		mV	V_{CC} = 5.0V, T_A = 25°C
-ΔV	Negative delta voltage detection		13 ± 4		mV	V_{CC} = 5.0V, T_A = 25°C

Note: All voltages relative to V_{SS}.

1

Impedance

Symbol	Parameter	Minimum	Typical	Maximum	Unit
$R_{BATA,B}$	Battery A/B input impedance	50			MP
$R_{TSA,B}$	$TS_{A,B}$ input impedance	50			MΩ
R_{TCO}	TCO input impedance	60			MΩ
$R_{SNSA,B}$	$SNS_{A,B}$ input impedance	50			MΩ

Timing (TA = 0 to +70°C; VCC ±10%)

Symbol	Parameter	Ynimum	Typical	Maximum	Unit	Notes
t_{PW}	Pulse width for $\overline{DCMD}_A$ pulse command	1			µs	Pulse start for charge or *discharge*-before-charge
d_{FCV}	Fast charge safety time variation	*0.84*	1.0	1.16	-	V_{CC} = 4.5V to 5.5V; see Table 3.
t_{REG}	MOD output regulation frequency			300	kHz	*Typical* regulation capability; V_{CC} = 5.0V
t_{MCV}	$V_{CELL} \geq V_{MCV}$ valid period	-		1	sec	If $V_{CELL} \geq V_{MCV}$ for t_{MCV}, then a transition of $V_{CELL} < V_{MCV}$ is recognized as battery replaced. Otherwise, $V_{CELL} < V_{MCV}$ is ignored.

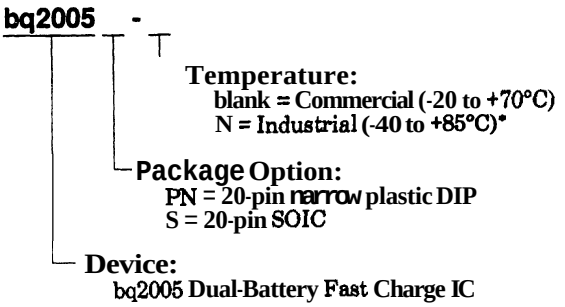
Note: Typical is at T_A = 25°C, V_{CC} = 5.0V.

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	10	Input leakage (I_L)	Was ± 400µA; $\overline{DCMD}_A$, V = V_{SS} to V_{CC}; is -400µA; $\overline{DCMD}_A$, V = V_{SS}.
2	10	Input current to $BAT_{A,B}$ when battery is removed (I_{BAT})	Was -1.0mA maximum; is -20µA maximum.
3	9	V_{SNSLO} Rating	Was V_{SNSHI} - (0.01 * V_{CC}); is 0.04 * V_{CC}

Note: Change 1 = July 1993 B "Preliminary" changes from May 1993 A draft data sheet.
Change 2 = Nov. 1993 C "Final" changes from July 1993 B "Preliminary."
Change 3 = Sept. 1996 D from Nov. 1993 C.

Ordering Information



* Contact factory for availability.

BENCHMARQ

Product Brief **DV2005L1**

Fast Charge Development System

1

Control of PNP Power Transistor

Features

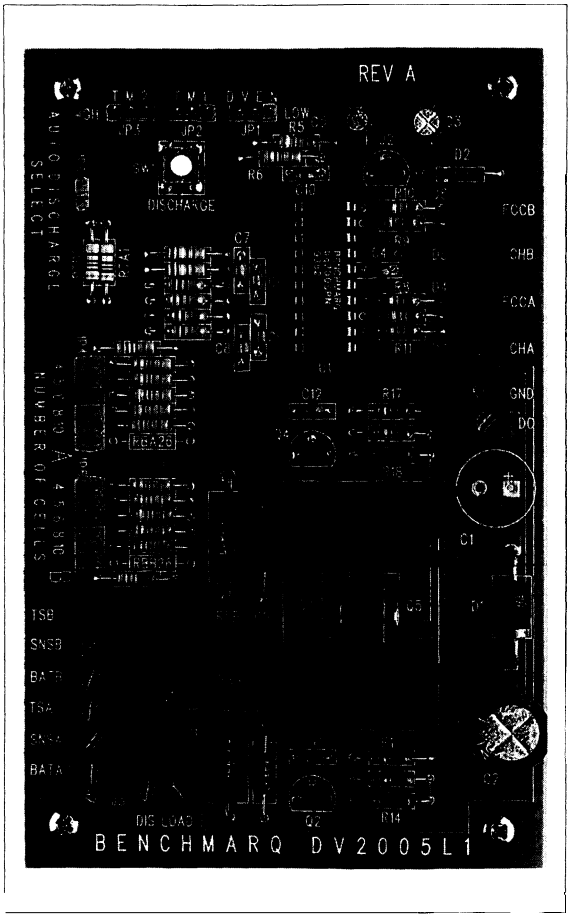
- bq2005 fast charge control evaluation and development
- Charge current sourced from two on-board frequency-modulated linear regulators (up to 3.0 A)
- Fast charge control and conditioning for one or two NiMH and/or NiCd batteries containing 4 to 10 NiCd or NiMH cells; user-configurable for applications that use other numbers of cells
- Sequential charging of two battery packs
- Fast charge termination by delta temperature/delta time ($\Delta T/\Delta t$), negative delta voltage ($-\Delta V$), maximum temperature, maximum time, and maximum voltage
- $-\Delta V$ enable, hold-off, top-off, trickle rate, maximum charge time, and number of cells are jumper-configurable
- Charging status displayed on LEDs (two for each battery)
- Discharge-before-charge control with push-button switch for battery A
- Selectable pulsed "top-off' charge and trickle charge

General Description

The DV2005L1 Linear Development System provides a development environment for the bq2005 Dual-Battery Fast Charge IC. The DV2005L1 incorporates a bq2005 and two frequency-modulated linear regulators to provide fast charge control for 4 to 10 NiCd or NiMH cells.

Review the bq2005 data sheet and the application note, "Using the bq2005 to Control Fast Charge," before using the DV2005L1 board.

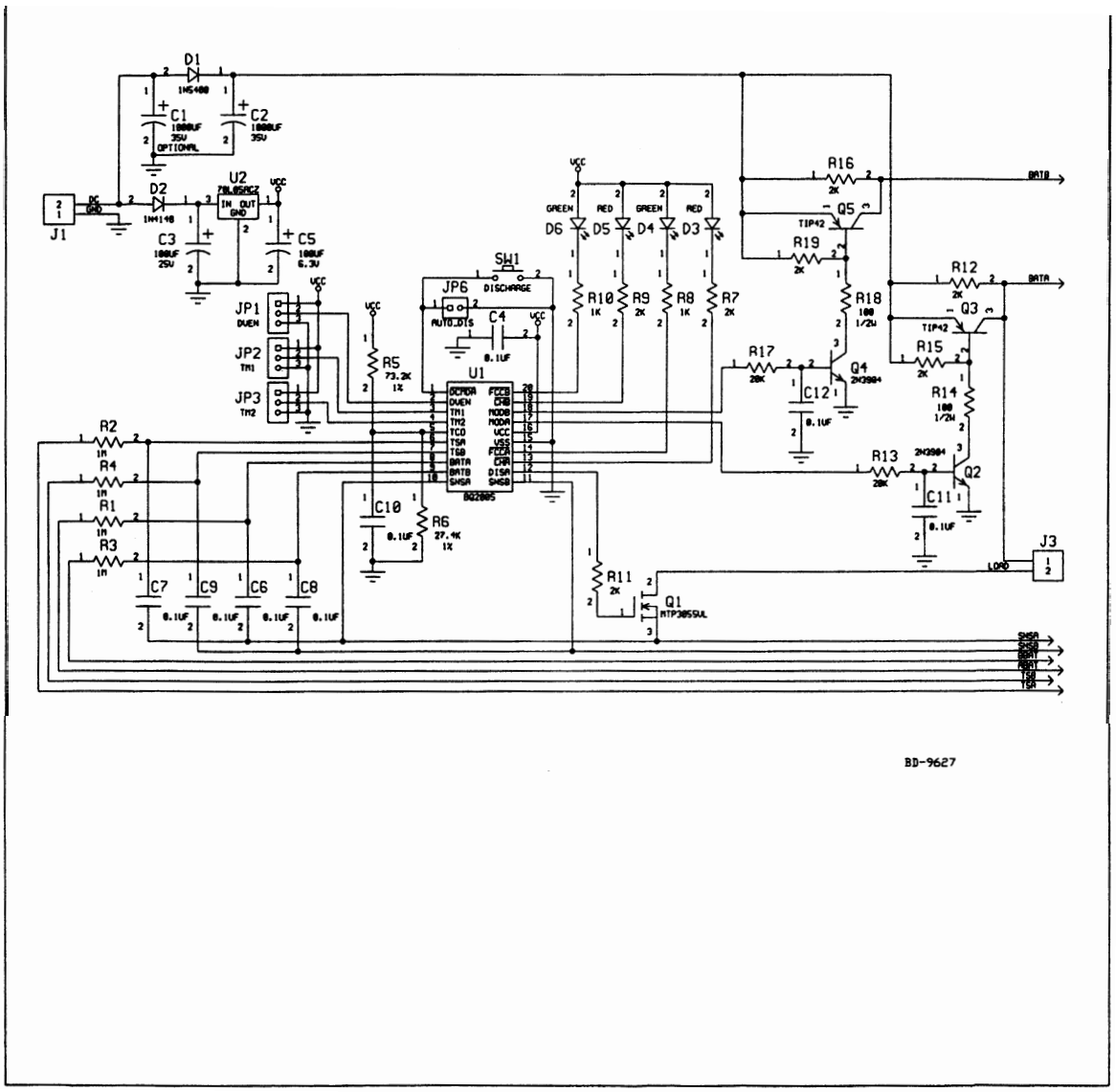
The fast charge is terminated by any of the following: $\Delta T/\Delta t$, $-\Delta V$, maximum temperature, maximum time, and maximum voltage. Jumper settings select the -AV enabled state, select the hold-off, top-off, trickle, and maximum time limits.



The user provides a power supply and batteries. The user configures the DV2005L1 for the number of cells, -AV charge termination enabled or disabled, and maximum charge time (with or without top-off), and commands discharge-before-charge with push-button switch SW1.

A full data sheet for this product is available on our web site (http://www.benchmarq.com), or you may contact our factory for one.

DV2005L1 Board Schematic



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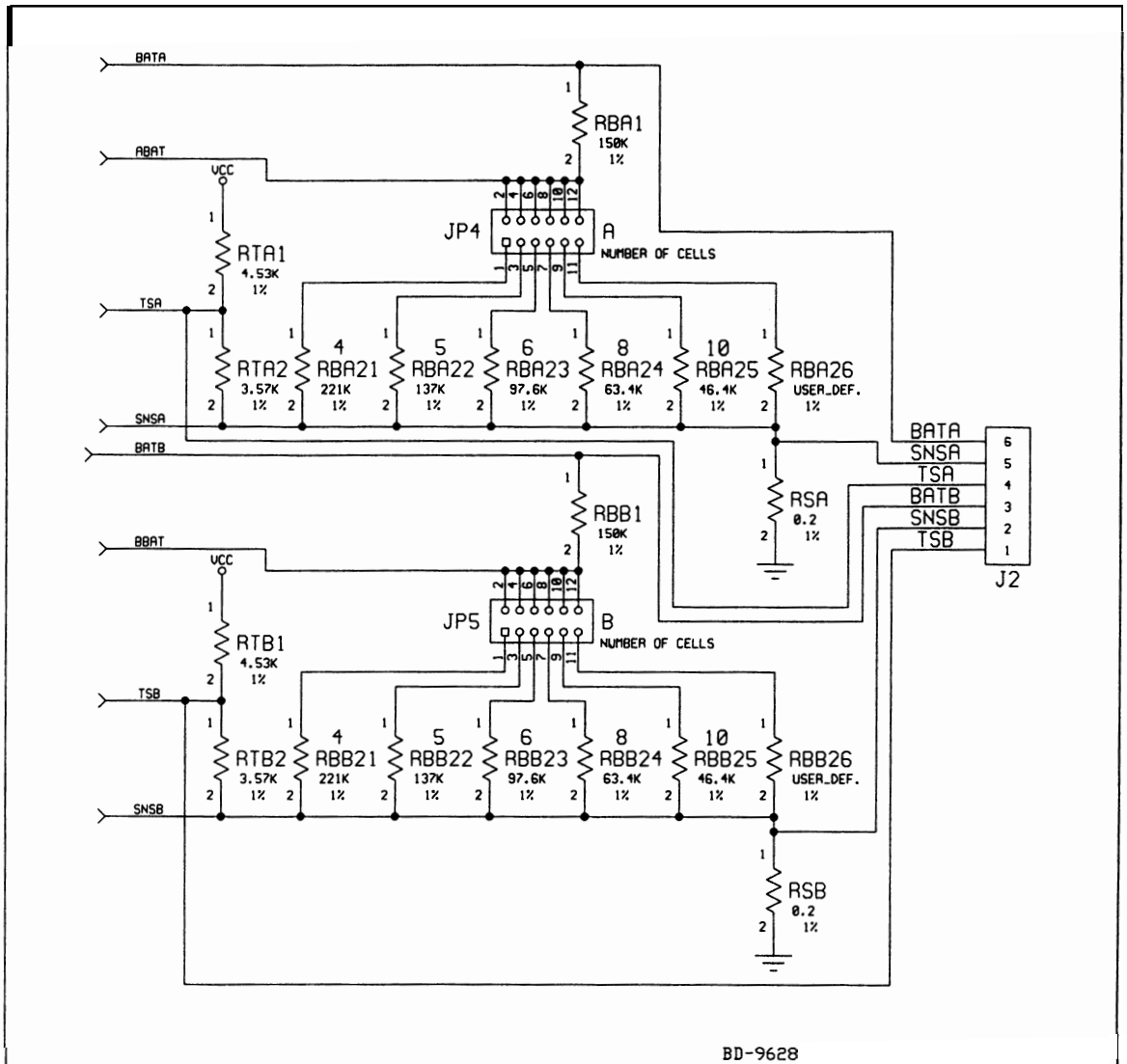
DV2005L1 Board Schematic (Continued)



Notes

BENCHMARQ

Product Brief **DV2005S1**

Fast Charge Development System

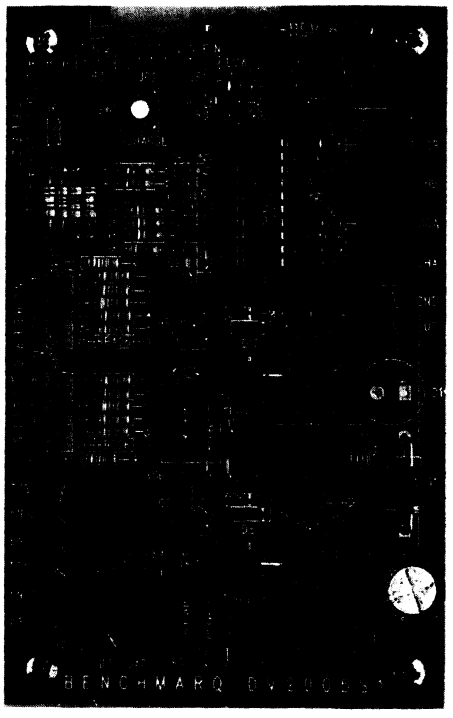
1

Control of On-Board p-FET Switch-Mode Regulator

Features

- bq2005 fast charge control evaluation and development
- ➤ Charge current sourced from two on-board switch-mode regulators (up to 3.0 A)
- ➤ Fast charge control and conditioning for one or two NiMH and/or NiCd batteries containing 4 to 10 NiCd or NiMH cells; user-configurable for applications that use other numbers of cells

  Sequential charging of two battery packs
- Fast charge termination by delta temperaturddelta time ($\Delta T/\Delta t$), negative delta voltage ($-\Delta V$), maximum temperature, maximum time, and maximum voltage
- -AV enable, hold-off, top-off,trickle rate, maximum charge time, and number of cells are jumper-configurable
- Charging status displayed on LEDs (two for each battery)
- Discharge-before-charge control with push-button switch for battery A
- ➤ Integrated switching charge current controller to 300KHz
- Selectable pulsed "top-off' charge and trickle charge



General Description

The DV2005S1 Switching Development System provides a development environment for the bq2005 Dual-Battery Fast Charge IC. The DV2005S1 incorporates a bq2005 and two buck-type switch-mode regulators to provide fast charge control for 4 to 10 NiCd or NiMH cells.

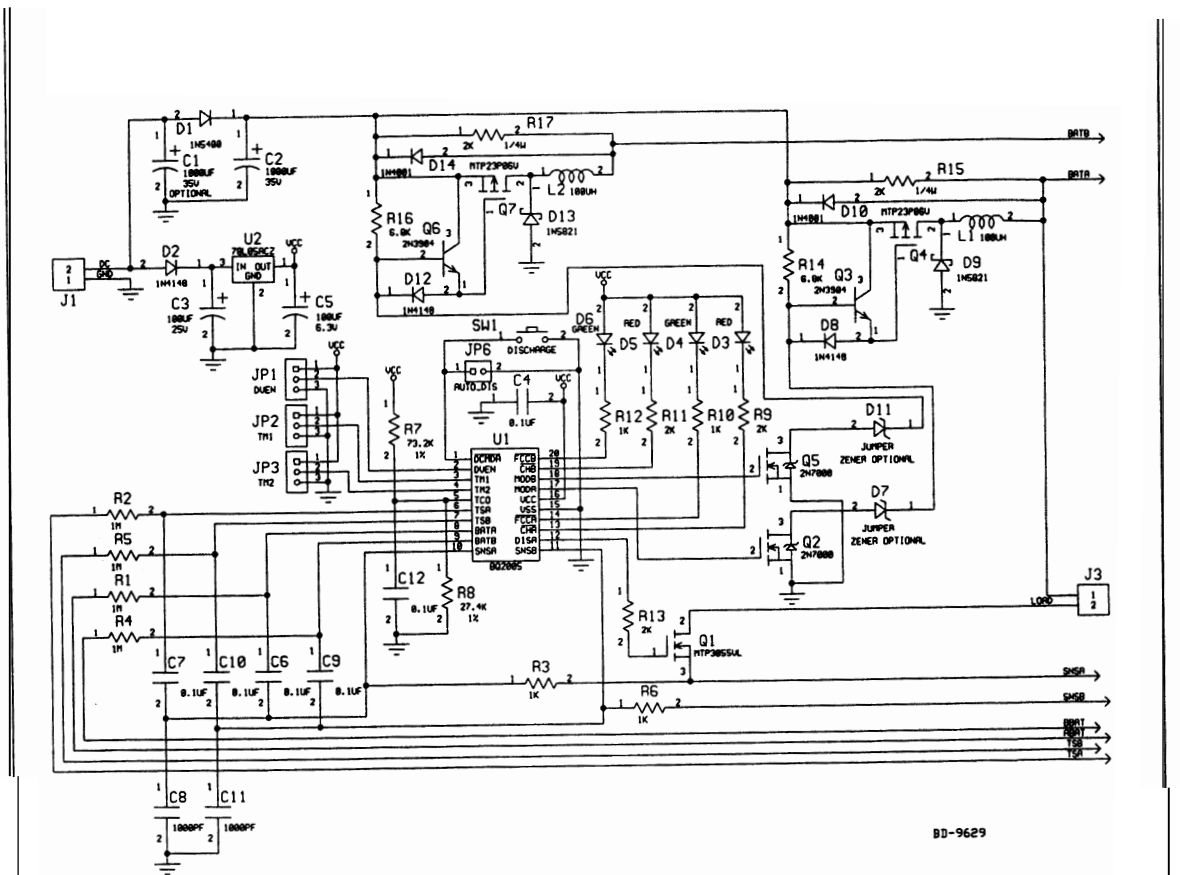
Review the bq2005 data sheet and the application note, "Using the bq2005 to Control Fast Charge," before using the DV2005S1 board.

The fast charge is terminated by any of the following: $\Delta T/\Delta t$, $-\Delta V$, maximum temperature, maximum time, and maximum voltage. Jumper settings select the $-\Delta V$ enabled state, select the hold-off, top-off, trickle, and maximum time limits.

The user provides a power supply and batteries. The user configures the DV2005S1 for the number of cells, $-\Delta V$ charge termination enabled or disabled, and maximum charge time (with or without top-off), and commands discharge-before-charge with push-button switch SW1.

A full data sheet for this product is available on our web site (http://www.benchmarq.com), or you may contact the factory for one.

DV2005S1 Board Schematic



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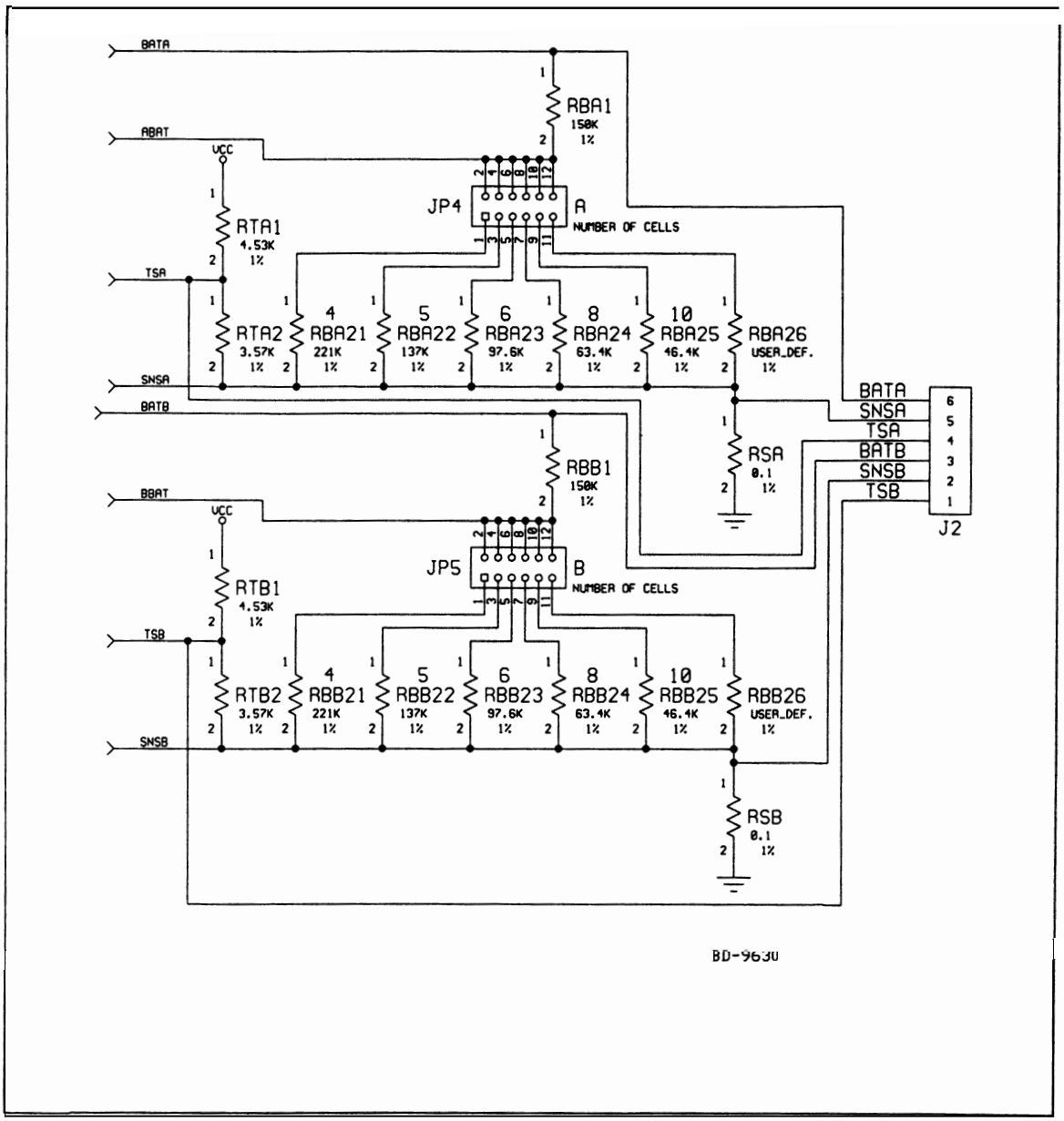
DV2005S1 Board Schematic (Continued)



Notes

BENCHMARQ

Product Brief **DV2005S3**

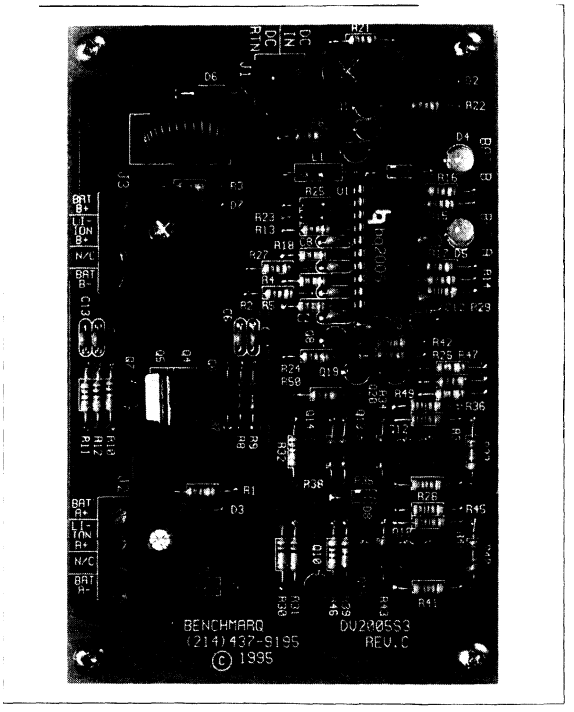
Nickel/Li-Ion Development System

1

Control of On-Board p-FET Switch-Mode Regulator

Features

- bq2005 fast charge control evaluation and development for NiMH, NiCd, and Li-Ion
- ➤ Charge current (up to 2.0A) sourced from an on-board switch mode regulator to 300kHz
- ➤ Sequential fast charge control for one or two batteries packs containing 3, 6, or 9 NiCd or NiMH cells or 1 to 3 Li-Ion cells
- Fast charge termination by $\Delta T/\Delta t$, $-\Delta V$, maximum time, temperature, and voltage, and minimum current (for voltage regulated Li-Ion charging)
- ➤ Charging status displayed on 2 LEDs per battery pack
- Jumper configurable for number of cells, maximum charge time, hold-off period, top-off rate, and pulse trickle rate and frequency.
- Discharge-before-charge control with push-button switch or auto discharge-before-charge with jumper
- Inhibit fast charge with on board jumper or logic-level input



General Description

The DV2005S3 Development System provides a dual-chemistry development environment for the bq2005 Dual-Battery Fast Charge IC. The DV2005S3 incorporates a bq2005 and a buck-type switch-mode regulator to provide fast charge control for two battery packs containing 3, 6, or 9 NiCd or NiMH cells or 1 to 3 Li-Ion cells.

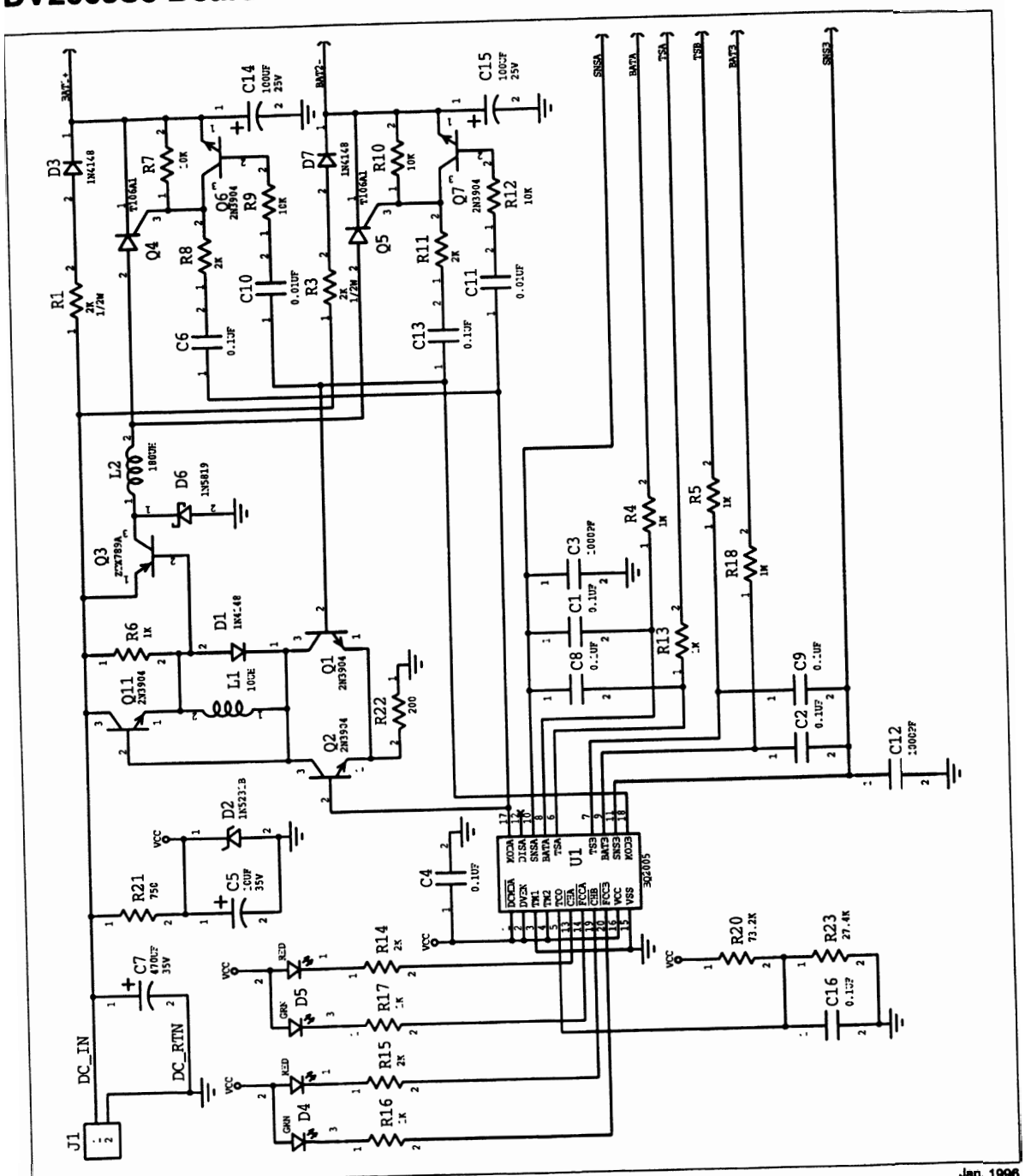
Fast charge for Nickel chemistry batteries is terminated by any of the following: $\Delta T/\Delta t$, $-\Delta V$, maximum charge time, maximum temperature, and maximum voltage. Li-Ion fast charging is accomplished by a current limited phase followed by a voltage regulated (within 1%) phase, and terminated by a minimum current criterion backed up by maximum voltage and maximum time.

Fast charge can be inhibited by an on-board jumper or an external logic level input.

The user supplies a power supply and batteries. Please review the bq2005 data sheet before using the DV2005S3 board. The user configures the DV2005S3 for number of cells, maximum time, hold-off period, top-off rate, pulse trickle rate and frequency, and manual (push button switch) or auto discharge-before-charge.

A full data sheet for this product is available on our web site (http://www.benchmarq.com), or you may contact the factory for one.

DV2005S3 Board Schematic



Jan. 1996

BENCHMARQ

Using the bq2005 to Control Fast Charge

1

Introduction

This application note describes the use and functions of the bq2005 controlling a current source to fast charge NiCd or NiMH batteries. The bq2005 may also serve as the modulator for a switching-mode constant-current regulator to provide an efficient charge current source. Examples illustrate the ease with which the bq2005 is incorporated into applications.

The bq2005 is targeted for applications requiring state-of-the-art dual-battery fast-charging at minimal cost. It provides sophisticated full-charge detection techniques such as ΔT/Δt (delta temperature/delta time) and -ΔV (negative delta voltage) that enable the user to take advantage of advanced battery technologies such as nickel metal-hydride (NiMH) and high-capacity fast-charge nickel cadmium (NiCd). Systems using the bq2005 can be easily upgraded from NiCd batteries to NiMH batteries without system redesign.

Background

A significant advantage of the bq2005 over other fast-charge solutions is the use of ΔT/Δt and/or -ΔV as the primary decisions for fast-charge termination. ΔT/Δt detection is one of the most sensitive and reliable methods for fast-charge termination when charging NiMH and NiCd batteries. Near full charge, the temperature rise begins to accelerate. The ΔT/Δt decision typically precedes the peak voltage, allowing for minimal overcharge stress. The ΔT/Δt method also tolerates varying rates of charge, which may be desirable when charging during system operation.

Compared to the ΔT method, which uses two sensors to monitor battery temperature and ambient temperature, the ΔT/Δt method uses a single thermistor to monitor the rate of temperature increase. This approach is more sound in cases when the initial battery temperature may be significantly different from the ambient temperature. This ΔT/Δt termination decision can easily be disabled.

An input from a battery voltage divider enables the bq2005 to detect -ΔV, which is a very reliable charge terminator for NiCd batteries and most NiMH batteries, depending on the application. -ΔV detection in the bq2005 may be temporarily disabled during periods when the charge current fluctuates greatly or during the beginning of a fast charge to eliminate false peaks. -ΔV termination is logic-level selectable without affecting other termination choices.

To help ensure safety for the battery and system, fast charging may also be terminated at a high-temperature cutoff threshold (TCO), a safety time period, or a maximum cell voltage threshold (MCV). To avoid possible premature fast-charge termination when charging batteries after long periods of storage, the bq2005 disables -ΔV detection during a short "hold-off" period at the start of fast charge. This hold-off period is configured as described in the bq2005 data sheet.

The bq2005 may be configured to have two or three charge stages. In a two-stage configuration, the fast-charge stage controlled by the bq2005 is preceded and followed by a pulse-trickle charge at a rate controlled by the programming pins of the bq2005. In a three-stage configuration, the fast charge is followed by a top-off charge stage at 1/8 the fast charge rate. This allows the battery to be quickly and safely brought to a full charge state. Following top-off, a trickle charge at a pulsed rate equivalent to C/64 is supplied to the battery to compensate for self-discharge

Basic Charge-Control Operation

Three detailed applications follow this section. One provides direct control of a linear regulator, and the other two provide switch-mode current regulation.

Gating Current

Figure 1 shows an example of external source gating. With SNS tied to V_{SS}, the bq2005 enables charge current to the battery by asserting MOD at the start of charge and maintaining this state until charge is terminated. In this example, R1, Q2, R4, R5, R6, and Q1 form the switching circuit. MOD drives Q2 into conduction—saturating Q1.

The current-handling capability of this c h i t depends on the components selected to perform the switching and current-regulation functions. Table 1 shows some suggested component combinations for corresponding currents.

The voltage-boost circuit shown in Figure 1 is necessary to keep the voltage on either BAT_A or BAT_B above MCV while the other battery is charging (assumes only one battery is inserted). This implementation is limited to 15V DC. Please contact Benchmarq's Applications Group for assistance with other input voltage configurations, or for alternative methods.

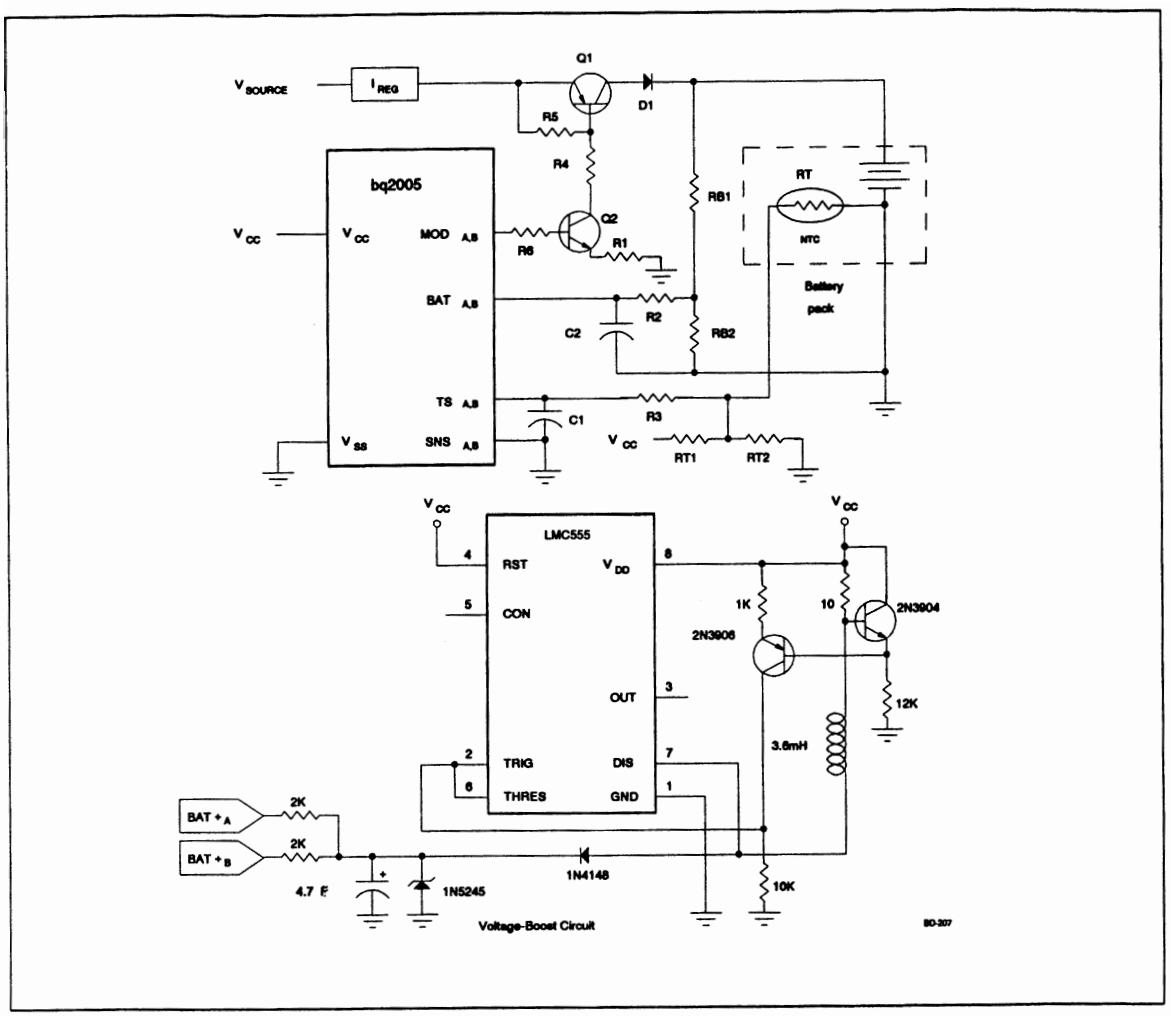


Figure 1. Gated External Source (Bipolar Switch Option)

Table 1. Suggested Component Combinations

I_{IN}	Q1	a 2	R1	R4	R5	R6
0.5A	MPS750	2N3904	150Ω ¼W	–	1KΩ	–
1A	MPS750	2N3904	68Ω ½W	100Ω ½W	1KΩ	–
2A	TIP42	2N3904	43Ω ½W	51Q ½W	200Ω	–
3A	TIP42	2N3904	27Q 1W	27R 1W	200Ω	–
5A	IRFR9010	2N3904	100Ω ¼W	–	1KΩ	33KΩ
8A	IRF9Z22	2N3904	100Ω ¼W	–	1KΩ	33KΩ

Charge Initiation

Charge may be initiated by applying power to the IC or by battery insertion. Charge initiation by application of power to the IC works as follows: When V_{CC} is applied, the bq2005 is held in reset for approximately one and one-half seconds. At the end of the reset period, a charge cycle initiates as soon as conditions allow. If both batteries are present, fast-charging battery B takes precedence over charging battery A. If battery A is inserted while fast charge is pending on battery B, the bq2005 trickle charges both batteries, and then fast charges battery B after conditions allow. If battery B is inserted while fast charge is pending on battery A, the bq2005 trickle charges both batteries, and then fast charges battery B when conditions allow.

Charge initiation on battery replacement relies on the $BAT_{A,B}$ pin voltage being greater than MCV in the absence of a battery, and falling below MCV when the battery is connected. To ensure this condition, pull-up resistors from $BAT_{A,B}$+ (positive pack terminals) to the charging voltage source (V_{DC} in step-down regulators, the boosted charging voltage in step-up regulators) are sized to elevate the empty battery location voltage on the $BAT_{A,B}$ pins such that MCV is exceeded.

When the battery is replaced, the voltage on $BAT_{A,B}$ should fall below MCV, at which time a charge cycle initiates as soon as conditions allow.

Table 2, Charge Action Truth Table, describes the bq2005 charge actions under a variety of battery and charge states.

Discharge-Before-Charge

It may occasionally be desirable to discharge the battery to a known voltage level prior to charge. The reason for this may either be to remedy a voltage-depression effect found in some NiCd batteries or to determine the battery's *charge* capacity.

Figure 2 illustrates the implementation of this function for battery A. If $\overline{DCMD_A}$ is directly connected to V_{SS}, automatic discharge-before-charge is enabled with battery replaced on application of power to the bq2005. A negative strobe signal on $\overline{DCMD_A}$ also initiates discharge-before-charge. This function takes precedence over a charge action and commences immediately when conditions warrant, forcing DIS_A to a high state until the voltage sensed on BAT_A falls below V_{EDV} (0.475 • Vcc). Charging begins as soon as conditions allow.

Care should be taken not to overheat the battery during this process; excessive temperature is not a condition that terminates discharge.

Note: Because V_{SNS} may be above V_{SS} in bq2005 switching regulation applications, the internal battery voltage monitoring uses $V_{BAT} - V_{SNS}$, or V_{CELL}. This battery voltage monitoring, V_{CELL}, maintains a representative comparison voltage independent of any current through R_{SNS}.

Table 2. Charge Action Truth Table

V_{CC}	BAT_A	BAT_B	Charge Action
0→5V	V	V	Fast charge B, pend A
0→5V	V	N	Fast charge A
0→5V	N	V	Fast charge B
5V	↑	F	Fast charge B, pend A
5V	↑	L	Trickle A and B, fast charge B and pend A when conditions allow
5V	L	↑	Trickle A and B, fast charge B and pend A when conditions allow
5V	F	↑	Fast charge A, pend B
5V	D	L	Trickle A, trickle B
5V	L	D	Trickle A, trickle B
5V	D	V	Fast charge B, pend top-off A
5V	V	D	Fast charge A, pend top-off B
5V	D	D	Top off B, trickle A, then top off A, trickle B
5V	D	↑	Abort top-off A
5V	↑	D	Abort top-off B
5V	T	L	Trickle A, trickle B
5V	L	T	Trickle A, trickle B
5V	T	V	Fast charge B, pend trickle A
5V	V	T	Fast charge A, pend trickle B
5V	T	T	Trickle A, trickle B

V = Battery inserted and valid charge conditions:
$0.475 \cdot V_{CC} \le V_{CELL} \le 0.95 \cdot V_{CC}$
$0.4 \cdot V_{CC} \ge V_{TS} \ge V_{HTF}$

L = Battery inserted and outside temperature limit or below V_{EDV}.

N = Battery removed: $V_{CEU} > 0.96 \cdot V_{CC}$

F = Fast charge

D = Top-off

T = Trickle

↑ = Battery insertion: V_{DIV} transitioning from ≥ 0.95 • Vcc to $V_{CELL} \le 0.95 \cdot V_{CC}$

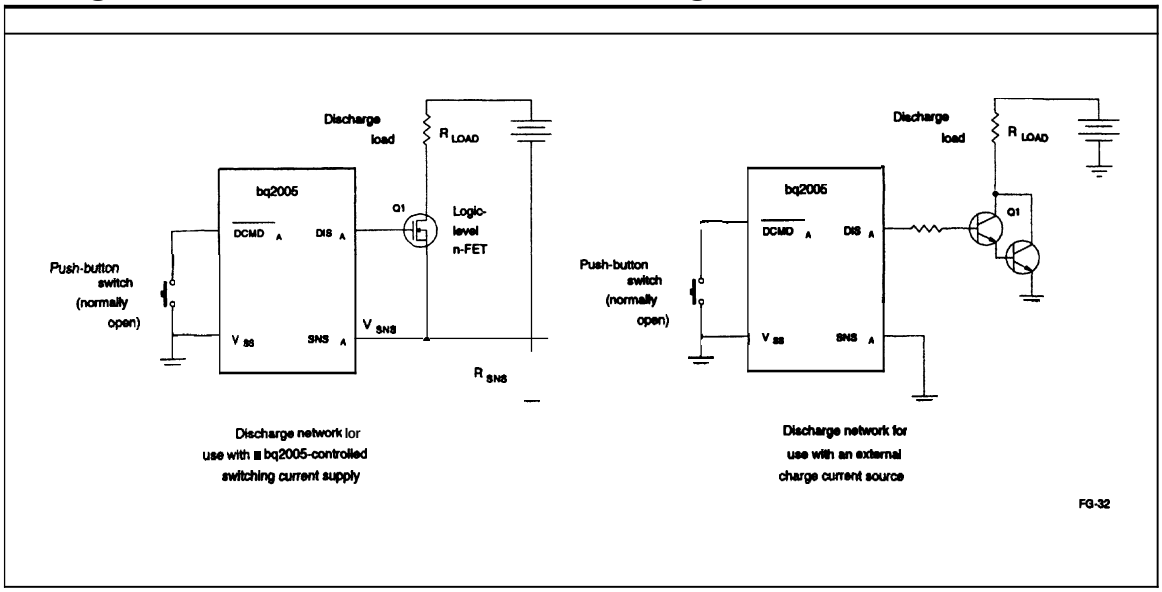


Figure 2. Battery Conditioning Network

The discharge-before-charge function is ignored or terminated when $V_{BAT} - V_{SNS} > V_{MCV}$ (battery removed). If the discharge-before-charge function is not desired, $\overline{DCMD_A}$ should be tied to Vcc or left floating. $\overline{DCMD_A}$ is internally pulled up to Vcc.

Configuring the $BAT_{A,B}$ Inputs

The bq2005 uses the battery voltage sense input on the $BAT_{A,B}$ pins to control discharge-before-charge, qualify charge initiation, terminate charge at an absolute limit, and facilitate negative delta voltage (-ΔV) detection.

V_{BAT} may be derived from a simple passive network across the battery. As shown in Figure 1, resistors RB1 and RB2 are chosen to divide the battery voltage down to the optimal detection range, which is between V_{MCV} and V_{EDV} ($0.475 \cdot V_{CC} \le V_{DN} \le 0.95 \cdot V_{CC}$).

For NiCd and NiMH batteries, the battery terminal voltage is divided down to this potential per the following equation:

$$\frac{RB1}{RB2} = \frac{N}{2.375} - 1$$

where N = number of cells, RB1 is the resistor connected to the positive battery terminal, and RB2 is the resistor connected to the negative $SNS_{A,B}$ pins.

Although virtually any value may be chosen for RB1 and RB2 due to the high input impedance of the $BAT_{A,B}$ pin, the values selected must not be so low as to appreciably drain the battery nor so large as to degrade the circuit's noise performance. Constraining the source resistance as seen from $BAT_{A,B}$ between 20KΩ and 1MΩ is acceptable over the bq2005 operating range. Total impedance between the battery terminal and Vss should typically be about 300KΩ to 1MΩ. See Table 3.

Table 3. Suggested RB1 and RB2 Values for NiCd and NiMH Cells

Number of Cells (V_{BAT} Divisor)	RB1	RB2
3	137 KΩ	523 KΩ
4	357 KR	523 KR
5	309 KΩ	280 KR
6	301 KR	196 KΩ
7	316 KΩ	162 KΩ
8	649 KΩ	274 KΩ
9	383 KΩ	137 KΩ
10	442 KΩ	137 KΩ
12	412 KΩ	102 KΩ
14	499KΩ	102 KΩ
16	649 KΩ	113 KΩ

MCV

Battery over-voltage protection is accomplished by comparing V_{CELL} to the internal MCV reference. If V_{CELL} becomes greater than V_{MCV}, then charging, top-off, and trickle charge terminate, and $\overline{CH}_{A,B}$ and $\overline{FCC}_{A,B}$ outputs are high impedance.

A typical MCV value equates to 2.0V per cell. To detect the presence of a battery, the DC supply voltage must be greater than 2.0 * N, where N is the number of battery cells. Battery packs with fewer than three cells require an external amplifier to use the bq2005 (see Figure 3).

Temperature Sensing and the TCO Pin

The bq2005 uses the temperature sense input on the $TS_{A,B}$ pins to qualify charge initiation and termination. A negative temperature coefficient (RNTC) thermistor referenced to SNS and placed in close proximity to the battery may be used as a temperature-to-voltage transducer as shown in Figure 4. This example shows a simple linearization network constituted by RT1 and RT2 in conjunction with the thermistor, RT. If this temperature sensor is to be used for charge control, it should be in direct contact with the cells.

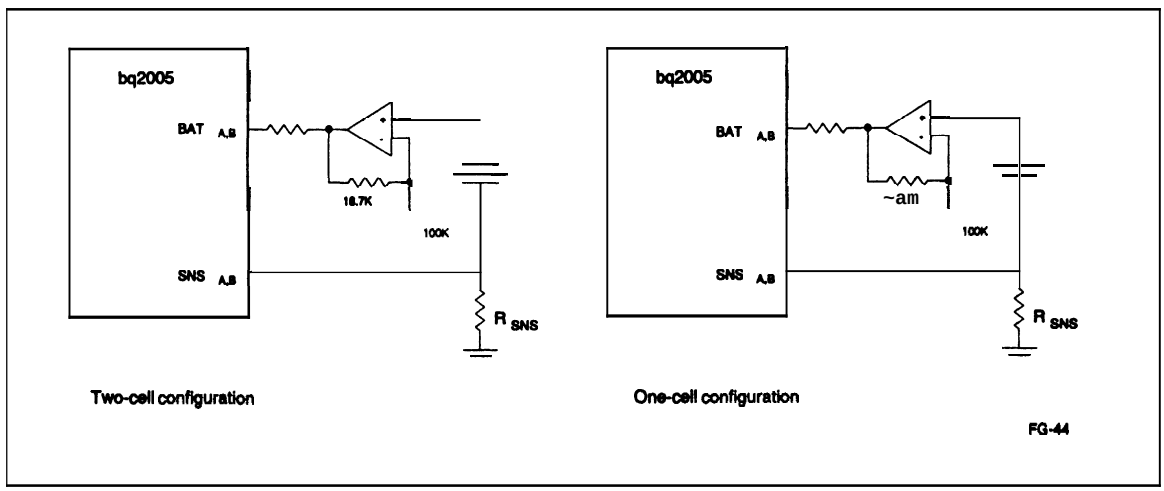


Figure 3. Battery Cell Voltage Amplifier for <3 Cells

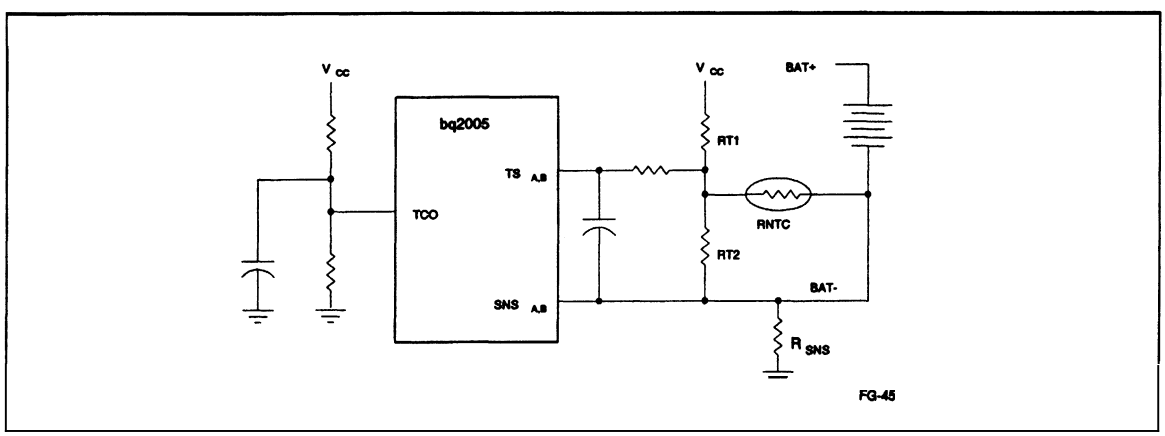


Figure 4. Temperature Sense Inputs

Temperature-decision thresholds are defined as LTF (low-temperature fault), HTF (hot-temperature fault), and TCO (temperature cutoff). Charge action initiation is inhibited if the temperature is not within the LTF-to-HTF range. In this case, $\overline{CH}_{A,B}$ is alternating high and low at a 4Hz rate, and charging does not initiate until the battery temperatures enter this range.

Once initiated, charging terminates if the temperature is either less than LTF or greater than TCO. The bq2005 interprets the reference points V_{LTF}, V_{HTF}, and V_{TCO} as V_{SS}-referenced voltages, with V_{LTF} fixed at 2/5 Vcc and V_{TCO} equal to the voltage presented on the TCO pin. See Figure 5. Note that since the voltage on pin $TS_{A,B}$ decreases as temperature increases, V_{TCO} should always be less than 2/5 Vcc. V_{HTF} is set internally 3/4 of the way from V_{LTF} to V_{TCO}. The resistive dividers shown in Figure 4 may be used to generate the desired V_{TCO}.

$\Delta T/\Delta t$ detection adds an additional constraint on the selection of temperature sense components. Detection occurs when the voltage $TS_{A,B} - SNS_{A,B}$ declines at a rate between 0.0024 Vcc and 0.0040 Vcc per 68 seconds, with a nominal 5V Vcc producing a nominal detection rate of 14mV/min (16mV/68sec). For example, assuming a 1°C/min desired average $\Delta T/\Delta t$ detection rate (TAT), and minimum and maximum charge temperatures of 0° and 40°C, respectively, V_{TCO} equals:

$$V_{TCO} = (2 \cdot V_{CC}/5) - (0.0028 \cdot V_{CC} \cdot (T_{TCO} - T_{LTF}))$$

$$= 2 - (0.014 \cdot (40 - 0))$$

$$= 1.44V$$

Table 4 shows the temperature control values that apply for the application example assuming the Philips thermistor. Appendix A explains the derivation of such component values.

New $\Delta T/\Delta t$ samples are processed every 34 seconds. To minimize the risk of premature termination, the design should be configured assuming a minimum charge cutoff rate of 0.0024 • Vcc, or 10.6mV per minute (at 25°C; Vcc = 5V). This is the lowest signal that may be recognized as meeting the decision threshold. Repeating samples cause a decision quickly as the voltage ramps between this minimum threshold and the nominal 14mV per minute. The system is self-compensating in that the thermistor provides increasingly overstated negative voltage change with increasing temperature, making the measurement more sensitive at higher temperatures. The last three columns of Table 4 are an example of this relationship.

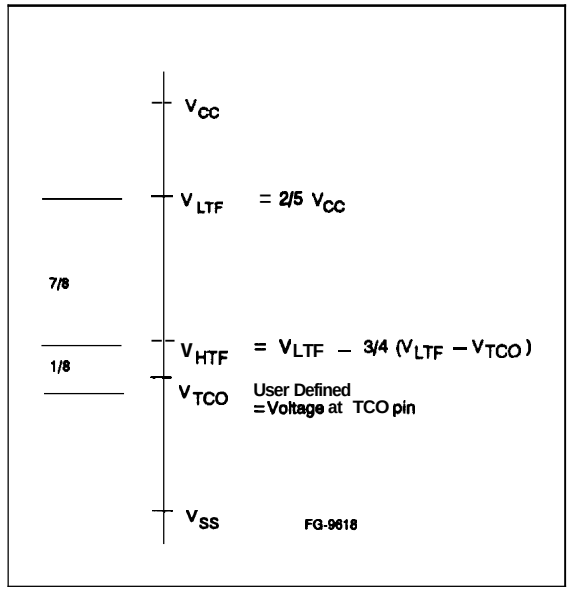


Figure 5. Temperature Reference Points

Table 4. Example Values, Temperature Sense Network

LTF (°C)	HTF (°C)	TCO (°C)	V_{TCO} (V)	RT1 (KΩ)	RT2 (KΩ)	$T_{\Delta T}$ (°C/min)	Minimum-to-Nominal ΔT/Δt Rate (°C/min)		
							[illegible]	[illegible]	[illegible]
10	44.4	50	1.303	5110	4120	1.00	0.75–1.00	0.63–0.83	0.56–0.74

Notes:
1. V_{SR} = 0V.
2. Temperature control and qualification may be disabled by tying pin TCO to V_{SS} and fixing the voltage on pin $TS_{A,B}$ to 0.2 • Vcc.

Vcc Supply

The V_{CC} supply provides both power and voltage reference to the bq2005. This reference directly affects the internal time-base voltage measurements.

The time-base is trimmed during manufacturing to within 5 percent of the typical value with V_{CC} = SV. The oscillator varies directly with V_{CC}. If, for example, a 5% regulator supplies V_{CC}, the time-base could be in error by as much as 10%.

For applications requiring even more cost-cutting measures, using a Zener diode-resistor combination as the bq2005 power supply sacrifices very little accuracy and performance. To minimize +5V loading, LEDs are camode-driven as shown in Figure 6.

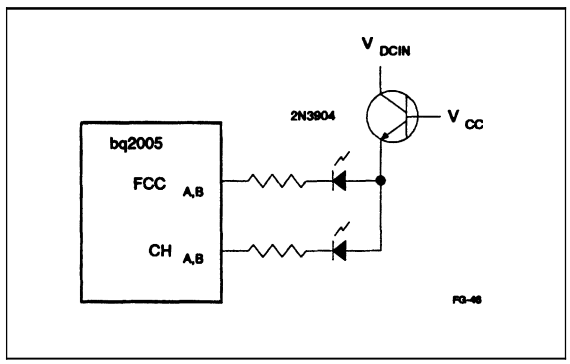


Figure 6. Cascode-Driven LEDs

The DC supply voltage, V_{DC}, must satisfy two requirements:

1. To support the bq2005 V_{CC} supply, V_{DC} must be adequate to provide for 5V regulation after the losses in the regulator and across D1 (V_{DC} 2 7.7V using the 78L05).
2. To support the proper charge operation and the rated current, V_{DC} must be greater than the number of cells • 2V + V_{LOSS} in the charging path.

Battery Removal Detection

An external 2K resistor in Figure 1 (lower left) is sized to pull $BAT_{A,B}$ above MCV with the removal of the battery. The resistance of R7 should be selected to pull the battery sense pin above MCV and yet keep input current on $BAT_{A,B}$ less than 20µA.

Top-Off Charge

The top-off charge option allows for filling up the last fraction of capacity after the fast-charge phase has terminated. Top-off is needed for NiMH batteries, which accept charge poorly at charge states above 85%. Top-off occurs at a 1/8 pulsed rate to prevent excess beat generation, and terminates after a period equal to the safety time-out. Top off terminates if TCO or MCV is exceeded or if charge or discharge is initiated on the other battery. Top-off has a lower priority than charge; it pends until both batteries have been charged and then charges the batteries in sequence—first battery B and then battery A.

Top-off is *not* recommended in applications where a battery charge is re-Sited with extremely high frequency (many times per day); for example, when the unit is returned to the charge cradle after each short period of use. Top-off is also *not* necessary for NiCd batteries.

Negative Delta Voltage Fast-Charge Detection

-AV full-charge detection may operate in parallel with ΔT/Δt detection. If temperature control is disabled by design, then -AV should be enabled (DVEN tied to V_{CC}). If -AV is enabled, a constant-current charging source is required. Otherwise a drop in current may cause a false -AV determination. DVEN may change state at any time.

Mode Selection Pins TM_1 and TM_2

These two pins are used to select the safety time-out (five selections, 23 to 360 minutes) and optional top-off charge (four selections, 23 to 180 minutes, equal to the safety time selection).

The safety time-out should be selected to be longer than any reasonably expected charge time. The nominal charge time (Ah capacity/charge rate) should be increased to allow for both charge inefficiency and the fact that many batteries hold more than the rated charge. A safety time-out 1.3–1.5 times the nominal time is normally adequate (i.e., 90 minutes for a 1C charge). The safety time-out may be far in excess of the nominal charge time if temperature termination is enabled.

Note: If the charge rate varies (such as fast charging during system operation using ΔT/Δt termination), then the safety time-out selection should allow for the slowest charges that may occur. The 180- or 360-minute selection may be appropriate.

In addition to selecting the safety timer period and top-off enabled/disabled, TM_1 and TM_2 select the appropriate pulse trickle period. C/32 is recommended for NiCd cells, while C/64 is recommended for NiMH batteries. Top-off and pulsed trickle can be disabled by tying TM_1 and TM_2 low, selecting a sir-hour charge time-out. TM_1 and TM_2 may be changed at any time during a charge cycle to select different conditions; however, changing them during charge may result in an indeterminate time-out period. TM_1 and TM_2 are held constant throughout the entire charge cycle.

System-Controlled Charge Inhibition

System control of battery charging is best accomplished by driving the temperature and voltage sense pins high, terminating or inhibiting charge. Driving $\overline{INH}$ voltage to V_{SS} results in a transition at the $BAT_{A/B}$ sense pin, terminating any fast charge, top-off, or trickle in process. When $\overline{INH}$ transitions to V_{CC}, charging is reinitiated if a battery is present and within temperature and voltage limits. *See* Figure 7.

Polarity Reversal Protection

If the DC input has any risk of being accidentally connected with power (+) and ground (–) reversed, then the system input should include either a protection diode to protect against circuit damage or a diode bridge to provide both protection and operation. This also increases minimum input voltage for charger operation by 1V to 2V. For maximum efficiency, a polyswitch may be used in combination *with* a suitably sized Schottky diode reversed across the electronics.

Layout Guidelines

PCB layout to minimize the impact of system noise on the bq2005 is important when the bq2005 is used as a switching modulator, with a separate nearby switching regulator, or close to any other si cant noise source.

1. Avoid mixing signal and power grounds by using a single-point ground technique incorporating both a small signal ground path and a power ground path.
2. The charging path components and associated traces should be kept isolated from the bq2005 and its supporting components.
3. 0.1µF and 10µF decoupling capacitors should be placed close together and very close to the Vcc pin.

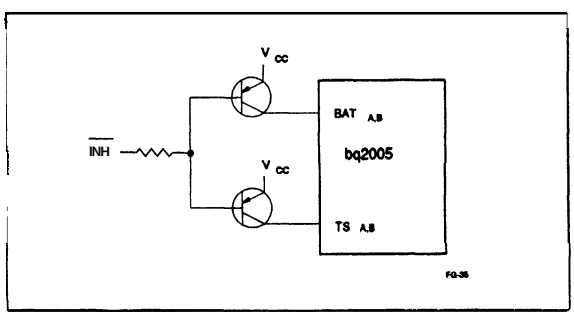


Figure 7. Inhibit Battery Charging Circuit

4. 0.1µF capacitors and resistors forming R-C filters connected to pine $BAT_{A,B}$, $TS_{A,B}$, and TCO should be as close as possible to their associated pins.
5. Because the bq2005 uses Vcc for its reference, additional loading on V_{CC} is not recommended.
6. Diode D1 (1N4148) is recommended for rectification and *filtering.*
7. If the $\overline{DCMD}_A$ input is electronically controlled, care should be taken to prevent noise-induced false transitions.
8. For bq2005-modulated switching applications:
   - A 1000pF capacitor/1KΩ resistor R-C filter should be as close as possible to the $SNS_{A,B}$ pins.
   - The 0.1µF capacitors for $BAT_{A,B}$ and $TS_{A,B}$ should be routed directly to $SNS_{A,B}$ and not to ground.

Application Example 1: Linear Regulator

In the frequency-modulated example of Figure 8, the bq2005 is used to implement a linear regulator/charge controller that can charge 4, 5, 6, 8, or 10 NiCd or NiMH cells (selected by JP4 and JP5) by controlling the base drive to a series pass PNP transistor. The current must be limited to stay within the power dissipation of the transistor in free air or connected to an appropriately sized heat sink. Table 5 contains the parts list for the board.

Charge is initiated on battery replacement or power-up. Jumper JP1 controls -AV detection: selecting Vcc enables -AV and GND disables it. Switch SW1 controls discharge of battery A. HTF = 48°C, TCO = 48°C, and LTF = 10°C for the component values listed in Table 6 for RTB1, RBT2, R5, and R6 with a Philips thermistor (Part No. 2322-640-63103) with $\Delta T/\Delta t$ termination set for 1°C/minute at 30°C.

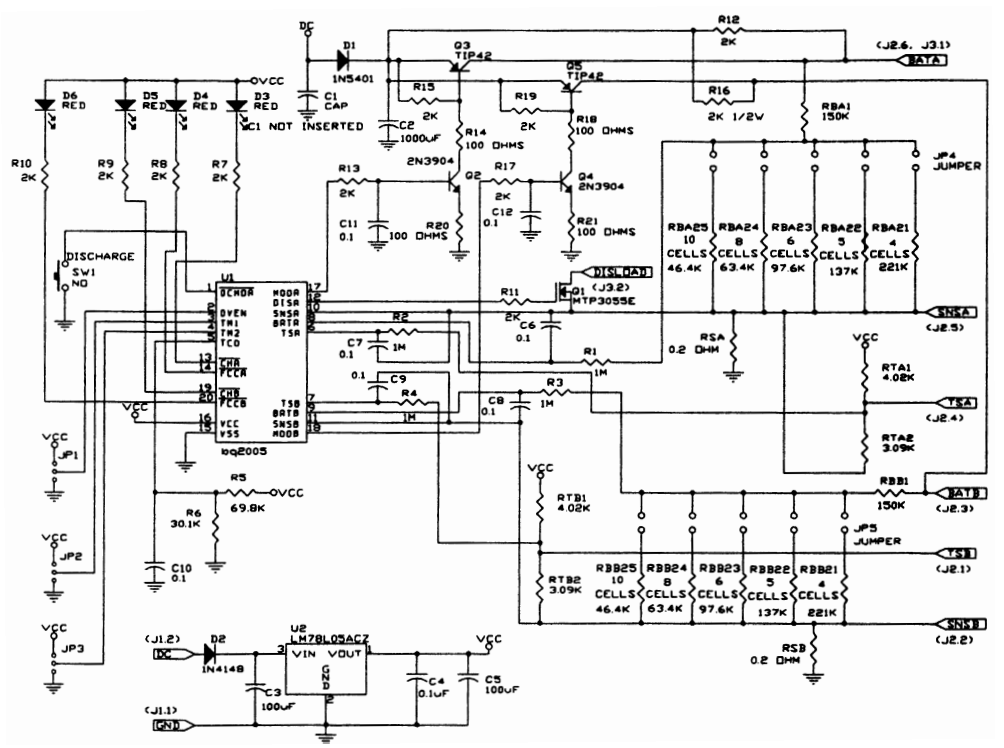
Safety time-out is selected by programming TM1 and TM2 with jumpers JP2 and JP3, respectively. To customize the design for a specific application, ensure that the power components are rated for the stresses they must handle. Charge current is a function of $RS_{A,B}$ and an internal bq2005 threshold:

$$I_{CHARGE} \approx \frac{0.225V}{RS_{A,B}}$$

The source power supply must provide sufficient voltage differential to the battery to account for losses in polarity protection diodes or resistive drops.

The selection of component values for R13, R17, C11, and C12 in this example affects the switching frequency of

MOD and the delay to full current sense at the sense pins of the bq2005. Although the effects on fast charge and top-off are minimal because the delay is small wmpared to the total time, the effect on pulse-trickle charge is significant. Transistors Q2 and Q4 may not turn on in some caees, which may be advantageous if no trickle charge is desired.



Thermistor values :

Thermistor	RT1	RT2
Keystone RL0703-5744-103-S1	3.83K	2.94K
Philips 2322-640-63103	4.02K	3.09K
Fenwal Type 16, 197-103LA6-A01	4.02K	3.09K
Ozhumi 150-108-00(4)	4.64K	3.74K
Semetic 103AT-2	4.87K	4.02K

BD-202

Figure 8. Linear Regulator/Charge Controller

Table 5. Linear Regulator/Charge Controller Board Parts List

Component Name	Quantity	Component Description
C1, C2	1	1000µF 25V aluminum (C1 is optional—not stuffed)
C3	1	100µF 25V aluminum
C5	1	100µF 6.3V aluminum
C4, C6, C7, C8, C9, C10, C11, C12	8	0.1µF ceramic
D1	1	1N5400
D2	1	1N4148
D3, D4, D5, D6	4	HMLP-D150 HP LED
J1, J3	2	2-position terminal block
J2	1	6-position terminal block
JP1, JP2, JP3	3	3-pin single-row header
JP4, JP5	2	12-pin dual-row header
JP6	1	2-pin single-row header
Q1	1	MTP3055EL FET
Q2, Q4	2	2N3904
Q3, Q5	2	TIP42
R1, R2, R3, R4	4	1MΩ 5% ¼W
R5	1	69.8KΩ 1% ¼W
R6	1	30.1KΩ 1% ¼W
R7, R8, R9, R10, R11, R12, R13, R15, R16, R17, R19	11	2KΩ 5% ¼W
R14, R18, R20, R21	2	100Ω 5% ¼W
RBA1, RBB1	2	150KΩ 1% ¼W
RBA21, RBB21	2	221KΩ 1% ¼W
RBA22, RBB22	2	137KΩ 1% ¼W
RBA23, RBB23	2	97.6KΩ 1% ¼W
RBA24, RBB24	2	63.4KΩ 1% ¼W
RBA25, RBB25	2	46.4KΩ 1% ¼W
RSA, RSB	2	0.2Ω 1% 3W wirewound Dale LVR3
RTA1, RTB1	2	4.53KΩ 1% ¼W
RTA2, RTB2	2	3.57KΩ 1% ¼W
S1	1	SPST momentary switch, Panasonic P8008S
U1	1	bq2005
U2	1	LM78L05ACZ
Heatsink	1	Thermalloy 6298B
Mounting kit	2	TO-220
Socket	1	20-pin solder tail ICO-203-58-T
PCB	1	DV2005L1
Screws	4	6-32 thread x ¼inch
Legs	4	Stand-off ½inch 6-32 thread

Application Example 2: Single-Magnetics Low-Cost Dual-Switching Charger

Figure 9 illustrates a low-coat dual-sequential switching charger using a small, low Q inductor to speed up the bipolar transistor commutation. Table 6 contains the parts list for the board. Bipolar transistors Q2 and Q5 are used to multiplex the energy stored in L1 by the charger's charge cycles.

Transistor Q3 is used to switch energy into L1 from the power source. Low-Q inductor L2 helps to turn Q3 off to limit its power dissipation. Thii circuit has the advantage of using bipolar transistors with saturation voltages far below the IR drops of comparably sized p-channel MOSFETs. This also results in significant cost savings. Designers must use care in selecting Q3 for suitability as a switching transistor. The Zetex Super-E line is ideal for applications up to 3A.

Layout guidelines are described on page 8. Possible layout concerns include:

- Diode D2 is installed to catch inductor energy in the event of battery removal during charge.
- Battery voltage differentials are applied to the base-emitter junctions of transistors Q5 and Q2 in the reverse direction. (Although the bq2005 will not charge a shorted battery, the design should ensure that Q5 and Q2 are protected if the battery could be shorted during charge.)

Q3 must be a high-speed switching transistor with suitably high V_{CE} rating for the application. The ZTX789A has a breakdown rating of 25V and a continuous current rating of 3A. This transistor's high gain enables it to saturate to a very low V_{CE} (< 0.25V) at 2A. The 'on-time' power dissipation makes up moat of the component power loss, but the switching loss must be added to give a complete picture of the transistor's required power dissipation.

A good switching transistor is gauged by its transition frequency (F_T) rating. A transistor with an F_T rating of >50MHz is a superior switching transistor for a switch-mode application, whereas a transistor with an F_T of 10MHz may be usable. In this example, the ZTX789A has an F_T of 100MHz. Manufacturers sometimes cite turnoff time as a sum of storage and fall time; some cite these values independently. The turnoff time is important for frequency selection, but the fall time is critical to determine power dissipation.

The influence of fall time on power dissipation can be estimated using the following formula:

$$P_{SW} = F \times T_F \times V_{IN} \times \frac{I_P}{6}$$

where:

P_{SW} = Power loss when switching

F = Switching frequency

T_F = Fall time

V_{IN} = Maximum input voltage

I_P = Peak switching current

Component power diesipation is the sum of P_{SW} and P_{ON}, which is estimated from the following formula:

$$P_{ON} = \frac{V_{BAT}}{V_{IN}} \times V_{CESAT} \times I_{AV}$$

where:

P_{ON} = Power diesipation when the transistor is on

V_{BAT} = Battery voltage

V_{IN} = Input voltage

V_{CESAT} = Maximum transistor saturation voltage

I_{AV} = Average battery charge current

The Zetex E-line package can dissipate the heat resulting from this design in free air.

Other switching transistors that may be useful in applications up to 3A are the MJE210 and the D45H series transistors. Q2 and Q5 are selected for high HFE and low V_{CESAT}.

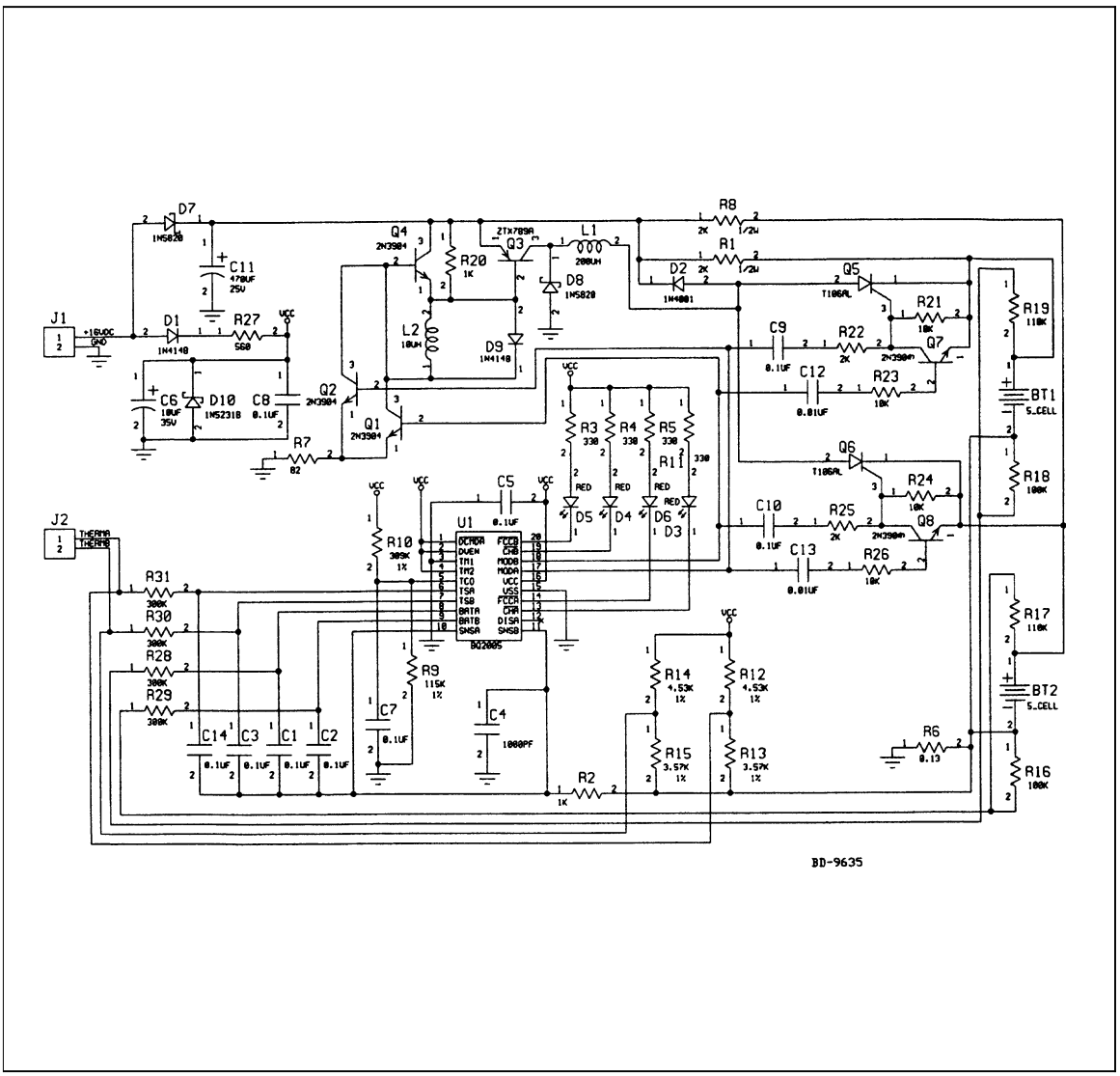


Figure 9. Single-Magnetics Low-Cost Dual-Switching Charger

Table 6. Single-Magnetics Low-Cost Dual-Switching Parts List

Component Name	Quantity	Component Description
C1, C6	2	1000pF 50V ceramic
C2, C3, C4, C5, C7, C10, C11, C12, C13	9	0.1µF 50V ceramic
C14, C15	2	0.01µF 50V ceramic
C8	1	10µF 35V aluminum
C9	1	470µF 35V aluminum
D1, D9	2	1N4148
D2	1	1N4001
D3, D4, D5, D6	4	HMLP-D150 red HP LED
D7, D8	2	1N5820 Schottky
D10	1	1N5231B Zener
L1	1	200µH toroid inductor
L2	1	10µH J.W.Miller 78F100J
Q1, Q2, Q4, Q7, Q8	5	2N3904
Q3	1	ZTX789A, Zetex high gain, med. power
Q5, Q6	2	T106A1, Teccor 4A SCR
R1, R10, R28, R31	4	2KΩ 5% ¼W carbon film
R2, R3, R26	3	1KΩ 5% ¼W carbon film
R4, R5, R6, R13	4	3308 5% ¼W carbon film
R7, R8	2	0.1352 5% 1W metal oxide
R9	1	8.28 5% ¼W carbon film
R11	1	115KΩ 1% ¼W metal film
R12	1	309Ω 1% ¼W metal film
R14, R16	2	4.53KΩ 1% ¼W metal film
R15, R17	2	3.57KΩ 1% ¼W metal film
R18, R20	2	100KΩ 5% ¼W carbon film
R19, R21	2	110KΩ 5% ¼W carbon film
R22, R23, R24, R25	4	1MKΩ 5% ¼W carbon film
R27, R29, R30, R32	4	10KΩ 5% ¼W carbon film
R33	1	560Ω 5% ¼W carbon film
U1	1	bq2005

Application Example 3: P-Channel MOSFET Buck-Topology Switch-Mode Charger

In this example, the bq2005 is used to implement a switching regulator/charge controller that can charge 4 to 10 NiCd or NiMH cells with current regulated up to 3A.

Figure 10 is a standard configuration for a p-FET switch-mode charger. MOD drives a small signal DMOS FET, Q2/Q5. When MOD is high, Q2/Q5 is on, turning on Q4/Q7 via the path through D8/D12 and D11/D7.

L1/L2 inductor current ramps up linearly while MOD is high. L1/L2 current is in series with the battery and RSA or RSB. The inductor current ramps up linearly until V_{SNS} reaches 0.250V, at which time MOD goes low and Q4/Q7 turns off. A flux reversal occurs in L1/L2, causing D9/D13 to conduct. Charge is now being transferred from L1/L2 into the battery. The L1/L2 current ramps down linearly until V_{SNS} reaches 0.20V. At this point the cycle repeats with MOD going high.

For input voltages that are higher than the rated Q4/Q7 safe operating gate voltage, Zener diode D7/D11 can be placed in series with the drain lead of Q2/Q5. The Zener voltage should be sized to allow full Q4/Q7 enhancement while Q2/Q5 is conducting. See Table 7.

Capacitor C2 is used to provide a low-impedance for the 62/65 source lead. Without C2 in place, Q2/Q5 can be connected to an overly inductive voltage supply. D1 is a blocking diode that keeps the battery from discharging via U2 during removal of the DC power source input.

Charge is initiated on battery replaced or Vcc valid. -AV detection can be enabled (DVEN high), and discharge control is through $\overline{DCMD}$ (SW1 low). MCV = 1.8V; LTF = 10°C; TCO = 50°C; $\Delta T/\Delta t$ at 30°C = 0.82°C/min. (i.e., typical = 1.10°C/min.). Timer-mode selection (see data sheet) and resistor R15/R17 are determined by the designer. RSA/RSB is selected such that $I_{CHG} \cdot RSA/RSB = 0.225V$.

The values of RB1 and RB2 to complete this schematic may be selected from Table 3.

Note: Temperature control and qualification may be disabled by tying the TCO pin to Vss and fixing the voltage on the $TS_{A,B}$ pins to 0.1 * Vcc.

Table 8 lists suggested components for different-rate chargers. Table 9 lists other components shown in Figure 10.

Table 7. Lookup Table for D7/D11 Selection

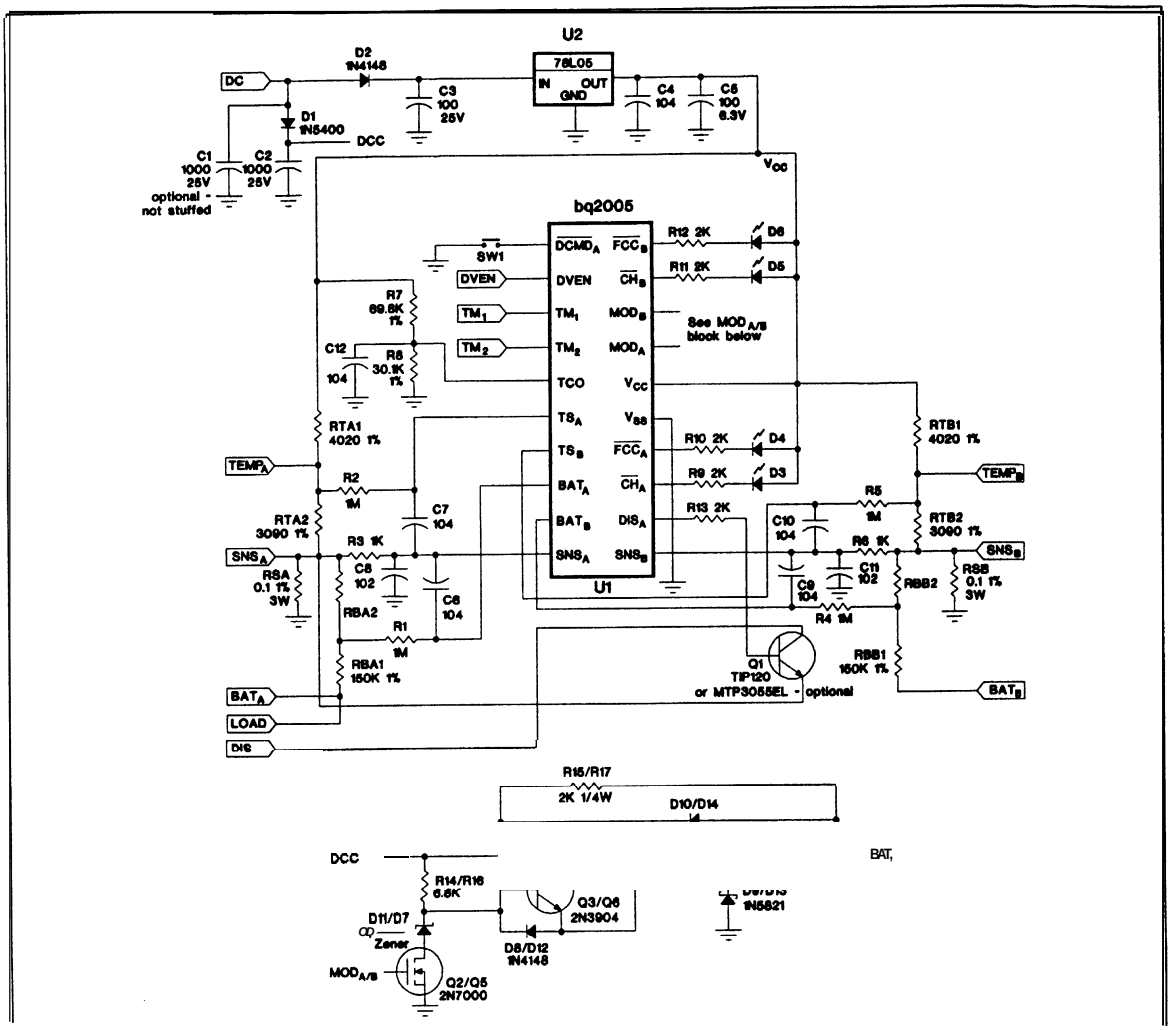
+VDC Input (Volts)	Motorola Part No.	Nominal Zener Voltage
Below 15	Shorted	0
15–18	1N749	4.3
18–21	1N755	7.5
21–24	1N758	10
24–27	1N964A	13
27–30	1N966A	16
30–32	1N967A	18
32–35	1N968A	20

Table 8. Suggested Components—P-Channel MOSFET Charger

Suggested Max. Charging Current	Q4/Q7	D9/ D13	D10/ D14	L1/L2
1A	IRF9Z14	1N4001	1N5818	30 turns, #26 AWG, wound on Magnetics, Inc., P/N 77040 core; nominal inductance 59µH; GFS Mfg., Inc., P/N 92-2156-1
2A	IRF9Z24	1N5821	1N5821	37 turns, #22 AWG, wound on Magnetics, Inc., P/N 77120 core; nominal inductance 98µH; GFS Mfg., Inc., P/N 92-2157-1
3A	IRF9Z34	1N5821	1N5821	
Source	International Rectifier	Motorola	Motorola	GFS Mfg., Inc. Dover, NH (603) 742-4375

Table 9. Other Components—P-Channel MOSFET Charger

Component Name	Component Description
C1, C2	1000µF 5V electrolytic
C3	100µF 25V electrolytic
C4, C6, C7, C9, C10, C12	0.1µF ceramic
C5	100µF 6.3V electrolytic
C8, C11	1000pF ceramic
D1	1N5400
D2, D8, D12	1N4148
D3, D4, D5, D6	HLMP 4700 red LED
D7/D11	Optional Zener; see Table 9
D9/D13	1N5821
D10/D14	1N4001
Q1	TIP120 or MTP3055EL
Q2, Q5	2N7000
Q3, Q6	2N3904
Q4/Q7	MTP23P06
R1, R2, R4, R5	1MΩ 5% ¼W or ⅛W
R3, R6	1KΩ 5% ¼W
R7, R8	User-defined 1% ¼W or ⅛W
R9, R10, R11, R12, R13	2KΩ 5% ¼W or ⅛W
R14/R16	6.8KΩ 5% ¼W or ⅛W
RSA, RSB	0.113 1% 3W
RBA1, RBB1	150KΩ 1% ¼W or ⅛W
RBA2, RBB2	User-defined 1% ¼W or ⅛W
RTA1, RTB1	User-defined 1% ¼W or ⅛W
RTA2, RTB2, R15, R17	User-defined 1% ¼W or ⅛W
L1/L2	See Table 10
U1	bq2005
U2	LM78L05ACZ



Thermistor values:

Thermistor	~~RT1~~	~~RT2~~
Keystone RL0703-5744-103-S1	3.83K	2.94K
Philips 2322-640-63103	4.02K	3.0%
Fenwal Type 18, 197-103LA6-A01	4.02K	3.09K
Ozhumi 150-108-00(4)	4.64K	3.74K
Semetic 103AT-2	4.87K	4.02K

BD-184

Notes: All 104 capacitors are 0.1µF ceramic.
All 102 capacitors are 0.001µF ceramic.

Figure 10. P-Channel MOSFET Switching-Mode Charger

Appendix A
Determining Temperature-Control Component Values

The bq2005 uses a negative temperature coefficient (NTC) thermistor to determine temperature. The ΔT/Δt sensitivity can be adjusted using different resistor values (RT1 and RT2 in Figure 1 and the application example) and a different high-tempera —— cutoff voltage. Table A-1 lists various thermistor manufacturers, with the appropriate part numbers.

Follow these steps to determine temperature-control component values (see Figure 6):

1a. The low-temperature fault (LTF) limit for charging must be established. LTF for charging is determined by the battery specification and the charge rate used. A typical value for the low-temperature limit is 10°C.

b. V_{LTF} is set within the bq2005 at 0.4 • Vcc.

2a. The high-temperature cutoff (TCO) for charging must be established. TCO for charging is determined by the battery specification, the charge rate, and the heat dissipation of the system. Typical values range from 40°C to 50°C, although values outside this range may be applicable.

b. The average ΔT/Δt sensitivity from LTF to TCO ($T_{\Delta T}$, expressed as °C/minute) for termination must be established. As mentioned in this application note, the bq2005 provides a typical ΔT/Δt charge termination of 14 mV per minute. The TAT value is determined by the battery specification, the charge rate, and the heat dissipation of the system. Typical nominal values for TAT range from 0.75°C/min to 1.5°C/min.

Relative to the average value TAT, the minimum-to-maximum range of ΔT/Δt at a specific temperature depends on two parameters:

- The measurement resolution of the bq2005, which contributes a ± 26% error.
- The non-linearity of the thermistor between LTF and TCO. As the temperature nears LTF, the expected ΔT/Δt is less than TAT (less sensitive), and as the temperature nears TCO, the expected ΔT/Δt is more than $T_{\Delta T}$ (more sensitive).

The ΔT/Δt *range* should be considered in determining the nominal TAT. Nominal TAT should be selected so that its minimum value represents an acceptable (non-premature) termination threshold. Thus a first bq2005 sample does not cause a premature termination. Multiple sampling ensures that the termination occurs well before the TAT max.

c. The high-temperature cutoff voltage, V_{TCO}, must be established. This V_{TCO} limit is determined by the TAT and may be calculated by:

$$V_{TCO} = (2 \bullet Vcc/5) \cdot [(0.0028 \bullet Vcc \bullet (TCO - LTF)) / T_{\Delta T}]$$

V_{TCO} is provided at the TCO pin by a resistor-divider network as shown in Figures 8 and 9: $V_{TCO} = Vcc \bullet R1/(R1 + R2)$.

4. Select the thermistor to be used. If it is not from Table A-1, the thermistor sensitivity at 25°C ehould be at least -4% and the AR steps between 30°C and 50°C should be comparable to or greater than those in Table A-1 to obtain the appropriate accuracy. Lower values affect the linearity of the ΔT/Δt.

5. Determine the thermistor resistance at LTF and TCO (R_{LTF} and R_{TCO}, respectively). This may be done using the thermistor temperature versus resistance conversion table provided with the thermistor specification. These tables are usually in 5°C increments.

6. The values for RT1 and RT2 may be calculated by:

$$T1 = R_{LTF} \bullet (1 - (2/Vcc)) / (2/Vcc)$$

$$T2 = R_{TCO} \bullet (1 - (V_{TCO}/(Vcc - V_{SNS}))) / (V_{TCO}/(Vcc - V_{SNS}))$$

$$RT2 = ((T2 \bullet R_{LTF}) - (T1 \bullet R_{TCO})) / (T1 - T2)$$

$$RT1 = (RT2 \bullet T1) / (R_{LTF} + RT2)$$

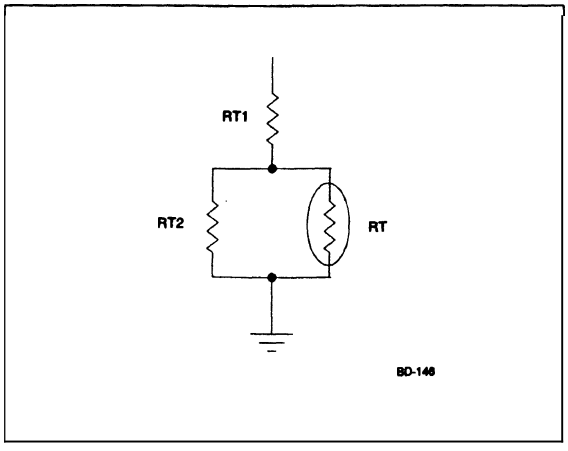


Figure A-1. Resistor Network

Table A-1. 10K NTC Thermistor Types and Resistance Values

Temperature (°C)	Nominal Resistance (Ω) at Temperature			
	Keystone Carbon Co. RL0703-5744-103-S1 (Tel: 814/781-1591)	Philips Components 232264083103 (Tel: 407/743-2112)	Fenwal Electronics Type 18; 197-103LA6-A01 (Tel: 508/478-6000)	Thermometrics C100Y103J (Tel: 908/287-2870)
-30	188172	173900	177000	-
-25	138043	128500	-	-
-20	102263	95890	97070	-
-15	76461	72230	-	-
-10	57672	54890	55330	-
-5	43864	42070	-	-
0	33630	32510	32650	29588
5	25988	25310	-	23515
10	20243	19860	19900	18813
15	15889	15690	-	15148
20	12562	12490	12490	12271
25	10000	10000	10000	10000
30	8013	8060	8057	8195
35	6461	6536	-	6752
40	5241	5331	5327	5593
45	4276	4373	-	4656
50	3507	3606	3603	3894
55	2894	2989	-	3273
60	2400	2490	2488	2762
65	2001	2085	-	2342
70	1677	1753	1752	1993.7
75	1412	1481	-	1704.0
80	1194	1256	1258	1462.0
85	1014	1070	-	1259.1
90	865.2	915.5	917.7	1088.3
95	741.0	786.1	-	943.9
100	636.9	677.5	680.0	821.4

bq2007

Fast Charge IC

1

Features

- Fast charging and conditioning of NiCd and NiMH batteries
  - Precise charging independent of battery pack number of cells
  - Discharge-before-charge on demand
  - Pulse trickle charge conditioning
  - Battery undervoltage and overvoltage protection
- Built-in 10-step voltage-based charge status monitoring
  - Charge status display options include seven-segment monotonic bargraph and fully decoded BCD digit
  - Display interface options for direct drive of LCD or LED segments
  - Charger state status indicators for pending, discharge, charge, completion, and fault
  - Audible alarm for charge completion and fault conditions
- Charge control flexibility
  - Fast or Standard speed charging
  - Top-off mode for NiMH
  - Charge rates from C/8 to 2C (30 minutes to 8 hours)
- Charge termination by:
  - Negative delta voltage (-ΔV)
  - Peak voltage detect (PVD)
  - Maximum voltage
  - Maximum time
  - Maximum temperature
- High-efficiency switch-mode design
  - Ideal for small heat-sensitive enclosures
- 24-pin, 300-mil SOIC or DIP

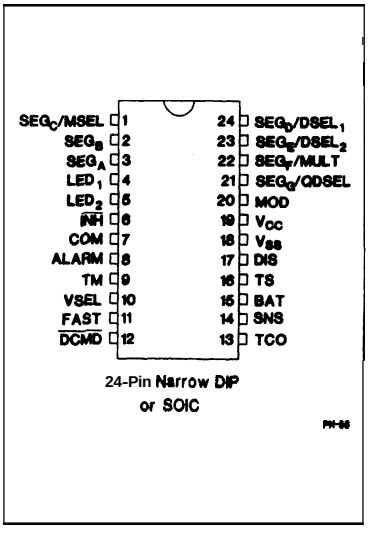
General Description

The bq2007 is a highly integrated monolithic CMOS IC designed to provide intelligent battery charging and charge status monitoring for stand-alone charge systems.

The bq2007 provides a wide variety of charge status display formats. The bq2007 internal *charge* statue monitor supports up to a seven-segment bargraph or a single BCD digit display. The bargraph display indicates up to seven monotonic steps, whereas the BCD digit counts in ten steps of 10% increments. The bq2007 output drivers can direct-drive either an LCD or LED display.

Charge action begins either by application of the charging supply or by replacement of the battery pack. For safety, charging is inhibited until battery temperature and voltage are within configured limits.

Pin Connections



24-Pin Narrow DIP or SOIC

PM-66

Pin Names

SEGC/MSEL	Display output segment C/ driver mode select
SEGB	Display output segment B
SEGA	Display output segment A
LED1	Charge status output 1
LED2	Charge status output 2
INH	Charge inhibit input
COM	Common LED/LCD output
ALARM	Audio alarm output
TM	Timer mode select
VSEL	Voltage termination select
FAST	Fast charge rate select
DCMD	Discharge command
TCO	Temperature cutoff
SNS	Sense resistor input
BAT	Battery voltage
TS	Temperature sense
DIS	Discharge control
VSS	System ground
VCC	5.0V ±10% power
MOD	Modulation control
SEGG/QDSEL	Display output segment G/ charge status display select
SEGF/MULT	Display output segment F/ multi-cell pack select
SEGE/DSEL2	Display output segment E/ display select 2
SEGD/DSEL1	Display output segment D/ display select 1

The acceptable battery temperature range is set by an internal low-temperature threshold and an external high-temperature cutoff threshold. The absolute temperature is monitored as a voltage on the TS pin with the external thermistor network shown in Figure 2.

The bq2007 provides for undervoltage battery protection from high-current charging if the battery voltage is less than the normal end-of-discharge value. In the case of a deeply discharged battery, the bq2007 enters the charge-pending state and attempts trickle-current conditioning of the battery until the voltage increases. Should the battery voltage fail to increase above the discharge value during the undervoltage time-out period, a fault condition is indicated.

Discharge-before-charge may be selected to automatically discharge the battery pack on battery insertion or with a push-button switch. Discharge-before-charge on demand provides conditioning services that are useful to correct or prevent the NiCd voltage depression, or "memory" effect, and also provide a zero capacity reference for accurate capacity monitoring.

After prequalification and any required discharge-before-charge operations, charge action begins until one of the full-charge termination conditions is detected. The bq2007 terminates charging by any of the following methods:

- Negative delta voltage (-ΔV)
- Peak voltage detect (PVD)
- Maximum absolute temperature
- Maximum battery voltage
- Maximum charge time-out

The bq2007 may be programmed for negative delta voltage (-ΔV) or peak voltage detect (PVD) charge termination algorithms. The VSEL input pin selects -ΔV or PVD termination to match the charge rate and battery characteristics.

To provide maximum safety for battery and system, charging terminates based on maximum temperature cutoff (TCO), maximum cutoff voltage (MCV), and maximum time-out (MTO). The TCO threshold is the maximum battery temperature limit for charging. TCO terminates charge action when the temperature sense input voltage on the TS pin drops below the TCO pin voltage threshold. MCV provides battery overvoltage protection by detecting when the battery cell voltage (V_{CELL} = V_{BAT} - V_{SNS}) exceeds the V_{MCV} value and terminates fast charge, standard charge, or top-off charge. The maximum-time-out (MTO) termination occurs when the charger safety timer has completed during the active charge state.

The bq2007 indicates charge state status with an audio alarm output option and two dedicated output pins with programmable display options. The $DSEL_{1-2}$ inputs can select one of the three display modes for the LED_{1-2} outputs.

Charger status is indicated for:

- Charge pending
- Charge in progress
- Charge complete
- Fault condition

Pin Descriptions

SEG_{A-G} Display output segments A-G

State-of-charge monitoring outputs. QDSEL input selects the bargraph or BCD digit display mode. See Table 3.

MSEL Display driver mode select

Soft-programmed input selects LED or LCD driver configuration at initialization. When MSEL is pulled up to V_{CC}, outputs SEG_{A-G} are LED interface levels; when MSEL is pulled down to V_{SS}, outputs SEG_{A-G} are LCD levels.

$DSEL_1$, $DSEL_2$ Display mode select 1–2

Soft-programmed inputs control the LED_{1-2} charger status display modes at initialization. See Table 2.

MULT Fixed-cell pack select

Soft-programmed input is pulled up to V_{CC} when charging multi-cell packs and is pulled down to V_{SS} for charging packs with a fixed number of cells.

QDSEL State-of-charge display select

The QDSEL input controls the SEG_{A-G} state-of-charge display modes. See Table 3.

LED_{1-2} Charger status outputs 1-2

Charger status output drivers for direct drive of LED displays. Display modes are selected by the DSEL input. See Table 2.

INH Charge inhibit input

When low, the bq2007 suspends all charge actions, drives all outputs to high impedance, and assumes a low-power operational state. When transitioning from low to high, a charge cycle is initiated. See page 10 for details.

COM **Common LCD/LED output**

Common output for **LCD/LED display** SEG_{A-G}. Output is **high-impedance** during initialization to allow reading of **soft-programmed inputs** $DSEL_1$, $DSEL_2$, MSEL, **MULT, and** QDSEL

ALARM **Audio output**

Audio alarm output.

TM **Timer mode select**

TM is a three-level input that controls the settings for charge control functions, *See* **Table** 5.

VSEL **Voltage termination select**

Thie input ewitchee the voltage detect **sensitivity.** *See* Table 5.

FAST **Fast charge rate select**

The FAST input switches between **Fast** and **Standard** *charge* **rates.** *See* Table 4.

$\overline{DCMD}$ **Discharge** command

The $\overline{DCMD}$ input controls the discharge-before-charge function. **A** negative-going **pulse initiates a** discharge action. If $\overline{DCMD}$ is connected to **Vss,** automatic diecharge-before-chargeis enabled. **See** Figure 3.

TCO **Temperature cut-off threshold input**

Minimum allowable battery temperature-sensor voltage. If the potential **between** TS and SNS is **less** than the voltage at the **TCO input, then any fast charging or top-off charging** is terminated.

SNS Sense resistor input

SNS controls the switching of MOD output based **on an external sense resistor. This provides the lower reference potential for the BAT pin and the TS pin.**

BAT **Battery voltage input**

Battery voltage sense input referenced to SNS for **the** battery pack **being charged. This resistor** divider **network** is connected **between** the positive and the negative terminals of the battery. *See* **Figure 1.**

TS **Temperature sense input**

Input **referenced** to SNS **for battery** temperature **monitoring** negative temperature **coefficient** (NTC) **thermistor.**

DIS **Discharge control**

DIS is a push-pull **output** that **controls** an external **transistor** to **discharge** the **battery before charging.**

Vss Ground

Vcc **Vcc supply input**

MOD **Current-switching control output**

Push/pull *output* that controls the **charging** *current* to the battery. MOD **switches** high to **enable current flow and low to inhibit current flow.**

Functional Description

Figure 1 illustrates *charge* control **and** display status during a bq2007 *charge* **cycle.** Table 1 summarizes the **bq2007** operational **features.** The charge action **states** and control outpute are given for **possible** input **conditions.**

Charge Action Control

The bq2007 charge action is controlled by input pine **$\overline{DCMD}$,** VSEL, FAST, and TM. When charge action is initiated, the **bq2007 enters** the **charge-pending** state. **checks** for acceptable battery voltage and temperature, and **performs** any required discharge-before-charge **operations. $\overline{DCMD}$ controls** the diecharge-before-charge function, **and** VSEL, FAST, and TM select the charger **configuration.** *See* **Tables** 4 and 5.

During charging, the **bq2007** continuously **tests** for charge termination wnditione: negative delta voltage, peak **voltage** detection, maximum time-out, **battery** over-voltage, and high-temperature **cutoff.** When the charge state is terminated, a trickle charge continues to compensate for **self-discharge** and maintain the **fully** charged **condition.**

Charge Status Indication

Table 2 summarizes the **bq2007** charge status display indications. The charge statue **indicators** include the DIS output, which can be used to indicate the discharge **state,** the audio **ALARM** output, which **indicates** charge wmpletion and fault conditions, and the dedicated statue outputa, LED_1 and LED_2.

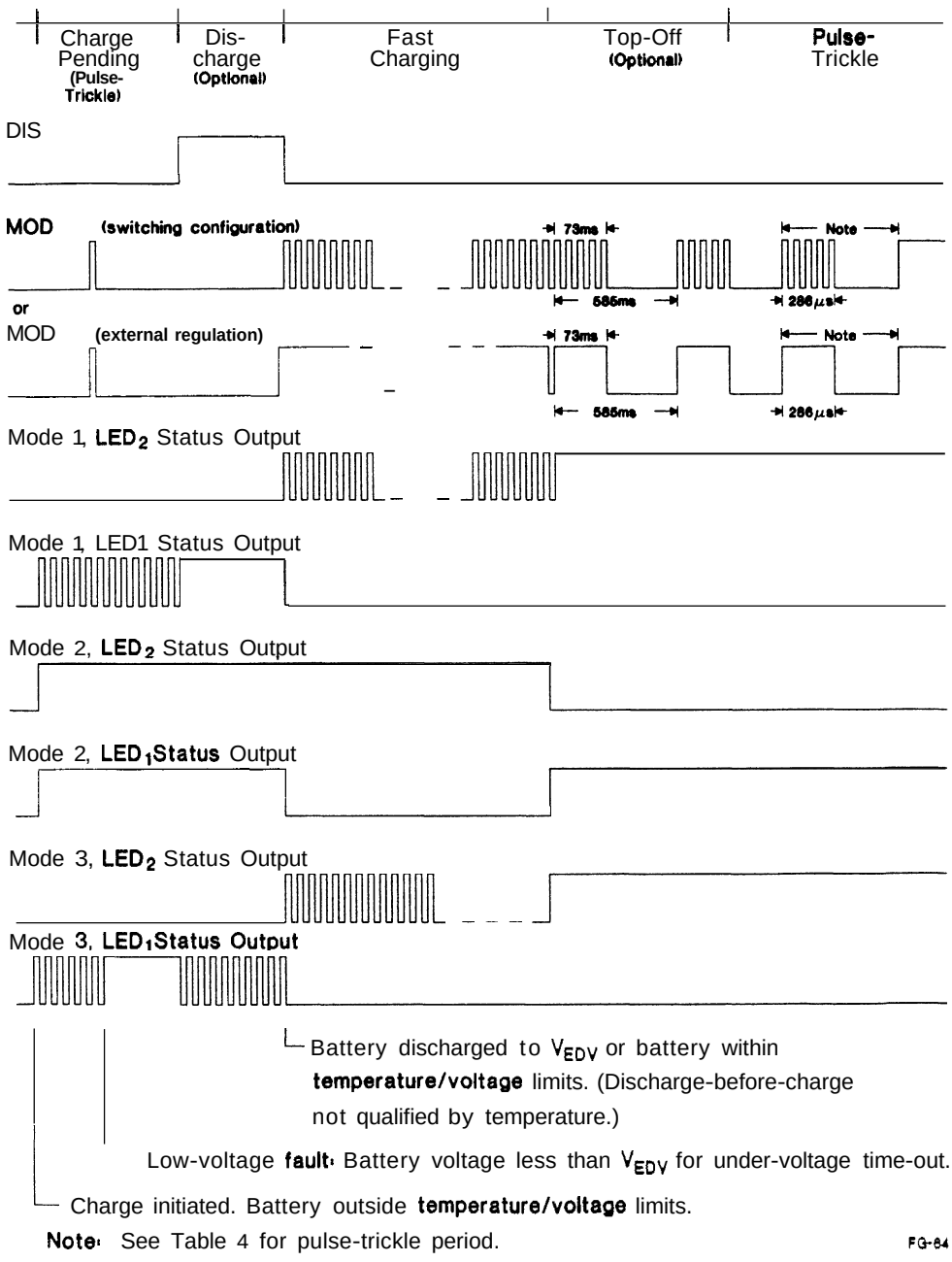


Figure 1. Example Charging Action Events

Outputs LED_{1-2} have three display modes that are selected at initialization by the input pins $DSEL_1$ and $DSEL_2$. The $DSEL_1$ and $DSEL_2$ input pins, when pulled down to Vss, are intended for implementation of a simple two-LED system. LED_2 indicates the precharge statue (i.e., *charge* pending and discharge) and LED_1 indicates the charge status (i.e., charging and completion). $DSEL_1$ pulled up to Vcc and $DSEL_2$ pulled down to Vss mode is for implementation of a single tri-color LED such that discharge, charging, and completion each have a unique color. $DSEL_1$ pulled down to Vss and $DSEL_2$ pulled up to Vcc allows for fault status information to be displayed.

Audio Output Alarm

The bq2007 audio alarm output generates an audii tone to indicate a charge completion or fault condi on. The audio alarm output is a symmetrical duty-cycle AC signal that is compatible with standard piezoelectric alarm elements. A valid battery insertion is indicated by a single high-tone beep of ½-second typical duration. The charge completion and fault conditions are indicated by a 9.5- to 15-second high-tone sequence of ½-second typical duration at a 2-second typical repetition rate.

Charge Status Monitoring

The bq2007 charge status monitor may display the battery voltage or charge safety timer as a percentage of the full-charged condition. These options are selected with the MULT soft-programmed input pin.

When MULT is pulled down to Vss, the battery charge statue is displayed as a percentage of the battery voltage, and the single-cell battery voltage at the BAT pin is compared with internal charge voltage reference thresholds. When V_{BAT} is greater than the internal thresholds of V_{20}, V_{40}, V_{60}, or V_{80}, the respective 20%, 40%, 60%, or 80% display outputs are activated. The battery voltage directly indicates 20% charge increments, while the 10% charge increments use a timer that is a function of the charge safety timer.

When MULT is pulled down to Vss and when V_{BAT} exceeds V_{20} during charging, the 20% charge indication is activated and the timer begins counting for a period equal to 1/64 to 1/32 of the charge safety time-out period. When the timer count is completed, the 30% charge indication is activated. Should V_{BAT} exceed V_{40} prior to the timer count completion, the charge status monitor

Table 1. bq2007 Operational Summary

Charge Action State	Conditions	MOD Output	DIS Output
Battery absent	Vcc applied and $V_{CELL} \geq V_{MCV}$	Trickle charge per Table 4	Low
Charge initiation	Vcc applied or V_{CELL} drop from $\geq V_{MCV}$ to $< V_{MCV}$		Low
Discharge-before-charge	$\overline{DCMD}$ high-to-low transition or to Vss on charge initiation and $V_{EDV} < V_{CELL} < V_{MCV}$	Low	High
Charge pending	Charge initiation occurred and $V_{TEMP} \geq V_{LTF}$ or $V_{TEMP} \leq V_{TCO}$ or $V_{CELL} < V_{EDV}$	Trickle charge per Table 4	Low
Fast charging	Charge pending complete and FAST = Vcc	Low if $V_{SNS} > 250mV$; high if $V_{SNS} < 200mV$	Low
Standard charging	Charge pending complete and FAST = Vss	Low if $V_{SNS} > 250mV$;	Low
Charge complete	-ΔV termination or ~TEM $\leq V_{TCO}$ or PVD $\geq$ 0 to -3mV/cell or maximum time-out or V c w $> V_{MCV}$		
Top-off pending	VSEL = Vcc, charge complete and $V_{TEMP} \geq V_{LTF}$ or $V_{TEMP} \leq V_{TCO}$ or $V_{CELL} <$ VEDV	Trickle charge per Table 4	Low
Top-off charging	VSEL = Vcc and charge complete and time-out not exceeded and $V_{TEMP} > V_{TCO}$ and $V_{CELL} < V_{MCV}$	Activated per V_{SNS} for 73ms of every 585ms	Low
Trickle charging	Charge complete and top-off disabled or top-off complete or pending	Trickle charge per Table 4	Low
Fault	Charge pending state and charge pending time-out (t_{PEND}) complete	Trickle charge per Table 4	Low

Definitions: $V_{CELL} = V_{BAT} - V_{SNS}$; $V_{MCV} = 0.8 \bullet V_{CC}$; $V_{EDV} = 0.262 \bullet V_{CC}$ or $0.4 \bullet V_{CC}$; $V_{TEMP} = V_{TS} - V_{SNS}$; $V_{LTF} = 0.6 \bullet V_{CC}$.

activates the 30% and 40% indications. This technique is used for all the odd percentage charge indications to assure a monotonic charge status display.

When MULT is pulled up to V_{CC}, the bq2007 charge status monitor directly displays 1/32 of the charge safety timer as a percentage of full charge. This method is recommended over the voltage-based method when *charging* fixed-cell packs where the battery terminal voltages can vary greatly between packs. This method offers an accurate charge status indication when the battery is fully discharged. When using the timer-based method, discharge-before-charge is recommended.

During *discharge* with MULT pulled down to V_{SS}, the charge status monitor indicates the percentage of the battery voltage by comparing V_{BAT} to the internal discharge voltage reference thresholds. In BCD format, the discharge thresholds V80, V60, V40, and V20 correspond to a battery charge state indication of 90%, 70%, 50%, and 30%, respectively. In bargraph format, the same discharge thresholds correspond to a battery charge state indication of 90%, 60%, 40%, and 30%, respectively. Differences in the battery charge state indications are due to the finer granularity of the BCD versus the bargraph format.

During discharge and when MULT is pulled up to Vcc, the state-of-charge monitor BCD format displays the discharge condition, letter "d," whereas the bargraph format has no indication.

The charge statue display is blanked during the charge pending state and when the battery pack is removed.

Charge Status Display Modes

The bq2007 charge status monitor can be displayed in two modes summarized in Table 3. The display modes are a seven-segment monotonic bargraph or a seven-segment BCD single-digit format. When QDSEL is pulled down to V_{SS}, pine SEG_{A-G} drive the decoded seven segments of a single BCD digit display, and when QDSEL is pulled up to V_{CC}, pine SEG_{A-G} drive the seven segmenta of a bargraph display.

In the bargraph display mode, outputs SEG_{A-G} allow options for a three–segment to seven-segment bargraph display. The three–segment charge *status* display uses outputa SEG_B, SEG_D, and SEG_F for 30%, 60%, and 90% *charge* indications, respectively. The four-segment charge status display uses outputs SEG_A, SEG_C, SEG_D, and SEG_E for 20%, 40%, 60%, and 80% indications, respectively. The seven-segmentcharge status monitor uses all segments.

The BCD display mode drives pins SEG_{A-G} with the decoded seven-segment single-digit information. The display indicates in 10% increments from a BCD zero count at charge initiation to a BCD nine *count* indicating 90% charge capacity. Charge completion is indicated by the letter "F," a fault condition by the letter "8," and the discharge condition by the letter "d." See Table 3.

Table 2. bq2007 Charge Status Display Summary

Mode	Charge Action State	LED_1	LED_2	DIS	ALARM
$DSEL_1$ = L $DSEL_2$ = L (Mode 1)	Battery absent	0	0	0	0
	Charge pending (temp. limit, low voltage)	0	Flashing	0	0
	Discharge in progress	0	1	1	0
	Charging	Flashing	0	0	0
	Charge complete	1	0	0	High tone
	Fault (low-voltage time-out)	0	0	0	High tone
$DSEL_1$ = H $DSEL_2$ = L (Mode 2)	Battery absent	0	0	0	0
	Discharge in progress, pending	1	1	1	0
	Charging	1	0	0	0
	Charge complete	0	1	0	High tone
	Fault (low-voltage time-out)	0	0	0	High tone
$DSEL_1$ = L $DSEL_2$ = H (Mode 3)	Battery absent	0	0	0	0
	Charge pending (temp. limit, low voltage)	0	Flashing	0	0
	Discharge in progress	0	Flashing	1	0
	Charging	Flashing	0	0	0
	Charge complete	1	0	0	High tone
	Fault (low-voltage time-out)	0	1	0	High tone

Note: 1 = on; 0 = off; L = pulled down to V_{SS}; H = pulled up to V_{CC}.

Display Driver Modes

The bq2007 is designed to interface with LCD or LED type displays. The LED signal levels are driven when the MSEL soft-programmed input is pulled to V_{CC} at initialization. The output pin COM is the common anode connection for LED SEG_{A-G}.

The LCD interface mode is enabled when the MSEL soft-programmed input pin is pulled to Vss at initialization. An internal oscillator generates all the timing signals required for the LCD interface. The output pin COM is the common connection for static direct-driving of the LCD display backplane and is driven with an AC signal at the frame period. When enabled, each of the SEG_{A-G} pins is driven with the correct-phase AC signal to activate the LCD segment. In bargraph or BCD mode, output pins SEG_{A-G} interface to LED or LCD segments.

Battery Voltage and Temperature Measurement

The battery voltage and temperature are monitored within set minimum and maximum limits. When MULT is pulled up to V_{CC}, battery voltage is sensed at the BAT pin by a resistive voltage divider that divides the terminal voltage between $0.262 \cdot V_{CC}$ (V_{EDV}) and $0.8 \cdot V_{CC}$ (V_{MCV}). The bq2007 charges multi-cell battery packs from a minimum of N cells, to a maximum of 1.5 • N cells. The battery voltage divider is set to the minimum cell battery pack (N) by the BAT pin voltage divider ratio equation:

$$\frac{R1}{R2} = \left(\frac{N}{1.33}\right) - 1$$

When MULT is pulled down to Vss, tighter charge voltage limits and voltage-based charge status display are selected. This is recommended for charging packs with a fixed number of cells where the battery voltage

Table 3. bq2007 Charge Status Display Summary

Mode	Display Indication	SEG_A	SEG_B	SEG_C	SEG_D	SEG_E	SEG_F	SEG_G
QDSEL = H	20% charge	1	0	0	0	0	0	0
	30% charge	1	1	0	0	0	0	0
	40% charge	1	1	1	0	0	0	0
	60% charge	1	1	1	1	0	0	0
	80% charge	1	1	1	1	1	0	0
	90% charge	1	1	1	1	1	1	0
	Charge complete	1	1	1	1	1	1	1
QDSEL = L	0% charge—digit 0	1	1	1	1	1	1	0
	10% charge—digit 1	0	1	1	0	0	0	0
	20% charge—digit 2	1	1	0	1	1	0	1
	30% charge—digit 3	1	1	1	1	0	0	1
	40% charge—digit 4	0	1	1	0	0	1	1
	50% charge—digit 5	1	0	1	1	0	1	1
	60% charge—digit 6	1	0	1	1	1	1	1
	70% charge—digit 7	1	1	1	0	0	1	0
	80% charge—digit 8	1	1	1	1	1	1	1
	90% charge—digit 9	1	1	1	1	0	1	1
	Charge complete—letter F	1	0	0	0	1	1	1
	Fault condition—letter E	1	0	0	1	1	1	1
	Discharge—letter d	0	1	1	1	1	0	1

Note: 1 = on; 0 = off; L = pulled down to Vss; H = pulled up to V_{CC}.

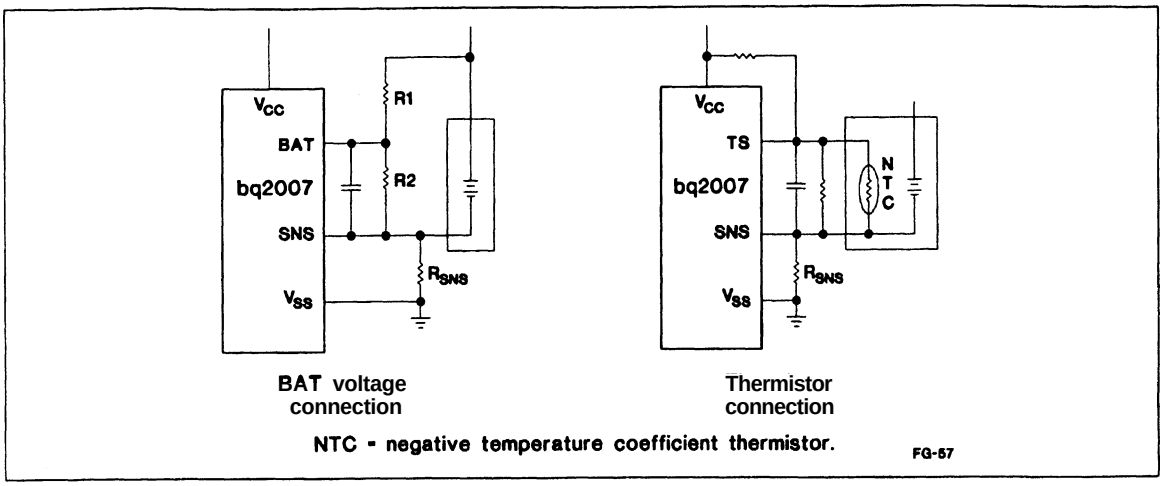


Figure 2. Voltage and Temperature Limit Measurement

divider range is between 0.4 • V_{CC} (V_{EDV}) and 0.8 • V_{CC} (V_{MCV}). The bq2007 charges fixed-cell battery packs of N cells. The battery voltage divider is set by the divider ratio equation:

$$\frac{R1}{R2} = \left(\frac{N}{1}\right) - 1$$

Note: The resistor-divider network impedance should be above 200KΩ to protect the bq2007.

battery temperature is monitored for maximum and minimum allowable limits, the bq2007 requires that the thermistor used for temperature measurement have a negative temperature coefficient. See Figure 2.

Temperature and Voltage Prequalifications

For charging to be initiated, the battery temperature must fall within predetermined acceptable limits. The voltage on the TS pin (V_{TS}) is compared to an internal low-temperature fault threshold (V_{LTF}) of (0.5 • V_{CC}) and the high temperature cutoff voltage (V_{TCO}) on the TCO pin. For charging to be initiated, V_{TS} must be less than V_{LTF} and greater than V_{TCO}. Since V_{TS} decreases as temperature increases, the TCO threshold should be selected to be lower than 0.5 • V_{CC} for proper operation. If the battery temperature is outside these limits, the bq2007 holds the charge-pending state with a pulse trickle current until the temperature is within limits. Temperature prequalification and termination is disabled if V_{TS} is greater than 0.8 • V_{CC}. See Figure 2.

The bq2007 provides undervoltage battery protection by trickle-current conditioning of a battery that is below the low-voltage threshold (V_{EDV}). The battery voltage (V_{CELL}) is compared to the low-voltage threshold (V_{EDV}) and charge will be inhibited if V_{CELL} < V_{EDV}. The condition trickle current and fault time-out are a percentage of the fast charge rate and maximum time-out (MTO).

Initiating Charge Action and Discharge-Before-Charge

A charge action is initiated under control of: (1) battery insertion or (2) power applied. Battery insertion is detected when the voltage at the BAT pin falls from above V_{MCV} to below V_{MCV}. Power applied is detected by the rising edge of Vcc when a battery is inserted.

Discharge-before-charge is initiated automatically on application of power or battery insertion when DCMD is connected to V_{SS}. Discharge-on-demand is initiated by a negative-going pulse on the $\overline{DCMD}$ pin regardless of

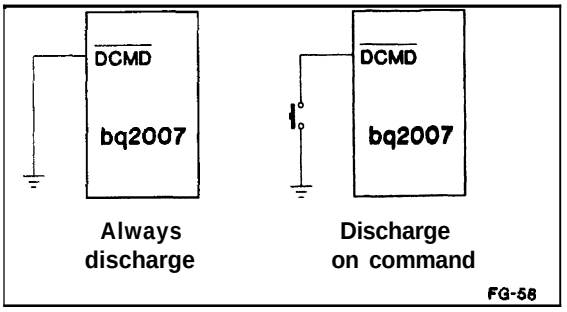


Figure 3. Discharge-Before-Charge

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Table 4. bq2007 Charge Action Control Summary

FAST Input State	TM Input State	Time-out Period (min)	MOD Duty Cycle	Hold-off period (sec)	Trickle Rep Rate -ΔV C/32	Trickle Rep Rate PVD C/64
Vss	Float	640 (C/8)	25%	2400	219Hz	109Hz
Vss	Vss	320 (C/4)	25%	1200	109Hz	55Hz
Vss	Vcc	160 (C/2)	25%	600	55Hz	27Hz
Vcc	Float	160 (C/2)	100%	600	219Hz	109Hz
Vcc	Vss	80 (C)	100%	300	109Hz	55Hz
Vcc	Vcc	40 (2C)	100%	150	55Hz	27Hz

charging activity. The $\overline{DCMD}$ pin is internally pulled up to Vcc; therefore, not connecting this pin results in disabling the discharge-before-charge function. See Figure 3. When the discharge begins, the DIS output goes high to activate an external transistor that connects a load to the battery. The bq2007 terminates discharge-before-charge by detecting when the battery cell voltage is leas than or equal to the end-of-diicharge voltage (V_{EDV}).

Charge State Actions

Once the required discharge is completed and temperature and voltage prequalifications are met, the charge state is initiated. The charge state is configured by the VSEL, FAST, and TM input pine. The FAST input selects between Fast and Standard charge rates. The Standard charge rate is ¼ of the Fast charge rate, which is accomplished by disabling the regulator for a period of 286µs of every 1144µs (25% duty cycle). In addition to throttling back the charge current, time-out and hold-off safety time are increased accordingly. See Table 4.

The VSEL input selects the voltage termination method. The termination mode sets the top-off state and trickle charge current rates. The TM input selects the Fast charge rate, the Standard rate, and the corresponding charge times. Once charging begins at the Fast or Standard rate, it continues until terminated by any of the following conditions:

- Negative delta voltage (-AV)
- Peak voltage detect (PVD)
- Maximum temperature cutoff (TCO)
- Maximum time-out (MTO)
- Maximum cutoff voltage (MCV)

Voltage Termination Hold-off

To prevent early termination due to an initial false peak battery voltage, the -ΔV and PVD terminations are disabled during a short "hold-off" period at the start of charge. During the hold-off period when fast charge is selected (FAST = 1), the bq2007 will top off charge to prevent excessive overcharging of a fully charged battery. Once past the initial *charge* hold-off time, the termination is enabled. TCO and MCV terminations are not affected by the hold-off time.

-ΔV or PVD Termination

Table 5 summarizes the two modes for full-charge voltage termination detection. When VSEL = Vss, negative delta voltage detection occurs when the voltage seen on the BAT pin falls 12mV (typical) below the maximum sampled value. VSEL = Vcc selects peak voltage detect termination and the top-off charge state. PVD termination occurs when the BAT pin voltage falls 6mV per cell below the maximum sampled value. When *charging* a battery pack with a fixed number of cells, the -AV and PVD termination thresholds are -6mV and 0 to -3mV per cell, respectively. The valid battery voltage range on V_{BAT} for -AV or PVD termination is from 0.262 • Vcc to 0.8 • Vcc.

Table 5. VSEL Configuration

VSEL	Detection Method	Top-Off	Pulse Trickle Rate
Vss	-ΔV	Disabled	C/32
Vcc	PVD	Enabled	C/64

Maximum Temperature, Maximum Voltage, and Maximum Time Safety Terminations

The bq2007 also terminates charge action for maximum temperature cutoff (TCO), maximum cutoff voltage (MCV), and maximum time-out (MTO). Temperature is monitored as a voltage on the TS pin (V_{TS}), which is compared to an internal high-temperature cutoff threshold of V_{TCO}. The TCO reference level provides the maximum limit for battery temperature during charging. MCV termination occurs when $V_{CELL} > V_{MCV}$. The maximum time-out (MTO) termination is when the charger safety timer countdown has completed during the active charge state. If the MTO, MCV, or TCO limit is exceeded during Fast charge, Standard charge, or top-off states, charge action is terminated.

Top-Off and Pulse Trickle Charging

The bq2007 provides a post-detection timed charge capability called top-off to accommodate battery chemistries that may have a tendency to terminate charge prior to achieving full capacity. When VSEL = Vcc, the top-off state is selected; charging continues after Fast charge termination for a period equal to the time-out value. In top-off mode, the Fast charge control cycle is modified so that MOD is activated for a pulse output of 73ms of every 585ms. This results in a rate 1/8 that of the Fast charge rate. Top-off charge is terminated by maximum temperature cutoff (TCO), maximum cutoff voltage (MCV), or maximum time-out termination.

Pulse trickle is used to compensate for self-discharge while the battery is idle and to condition a depleted low-voltage battery to a valid voltage prior to high-current charging. The battery is pulse trickle charged when Fast, Standard, or top-off charge is not active. The MOD output is active for a period of 286µs of a period specified in Table 4. This results in a trickle rate of C/64 for PVD and C/32 when -ΔV is enabled.

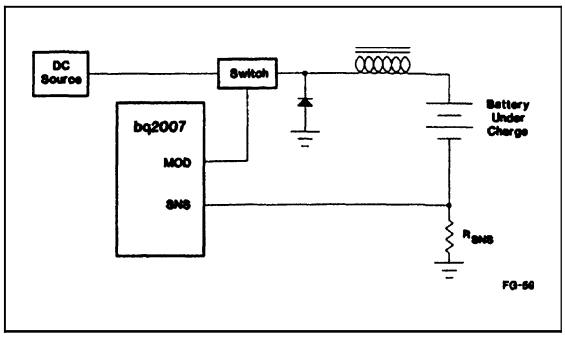

Figure 4. Constant-Current Switching Regulation

Charge Inhibit

Fast charge, top-off, and pulse trickle may be inhibited by using the $\overline{INH}$ input pin. When low, the bq2007 suspends all charge activity, drives all outputs to high impedance, and assumes a low-power operational state. When $\overline{INH}$ returns high, a fast-charge cycle is qualified and begins as soon as conditions allow.

Charge Current Control

The bq2007 controls charge current through the MOD output pin. In a frequency-modulated buck regulator configuration, the control loop senses the voltage at the SNS pin and regulates to maintain it between 0.04 • Vcc and 0.05 • Vcc. The nominal regulated current is I_{REG} = 0.225V/R_{SNS}. See Figure 4.

MOD pin is switched high or low depending on the voltage input to the SNS pin. If the voltage at the SNS pin is less than V_{SNSLO} (0.04 • Vcc nominal), the MOD output is switched high to gate charge current through the inductor to the battery. When the SNS voltage is greater than V_{SNSHI} (0.05 • Vcc nominal), the MOD output is switched low-shutting off charge current from the supply. The MOD pin can be used to gate an external charging current source. When an esternal current source is used, no sense resistor is required, and the SNS pin is connected to V_{SS}.

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Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	V_{CC} relative to V_{SS}	-0.3	+7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3	+7.0	V	
T_{OPR}	Operating ambient temperature	-20	+70	°C	Commercial
T_{STG}	Storage temperature	-40	+85	°C	
T_{SOLDER}	Soldering temperature		+260	°C	

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds ($T_A = T_{OPR}$; V_{CC} = 5V ± 10%)

Symbol	Parameter	Rating	Tolerance	Unit	Notes
V_{SNSHI}	High threshold at SNS resulting in MOD = Low	0.05 • V_{CC}	±25	mV	
V_{SNSLO}	Low threshold at SNS resulting in MOD = High	0.04 • V_{CC}	±10	mV	
V_{LTF}	TS pin low-temperature threshold	0.5 • V_{CC}	±30	mV	SNS = 0V
V_{HTF}	TS pin high-temperature threshold	V_{TCO}	±30	mV	SNS = 0V
V_{EDV}	Endsf-discharge voltage MULT is pulled up to V_{CC}	0.262 • Vcc	±30	mV	SNS = 0V
	End-of-diechargevoltage MULT is pulled down to V_{SS}	0.4 • V_{CC}	±30	mV	SNS = 0V
V_{MCV}	BAT pin maximum cell voltage threshold	0.8 • V_{CC}	±30	mV	SNS = 0V
V_{20}	20% state-of-charge voltage threshold at the BAT pin	$^{187}/_{320}$ • V_{CC}	±30	mV	Fast or standard charge state; MULT pulled to V_{SS}
V_{40}	40% state-of-charge voltage threshold at the BAT pin	$^{191}/_{320}$ • V_{CC}	±30	mV	Fast or standard charge state; MULT pulled to V_{SS}
V_{60}	60% state-of-charge voltage threehold at the BAT pin	$^{195}/_{320}$ • Vcc	±30	mV	Fast or standard charge state; MULT pulled to V_{SS}
V_{80}	80% state-of-charge voltage threehold at the BAT pin	$^{203}/_{320}$ • V_{CC}	±30	mV	Fast or standard charge state; MULT pulled to V_{SS}
V_{20}	20% state-of-charge voltage threehold at the BAT pin	$^{158}/_{320}$ • Vcc	±30	mV	Discharge-before-charge etate; MULT pulled to V_{SS}; DIS = 1
V_{40}	40% state-of-charge voltage threehold at the BAT pin	$^{163}/_{320}$ • V_{CC}	±30	mV	Discharge-before-chargestate; MULT pulled to V_{SS}; DIS = 1
V_{60}	60% state-of-charge voltage threshold at the BAT pin	$^{167}/_{320}$ • V_{CC}	±30	mV	Diecharge-before-chargestate; MULT pulled to V_{SS}; DIS = 1
V_{80}	80% state-of-charge voltage threshold at the BAT pin	$^{171}/_{320}$ • V_{CC}	±30	mV	Discharge-before-chargeetate; MULT pulled to V_{SS}; DIS = 1

Recommended DC Operating Conditions (T_A = 0 to +70°C)

Symbol	Parameter	Inlmum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	10%
V_{BAT}	Voltage on BAT pin	0	-	Vcc	V	
V_{TS}	Voltage on TS pin	0		Vcc	V	Thermistor input
V_{TCO}	Temperature cutoff on TCO	0	-	0.5 • Vcc	V	Note 2
V_{CELL}	Battery voltage potential	0		Vcc	V	V_{BAT} - V_{SNS}
V_{TEMP}	Voltage potential on TS	0		Vcc	V	V_{TS} - V_{SNS}
V_{IH}	Logic input high	2.0			V	$\overline{DCMD}$, FAST, VSEL, $\overline{INH}$
	Tri-level input high	Vcc - 0.3	-		V	TM
V_{IL}	Logic input low			0.8	V	$\overline{DCMD}$, FAST, VSEL, $\overline{INH}$
	Tri-level input low			0.3	V	TM
V_{OH}	Logic output high	Vcc - 0.8	-		V	DIS, LED_{1-2}, SEG_{A-G} @ I_{OH} = -10mA; MOD @ I_{OH} = -5mA
V_{OL}	Logic output low			0.8	V	DIS, LED_{1-2}, SEG_{A-G} @ I_{OL} = 10mA; MOD @ I_{OL} = 5mA
V_{OHCOM}	COM output	Vcc - 0.8	-	-	V	@ I_{OHCOM} = -40mA
I_{OHCOM}	COM source	-40	-	-	mA	@ V_{OHCOM} = Vcc - 0.8V
I_{CC}	Supply current	-	1	2.5	mA	No output load
I_{OH}	DIS, LED_{1-2}, SEG_{A-G} source	-10			mA	@V_{OH} = Vcc - 0.8V
I_{OH}	MOD	-5			mA	@V_{OH} = Vcc - 0.8V
I_{OL}	DIS, LED_{1-2}, SEG_{A-G} sink	10			mA	@V_{OL} = Vss + 0.8V
I_{OL}	MOD	5	-	-	mA	@V_{OL} = Vss + 0.8V
I_{IZ}	Tri-state inputs floating for Z state	-2.0	-	2.0	µA	TM
I_L	Input leakage			±1	µA	$\overline{INH}$, VSEL, V = Vss to Vcc
	Input leakage	50		400	µA	$\overline{DCMD}$, FAST, V = Vss to Vcc
I_{IL}	Logic input low current			70	µA	TM, V = Vss to Vss + 0.3V
I_{IH}	Logic input high current	-70			µA	TM, V = Vcc - 0.3V to Vcc

Impedance

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
R_I	DC input impedance: pine TS, BAT, SNS, TCO	50	-	-	MΩ	
R_{PROG}	Soft-programmed pull-up resistor	150	-	200	KΩ	MSEL, $DSEL_1$, $DSEL_2$, MULT, QDSEL; resistor value ± 1% tolerance
R_{FLT}	Float state external resistor	-	5	-	MΩ	TM

Timing (TA = 0 to +70°C; VCC ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
d_{FCV}	Deviation of fast charge safety time-out	0.84	1.0	1.16	-	At V_{CC} = ±10%, T_A = 0 to 60°C; see Table 3
t_{REG}	MOD output regulation frequency	-	-	300	kHz	Typical regulation range; V_{CC} = 5.0V
t_{PEND}	Charge pending time-out	-	25	-	%	Ratio of fast charge time-out; see Table 4.
F_{COM}	Common LCD backplane frequency		73		Hz	LCD segment frame rate
F_{ALARM}	Alarm frequency output		3500		kHz	High tone
t_{PW}	Pulse width for $\overline{DCMD}$ and $\overline{INH}$ pulse command	1	-	-	µs	Signal valid time
t_{MCV}	Valid period for $V_{CELL} > V_{MCV}$	0.5	-	1	sec	If $V_{CELL} \geq V_{MCV}$ for t_{MCV} during charge or top-off, then a transition a battery replacement.

Note: Typical is at T_A = 25°C, V_{CC} = 5.0V.

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	11	V_{SNSLO} Rating	Wbe V_{SNSHI} - (0.01 • V_{CC}); is 0.04 • V_{CC}

Note: Change 1 = Sept. 1996 B changes from Dec. 1995.

Ordering Information

bq2007 -

Temperature:
blank = Commercial (-20 to +70°C)
N = Industrial (-40 to +85°C)*

Package Option:
PN = 24-pin narrow plastic DIP
S = 24-pin SOIC

Device:
bq2007 Fast Charge IC

* Contact factory for availability.

BENCHMARQ

Product Brief **DV2007S1**

Fast Charge Development System

Features

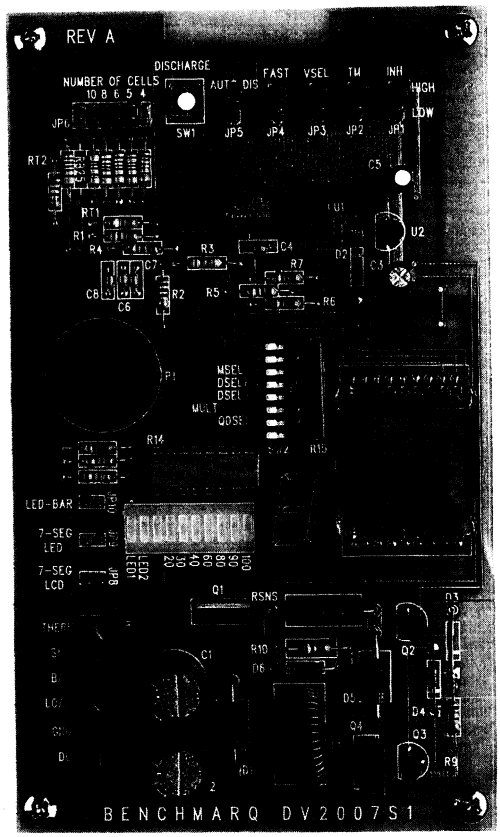
- bq2007 fast charge control evaluation and development
- Battery charge status display modes and driver interfaces are jumper configurable
  - On-board seven-step LED bargraph or ten-step BCD digit display
  - Charge status monitoring interface option
  - On-board charge status indication LEDs
- Fast charge termination by -ΔV, peak voltage detect (PVD), maximum voltage, maximum time, and maximum temperature
- Jumper-selectable for 4, 5, 6, 8, or 10 NiCd or NiMH cell pack charging
- Jumper-selectable standard or fast charge rates from 1 to 4 hours
- Discharge-before-charge push-button or automatic control

Introduction

The bq2007 Fast Charge IC is a single-chip CMOS IC that performs charge control, charge status, and charge status display in a 24-pin DIP package. The DV2007S1 Development System offers a quick method to evaluate the bq2007 functional features and to validate selected parameters prior to design implementation.

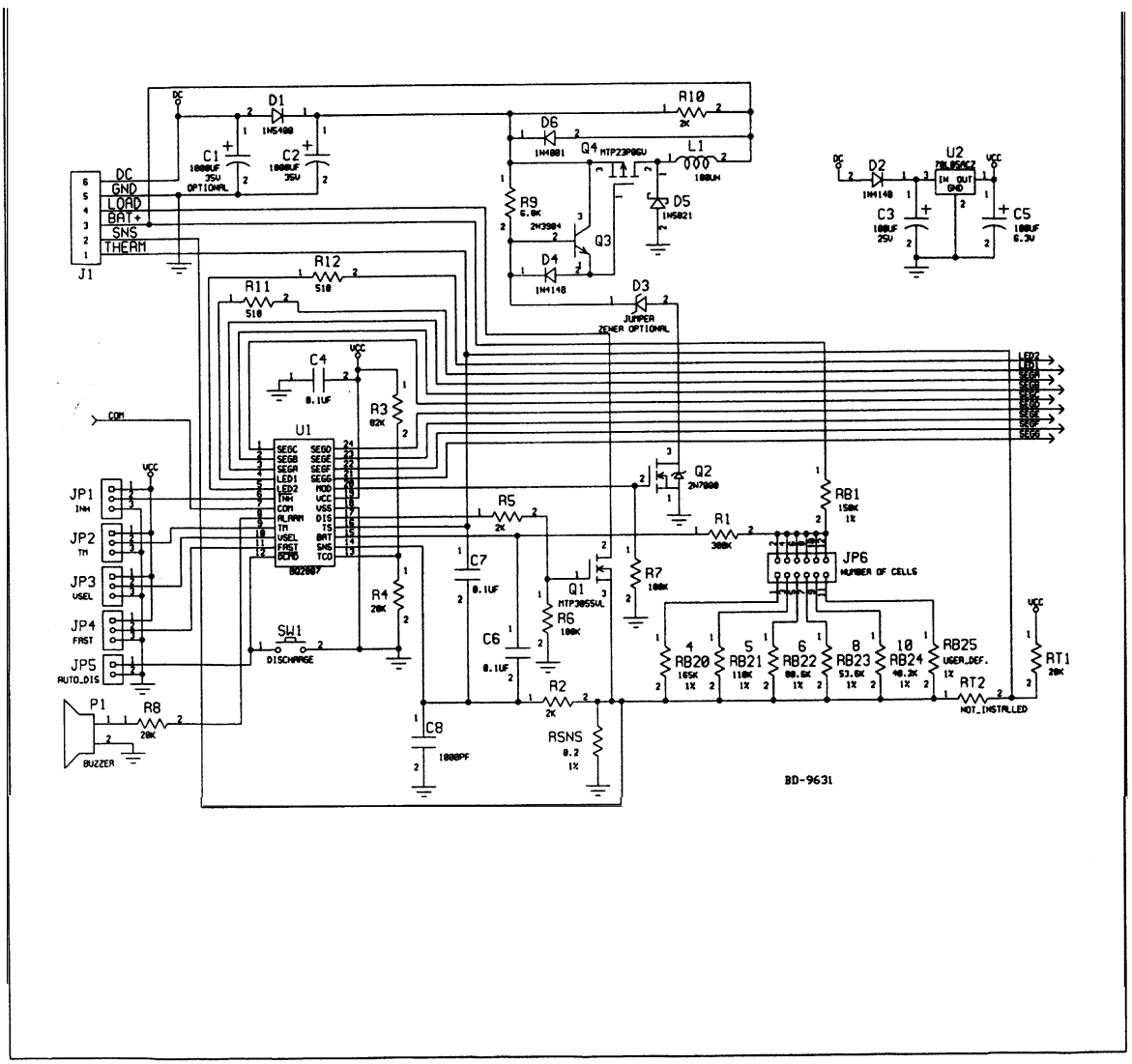
Functional Description

The DV2007S1 provides the platform for a functional evaluation of the bq2007 features on single PCB. The board contain all the connections required to fully exercise the bq2007 feature sets. See the bq2007 data sheet and application note AB-0019 entitled "Using the bq2007 Display Mode Options."



A full data sheet of this product is available on our web site (http:/lwww.benchmarq.com), or you may contact the factory for one.

DV2007S1 Board Schematic



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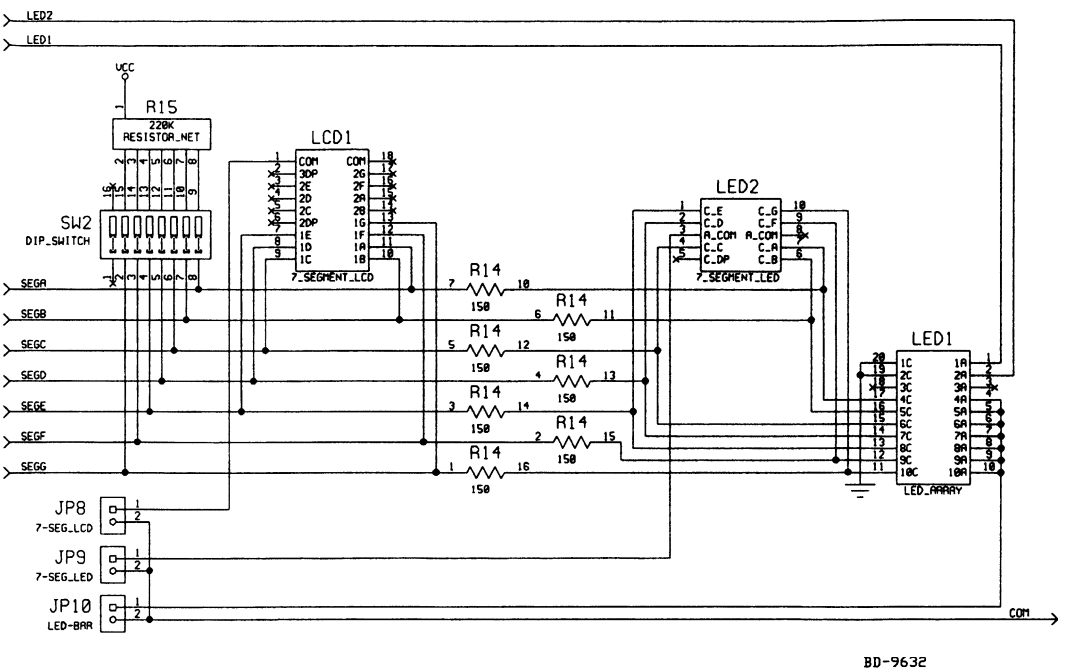
DV2007S1 Board Schematic (Continued)



Using the bq2007
Display Mode Options

Introduction

The bq2007 Fast Charge IC provides flexibility with a wide variety of charge status monitor display mode formate. The bq2007 internal charge status monitor can be configured to support up to a seven-segment bargraph or a eingle BCD digit display. The bargraph display indicates up to seven monotonic steps, whereas the BCD digit indicates ten steps of 10% increments. The bq2007 output drivers can direct-drive either LCD or LED interface levels.

Display Driver Modes

The bq2007 is designed to interface directly with LCD or LED type displays. The display driver mode is selected with the soft-programmed input MSEL and is independent of the state-of-charge monitor format or indications. The LED signal levels are driven when the MSEL &programmed input is pulled to V_{CC} at initialization. The output pin COM is the common-anode connection for LED SEG_{A-G}. See Figure 1.

The LCD interface mode is enabled when the MSEL soft-programmed input is pulled to V_{SS} at initialization. An internal oscillator generates all timing signals required for the LCD interface. Output pin COM is the common connection for static direct-driving of the LCD display backplane and is driven with an AC signal at the frame period. When enabled, each of the SEG_{A-G} pine are driven with the correct-phase AC signal to activate the LCD segment. See Figure 1.

Charge Status Indication

Table 1 summarizes the bq2007 charge status display indicatione. The charge statue indicators include the DIS output, which can be used to indicate the discharge state. the audio ALARM output, which indicatee charge completion and fault conditions, and the dedicated status outputs, LED_1 and LED2

Outputs LED_{1-2} have three display modes that are selected at initialization by the input pine $DSEL_1$ and $DSEL_2$. The $DSEL_1$ and $DSEL_2$ input pine, when pulled down to V_{SS}, are intended for implementationof a simple two-LED system, where LED_1 indicatee the precharge status (i.e., charge pending and discharge) and LED_2 indicates the charge statue (i.e., charging and completion). $DSEL_1$ pulled up to V_{CC} and $DSEL_2$ pulled down to V_{SS} mode allows the implementationof a eingle tri-color LED such that discharge, charging, and completion each have a unique color. $DSEL_1$ pulled down to V_{SS} and $DSEL_2$ pulled up to V_{CC} mode allows for fault status information. See Figure 2.

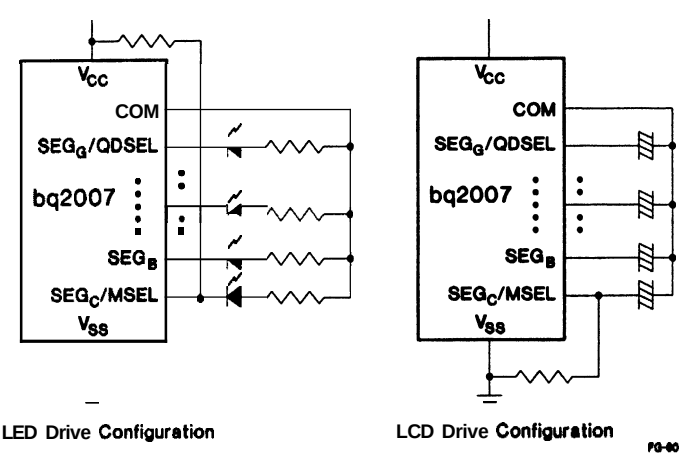


Figure 1. Display Driver Configurations

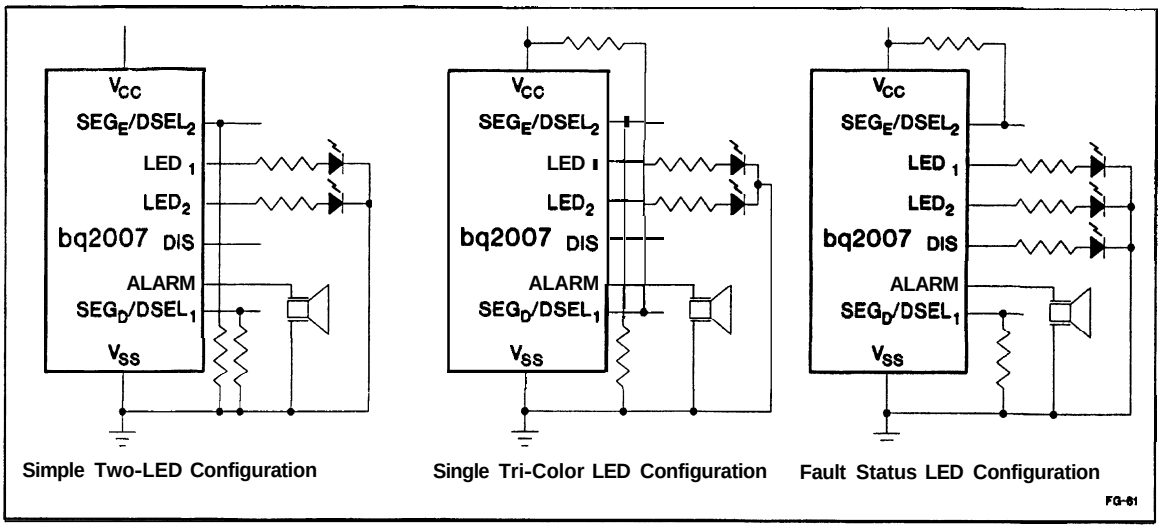


Figure 2. Charge Status Display Configurations

Table 1. bq2007 Charge Status Display Summary

Mode	Charge Action State	LED_1	LED_2	DIS	ALARM
$DSEL_1$ = L $DSEL_2$ = L (Mode 1)	Battery absent	0	0	0	0
	Charge pending (temp. limit, low voltage)	0	Flashing	0	0
	Discharge in progress	0	1	1	0
	Charging	Flashing	0	0	0
	Charge complete	1	0	0	High tone
	Fault (low-voltage time-out)	0	0	0	High tone
$DSEL_1$ = H $DSEL_2$ = L (Mode 2)	Battery absent	0	0	0	0
	Discharge in progress, pending	1	1	1	0
	Charging	1	0	0	0
	Charge complete	0	1	0	High tone
	Fault (low-voltage time-out)	0	0	0	High tone
$DSEL_1$ = L $DSEL_2$ = H (Mode 3)	Battery absent	0	0	0	0
	Charge pending (temp. limit, low voltage)	0	Flashing	0	0
	Discharge in progress	0	Flashing	1	0
	Charging	Flashing	0	0	0
	Charge complete	1	0	0	High tone
	Fault (low-voltage time-out)	0	1	0	High tone

Note: 1 = on; 0 = off; L = pulled down to Vss; H = pulled up to Vcc.

Audio Output Alarm

The bq2007 audio alarm output generates an audio tone to indicate a charge completion or fault condition. The audio alarm output is a symmetrical duty-cycle AC signal that is compatible with standard piezoelectric alarm elements. A valid battery insertion is indicated by a single 3.5kHz beep of ½-second typical duration. The charge completion and fault conditions are indicated by a 9.5- to 16-second high-tone sequence of 42-second typical duration at a 2-second typical repetition rate.

Charge Status Monitoring

The bq2007 charge status monitor may display the battery voltage or charge safety timer as a percentage of the full-charged condition. These options are selected with the MULT soft-programmed input pin.

When MULT is pulled down to Vss, the battery charge status is displayed as a percentage of the battery voltage, and the single-cell battery voltage at the BAT pin is compared with internal charge voltage reference thresholds. When V_{BAT} is greater than the internal thresholds of V_{20}, V_{40}, V_{60}, or V_{80}, the respective 20%, 40%, 60%, or 80% display outputs are activated. The battery voltage directly indicates 20% charge increments, while the 10% charge increments use a timer that is a function of the charge safety timer.

When MULT is pulled down to V_{SS} and when V_{BAT} exceeds V_{20} during charging, the 20% charge indication is activated and the timer begins counting for a period equal to 1/64 to 1/32 of the charge safety time-out period. When the timer count is completed, the 30% charge indication is activated. Should V_{BAT} exceed V_{40} prior to the timer count completion, the charge status monitor activates the 30% and 40% indications. This technique is used for all the odd percentage charge indications to assure a monotonic charge status display.

When MULT is pulled up to V_{CC}, the bq2007 charge status monitor directly displays 1/32 of the charge safety timer as a percentage of the full-charge time. This method is recommended over the voltage-based method when charging packs with different cell configuration (i.e. 5-cell or 6-cell pack) where the battery terminal voltages will vary greatly between packs. This method offers an accurate charge status indication when the battery is fully discharged. When using the timer-based method, diecharge-before-charge is recommended.

During discharge with MULT pulled down to V_{SS}, the charge statue monitor indicates the percentage of the battery voltage by comparing V_{BAT} to the internal discharge voltage reference thresholds. In BCD format, the diecharge thresholds V80, V60, V40, and V20 correspond to a battery charge state indication of 90%, 70%, 50%, and 30%, respectively. In bargraph format, the same discharge thresholds correspond to a battery charge state indication of 90%, 60%, 40%, and 30%, respectively. Differences in the battery charge state indications are due to the finer granularity of the BCD versus the bargraph format.

During discharge and when MULT is pulled up to V_{CC}, the state-of-charge monitor BCD format displays the discharge condition, letter "d," whereas the bargraph format has no indication.

The charge status display is blanked during the charge pending state and when the battery pack is removed.

Charge Status Display Modes

The bq2007 charge status monitor can be displayed in two modes summarized in Table 2. The display modes are a seven-segment monotonic bargraph or a seven-segment BCD single-digit format. When QDSEL is pulled down to V_{SS}, pins SEG_{A-G} drive the decoded seven segments of a single BCD digit display, and when QDSEL is pulled up to V_{CC}, pins SEG_{A-G} drive the seven segments of a bargraph display.

In the bargraph display mode, outputs SEG_{A-G} allow options for a three-segment to seven-segment bargraph display. The three-segment charge statue display uses outputs SEG_B, SEG_D, and SEG_F for 30%, 60%, and 90% charge indications, respectively. The four-segment charge status display uses outputs SEG_A, SEG_C, SEG_D, and SEG_E for 20%, 40%, 60%, and 80% indications. respectively. The seven-segment charge status monitor uses all segments. See *Figure* 3.

The BCD display mode drives pins SEG_{A-G} with the decoded seven-segment single-digit information. The display indicates in 10% increments from a BCD zero count at charge initiation to a BCD nine count indicating 90% charge capacity. Charge completion is indicated by the letter "F," a fault condition by the letter "E," and the discharge condition by the letter "d." See Figure 4.

Table 2. bq2007 Charge Status Display Summary

Mode	Display Indication	SEG_A	SEG_B	SEG_C	SEG_D	SEG_E	SEG_F	SEG_G
QDSEL = H	20% charge	1	0	0	0	0	0	0
	30% charge	1	1	0	0	0	0	0
	40% charge	1	1	1	0	0	0	0
	60% charge	1	1	1	1	0	0	0
	80% charge	1	1	1	1	1	0	0
	90% charge	1	1	1	1	1	1	0
	Charge complete	1	1	1	1	1	1	1
QDSEL = L	0% charge—digit 0	1	1	1	1	1	1	0
	10% charge—digit 1	0	1	1	0	0	0	0
	20% charge—digit 2	1	1	0	1	1	0	1
	30% charge—digit 3	1	1	1	1	0	0	1
	40% charge—digit 4	0	1	1	0	0	1	1
	50% charge—digit 5	1	0	1	1	0	1	1
	60% charge—digit 6	1	0	1	1	1	1	1
	70% charge—digit 7	1	1	1	0	0	1	0
	80% charge—digit 8	1	1	1	1	1	1	1
	90% charge—digit 9	1	1	1	1	0	1	1
	Charge complete—letter F	1	0	0	0	1	1	1
	Fault condition—letter E	1	0	0	1	1	1	1
	Discharge—letter d	0	1	1	1	1	0	1

Note: 1 = on; 0 = off; L = pulled down to Vss; H = pulled up to Vcc.

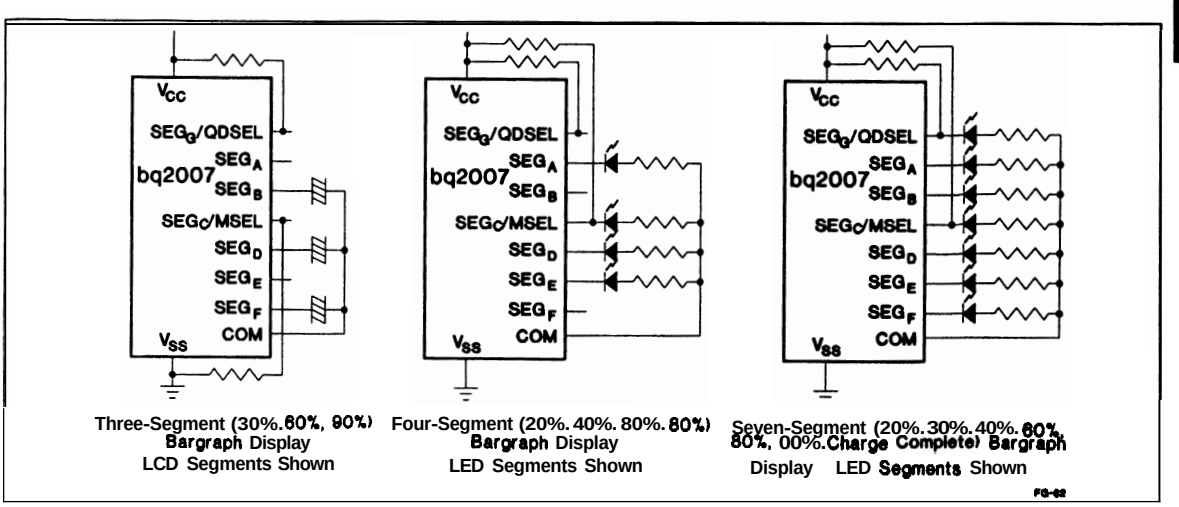


Figure 3. Charge Status Bargraph Display Configurations

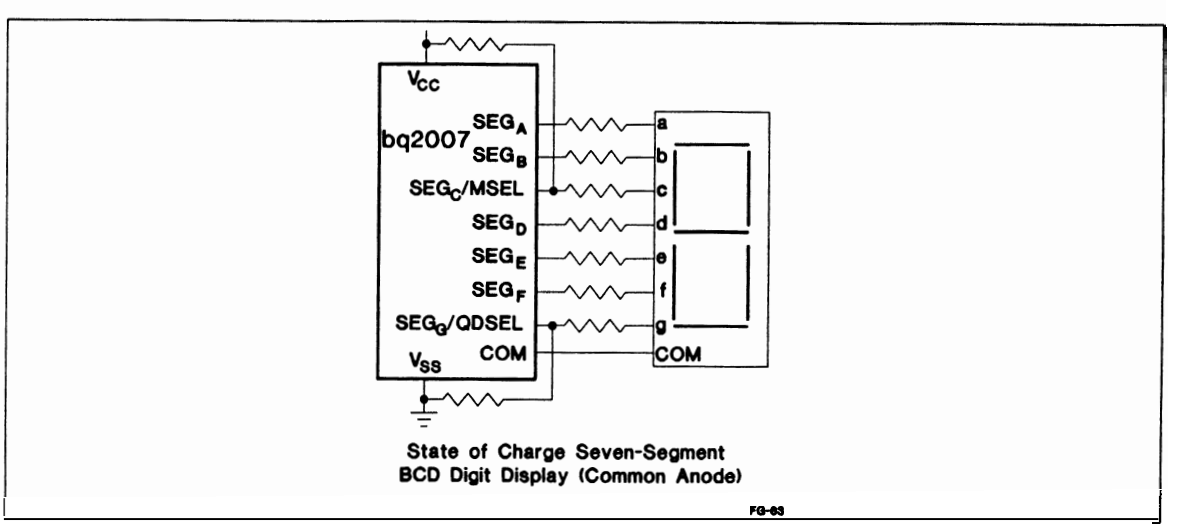


Figure 4. Charge Status BCD Digit Display Mode

Notes

BENCHMARQ

Using the bq2007

Enhanced Features for Fast Charge

1

Introduction

This application note describes the correct setup of the bq2007 features and gives design examples for a NiCd or NiMH switch-mode and gated current source fast charger applications.

The bq2007 is targeted for applications requiring fast-charging and charge status monitoring at minimal cost. It provides sophisticated full-charge detection techniques such as PVD (peak voltage detection) and -ΔV (negative delta voltage) that enable the user to take advantage of advanced battery technologies such as nickel metal-hydride (NiMH) and high-capacity fast-charge nickel cadmium (NiCd).

The bq2007 offers flexibility by providing a wide variety of charge status monitoring and charge state display formats. The internal charge status monitor can be configured to support up to a seven-segment bargraph or a single-digit display. The bargraph display indicates seven monotonic steps, whereas the single digit counts in ten steps of 10% increments. The output can direct-drive either LCD or LED interface levels.

The bq2007 indicates charge state status with an audio alarm output option and two dedicated output pins with programmable display options. The $DSEL_{1-2}$ inputs can select one of the three display modes for the LED_{1-2} outputs.

Background

A significant advantage of the bq2007 over other fast-charge solutions is the flexibility to select PVD or -ΔV as the primary decisions for fast-charge termination PVD is the recommended termination method for NiMH batteries, while -ΔV is recommended for NiCd batteries. -ΔV or PVD detection in the bq2007 may be temporarily disabled during periods when the charge current fluctuates. -ΔV or PVD may be permanently disabled without affecting other bq2007 charge-termination functions.

The bq2007 pmvidea battery protection by trickle-charge conditioning of a battery that is below the low-voltage threshold (V_{EDV}). The battery voltage (V_{CELL}) is compared to the low-voltage threshold (V_{EDV}) and charge will be inhibited if $V_{CELL} < V_{EDV}$. The condition trickle current and fault time-out are a percentage of the fast charge rate and maximum time-out (MTO).

To ensure safety for the battery and syatem, fast charging also terminates baaed on a high-temperature cutoff threshold (TCO), a safety time-out, and a maximum cell voltage threshold (MCV). To avoid possible premature fast-charge termination when charging batteries after long periods of storage, the bq2007 disables PVD, and -ΔV detection during a ehort %old-off period at the start of fast charge. During the hold-off period when fast charge is selected, the bq2007 charges at the topoff rate to prevent excessive overcharging of a fully charged battery. This hold-off period is configured as described in the bq2007 data sheet.

The bq2007 may be configured to have two or three charge stages. In a two-stage configuration, the fast-charge stage controlled by the bq2007 is preceded and followed by a pulse trickle charge at a rate controlled by bq2007 input pins FAST, TM, and VSEL. In a three-stage configuration, the fast charge is followed by a 'top-off" charge stage where the battery is charged at 1/8 of the fast charge rate. This allows the battery to be quickly and safely brought to a full charge state. Following top-off, pulse trickle is used to compensate for eelf-discharge while the battery is idle. The trickle rate is $C/_{64}$ for PVD and $C/_{32}$ when -ΔV is enabled.

Charger Circuit Examples

Two detailed applications follow this section. One pmvidea direct control of a switch-mode regulator, and the other provides control of an external current source.

The switching-mode constant-current regulator is used on the DV2007S1 development system. The board layout and schematic is described in the layout guidelines section.

Gating Current

Figure 1 shows an example of external gated current source. With SNS connected to V_{SS}, the bq2007 enables charge current to the battery by taking MOD high at the start of charging and maintaining this state until charging is terminated. In this example, R7, R19, R15, and Q1 and Q2 form the switching circuit. When MOD goes high, Q2 switches on—turning on Q1. When MOD goes low, the base current in Q1 is turned off and the charging path is switched off.

The current-handling capability of this circuit is limited by the product of the current gains of the transistors and by the 5mA drive capability of the MOD pin.

This limitation may be removed by replacing the PNP at Q1 with a pFET. See Table 1 for suggested transistors.

Table 1. Suggested Transistors (Q1)

Q1	Type	Package	Maximum Current	Maximum Voltage
IRFR9010	pFET	DPAK	5.3	-50
IRFR9022	pFET	DPAK	9.0	-50
IRFR9020	pFET	DPAK	9.9	-50
IRFD9014	pFET	HEXDIP	1.1	-60
IRFD9024	pFET	HEXDIP	1.6	-60
IRF9Z10	pFET	TO-220	4.7	-50
IRF9Z22	pFET	TO-220	8.9	-50
IRF9Z20	pFET	TO-220	9.7	-50
IRF9Z32	pFET	TO-220	15	-50
BD136	PNP	TO-225	1.5	-60
MJE171	PNP	TO-225	3.0	-60
TIP42A	PNP	TO-220	6.0	-60

Note: For very high currents, two parallel pFETs or an nFET with a high-side driver circuit may be suitable.

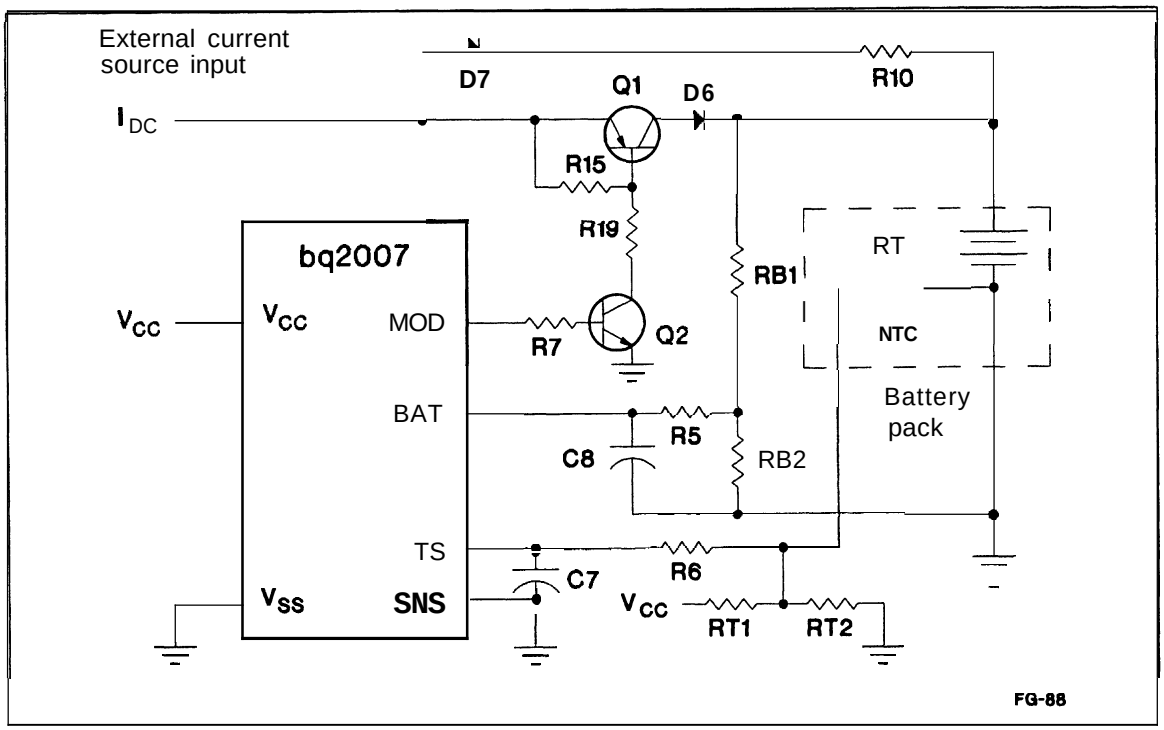


Figure 1. Gated External Source (Bipolar Switch Option)

Charge Action Control

The bq2007 charge action is controlled by input pins DCMD, VSEL, FAST, and TM. When charge action is initiated, the bq2007 enters the charge-pending state, checks for acceptable battery voltage and temperature, and performs any required diecharge-before-charge operations. DCMD controls the diecharge-before-charge function, and VSEL, FAST, and TM select the charger configuration. See Tables 4 and 5 of the bq2007 data sheet.

Charge Status Indication

Table 2 summarizes the bq2007 charge statue display. The charge status indicators include the DIS output, which can be used to indicate the discharge state, the audio ALARM output, which indicates charge completion and fault conditions, and the dedicated status outputs. LED_1 and LED_2.

Outputa LED_{1-2} have three display modes that are selected at initialization by the input pins $DSEL_1$ and $DSEL_2$. The $DSEL_1$ and $DSEL_2$ input pins, when pulled down to V_{SS}, are intended for implementation of a simple two-LED system, where LED_2 indicates the precharge statue (i.e., charge pending and discharge) and LED_1 indicates the charge status (i.e., charging and completion). $DSEL_1$ pulled up to V_{CC} and $DSEL_2$ pulled down to V_{SS} mode is for implementation of a single tri-color LED such that discharge, charging, and completion each have a unique color. $DSEL_1$ pulled down to V_{SS} and $DSEL_2$ pulled up to V_{CC} mode allows for fault status information.

Audio Alarm Selection

The alarm output waveform is a 3.5KHz square wave signal that allows a direct connection to drive standard piezoelectric alarm elements. Piezoelectric alarm elements are designed for a maximum sound output at a specific frequency and drive voltage. The alarm element must be selected for a maximum sound output at a frequency of 3.5kHz with a 5V peak-to-peak drive signal. The PCB mount element can be connected directly to the bq2007 alarm output with a 20K isolation resistor. The design of a molded resonant cavity should follow the manufacturers recommended procedures to assure maximum sound output. Manufactures also provide several boost circuits that can be used to increase the drive voltage for increased sound output levels.

Table 2. bq2007 Charge Status Display Summary

Mode	Charge Action State	LED_1	LED_2	DIS	ALARM
$DSEL_1$ = L $DSEL_2$ = L (Mode 1)	Battery absent	0	0	0	0
	Charge pending (temp. limit, low voltage)	0	Flashing	0	0
	Discharge in progress	0	1	1	0
	Charging	Flashing	0	0	0
	Charge complete	1	0	0	High tone
	Fault (low-voltage time-out)	0	0	0	High tone
$DSEL_1$ = H $DSEL_2$ = L (Mode 2)	Battery absent	0	0	0	0
	Discharge in progress, pending	1	1	1	0
	Charging	1	0	0	0
	Charge complete	0	1	0	High tone
	Fault (low-voltage time-out)	0	0	0	High tone
$DSEL_1$ = L $DSEL_2$ = H (Mode 3)	Battery absent	0	0	0	0
	Charge pending (temp. limit, low voltage)	0	Flashing	0	0
	Discharge in progress	0	Flashing	1	0
	Charging	Flashing	0	0	0
	Charge complete	1	0	0	High tone
	Fault (low-voltage time-out)	0	1	0	High tone

Note: 1 = on; 0 = off; L = pulled down to V_{SS}; H = pulled up to V_{CC}.

Selecting the BAT Divider for Charge Monitoring

The voltage based state of charge monitoring is enabled when charging packs with a fixed number of cells by pulling the multi-cell pack select input MULTI to Vss. When MULT = 0, internal voltage thresholds are compared with the BAT pin input voltage for both charge and discharge capacity status indications. When discharge-before-charge is initiated, the state-of-charge monitor indicates the discharge condition as monotonic decreasing steps from the charged condition. The voltage charge status monitoring circuit is shown in Fig. 2. The circuit changes its voltage threshold reference divider for charge or discharge monitoring when the discharge signal is zero or one, respectively. The voltage thresholds are a fixed ratio of the VCC supply voltage and are specified in the bq2007 data sheet in the section entitled 'DC Thresholds.' The voltage thresholds were selected based on typical NiCad and NiMH battery characteristics for a typical charge rate of 1C and a typical discharge rate of 1 Amp.

To optimize the charge status monitoring for a range of fixed-cell packs (i.e. MULTI = 1), the BAT divider should be calculated such that the highest fixed cell pack will be centered at the EDV threahold. For example, to charge packs that range from 4 to 6 fixed cells, select the BAT divider MULTI = 0. The BAT divider should be determined by BAT divider equation 2 for values shown in Table 4. To further optimize, you can fit the battery characteristics to the end points of the EDV and MCV thresholds. This will center the battery voltage charge characteristics in the center of the bq2007 charge monitoring thresholds. This is possible since the full charge detection methods (PVD, -DV) are not dependent on absolute voltage value. When adjusting the battery divider, the maximum cutoff voltage (V_{MCV}) must not be exceeded.

Charge Status Monitoring

The bq2007 charge status monitor may display the battery voltage or charge safety timer as a percentage of the full-charged condition. These options are selected with the MULT input pin.

When MULT is pulled down to Vss, the battery charge status is displayed as a percentage of the battery voltage, and the single-cell battery voltage at the BAT pin is compared with internal charge voltage reference thresholds. When V_{BAT} is greater than the internal thresholds of V_{20}, V_{40}, V_{60}, or V_{80}, the respective 20%, 40%, 60%, or 80% display outputs are activated. The battery voltage directly

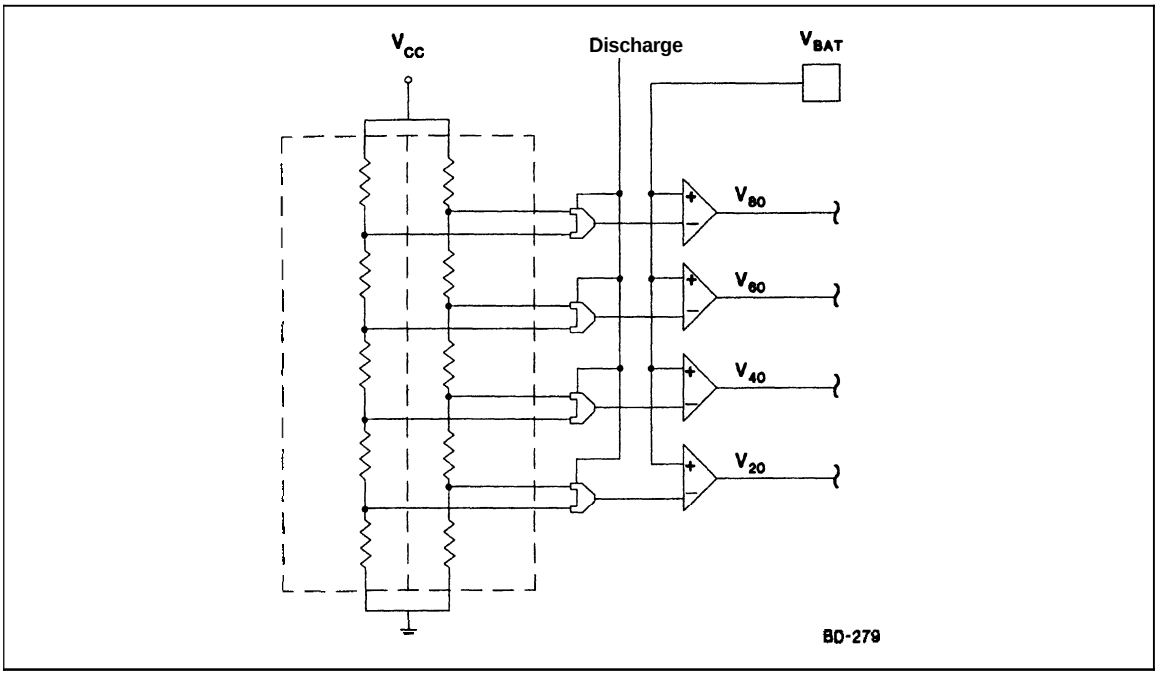


Figure 2. Voltage Charge Status Monitoring Circuit

indicates 20% charge increments, while the 10% charge increments use a timer that is a function of the charge safety timer.

When MULT is pulled down to Vss and when VBAT exceeds V_{20} during charging, the 20% charge indication is activated and the timer begins counting for a period equal to 1/64 to 1/32 of the charge safety time-out period. When the timer count is completed, the 30% charge indication is activated. Should V_{BAT} exceed V_{40} prior to the timer count completion, the charge status monitor activates the 30% and 40% indications. This technique is used for all the odd percentage charge indications to assure a monotonic charge status display.

When MULT is pulled up to V_{CC}, the bq2007 charge status monitor directly displays 1/32 of the charge safety timer as a percentage of full charge. This method is recommended over the voltage-based method when charging multi-cell packs where the battery terminal voltages can vary greatly between packs. This method offers an accurate charge status indication when the battery is fully discharged.

During discharge with MULT pulled down to V_{SS}, the charge status monitor indicates the percentage of the battery voltage by comparing VBAT to the internal die-charge voltage reference thresholds. In BCD format, the discharge thresholds V80, V60, V40, and V20 correspond to a battery charge state indication of 90%, 70%, 50%, and 30%, respectively. In bargraph format, the same discharge thresholds correspond to a battery charge state indication of 90%, 60%, 40%, and 30%, respectively. Differences in the battery charge state indications are due to the finer granularity of the BCD versus the bargraph format.

During discharge and when MULT is pulled up to V_{CC}, the state-of-charge monitor segment format displays the discharge condition, letter "d," whereas the bargraph format has no indication.

The charge status display is blanked during the charge pending state and when the battery pack is removed.

Charge Status Display Modes

The bq2007 charge status monitor can be displayed in two modes summarized in Table 3. The display modes are a seven-segment monotonic bargraph or a seven-segment single-digit format. When QDSEL is pulled down to V_{SS}, pins SEG_{A-G} drive the decoded seven segments of a single segment digit display, and when QDSEL is pulled up to V_{CC}, pins SEG_{A-G} drive the seven segments of a bargraph display.

In the bargraph display mode, outputs SEG_{A-G} allow options for a three-segment to seven-segment bargraph display. The three-segment *charge* status display uses outputs SEG_B, SEG_D, and SEG_F for 30%, 60%, and 90% charge indications, respectively. The four-segment charge status display uses outputs SEG_A, SEG_C, SEG_D, and SEG_E for 20%, 40%, 60%, and 80% indications, respectively. The seven-segment charge status monitor uses all segments.

The segment display mode drives pins SEG_{A-G} with the decoded seven-segment single-digit information. The display indicates in 10% increments from a segment zero count at *charge* initiation to a segment nine count indicating 90% *charge* capacity. Charge completion is indicated by the letter "F," a fault condition by the letter "E," and the discharge condition by the letter "d." See Table 3.

Display Driver Modes

The bq2007 is designed to interface with LCD or LED type displays. The LED signal levels are driven when the MSEL input is pulled to V_{CC} at initialization. The output pin COM is the common anode connection for LED SEG_{A-G}.

The LCD interface mode is enabled when the MSEL input pin is pulled to V_{SS} at initialization. An internal oscillator generates all the timing signals required for the LCD interface. The output pin COM is the common connection for static direct-driving of the LCD display backplate and is driven with an AC signal at the frame period. When enabled, each of the SEG_{A-G} pins is driven with the correct-phase AC signal to activate the LCD segment. In segment mode, output pins SEG_{A-G} interface to LED or LCD segments.

Discharge Before Charge

It may be desirable in the application to allow the user to occasionally discharge the battery to a known voltage level prior to charge. The reason for this may either be to remedy a voltage-depression effect found in some NiCd batteries or to determine the battery's charge capacity.

Figure 3 illustrates the implementation of this function. Discharge-before-charge is initiated on a positive strobe signal on DCMD.

Note: This function takes precedence over a charge action and commences immediately when conditions warrant, forcing DIS to a high state until the voltage sensed on BAT falls below $V_{CC}/5$. Charging begins as soon as conditions allow.

Care should be taken not to overheat the battery during this process; excessive temperature is not a condition that terminates discharge.

Configuring the BAT Input

The bq2007 uses the battery voltage sense input on the BAT pin to control discharge-before-charge, qualify

charge initiation, terminate charge at an absolute limit, facilitate peak voltage detect (PVD) and negative delta voltage (-ΔV) detection, and detect a battery replacement.

V_{BAT} may be derived from a simple resistive network across the battery. As shown in Figure 1, resistors RB1 and RB2 are chosen to divide the battery voltage down to the optimal detection range. When MULT is pulled up to V_{CC}, battery voltage is sensed at the BAT pin by a resistive voltage divider that divides the terminal voltage between 0.262 • V_{CC} (V_{EDV}) and 0.8 • V_{CC} (V_{MCV}). The bq2007 charges multi-cell battery packs from a minimum of N cells, to a maximum of 1.5 • N cells. The battery voltage divider is set to the minimum cell battery pack (N) by the BAT pin voltage divider ratio equation:

$$\frac{R1}{R2} = \left(\frac{N}{1.33}\right) - 1 \qquad \text{Equation 1}$$

When MULT is pulled down to V_{SS}, tighter charge voltage limits and voltage-based charge status display are selected. This is recommended for charging packs with a fixed number of cells where the battery voltage divider range is between 0.4 • V_{CC} (V_{EDV}) and 0.8 • V_{CC} (V_{MCV}). The bq2007 charges fixed-cell battery packs of N cells. The battery voltage divider is set by the divider ratio equation:

$$\frac{R1}{R2} = \left(\frac{N}{2}\right) - 1 \qquad \text{Equation 2}$$

Although virtually any value may be chosen for RB1 and RB2 due to the high input impedance of the BAT pin, the values selected must not be so low as to appreciably drain the battery nor so large as to degrade the circuit's noise performance. Constraining the source resistance as seen from BAT between 20KΩ and 1MΩ is acceptable over the bq2007 operating range. Total impedance between the battery terminal and VSS should typically be about 300KΩ to 1MΩ. See Table 4.

Note: Because V_{SNS} may be positive in bq2007 switching regulation applications, the actual internal comparison uses $V_{BAT} - V_{SNS}$, or V_{CELL}. This internal value V_{CELL} maintains a representative voltage independent of any current through R_{SNS}.

Table 3. bq2007 Charge Status Display Summary

Mode	Display Indication	SEG_A	SEG_B	SEG_C	SEG_D	SEG_E	SEG_F	SEG_G
QDSEL = H	20% charge	1	0	0	0	0	0	0
	30% charge	1	1	0	0	0	0	0
	40% charge	1	1	1	0	0	0	0
	60% charge	1	1	1	1	0	0	0
	80% charge	1	1	1	1	1	0	0
	90% charge	1	1	1	1	1	1	0
	Charge complete	1	1	1	1	1	1	1
QDSEL = L	0% charge—digit 0	1	1	1	1	1	1	0
	10% charge—digit 1	0	1	1	0	0	0	0
	20% charge—digit 2	1	1	0	1	1	0	1
	30% charge—digit 3	1	1	1	1	0	0	1
	40% charge—digit 4	0	1	1	0	0	1	1
	50% charge—digit 5	1	0	1	1	0	1	1
	60% charge—digit 6	1	0	1	1	1	1	1
	70% charge—digit 7	1	1	1	0	0	1	0
	80% charge—digit 8	1	1	1	1	1	1	1
	90% charge—digit 9	1	1	1	1	0	1	1
	Charge complete—letter F	1	0	0	0	1	1	1
	Fault condition—letter E	1	0	0	1	1	1	1
	Discharge—letter d	0	1	1	1	1	0	1

Note: 1 = on; 0 = off; L = pulled down to VSS; H = pulled up to VCC.

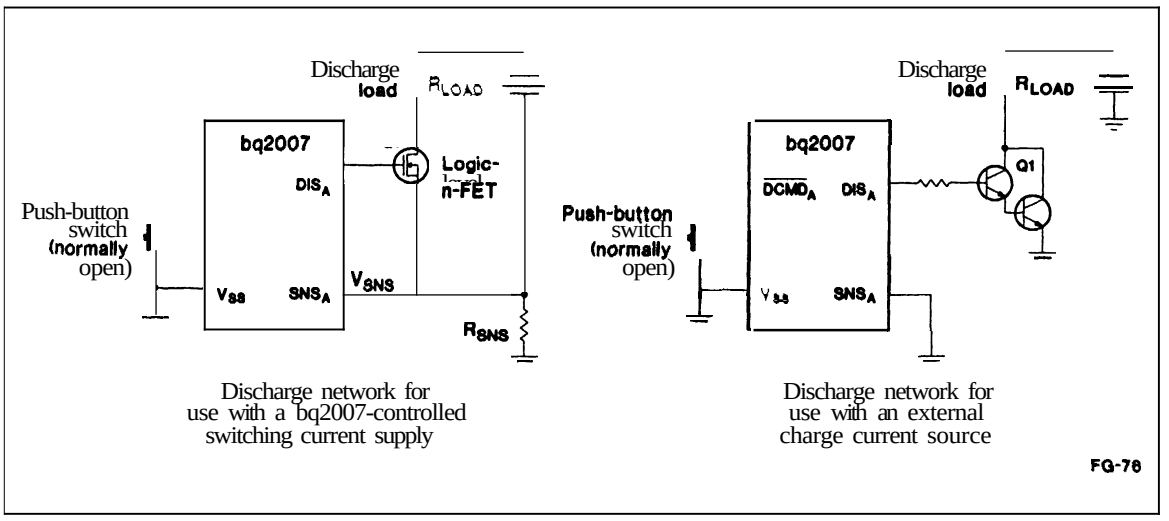


Figure 3. Battery Conditioning Network

Table 4. Suggested RB1 and RB2 Values for NiCd and NiMH Cells

Number of Cells (V_{BAT} Divisor)	RB1(KΩ)	RB2(KΩ)
4	150	165
5	150	110
6	150	80.6
8	150	53.6
10	150	40.2

Note: MULTI = 0; RB1/RB2 = (N/2) - 1.

Temperature Sensing and the TCO Pin

The bq2007 uses the temperature sense input on the TS pin to qualify charge initiation and termination. A negative temperature coefficient (NTC) thermistor referenced to SNS and placed in close proximity to the battery may be used as a temperature-to-voltage transducer as shown in Figure 1. This example shows a simple linearization network constituted by RT1 and RT2 in conjunction with the thermistor, RT.

Temperature-decision thresholds are defined as LTF (low-temperature fault) and TCO (temperature cutoff). Charge action initiation is inhibited if the temperature is not within the LTF-to-TCO range. In this case, the charge pending state is active on the charge status display (see Table 2), and charging does not initiate until the battery temperature returns to this range.

Once initiated, charging terminates if the temperature is either less than LTF or greater than TCO. The bq2007 interprets the reference points V_{LTF} and V_{TCO} as Vss-referenced voltages, with V_{LTF} fixed at ½ V_{CC} and V_{TCO} equal to the voltage presented on the TCO pin. See Figure 4. Note that since the voltage on pin TS decreases as temperature increases, V_{TCO} should always be less than ½ V_{CC}. The resistive dividers may be used to generate the desired V_{TCO}.

Vcc Supply

The Vcc supply provides both power and voltage reference to the bq2007. This reference directly affects BAT voltage and internal time-base voltage measurements.

The time-base is trimmed during manufacturing to within 5 percent of the typical value with V_{CC} = 5V. The oscillator varies directly with Vcc. If, for example, a 5% regulator supplies V_{CC}, the time-base could be in error by as much as 10%.

Charge State Actions

Once the required discharge is completed and temperature and voltage prequalifications are met, the charge state is initiated. The charge state is c o n f i i by the VSEL, FAST, and TM input p i . . The FAST input selects between Fast and Standard charge rates. The Standard charge rate is ¼ of the Fast charge rate, which is accomplished by disabling the regulator for a period of 286µs of every 1144µs (25% duty cycle). In addition to

Table 5. bq2007 Charge Action Control Summary

FAST Input State	TM Input State	Time-out Period (min)	MOD Duty Cycle	Hold-off period (sec)	Trickle Rep Rate -ΔV C/32	Trickle Rep Rate PVD C/64
Vss	Float	640 (C/8)	25%	2400	219Hz	109Hz
Vss	Vss	320 (C/4)	25%	1200	109Hz	55Hz
Vss	Vcc	160 (C/2)	25%	600	55Hz	27Hz
Vcc	Float	160 (C/2)	100%	600	219Hz	109Hz
Vcc	Vss	80 (C)	100%	300	109Hz	55Hz
Vcc	Vcc	40 (2C)	100%	150	55Hz	27Hz

throttling back the charge current, time-out and hold-off safety time are increased accordingly.

The VSEL input selects the voltage termination method. The termination mode sets the top-off state and trickle charge current rates. The TM input selects the Fast charge rate, the Standard rate, and the corresponding charge times. Once charging begins at the Fast or Standard rate, it continues until terminated by any of the following conditions:

- Negative delta voltage (-ΔV)
- Peak voltage detect (PVD)
- Maximum temperature cutoff (TCO)
- Maximum time-out (MTO)
- Maximum cutoff voltage (MCV)

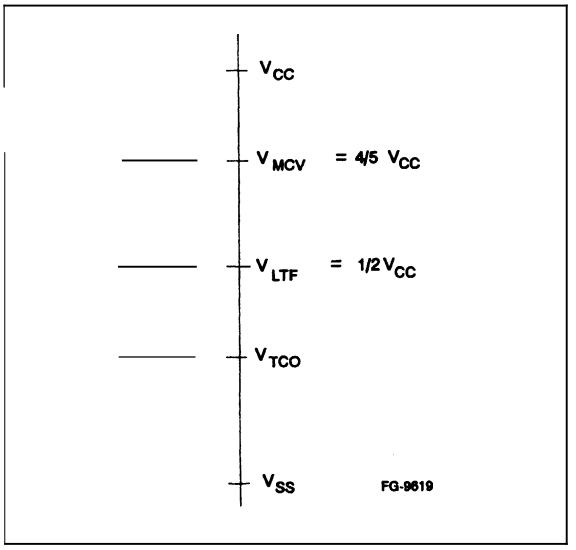


Figure 4. Temperature Reference Points

Voltage Termination Hold-off

To prevent early termination due to an initial false peak battery voltage, the -ΔV and PVD terminations are disabled during a short %old-off period at the start of charge. During the hold-off period when fast charge is selected (FAST = 1), the bq2007 will top off charge to prevent excessive overcharging of a fully charged-battery. Once past the initial charge hold-off time, the termination ie enabled. TCO and MCV terminations are not affected by the hold-off time.

-AV or PVD Termination

Table 6 summarizee the two modee for full-charge voltage termination detection. When VSEL = Vss, negative delta voltage detection occurs when the voltage seen on the BAT pin falls 12mV (typical) below the maximum sampled value. VSEL = Vcc selects peak voltage detect termination and the top-off charge state. When charging a battery pack with a fixed number of cells, the -ΔV and PVD termination thresholds are -6mV and 0 to -3mV per cell, respectively. The valid battery voltage range on V_{BAT} for -AV or W D termination is from 0.262 * VCC to 0.8• VCC.

Top-Off Charge

The top-off charge option allows for the self-discharge replacement trickle current to be very low, but still provides for filling up the last fraction of capacity after the fast-charge phase hae terminated Top-off occurs at 1/8 of the fast charge rate to prevent excess heat generation, and terminates after a period equal to the safety time-out. It also terminates if TCO or MCV is detected.

Top-off is not recommended in applications where a battery *charge* is re-initiated with extremely high frequency (many times per day); for example, when the unit is returned to the charge cradle after each short period of use.

Pulse trickle is used to compensate for self-discharge while the battery is idle and to condition a depleted low-voltage battery to a valid voltage prior to high-current charging. The battery is pulse trickle charged when Fast, Standard, or top-off charge is not active. This results in a trickle rate of C/64 for PVD and C/32 when -AV is enabled.

Table 6. VSEL Configuration

VSEL	Detection Method	Top-Off	Pulse Trickle Rate
V_{SS}	-AV	Disabled	C/32
V_{CC}	PVD	Enabled	C/64

Charge Inhibit

Fast charge, top-off, and pulse trickle may be inhibited by using the $\overline{INH}$ input pin. When low, the bq2007 suspends all charge activity, drives all outputs to high impedance, and assumes a low-power operational state. When $\overline{INH}$ returns high, a fast-charge cycle is qualified and begins as soon as conditions allow.

Power Supply Selection

The DC supply voltage, V_{DC}, must satisfy two requirements:

1. To support the bq2007 V_{CC} supply, V_{DC} must be adequate to provide for 5V regulation after the losses in the regulator and across D1 ($V_{DC} \geq 7.7V$ using the 78L05).
2. To support the charge operation, V_{DC} > (number of cells • MCV_{MAX}) + V_{LOSS} in the charging path. (MCV_{MAX} is the maximum cell voltage threshold with the maximum bq2007 V_{CC}.)

Polarity Reversal Protection

If the DC input has *any* risk of being accidentally connected with power (+) and ground (–) reversed, then the system input should include either a protection diode to protect against circuit damage or a diode bridge to provide both protection and operation. This also increases minimum input voltage for charger operation by approximately 1V to 2V.

Layout Guidelines

PCB layout to minimize the impact of system noise on the bq2007 is important when the bq2007 is used as a switching modulator, with a separate nearby switching regulator, or close to any other significant noise source.

1. Avoid mixing signal and power grounds by using a single-point ground technique incorporating both a small signal ground path and a power ground path.
2. The charging path components and associated traces should be kept relatively isolated from the bq2007 and its supporting components.
3. 0.1µF and 10µF decoupling capacitors should be placed close together and very close to the V_{CC} pin.
4. 0.1µF capacitors and resistors forming R·C filters connected to pins BAT, TS, TCO, and MCV should be as close as possible to their associated pins.
5. Because the bq2007 uses V_{CC} for its reference, additional loading on V_{CC} is not recommended.
6. Diode D1 (1N4148) is recommended for rectification and filtering.
7. If the DCMD input is electronically controlled, care should be taken to prevent noise-induced false transitions.
8. For bq2007-modulated switching applications:

   A 2KΩ resistor is required between the MOD pin and the transistor.

   - A 1000pF capacitor/1KΩ resistor R·C filter should be as close as possible to the SNS pin.
   - The 0.1µF capacitors for BAT and TS should be routed directly to SNS and not to ground.

Figures 6, 7, and 8 show an example layout of the DV2007S1 Development Board. Figure 9 is a schematic of the board. Table 7 contains the parts list for the board. A comparable layout is recommended.

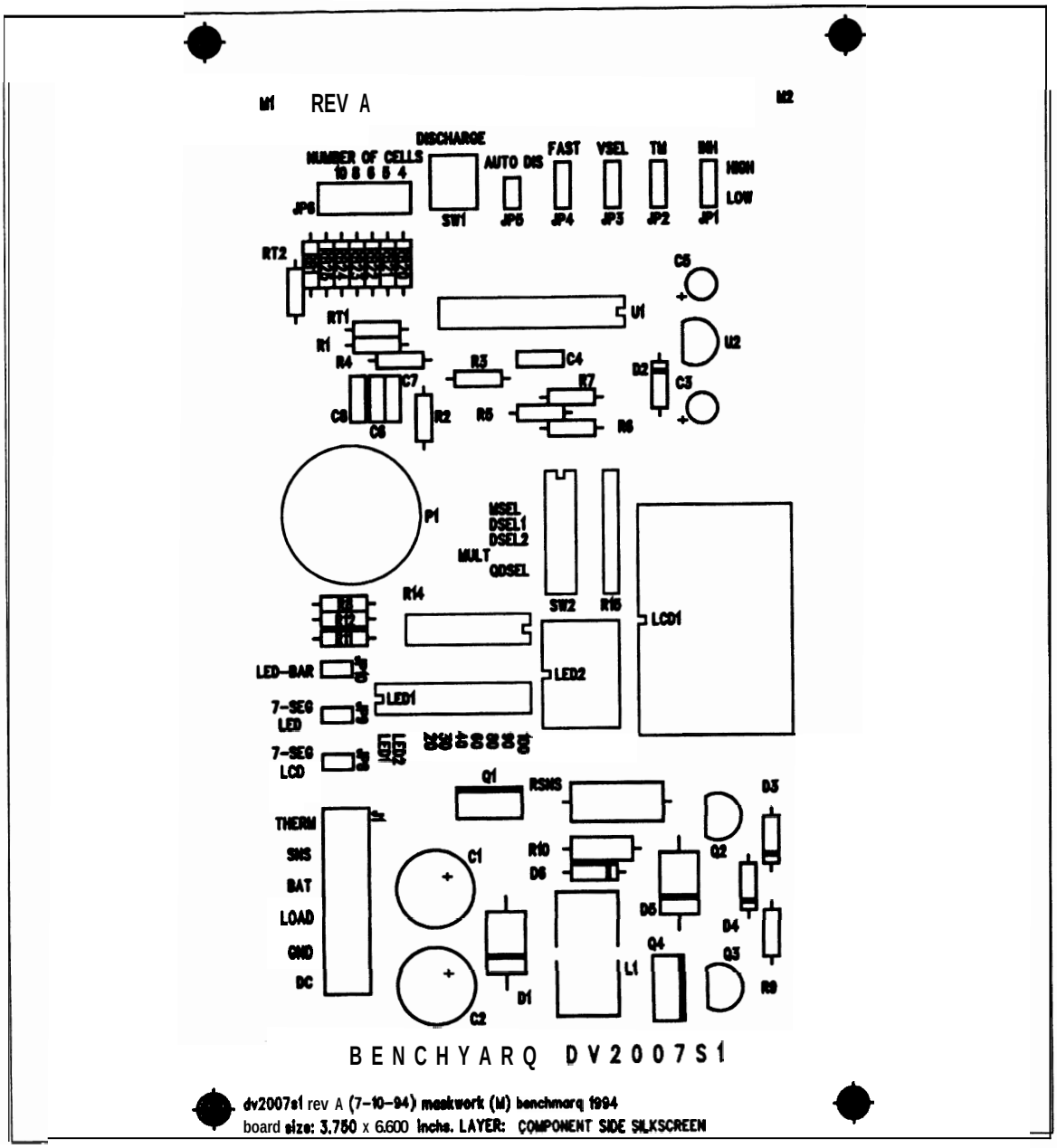


Figure 6. DV2007S1 Development Board Layout

Component Placement

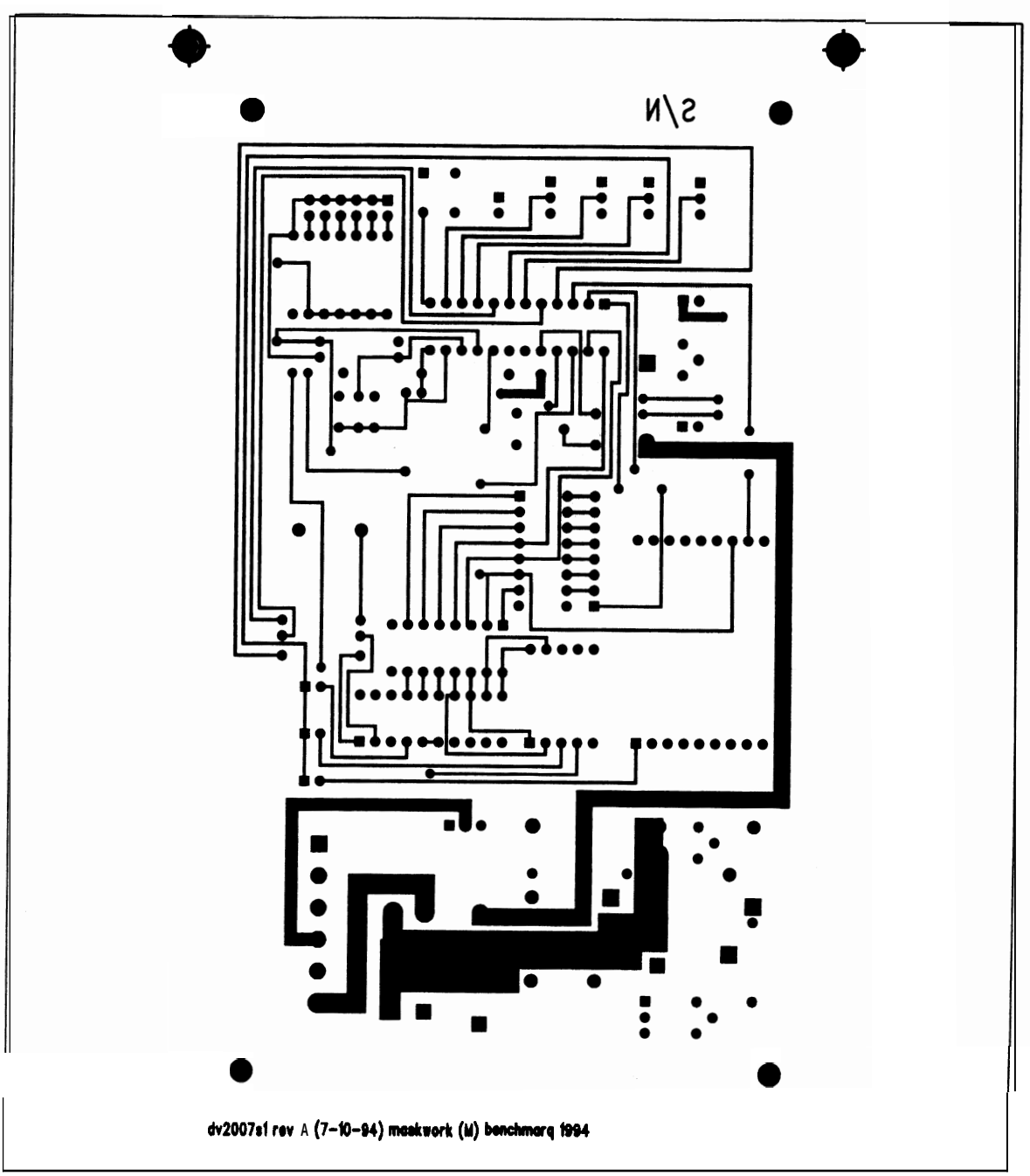


Figure 7. DV2007S1 Development Board Layout

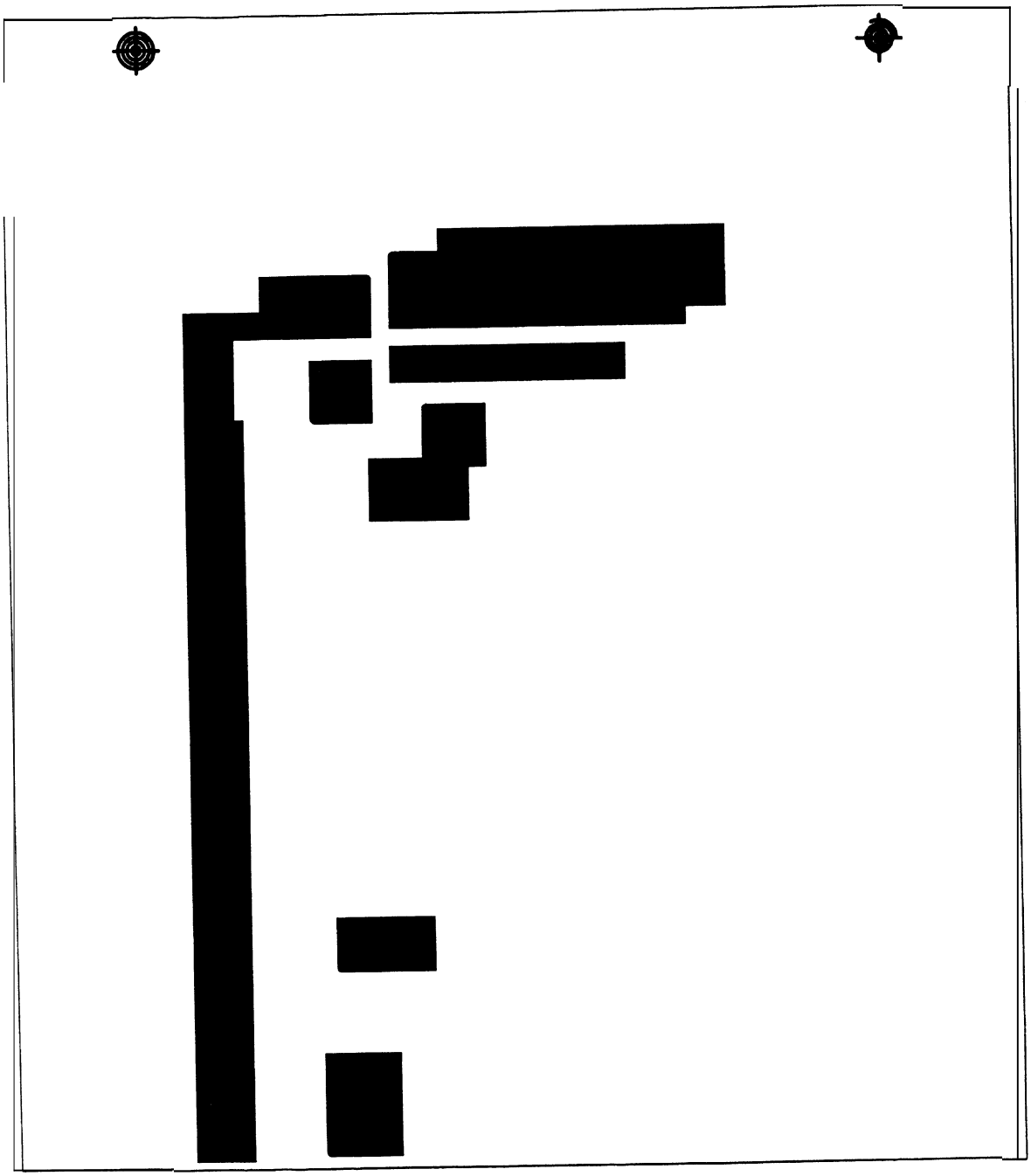


Figure 8. DV2007S1 Development Board Layout

Table 7. DV2007S1 Development Board Parts List

Component Name	Component Description
C2, C1– Optional	1000µF
C5, C3	100µF
C4, C6, C7	0.1µF
C8	1nF
D1	1N5400
D4, D2	1N4148
D3	1N751A
D5	1N5821
D6	1N4001
JP1, JP2, JP3, JP4	HEADER 3
JP5, JP8, JP9, JP10	HEADER 2
J1	CON6
LCD1	7-SEG LED
LED1	LED BAR
LED2	7-SEG LCD
L1	100µH
P1	BUZZER
Q1	MTP3055EL
Q2	2N7000
Q3	2N3904
Q4	MTP23P06E
R14	Resistor 8pack
RB1	150K
RB2X	User Selected
RSNS	0.2
RT1	20K
RT2	Open
R1	300K
R6, R7	100K
R2, R5, R10	2K
R3	82K
R4	20K
R8	20K
R9	6.8K
R12, R11	510
SR	SIP8
SW1	SW pushbutton
SW2	SW DIP-8
U1	bq2007
u 2	78L05

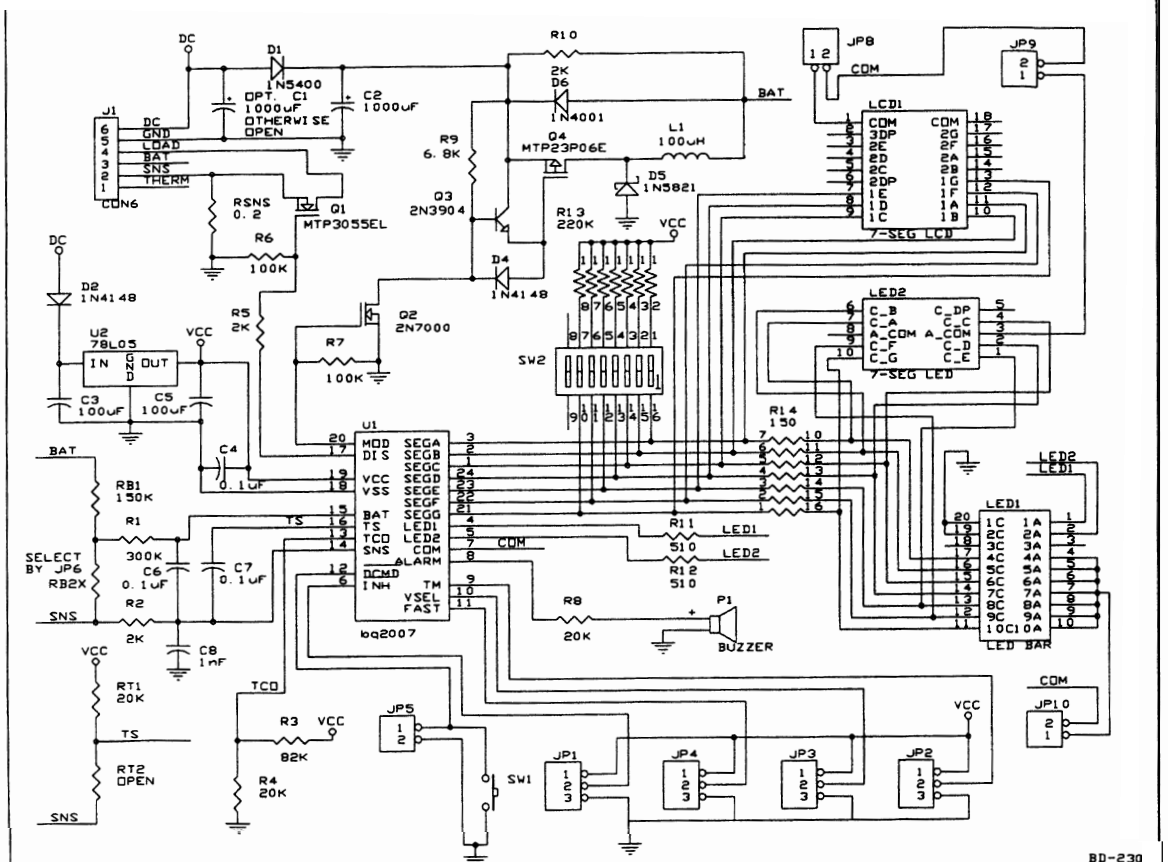


Figure 9. DV2007S1 Development Board Schematic

bq2031

Lead-Acid Fast Charge IC

Features

- Conforms to battery manufacturers' charge recommendations for cyclic and float charge
- Pin selectable charge algorithms
  - Two-Step Voltage with temperature-compensated constant-voltage maintenance
  - Two-Step Current with constant-rate pulsed current maintenance
  - Pulsed Current: hysteretic, on-demand pulsed current
- Pin-selectable charge termination by maximum voltage, Δ^2V, minimum current, and maximum time
- Pre-charge qualification detects shorted, opened, or damaged cells and conditions battery
- Charging continuously qualified by temperature and voltage limits
- Internal temperature-compensated voltage reference
- Pulse-width modulation control
  - Ideal for high-efficiency switch-mode power conversion
  - Configurable for linear or gated current use
- Direct LED control outputs display charge statue and fault conditions

General Description

The bq2031 Lead-Acid Fast Charge IC is designed to optimize charging of lead-acid chemistry batteries. A flexible pulse-width modulation regulator allows the bq2031 to control constant-voltage, constant-current, or pulsed-current charging. The regulator frequency is set by an external capacitor for design flexibility. The switch-mode design keeps power dissipation to a minimum for high charge current applications.

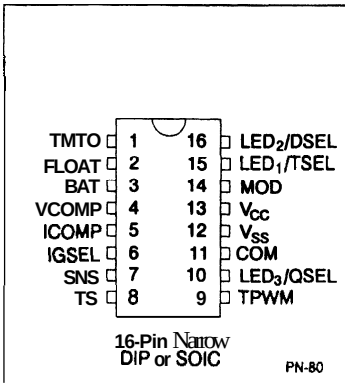
A charge cycle begins when power is applied or the battery is replaced. For safety, charging is inhibited until the battery voltage is within configured limits. If the battery voltage is less than the low-voltage threshold, the bq2031 provides trickle-current charging until the voltage rises into the allowed range or an internal timer runs out and places the bq2031 in a Fault condition. This procedure prevents high-current charging of cells that are possibly damaged or reversed. Charging is inhibited anytime the temperature of the battery is outside the configurable, allowed range. All voltage thresholds are temperature-compensated.

The bq2031 terminates fast (bulk) charging based on the following:

- Maximum voltage
- Second difference of cell voltage (Δ^2V)
- Minimum current (in constant-voltage charging)
- Maximum time-out (MTO)

After bulk charging, the bq2031 provides temperature-compensated maintenance (float) charging to maintain battery capacity.

Pin Connections



16-Pin Narrow DIP or SOIC

PN-80

Pin Names

TMTO	Time-out timebase input	LED_3/QSEL	Charge status output 3/ Charge algorithm select input1
FMAT	State control output		
BAT	Battery voltage input	COM	Common LED output
VCOMP	Voltage loop comp input	Vss	System ground
ICOMP	Current loop comp input	Vcc	5.0V±10% power
IGSEL	Current gain select input	MOD	Modulation control output
SNS	Sense resistor input	LED_1/TSEL	Charge status output 1/ Charge algorithm select input 2
TS	Temperature sense input		
TPWM	Regulator timebase input	LED_2/DSEL	Charge status output 2/ Display select input

Pin Descriptions

TMTO Time-out timebase input

This input sets the maximum charge time. The resistor and capacitor values are determined using equation 6. Figure 9 shows the resistor/capacitor connection.

FLOAT Float state control output

This open-drain output uses an external resistor divider network to control the BAT input voltage threshold (V_{FLT}) for the float charge regulation. See Figure 1.

BAT Battery voltage input

BAT is the battery voltage sense input. This potential is generally developed using a high-impedance resistor divider network connected between the positive and the negative terminals of the battery. See Figure 6 and equation 2

VCOMP Voltage loop compensation input

This input uses an external C or R-C network for voltage loop stability.

IGSEL Current gain select input

This three-state input is used to set I_{MIN} for fast charge termination in the Two-Step Voltage algorithm and for maintenance current regulation in the Two-Step Current algorithm. See Tables 3 and 4.

ICOMP Current loop compensation input

This input uses an external C or R-C network for current loop stability.

SNS Charging current sense input

Battery current is sensed via the voltage developed on this pin by an external sense resistor, R_{SNS}, connected in series with the low side of the battery. See equation 8.

TS Temperature sense input

This input is for an external battery temperature monitoring thermistor or probe. An external resistor divider network sets the lower and upper temperature thresholds. See Figures 7 and 8 and equations 4 and 5.

TPWM Regulation timebase input

This input uses an external timing capacitor to ground the pulse-width modulation (PWM) frequency. See equation 9.

COM Common LED output

Common output for LED_{1-3}. This output is in a hiih-impedance state during initialization to read program inputs on TSEL, QSEL, and DSEL

QSEL Charge regulation select input

With TSEL, selects the charge algorithm. See Table 1.

MOD Current-switching control output

MOD is a pulse-width modulated push/pull output that is used to control the charging current to the battery. MOD switches high to enable current flow and low to inhibit current flow.

LED_{1-3} Charger display status 1 3 outputs

These charger statue output drivers are for the direct drive of the LED display. Display modes are shown in Table 2. These outputs are tri-stated during initialization so that QSEL, TSEL, and DSEL can be read.

DSEL Display select input

This three-level input controls the LED_{1-3} charge display modes. See Table 2.

TSEL Termination select input

With QSEL, selects the charge algorithm. See Table 1.

V_{CC} Vcc supply

5.0V, ± 10% power

Vss Ground

Functional Description

The bq2031 functional operation is described in terms of:

- Charge algorithms
- Charge qualification
- Charge status display
- Voltage and current monitoring
- Temperature monitoring

- Fast charge termination
- Maintenancecharging
- Charge regulation

Charge Algorithms

Three charge algorithms are availablein the **bq2031:**

- Two-Step Voltage
- Two-Step Current
- **Pulsed Current**

The state **transitions** for these algorithms are **described** in Table 1 and are shown graphically in Figures 2 through 4. The **user selects** a charge algorithm by configuring pins QSEL and TSEL.

Charge Qualification

The **bq2031 starts** a **charge** cycle when power is applied while a battery is present or when a battery is inserted. **Figure 1 shows** the state diagram for pre-charge qualification and temperature monitoring. The **bq2031** first checks that the battery temperature is within the allowed, **user-configurable** range. If the temperature is out-of-range (or the thermistor is **missing),** the **bq2031 enters** the Charge Pending state and waits until the **bat-**

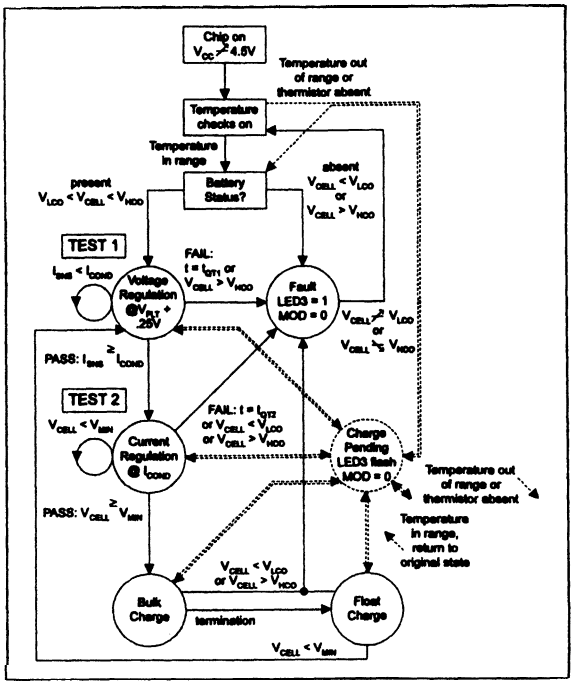


Figure 1. Cycle Start/Battery Qualification State Diagram

Table 1. bq2031 Charging Algorithms

Algorithm/State	QSEL	TSEL	Conditions	MOD Output
Two-Step Voltage	L	H/L[Note 1]	-	-
Fast charge, phase 1			while $V_{BAT} < V_{BLK}$, $I_{SNS} = I_{MAX}$	Current regulation
Fast charge, phase 2			while $I_{SNS} > I_{MIN}$, $V_{BAT} = V_{BLK}$	Voltage regulation
Primary termination			$I_{SNS} = I_{MIN}$	
Maintenance			$V_{BAT} = V_{FLT}$	Voltage regulation
Two-Step Current	H	L	-	-
Fast charge			while $V_{BAT} < V_{BLK}$, $I_{SNS} = I_{MAX}$	Current regulation
Primary termination			$V_{BAT} = V_{BLK}$ or $\Delta^2V < -8mV$[Note 2]	
Maintenance			I_{SNS} pulsed to average I_{FLT}	Fixed pulse current
Pulsed Current	H	H	-	-
Fast charge			while $V_{BAT} < V_{BLK}$, $I_{SNS} = I_{MAX}$	Current regulation
Primary termination			$V_{BAT} = V_{BLK}$	
Maintenance			$I_{SNS} = I_{MAX}$ after $V_{BAT} = V_{FLT}$; $I_{SNS} = 0$ after $V_{BAT} = V_{BLK}$	Hysteretic pulsed current

Notes: 1. May be high or low, but do not float.

2. A **Benchmarq** proprietary algorithm for accumulating **successive** differences between **samples** of V_{BAT}.

tery temperature is within the allowed range. Charge Pending is annunciated by LED_3 flashing.

Thermal monitoring continues throughout the charge cycle, and the bq2031 enters the Charge Pending state anytime the temperature is out of range. (There is one exception; if the bq2031 is in the Fault state—see below—the out-of-range temperature is not recognized until the bq2031 leaves the Fault state.) All timers are suspended (but not reset) while the bq2031 is in Charge Pending. When the temperature comes back into range, the bq2031 returns to the point in the charge cycle where the out-of-range temperature was detected.

When the temperature is valid, the bq2031 performs two tests on the battery. In test 1, the bq2031 regulates a voltage of V_{FLT} + 0.25V across the battery and observes I_{SNS}. If I_{SNS} does not rise to at least I_{COND} within a time-out period (e.g., the cell has failed open), the bq2031 enters the Fault state. If test 1 passes, the bq2031 then regulates current to I_{COND} (= I_{MAX}/5) and watches V_{CELL} (= V_{BAT} - V_{SNS}). If V_{CELL} does not rise to at least V_{FLT} within a time-out period (e.g., the cell has failed short), again the bq2031 enters the Fault state. A hold-off period is enforced at the beginning of qualification test 2 before the bq2031 recognizes its "pass" criterion. If this second test passes, the bq2031 begins fast (bulk) charging.

Once in the Fault state, the bq2031 waits until V_{CC} is cycled or a battery insertion is detected. It then starts a new charge cycle and begins the qualification process again.

Charge Status Display

Charge status is annunciated by the LED driver outputs LED_1–LED_3. Three display modes are available in the bq2031; the user selects a display mode by configuring pin DSEL. Table 2 shows the three modes and their programming pins.

The bq2031 does not distinguish between an over-voltage fault and a "battery absent" condition. The bq2031 enters the Fault state, annunciated by turning on LED_3, when-

Table 2. bq2031 Display Output Summary

Mode	Charge Action State	LED_1	LED_2	LED_3
DSEL = 0 (Mode 1)	Battery absent or over-voltage fault	Low	Low	High
	Pre-charge qualification	Flash	Low	Low
	Fast charging	High	Low	Low
	Maintenance charging	Low	High	Low
	Charge pending (temperature out of range)	X	X	Flash
	Charging fault	X	X	High
DSEL = 1 (Mode 2)	Battery absent or over-voltage fault	Low	Low	High
	Pre-charge qualification	High	High	Low
	Fast charge	Low	High	Low
	Maintenance charging	High	Low	Low
	Charge pending (temperature out of range)	X	X	Flash
	Charging fault	X	X	High
DSEL = Float (Mode 3)	Battery absent or over-voltage fault	Low	Low	High
	Pre-charge qualification	Flash	Flash	Low
	Fast charge: current regulation	Low	High	Low
	Fast charge: voltage regulation	High	High	Low
	Maintenance charging	High	Low	Low
	Charge pending (temperature out of range)	X	X	Flash
	Charging fault	X	X	High

Notes: 1 = V_{CC}; 0 = V_{SS}; X = LED state when fault occurred; Flash = ⅙ s low, ⅙ s high.
In the Pulsed Current algorithm, the bq2031 annunciates maintenance when charging current is off and fast charge whenever charging current is on.

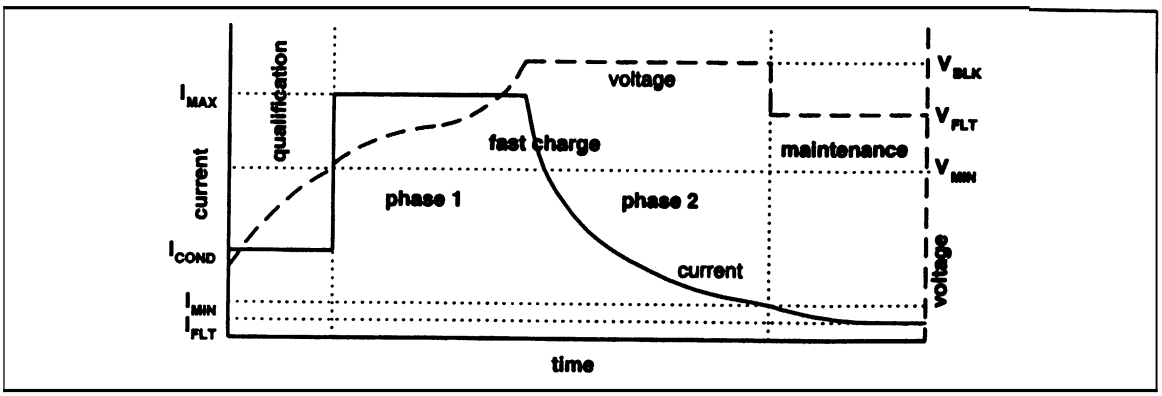


Figure 2. Two-Step Voltage Algorithm

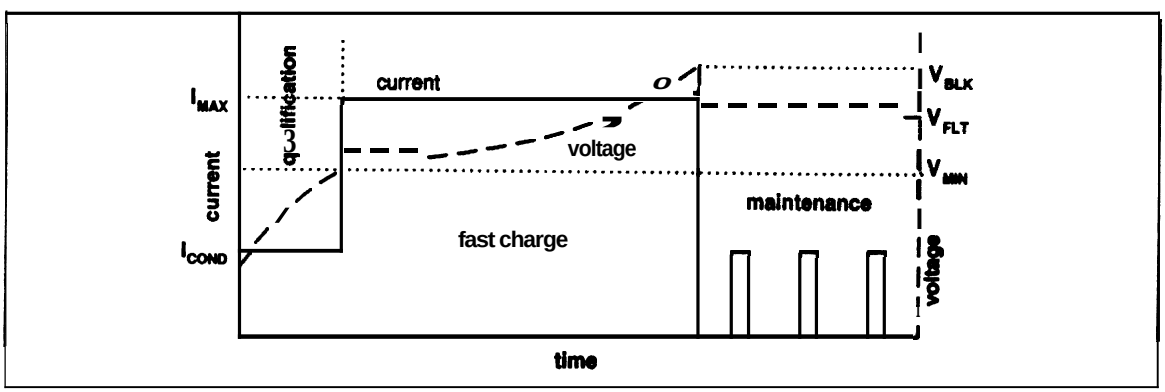


Figure 3. Two-Step Current Algorithm

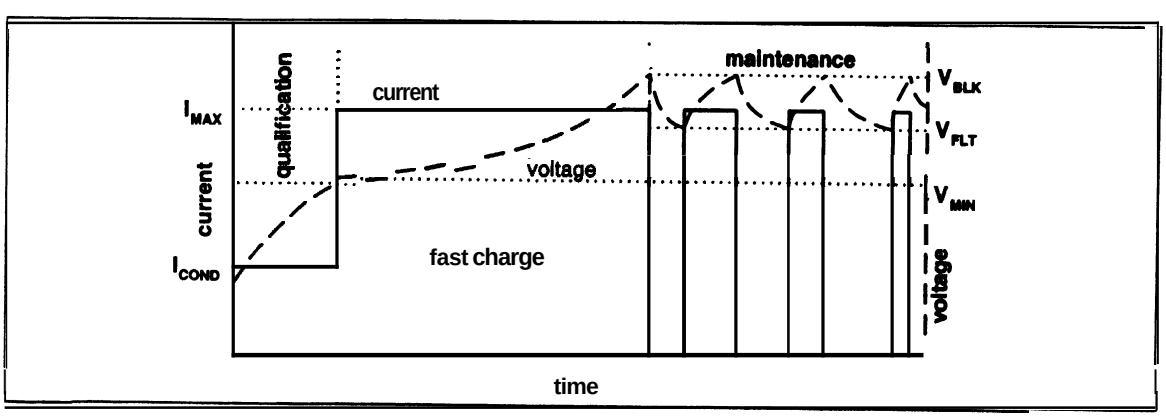


Figure 4. Pulsed Current Algorithm

ever the battery is absent. The bq2031, therefore, gives an indication that the charger is on even when no battery is in place to be charged.

Configuring Algorithm and Display Modes

QSEL/LED3, DSEL/LED2, and TSEL/LED1 are bi-directional pins with two functions; they are LED driver pine as outputa and programming pins for the bq2031 as inputs. The selection of pull-up, pull-down, or no pull resistor programs the charging algorithm on QSEL and TSEL per Table 1 and the display mode on DSEL per Table 2. The bq2031 latches the program states when any of the following eventa occurs:

1. V_{CC} rises to a valid level.
2. The bq2031 leaves the Fault state.
3. The bq2031 detects battery insertion.

The LEDs will go blank for approximately 750ms (typical) while new programming data is latched.

For example, Figure 5 shows the bq2031 configured for the Pulsed Current algorithm and display mode 2.

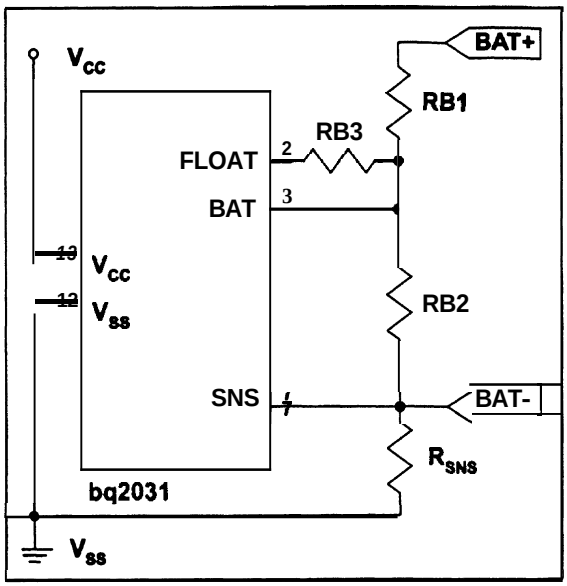


Figure 6. Configuring the Battery Divider

Voltage and Current Monitoring

The bq2031 monitors battery pack voltage at the BAT pin. A voltage divider between the positive and negativeterminals of thebattery packisused topresent a scaled battery pack voltage to the BAT pin and an appropriate value for regulation of float (maintenance) voltage to the FLOAT pin. The bq2031 also uses the volt-

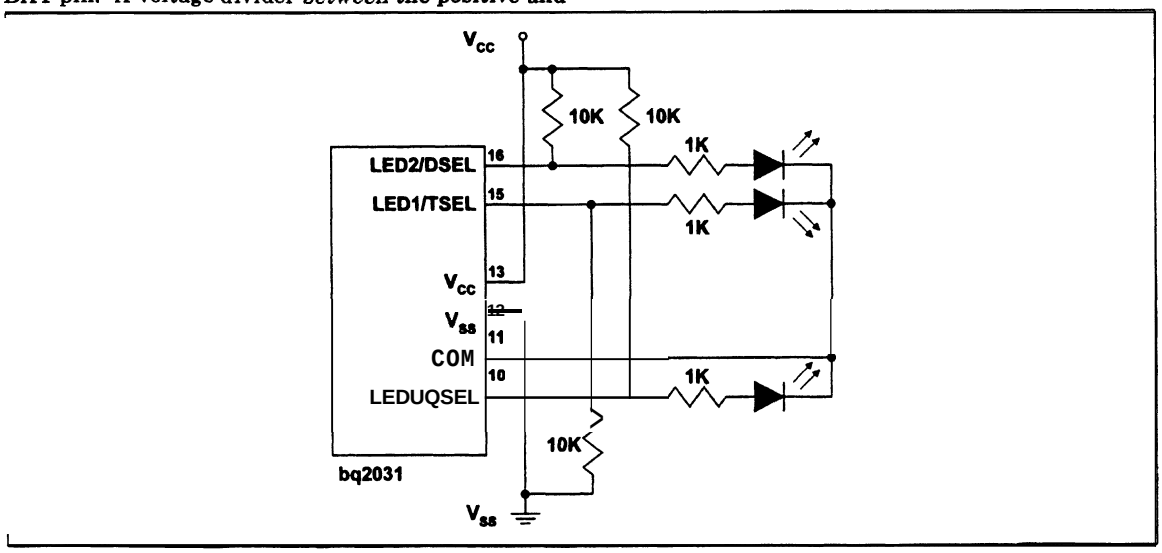


Figure 5. Configuring Charging Algorithm and Display Mode

ageacross a sense resistor (R_{SNS}) between the negative terminal of the battery pack and ground to monitor current. *See* Figure 6 for the configuration of this network.

The resistor valuee are calculated from the following:

Equation 1

$$\frac{RB1}{RB2} = \frac{(N * V_{FLT})}{2.2V} - 1$$

Equation 2

$$\frac{RB1}{RB2} = \frac{RB1}{RB3} = \left(\frac{* V_{BLK}}{2.2}\right) - 1$$

Equation 3

$$I_{MAX} = \frac{0.275V}{R_{SNS}}$$

where:

- N = Number of cells
- V_{FLT} = Desired float voltage
- V_{BLK} = Desired bulk charging voltage
- I_{MAX} = Desired maximum charge current

These parameters are typically specified by the battery manufacturer. The total resistance presented across the battery pack by RB1 + RB2 should be between 150kΩ and 1MΩ.. The minimum value ensures that the divider network does not drain the battery excessively when the power source is disconnected. Exceeding the maximum value increases the noise susceptibility of the BAT pin.

An empirical procedure for setting the valuee in the resistor network is as follows:

1. Set RB2 to 49.9 kΩ. (for 3 to 18 series cells)
2. Determine RB1 from equation 1 given V_{FLT}
3. Determine RB3 from equation 2 given V_{BLK}
4. Calculate R_{SNS} from equation 3 given I_{MAX}

Battery Insertion and Removal

The bq2031 uses V_{BAT} to detect the presence or absence of a battery. The bq2031 determines that a battery is present when V_{BAT} is between the High-Voltage Cutoff (V_{HCO} = 0.6 • V_{CC}) and the Low-Voltage Cutoff (V_{LCO} = 0.8V). When V_{BAT} is outside this range, the bq2031 determines that no battery is present and transitions to the Fault state. Transitions into and out of the range between V_{LCO} and V_{HCO} are treated as battery insertions and removals, respectively. Besides being used to detect battery insertion, the V_{HCO} limit implicitly serves as an over-voltage *charge* termination, because exceeding this limit causes the bq2031 to believe that the battery has been removed.

The user must include a pull-up resistor from the positive terminal of the battery stack to VDC (and a diode to prevent battery discharge through the power eupply when the eupply is turned off)in order to detect battery removal during periods of voltage regulation. Voltage regulation occurs in pre-charge qualification test 1 prior to all of the fast charge algorithms, and in phase 2 of the Two-Step Voltage fast charge algorithm.

Temperature Monitoring

The bq2031 monitors temperature by examining the voltage presented between the TS and SNS pine (V_{TEMP}) by a resistor network that includes a Negative Temperature Coefficient (NTC) thermistor. Resistance variations around that value are interpreted as being proportional to the battery temperature (see Figure 7).

The temperature thresholds used by the bq2031 and their corresponding TS pin voltage are:

- TCO—Temperature cutoff—Higher limit of the temperature range in which charging is allowed. V_{TCO} = 0.4 • V_{CC}

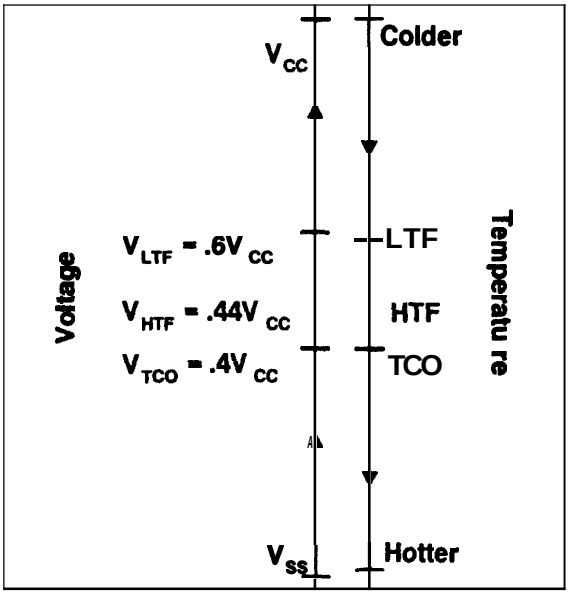


Figure 7. Voltage Equivalent of Temperature Thresholds

- HTF — High-temperature fault—Threshold to which temperature must drop after temperature cutoff is exceeded before charging can begin again. V_{HTF} = 0.44 • Vcc
- LTF—Low-temperature fault—Lower limit of the temperature range in which charging is allowed. V_{LTF} = 0.6 • Vcc

A resistor divider network must be implemented that presents the defined voltage levels to the TS pin at the desired temperatures (see Figure 8).

The equations for determining RT1 and RT2 are:

Equation 4

$$0.6 * V_{CC} = \frac{(V_{CC} - 0.275)}{1 + \frac{RT1 * (RT2 + R_{LTF})}{(RT2 * R_{LTF})}}$$

Equation 5

$$0.44 = \frac{1}{1 + \frac{RT1 * (RT2 + R_{HTF})}{(RT2 * R_{HTF})}}$$

where:

- R_{LTF} = thermistor resistance at LTF

  R_{HTF} = thermistor resistance at HTF

TCO is determined by the values of RT1 and RT2. 1% resistors are recommended.

Disabling Temperature Sensing

Temperature sensing can be disabled by removing RT and using a 100kΩ resistor for RT1 and RT2.

Temperature Compensation

The internal voltage reference used by the bq2031 for all voltage threshold determinations is compensated for temperature. The temperature coefficient is -3.9mV/°C, normalized to 25°C. Voltage thresholds in the bq2031 vary by this proportion as ambient conditions change.

Fast Charge Termination

Fast charge termination criteria are programmed with the fast charge algorithm per Table 1. Note that not all criteria are applied in all algorithms.

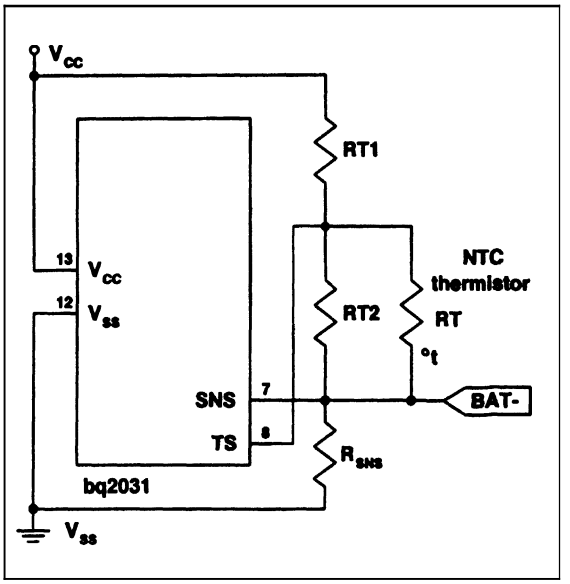


Figure 8. Configuring Temperature Sensing

Minimum Current

Fast charge terminates when the charging current drops below a minimum current threshold programmed by the value of IGSEL (see Table 3). This is used by the Two-Step Voltage algorithm.

Table 3. I_{MIN} Termination Thresholds

IGSEL	I_{MIN}
0	I_{MAX}/10
1	I_{MAX}/20
Z	I_{MAX}/30

Second Difference (Δ^2V)

Second difference is a Benchmarq proprietary algorithm that accumulates the difference between successive samples of V_{BAT}. The bq2031 takes a sample and makes a termination decision at a frequency equal to 0.008 • t_{MTO}. Fast charge terminates when the accumulated difference is ≤ -8mV. Second difference is used only in the Two-Step Current algorithm, and is subject to a hold-off period (see below).

Maximum Voltage

Fast charge terminates when $V_{CELL} \geq V_{BLK}$. V_{BLK} is set per equation 2. Maximum voltage is used for fast charge termination in the Two-Step Current and Pulsed Current algorithms, and for transition from phase 1 to phase 2 in the Two-Step Voltage algorithm. This criterion is subject to a hold-off period.

Hold-off Periods

Maximum V and Δ^2V termination criteria are subject to a hold-off period at the start of fast charge equal to 0.15 • t_{MTO}. During this time, these termination criteria are ignored.

Maximum Time-Out

Fast charge terminates if the programmed MTO time is reached without some other termination shutting off fast charge. MTO is programmed from 1 to 24 hours by an R-C network on TMTO (see Figure 9) per the equation:

Equation 6

$$t_{MTO} = 0.5 \cdot R \cdot C$$

where R is in kΩ, C is in µF, and t_{MTO} is in hours. Typically, the maximum value for C of 0.1µF is used.

Fast charge termination by MTO is a Fault only in the Pulsed Current algorithm; the bq2031 enters the Fault state and waits for a new battery insertion, at which time it begins a new charge cycle. In the Two-Step Voltage and Two-Step Current algorithms, the bq2031 transitions to the maintenance phase on MTO time-out.

The MTO timer starts at the beginning of fast charge. In the Two-Step Voltage algorithm, it is cleared and restarted when the bq2031 transitions from phase 1 (current regulation) to phase 2 (voltage regulation). The MTO timer is suspended (but not reset) during the out-of-range temperature (Charge Pending) state.

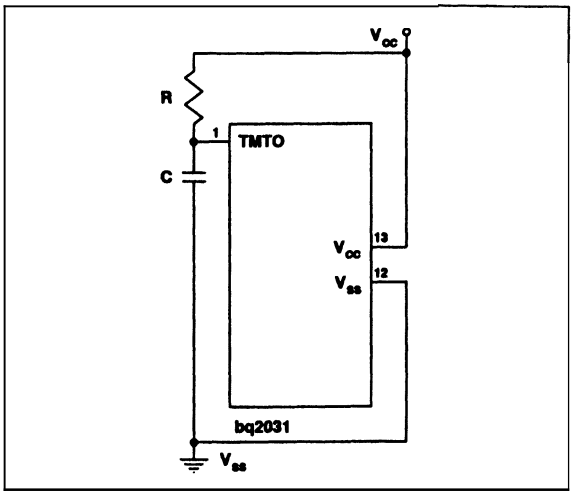


Figure 9. R-C Network for Setting MTO

Maintenance Charging

Three algorithms are used in maintenance charging:

- Two-Step Voltage algorithm
- Two-Step Current algorithm
- Pulsed Current algorithm

Two-Step Voltage Algorithm

In the Two-Step Voltage algorithm, the bq2031 provides charge maintenance by regulating charging voltage to V_{FLT}. Charge current during maintenance is limited to I_{COND}.

Two-Step Current Algorithm

Maintenance charging in the Two-Step Current Algorithm is implemented by varying the period (T_P) of a fixed current ($I_{COND} = I_{MAX}/5$) and duration (0.2 seconds) pulse to achieve the configured average maintenance current value. See Figure 10.

Maintenance current can be calculated by:

Equation 7

$$\text{Maintenance current} = \frac{((0.2) * I_{COND})}{T_P} - \frac{((0.04) * I_{MAX})}{T_P}$$

where T_P is the period of the waveform in seconds.

Table 4 gives the values of P programmed by IGSEL.

Table 4. Fixed-Pulse Period by IGSEL

IGSEL	T_P (sec.)
L	0.4
H	0.8
Z	1.6

Pulsed Current Algorithm

In the Pulsed Current algorithm, charging current is turned off after the initial fast charge termination until V_{CELL} falls to V_{FLT}. Full fast charge current (I_{MAX}) is then re-enabled to the battery until V_{CELL} rises to V_{BLK}. This cycle repeats indefinitely.

Charge Regulation

The bq2031 controls charging through pulse-width modulation of the MOD output pin, supporting both constant-current and constant-voltage regulation. Charge current is monitored by the voltage at the SNS pin, and charge voltage by voltage at the BAT pin. These voltages are compared to an internal temperature-compensated reference, and the MOD output modulated to maintain the desired value.

Voltage at the SNS pin is determined by the value of resistor R_{SNS}, so nominal regulated current is set by:

Equation 8

$$I_{MAX} = 0.275V/R_{SNS}$$

The switching frequency of the MOD output is determined by an external capacitor (CPWM) between the pin TPWM and ground, per the following:

Equation 9

$$F_{PWM} = 0.1/C_{PWM}$$

where C is in µF and F is in kHz. A typical switching rate is 100kHz, implying C_{PWM} = 0.001µF. MOD pulse width is modulated between 0 and Woof the *switching* period.

To prevent oscillation in the voltage and current control loop, frequency compensation networks (C or R-C) are typically required on the VCOMP and ICOMP pine (respectively) to add poles and zeros to the loop control equations. A software program, "CNFG2031," is available to assist in configuring these networks for buck type regulators. For more detail on the control loop in buck topology, see the application note, "Compensating the bq2031 in Buck-Mode Switching Applications.' For assistance with other power supply topologies, contact the factory.

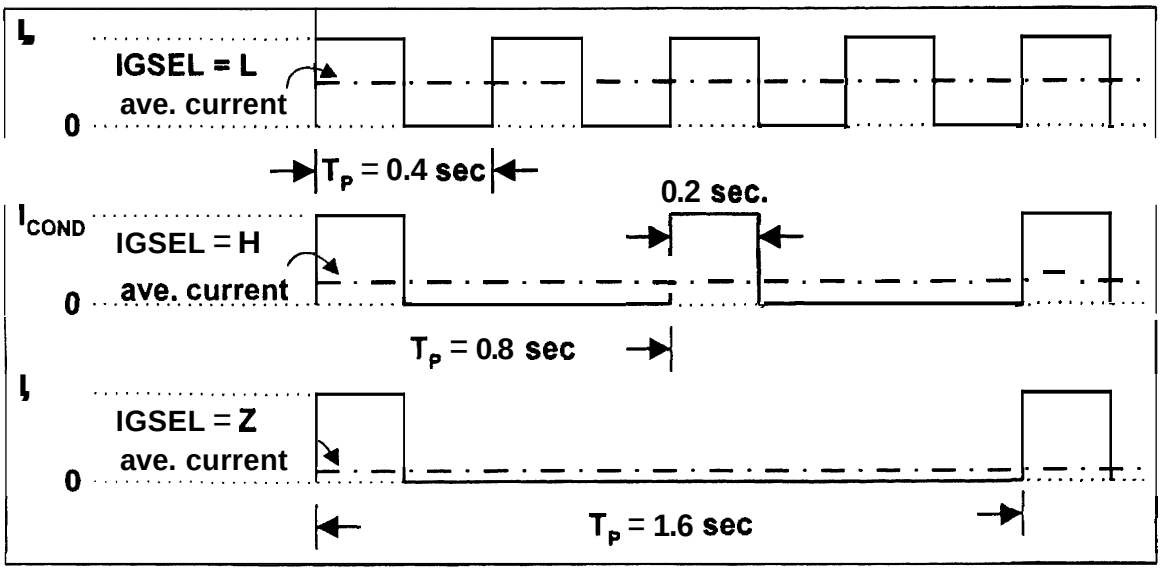


Figure 10. Implementation of Fixed-Pulse Maintenance Charge

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	V_{CC} relative to V_{SS}	-0.3	+7.0	V	
V_T	DC voltage applied on any pin excluding Vcc relative to Vss	-0.3	+7.0	V	
T_{OPR}	Operating ambient temperature	-20	+70	°C	Commercial
		-40	+85	°C	Industrial "N"
T_{STG}	Storage temperature	-55	+125	°C	
T_{SOLDER}	Soldering temperature		+260	°C	10 s. max.
T_{BIAS}	Temperature under bias	-40	+85	°C	

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds ($T_A = T_{OPR}$; V_{CC} = 5V ±10%)

Symbol	Parameter	Rating	Unit	Tolerance	Notes
V_{REF}	Internal reference voltage	2.20	V	1%	T_A = 25°C
	Temperature coefficient	-3.9	mV/°C	10%	
V_{LTF}	TS maximum threshold	0.6 • V_{CC}	V	±0.03V	Low-temperature fault
V_{HTF}	TS hysteresis threshold	0.44 • V_{CC}	V	±0.03V	High-temperature fault
V_{TCO}	TS minimum threshold	0.4 • V_{CC}	V	±0.03V	Temperature cutoff
V_{HCO}	High cutoff voltage	0.60 • V_{CC}	V	±0.03V	
V_{MIN}	Under-voltage threshold at BAT	0.34 • Vcc	V	±0.03V	
V_{LCO}	Low cutoff voltage	0.8	V	±0.03V	
V_{SNS}	Current sense at SNS	0.275	V	10%	I_{MAX}
		0.05	V	10%	I_{COND}

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	
V_{TEMP}	TS voltage potential	0		Vcc	V	$V_{TS} - V_{SNS}$
V_{CELL}	Battery voltage potential	0		V_{CC}	V	$V_{BAT} - V_{SNS}$
I_{CC}	Supply current		2	4	mA	Outputs unloaded
I_{IZ}	DSEL tri-state open detection	-2		2	µA	Note2
	IGSEL tri-state open detection	-2		2	µA	
V_{IH}	Logic input high	V_{CC}-1.0	-		V	QSEL,TSEL
		Vcc-0.3	-		V	DSEL, IGSEL
V_{IL}	Logic input low		-	V_{SS}+1.0	V	QSEL,TSEL
			-	V_{SS}+0.3	V	DSEL, IGSEL
V_{OH}	LED_1, LED_2, LED_3, output high	Vcc-0.8	-		V	$I_{OH} \le 10mA$
	MOD output high	Vcc-0.8	-		V	$I_{OH} \le 10mA$
V_{OL}	LED_1, LED_2, LED_3, output low		-	V_{SS}+0.8V	V	$I_{OL} \le 10mA$
	MOD output low		-	V_{SS}+0.8V	V	$I_{OL} \le 10mA$
	FLOAT output low		-	V_{SS}+0.8V	V	$I_{OL} \le 5mA$, Note 3
	COM output low		-	V_{SS}+0.5	V	$I_{OL} \le 30mA$
I_{OH}	LED_1, LED_2, LED_3, source	-10			mA	$V_{OH} = V_{CC}$-0.5V
	MOD source	-5.0			mA	$V_{OH} = V_{CC}$-0.5V
I_{OL}	LED_1, LED_2, LED_3, sink	10			mA	$V_{OL} = V_{SS}$+0.5V
	MOD sink	5			mA	$V_{OL} = V_{SS}$+0.8V
	FLOAT sink	5			mA	$V_{OL} = V_{SS}$+0.8V, Note 3
	COM sink	30			mA	$V_{OL} = V_{SS}$+0.5V
I_{IL}	DSEL logic input low source			+30	µA	V = Vss to Vss+ 0.3V, Note 2
	IGSEL logic input low source			+70	µA	V = Vss to Vss+ 0.3V
I_{IH}	DSEL logic input high source	-30			µA	V = V_{CC} - 0.3V toV_{CC}
	IGSEL logic input high source	-70	-		µA	V = V_{CC} - 0.3V toV_{CC}
I_L	Input leakage	-	-	±1	µA	QSEL, TSEL, Note 2

Notes: 1. All voltages relative to Vss except where noted.

2. Conditions during initialization after Vcc applied.

3. SNS = OV

Impedance

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
R_{BATZ}	BAT pin input impedance	50			MΩ	
R_{SNSZ}	SNS pin input impedance	50			MΩ	
R_{TSZ}	TS pin input impedance	50			MΩ	
R_{PROG1}	Soft-programmed pull-up or pull-down resistor value (for programming)			10	kΩ	DSEL, TSEL, and QSEL
R_{PROG2}	Pull-up or pull-down resistor value			3	kΩ	IGSEL
R_{MTO}	Charge timer resistor	20		480	kΩ	

Timing (TA = TOPR; VCC = 5V ±10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{MTO}	Charge time-out range	1		24	hours	See Figure 9
t_{QT1}	Pre-charge qual test 1 time-out period		$0.02t_{MTO}$			
t_{QT2}	Pre-charge qual test 2 time-out period		$0.16t_{MTO}$			
t_{DV}	Δ^2V termination sample frequency	-	$0.008t_{MTO}$			
t_{H01}	Pre-charge qual test 2 hold-off period	-	$0.002t_{MTO}$			
t_{H02}	Bulk charge hold-off period	-	$0.015t_{MTO}$			
F_{PWM}	PWM regulator frequency range		100		kHz	See Equation9

Capacitance

Symbol	Paramater	Minimum	Typical	Maximum	Unit
C_{MTO}	Charge timer capacitor		0.1	0.1	µF
C_{PWM}	PWM R-C capacitance		0.001		µF

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1		Descriptions	Clarified and consolidated
1		Renamed	Dual-Level Constant Current Mode to Two-Step Current Mode V_{MCV} to V_{HCO} V_{INT} to V_{LCO} t_{UV1} to t_{QT1} t_{UV2} to t_{QT2}
1		Consolidation	Tables 1 and 2
1		Added figures	Start-up states Temperature sense input voltage thresholds Pulsed maintenance current implementation
1		Updated figures	Figures 1 through 6
1		Added equations	Thermistor divider network configuration equations
1		Raised condition	MOD V_{OL} and V_{OH} parameters from ≤5mA to ≤10µA
1		Corrected Conditions	VSNS rating from V_{MAX} and V_{MIN} to I_{MAX} and I_{MIN}
1		Added table	Capacitance table for C_{MTO} and C_{PWM}
2	6	Changed values in Figure 5	Was 51K; is now 10K

Note: Change 1 = Dec. 1995 B changes from June 1995 A data sheet.
Change 2 = Sept. 1996 C from Dec. 1995 B.

Ordering Information

bq2031 _ _

Temperature:
blank = Commercial (-20 to +70°C)
N = Industrial (-40 to +85°C)*

Package Option:
PN = 16-pin plastic DIP
SN = 16-pin narrow SOIC

Device:
bq2031 Lead Acid Charge IC

* Contact factory for availability.

BENCHMARQ

Product Brief **DV2031S1**

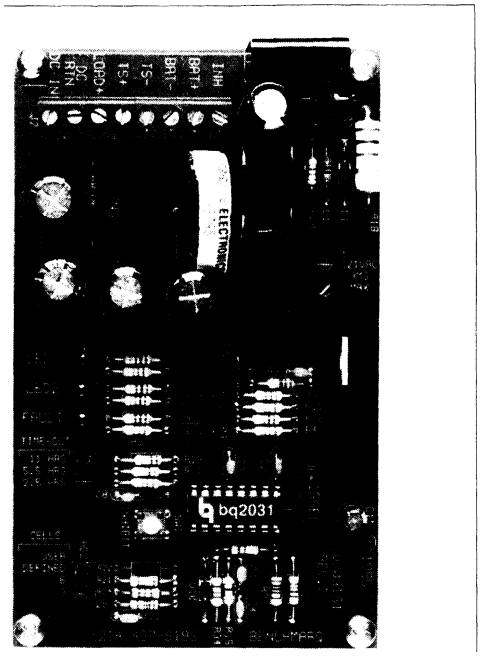
Fast Charge Development System

Control of On-Board PNP Switch-Mode Regulator

Features

- bq2031 fast charge control evaluation and development
- ➤ Accepts AC (21V RMS max.) or DC (30V max.) inputs
- ➤ On-board configuration for fast charge of 3 or 6 lead-acid cells; user-defined option allows other configurations
- ➤ Selectable charge algorithms: Two-Step Voltage, Two-Step Current, or Pulsed Current

  Constant current (up to 3.5A) and constant voltage (up to 15V) provided by on-board switch-mode regulator
- Charge termination by maximum voltage, second difference of cell voltage, minimum current, or maximum time-out
- ➤ Direct connections for battery, thermistor, and reset signal
- Jumper-configurable three-LED display



General Description

The DV2031S1 Development System provides a development environment for the bq2031 Lead-Acid Fast Charge IC. The DV2031S1 incorporates a bq2031 and a buck-type switch-mode regulator to provide fast charge control for 3 or 6 lead-acid cells.

The DV2031S1 can be configured for three different charge algorithms with jumpers JP2 and JP3. The charge algorithms available are:

- Two-Step Voltage
- Two-Step Current
- Pulsed Current

Each algorithm consists of pre-charge qualification, fast charge, and maintenance charge periods.

Fast charge termination occurs on:

- Maximum voltage
- The second difference of cell voltage (Δ^2V)
- Minimum current
- Maximum time-out

The maintenance charge may be configured for either a regulated float voltage or a pulsed current.

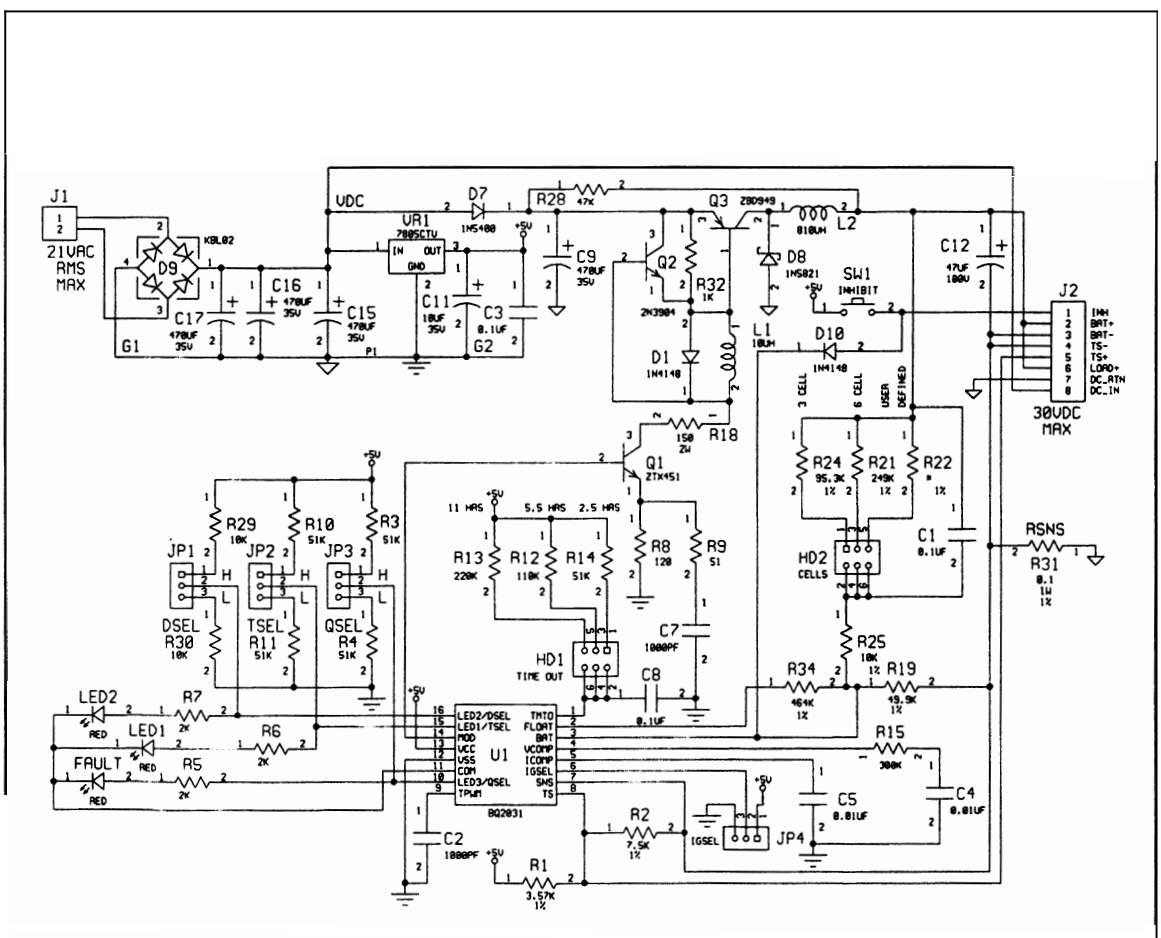
The bq2031 can be reset and a new charge cycle started with either the momentary on-board switch (SW1) or via the INH input on connector J2. The reset signal simulates a "Battery Absent" condition. Charging is inhibited as long as the reset signal is active; once it is released, the charge cycle re-starts at pre-charge qualification.

A full data sheet for this product is available on our web site (http://www.benchmarq.com), or you may contact the factory for one.

The VV provides a power supply (AC or DC) and batteries and configures the board for the number of cells, the maximum time-out period, the minimum current threshold, and the LED display mode. The board has direct connections for the battery and the provided thermistor.

Before using the DV2031S1 board, please review the bq2031 data sheet and the application note entitled "Using the bq2031 to *Charge* Lead-Acid Batteries".

DV2031S1 Board Schematic



Using the bq2031 to Charge Lead-Acid Batteries

1

Description of Operation

The bq2031 has two primary functions: lead-acid battery charge control and switch-mode power conversion control. Figure 1 is a block diagram of the bq2031. The charge contml circuitry is capable of a variety of full-charge detection techniques and supports three different charging algorithms. The Pulse-Width Modulator (PWM) provides control for high-efficiency current and voltage regulation.

Starting a Charge Cycle and Battery Qualification

When Vcc becomes valid (rises past its minimum value), the first activates battery temperature monitoring. Temperature is indicated by the voltage between the pins TS and SNS (V_{TEMP}). If the bq2031 finds the temperature out of range (or the thermistor is absent), it enters the Charge Pending State. In this state, all timers are suspended, charging current is kept off by MOD being held low, and the state is annunciated by LED_3 alternating high and low at approximately 1/6th second intervals.

Temperature checks remain active throughout the charge cycle. They are masked only when the bq2031 is in the Fault state (see below). When the temperature returns to the allowed charging range, timers are restarted (not reset) and the bq2031 returns to the state it was in when the temperature fault occurred.

When the thermistor is present and the temperature is within the allowed range, the bq2031 then checks for the presence of a battery. If the voltage between the BAT and SNS pine (V_{CELL}) is between the Low-Voltage Cut-Off threshold (V_{LCO}) and the High-Voltage Cut-Off (V_{HCO}), the bq2031 perceives a battery to be present and begins pre-charge battery qualification after a 500ms (typical) delay. If any new temperature or voltage faults occur during this time, the bq2031 immediately transitions to the appropriate state.

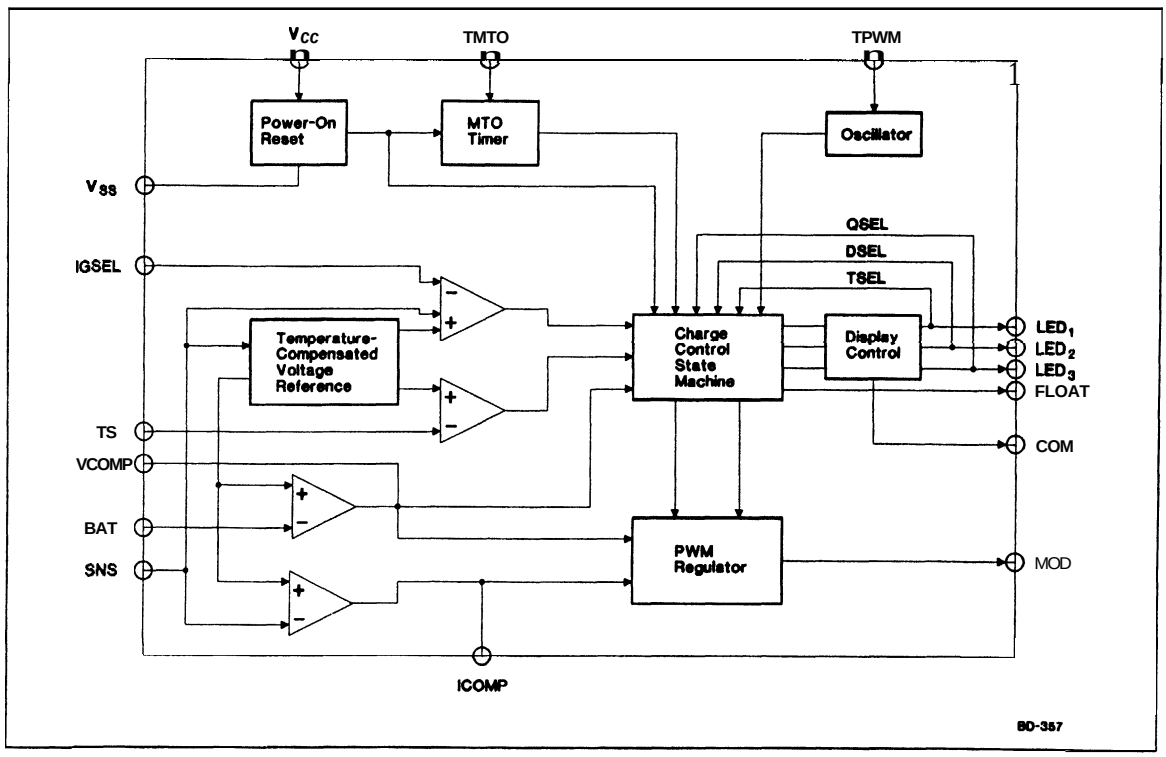


Figure 1. Block Diagram of the bq2031

If V_{CELL} is less than V_{LCO} or above V_{HCO}, the bq2031 believes no battery is present and enters the Fault state; MOD is held low and LED3 is turned on. This light gives the customer an indication that the charger is on, even though no battery is present. The bq2031 leaves the Fault state only if it sees V_{BAT} rise past V_{LCO} or fall past V_{HCO}, indicating a new battery insertion. If temperature is within bounds, there will again be a 500ms delay before battery qualification tests start.

Battery Qualification Tests

In teat 1, the bq2031 attempts to regulate a voltage = V_{FLT} + 0.25V across the battery pack. The bq2031 monitors the time required for I_{SNS}, the charging current, to rise to $I_{COND} = I_{MAX}/5$. If the current fails to rise to this level before the time-out period t_{QT1} expires (e.g. the battery has failed open), the bq2031 enters the Fault state, indicated by the LED3 pin going high. Charging current is removed from the battery by driving the MOD pin low, and the bq2031 remains in this state until it detects the wnditions to start a new charge cycle; the battery is replaced or V_{CC} is cycled off and then back on.

If test 1 passes, the bq2031 will start test 2 by attempting to regulate a charging current of I_{COND} into the battery pack. It will monitor the time required for the pack voltage to rise above V_{MIN} (the voltage may already be over this limit). If the voltage fails to rise to this level before the time out period t_{QT2} expires (e.g., the battery has failed short), the bq2031 again enters the Fault state as described above. If teat 2 passes, the bq2031 then begins fast (bulk) charging.

Fast Charging

The user configures the bq2031 for one of three fast charge and maintenance algorithms.

Two-Step Voltage (Figure 3)

This algorithm consists of three phases:

- Fast Charge phase 1: The charging current is limited at I_{MAX} until the cell voltage rises to V_{BLK}.
- Fast Charge phase 2: The charging voltage is regulated at V_{BLK} until the charging current drops below I_{MIN}.
- Maintenance phase: The charging voltage is regulated at V_{FLT}.

Two-Step Current (Figure 4)

This algorithm consists of two phases:

- Fast Charge phase: The charging current is regulated at I_{MAX} until the cell voltage rises to V_{BLK} or the

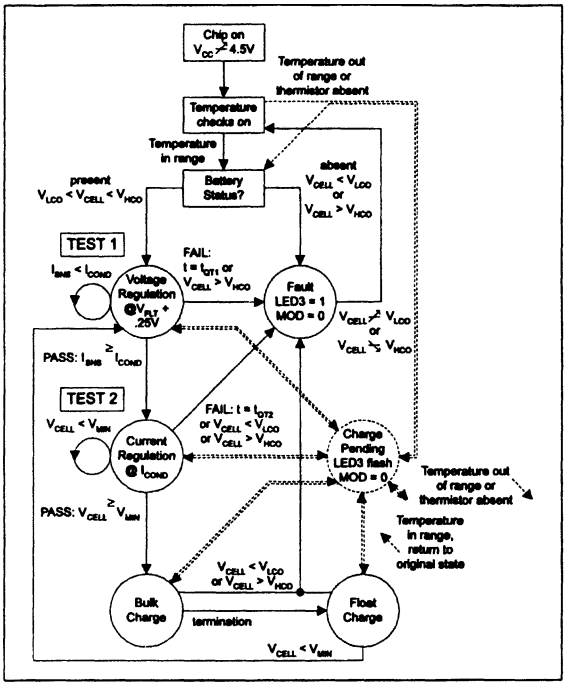


Figure 2. Cycle Start/Battery Qualification State Diagram

"Second Difference" of cell voltage drops below -8mV while V_{BAT} is over 2.0V. Second Difference is the accumulated differences between successive samples of V_{BAT}. The Second Difference technique looks for a negative change in battery voltage as the battery begins overcharging (see Figure 6).

- Maintenance phase: Fixed-width pulses of charging current = I_{COND} are modulated in frequency to achieve an average value of I_{MIN}. See Appendix A for implementation details.

Pulsed Current (Figure 5)

This algorithm consists of two phases:

- Fast Charge phase: The charging current is regulated at I_{MAX} until the cell voltage rises to V_{BLK}.
- Maintenance phase: Charging current is removed until the battery voltage falls to V_{FLT}; charging current is then restored and regulated at I_{MAX} until the battery voltage once again rises to V_{BLK}. This cycle is repeated indefinitely.

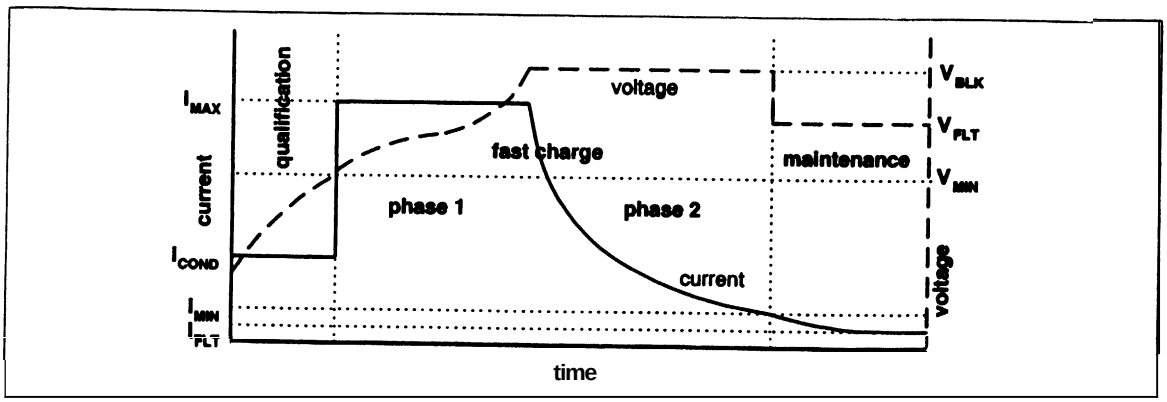


Figure 3. Two-Step Voltage Algorithm

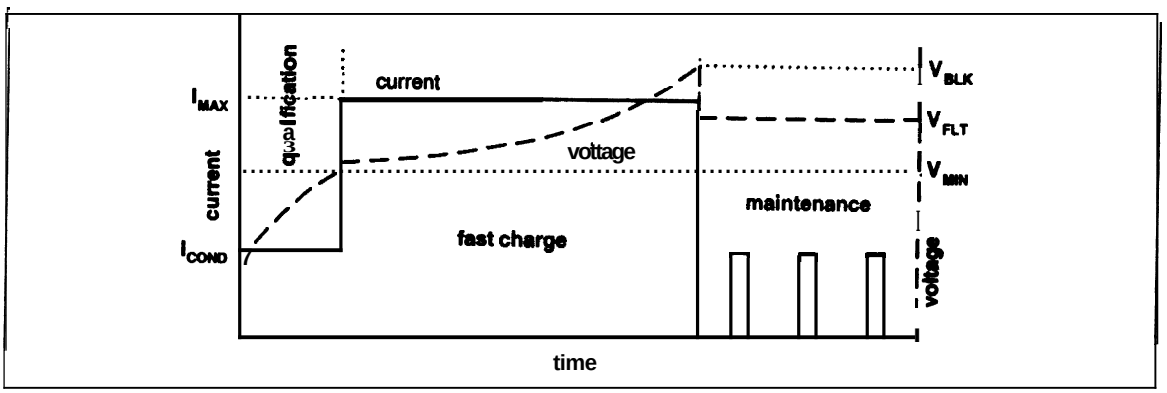


Figure 4. Two-Step Current Algorithm

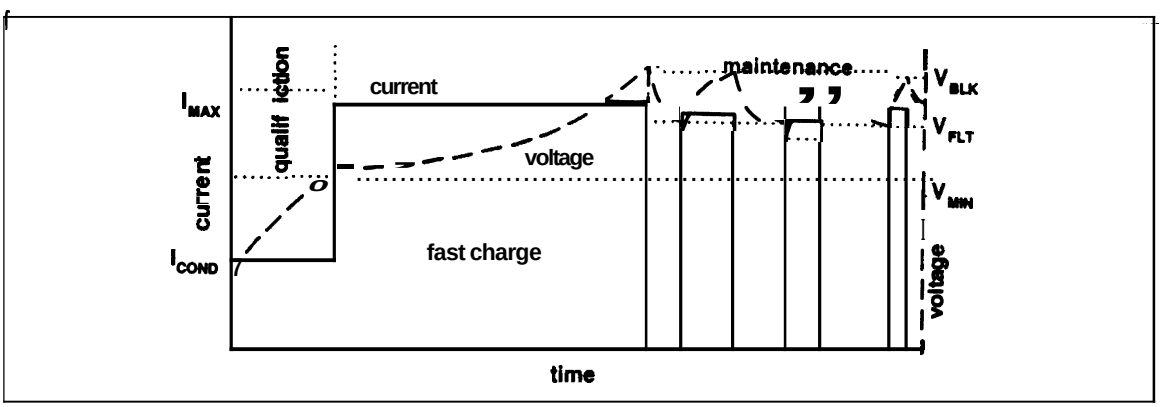


Figure 5. Pulsed Current Algorithm

Safety Time-Out

A safety timer limits the time the charger can spend in any phase of the charging cycle except maintenance. This Maximum Time-Out (MTO) timer is reset at the end of successful pre-charge qualification when the bq2031 begins fast charging[1]. If MTO times out before a fast charge termination criterion is met, the charging current is turned off (MOD driven low) and the bq2031 enters the Fault state exactly as if it had failed a pre-charge qualification test.

There is one exception. In the Two-Step Voltage algorithm, MTO is reset when the bq2031 transitions from the current-limited phase 1 to the voltage-regulated phase 2 of fast charging. If MTO expires while the bq2031 is still in phase 1, it does not enter the Fault state but instead transitions to phase 2 (and MTO is reset). If MTO expires while the bq2031 is still in state 2, the bq2031 enters the Fault state.

During maintenance, the MTO timer is reset at the beginning of each new pulse in the Two-Step Current and Pulsed Current algorithms. It expires (and puts the bq2031 in the Fault state) only if the bq2031 became 'jammed" with a pulse stuck on. The MTO timer is not active during the maintenance phase of the Two-Step Voltage algorithm.

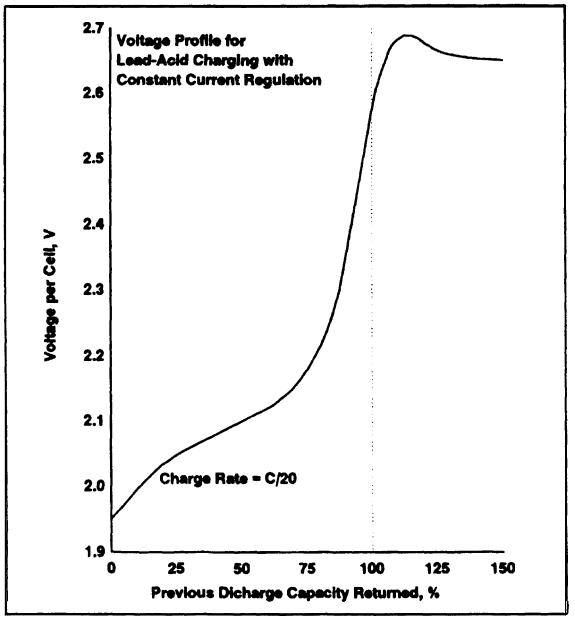


Figure 6. Voltage Roll-Off In Constant Current Charging Profile

Hold-off Periods

Old age and/or abuse can create conditions in lead-acid batteries that may generate a large transient voltage spike when current-regulated charging is first applied. This spike could cause early termination in the fast charge algorithms by mimicking their voltage-based termination criteria. To prevent this, the bq2031 uses a "hold-off" period at the beginning of the fast charge phase. During this time, all voltage criteria are ignored except cutoff voltages. (Straying outside the range between V_{HCO} and V_{LCO} still causes the bq2031 to believe the battery has been removed, and the bq2031 enters the Fault state and shuts off charging current.) A hold-off period is also enforced during test 2 of pre-charge qualification for the same reason.

Configuration Instructions

Selecting Charge Algorithm and Display Mode

QSEL/LED3, DSEL/LED2, and TSEL/LED1 are bidirectional pins with two functions: they are LED driver pins as outputs and programming pins for the bq2031 as inputs. The selection of pull-up, pull-down, or no pull resistor for these pins programs the charging algorithm on QSEL and TSEL per Table 1 and the diilay mode on DSEL per Table 2 The bq2031 forces the output driver on these bi-directional pins to their high-impedancestate (as well as their common return output pin, COM) and latches the programming data sensed on the inputs when any one of the following three events occurs:

1. V_{CC} rises to a valid level.
2. The bq2031 leaves the Fault state.
3. The bq2031 detects battery insertion.

The LEDs go blank for approximately 0.75s. (typical) while new programming data is latched.

Figure 7 shows the bq2031 configured for the Pulsed Current algorithm and display mode 2.

Table 1. Programming Charge Algorithms

Charge Algorithms	QSEL	TSEL	Programmable Thresholds
Two-Step Voltage	L	H/L*	I_{MAX}, V_{BLK}, V_{FLT}
Two-Step Current	H	L	I_{MAX}, V_{BLK}, I_{MIN}
Pulsed Current	H	H	I_{MAX}, V_{BLK}, V_{FLT}

Note: * Set either high or low; do not float pin.

[1] The MTO timer also resets at the beginning of the pre-charge qualification period. However, t_{QT1} or t_{QT2} (the qualification test time limits) expire and put the bq2031 in the Fault state before the MTO limit can be reached. The MTO timer is suspended while the bq2031 is in the Fault state, and is reset by the conditions that allow the bq2031 to exit that state.

Table 2. bq2031 Display Output Summary

Mode	Charge State	LED_1	LED_2	LED_3
DSEL = 0 (Mode 1)	Battery absent	Low	Low	High
	Pre-charge qualification	Flash*	Low	Low
	Fast charging	High	Low	Low
	Maintenance charging	Low	High	Low
	Charge pending (temperature out of range)	X	X	Flash*
	Fault	X	X	High
DSEL = 1 (Mode 2)	Battery absent	Low	Low	High
	Pre-charge qualification	High	High	Low
	Fast charge	Low	High	Low
	Maintenance charging	High	Low	Low
	Charge pending (temperature out of range)	X	X	Flash*
	Fault	X	X	High
DSEL = Float (Mode 3)	Pre-charge qualification	Flash*	Flash*	Low
	Battery absent	Low	Low	High
	Fast charge: current regulation	Low	High	Low
	Fast charge: voltage regulation	High	High	Low
	Maintenance charging	High	Low	Low
	Charge pending (temperature out of range)	X	X	Flash*
	Fault	X	X	High

Note: 1 = V_{CC}, 0 = V_{SS}, X = LED state when fault occurred.
* Flash = 1/6 sec. low, 1/6 sec. high

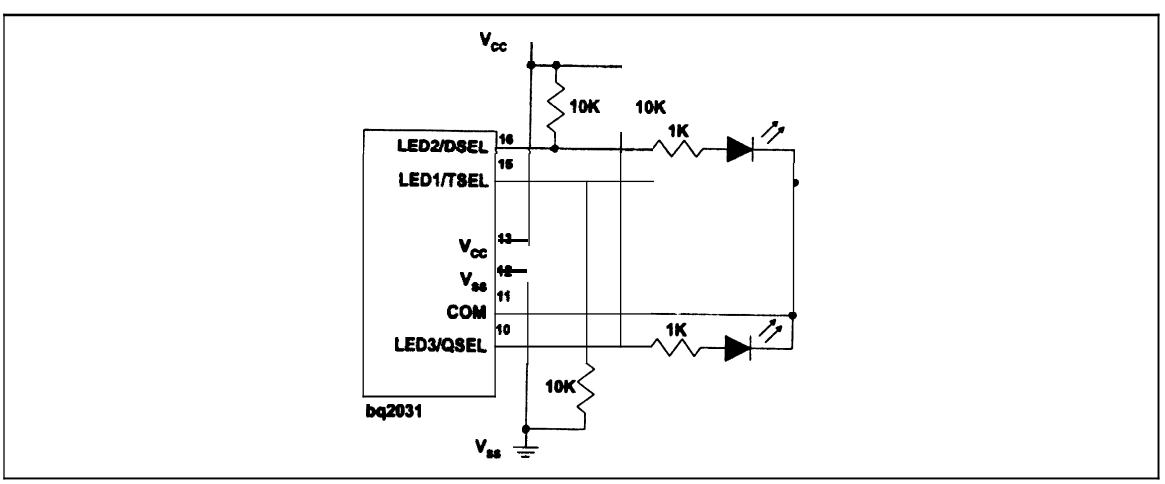


Figure 7. Configuring 10K Two-Step Charging Algorithm and Display Mode Selection

A resistor-divider network must be implemented that presents the defined voltage levels to the TS pin at the desired temperatures (see Figure 10).

The equations for determining RT1 and RT2 are:

Equation 4

$$0.6 * V_{CC} = \frac{(V_{CC} - 0.275)}{1 + \frac{RT1 * (RT2 + R_{LTF})}{(RT2 * R_{LTF})}}$$

Equation 5

$$0.44 = \frac{1}{1 + \frac{RT1 * (RT2 + R_{HTF})}{(RT2 * R_{HTF})}}$$

where:

- R_{LTF} = Thermistor resistance at LTF
- R_{HTF} = Thermistor resistance at HTF

TCO is determined by the values of RT1 and RT2. 1% resistors are recommended. As an example, the resistor values for several temperature windows computed for a Philips 2333-640-63103 thermistor are shown in Table 5.

Table 5. RT1 and RT2 Values for Temperature Thresholds

LTF (°C)	HTF (°C)	TCO (°C)	RT1 (kΩ)	RT2 (kΩ)
0	45	47	3.57	7.50
5	45	47	3.65	8.66
–5	50	52	2.74	5.36

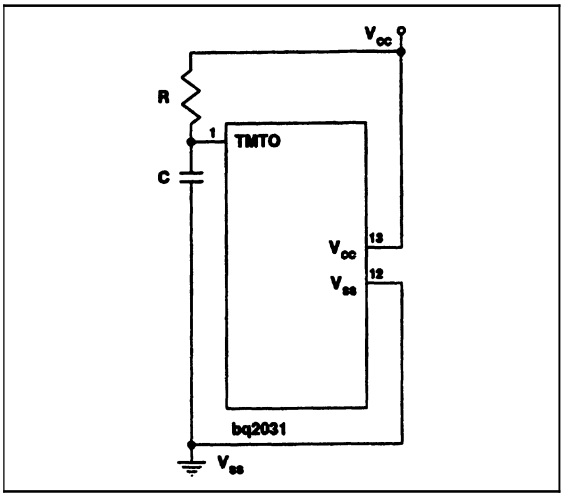


Figure 11. RC Network for Setting MTO

Disabling Temperature Sensing

Temperature sensing may be disabled by removing the thermistor and RT1, and using a value of 100kΩ for RT1 and RT2.

Setting Timers

The user sets the Maximum Time-Out (MTO) value. All other timing periods used in the bq2031 are fixed as fractions of MTO (see Table 6). MTO is set by an R-C network on the TMTO pin as shown in Figure 11.

Table 6. Timing Parameters

Symbol	Parameter	Minimum	Typical	Maximum	Unit
t_{MTO}	Maximum Time Out range	1		24	hours
t_{QT1}	Qualification time-out test 1		$0.02t_{MTO}$		
t_{QT2}	Qualification time-out test 2		$0.16t_{MTO}$		
t_{DV}	$-\Delta^2V$ termination sample frequency		$0.008t_{MTO}$		
t_{HO1}	Qu cation test 2 hold-off period		$0.002t_{MTO}$		
t_{HO2}	Bulk-charge hold-off period		$0.015t_{MTO}$		

alifi

The equation for MTO is:

Equation 6

$$\text{MTO (in hours)} = 0.5 * R * C$$

where R is in kΩ and C is in µF. The value for C must not exceed 0.1µF.

Example: An MTO of 5 hours is set by R = 100kΩ and C = 0.1µF

Switch-Mode Power Conversion

The bq2031 incorporates the necessary PWM control circuitry to support switch-mode voltage and current regulation

Figure 12 shows a functional block diagram of a switch-mode buck topology converter using the bq2031. The battery voltage is divided down to a per-cell equivalent value at the BAT pin. During voltage regulation, the voltage on the BAT pin (V_{BAT}) is regulated to the internal band-gap reference of 2.2V at 25°C (with a temperature drift of -3.9 mV/°C). The charge current through the inductor L is sensed across the resistor R_{SNS}. During current regulation, the bq2031 regulates the voltage on the SNS pin (V_{SNS}) to a temperature-compensated reference of 0.275V.

The passive components C_I on the I_{COMP} pin, Rv and Cv on the V_{COMP} pin, and C_F across the high side of the battery voltage divider form the phase compensation network for the current and voltage control loops, respectively, The diodes (D_{b1} and D_{b2}) serve to prevent battery drain when VDC is absent, while the pull-up resistor (R_P) is used to detect battery removal. The resistor R_S, typically a few tens of mΩ, is optional and depends on the battery impedance and the resistance of the battery leads to and from the charger board.

Pulse-Width Modulator

The bq2031 incorporates two PWM circuits, one for each control loop (voltage and current, see *Figure* 13). Each PWM circuit runs off a common saw-tooth waveform (V_S) whose time-base is controlled by a timing capacitor (C_{PWM}) on the TPWM pin.

The relationship between C_{PWM} and the switching frequency (F_S) is given by:

Equation 7

$$F_S = \frac{0.1}{C_{PWM}} \text{ kHz}$$

where C_{PWM} is in µF.

Each PWM loop starts with a comparator whose positive terminal is driven by V_S. The negative terminal is driven by the output of an Operational Transconductance Amplifier (OTA) which, with the compensation network connected h a V_{COMP} & I_{COMP}, generates the control signal V_C. The OTA characteristics are: R_O = 250kΩ; G_M = 0.42m-mho; gain bandwidth = 80MHz. The output of each comparator, along with the ramp waveform (V_S), is used to generate a pulse-width modulated waveform at a constant frequency on the MOD output. Figure 14 shows the relationehip of MOD with Vc and Vs.

The MOD output swings rail-to-rail and can source and sink 10mA. It is used to control the drive circuitry of the switching transistor.

The pulse-width modulated square-wave signal on the MOD pin is synchronized to the internal sawtooth ramp signal. The ramp-down time (T_D) is fixed at approximately 20% of the ramp time-period (T_P). This limits the maximum duty-cycle achievable to approximately 80%. See Figure 14.

Example: At a switching frequency of F_S = 100kHz, T_D = 2µs.

Inductor Selection

The inductor selection criteria for a DC-DC buck converter vary depending on the charging algorithm used. For the Two-Step Current and Pulsed Current charge algorithms, the inductor equation is:

Equation 8

$$L = \frac{(N * V_{BLK} * 0.5)}{F * \Delta I}$$

where:

- N = Number of cells
- V_{BLK} = Bulk voltage per cell, in volts
- F_S = Switching frequency, in hertz
- ΔI = Ripple current at I_{MAX}, in amps

The ripple current is usually set between 20–25% of I_{MAX}.

Example: A 6-cell SLA battery is to be charged at I_{MAX} = 2.75A in a buck topology running at 100kHz. The V_{BLK} threshold is set at 2.45V per cell and the charger is conf i d for Pulsed Current mode. Assuming a ripple = 2590of I_{MAX}, the inductor value required is:

Equation 9

$$L = \frac{(6 * 2.45 * 0.5)}{(100000 * 0.6875)} = 107\mu H$$

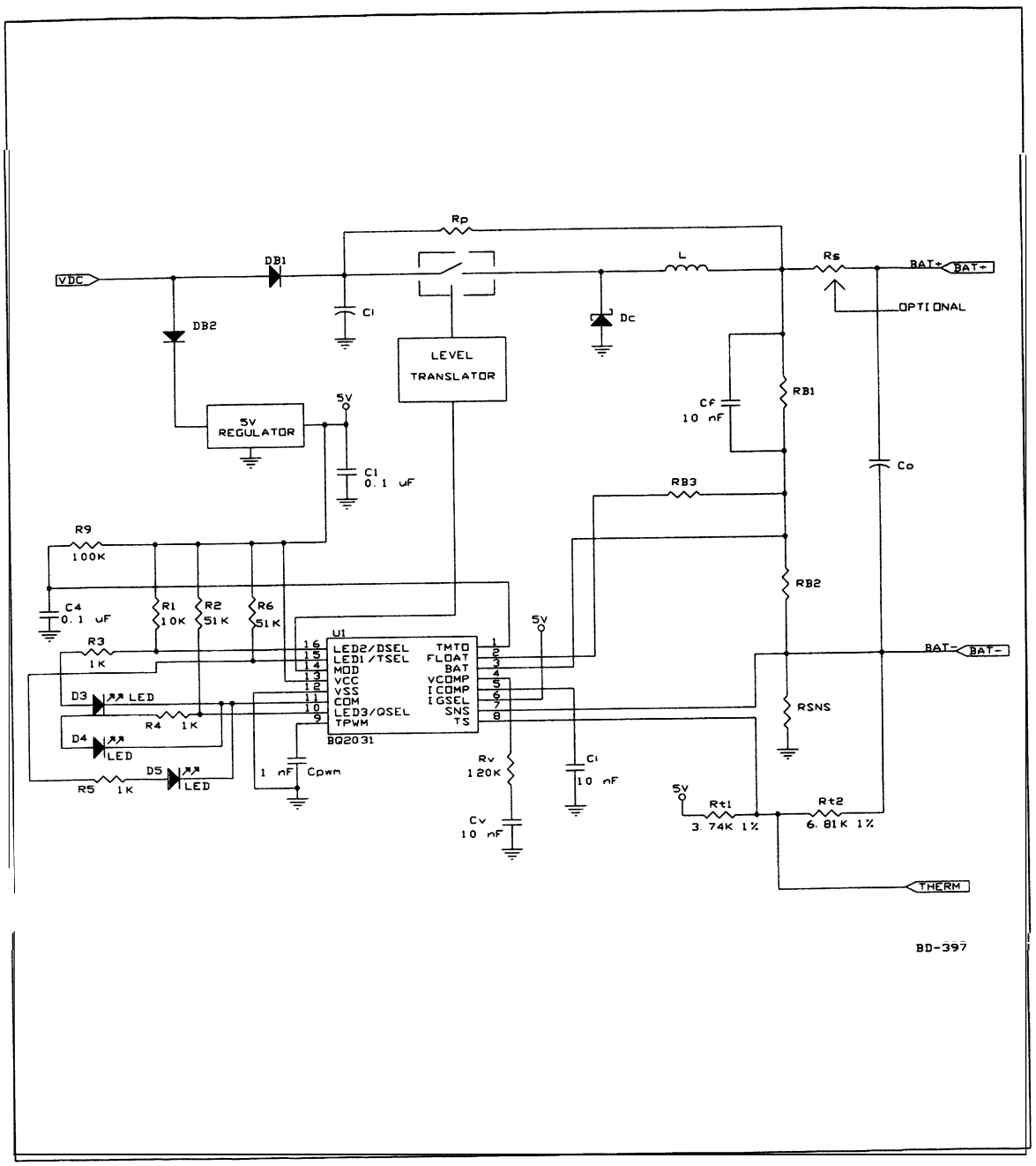


Figure 12. Functional Diagram of a Switch-Mode Buck Regulator Lead-Acid Charger Using the bq2031

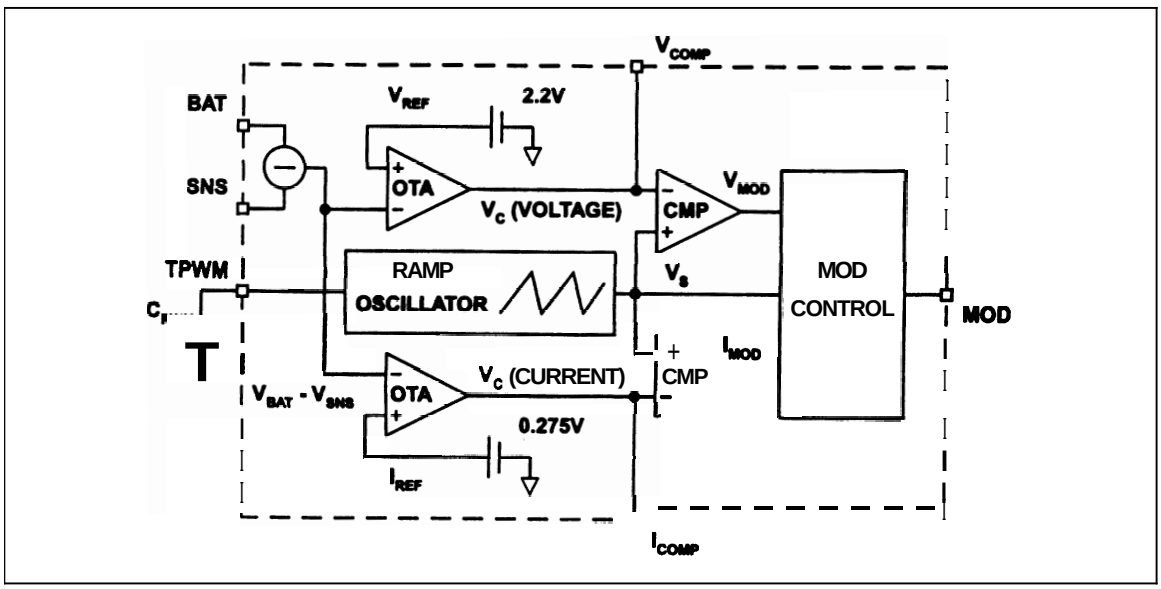


Figure 13. Block Diagram of the bq2031 PWM Control Circuitry

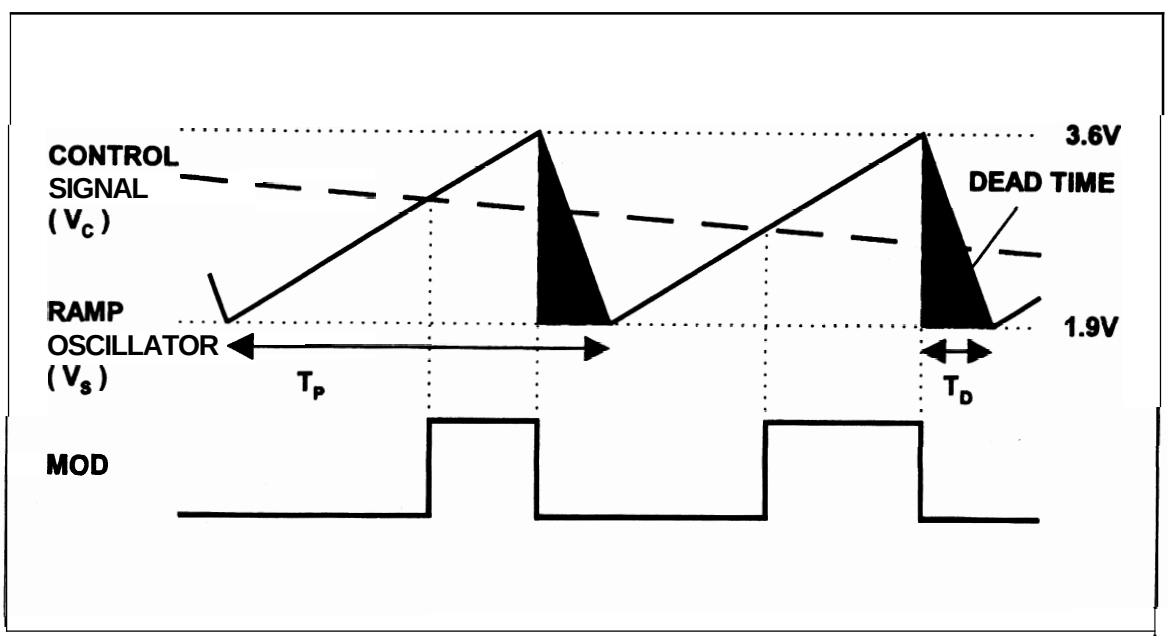


Figure 14. Relationship of MOD output to Sawtooth Waveform Vs and Control Signal Vc

The inductor formula for the Two-Step Voltage charge algorithm is dictated by the inductor current, which must remain continuous down to I_{MIN} during Fast Charge phase 2 (voltage regulation phase).

Equation 10

$$L = \frac{N * V_{BLK} * 0.5}{F_S * 2 * I_{MIN}}$$

Example: A 6-cell SLA battery is to be charged at I_{MAX} = 2.75A in a buck topology running at 100 kHz. The V_{BLK} threshold is set at 2.45V per cell and the charger is configured for Two-Step Voltage mode, with $I_{MIN} = I_{MAX}/20$. The inductor value required is:

Equation 11

$$L = \frac{6 * 2.45 * 0.5}{(100000 * 2 * 0.1375)} = 267\mu H$$

Phase Compensation

For buck-mode switching applications, the suggested component values shown in *Figure* 12 are *good* starting points. Further assistance is available from the bq2031 configuration software program "CNFG2031." More details on the calculations used in this program are available in the application note entitled "Compensating the bq2031 in Buck-Mode Switching Applications." For assistance with other power supply topologies, contact the factory.

Miscellaneous Issues

Vcc Supply

The Vcc supply provides bq2031 power and serves as the reference voltage for all temperature sense thresholds (V_{LTF}, V_{HTF}, and V_{TCO}) and the battery voltage thresholds V_{HCO} and V_{MIN}. The timer thresholds (MTO and its derivatives) are trimmed within 6% of the typical value with Vcc = 5V.

The V_{BLK} and V_{FLT} thresholds are set from an external divider network powered by the battery. These thresholds are referenced to an internal band-gap reference, and the accuracy of voltage regulation will not be adversely affected by variation in Vcc. The current regulation threshold (I_{MAX}) is referenced to a temperature compensated reference and is also unaffected by Vcc.

DC Power Supply

The DC power supply voltage (V_{DC}) for a switch-mode application must satisfy the following criterion:

Equation 12

$$V_{DC} = (N * V_{BLK}) + 3V$$

where:

- N = Number of cells
- V_{BLK} = Bulk voltage threshold per cell

Logical Control of Charging

Charge Inhibit

An inhibit input may be implemented by connecting the cathode of a emall-signal diode to the TS pin. A CMOS logic-level "1" applied to the anode of the diode then functions as an inhibit input, by driving the temperature sense voltage out of its allowed range and simulating an under-temperature condition. The bq2031 enters the Charge Pending state, shutting off charging current (driving MOD low) and suspending all timers. When the Inhibit signal is allowed to float, the bq2031 returns to its previous state (as long as the temperature is still within the allowed range). The bq2031 restarts (but does not reset) its timers, and the suspended charge cycle resumes at the point where it stopped.

Reset

A logical Reset signal for the bq2031 can be created in a manner similar to the Charge Inhibit input described above. Instead of being connected to the TS pin, however, the diode is connected to the BAT input. In this confiiation, a logic "1" on the diode drives V_{BAT} above V_{HCO}, simulating battery removal. The bq2031 enters the Fault state and waits to see a battery insertion; V_{BAT} rising past V_{LCO} or falling past V_{HCO}. Removing the logic "1" from the diode creates this transition (as long a battery is still present), and the bq2031 starts a new charge cycle.

Caution: To avoid damage the bq2031, always keep the voltage applied to the anode of the diode below Vcc for either the Charge Inhibit or Reset implementations.

Layout Guidelines

Printed circuit board layout must adhere to the following guidelines to minimize noise injection on the high-impedance pins (BAT, V_{COMP}, I_{COMP}, and SNS).

1. Use a single-point grounding technique such that the isolated small-signal ground path and the high-current power ground path return to the power supply ground.
2. The charging path components and traces must be isolated from the voltage and current feedback small signal paths.
3. 0.1µF and 10µF decoupling capacitors must be placed close to the Vcc pin. This also helps to prevent voltage dips while the bq2031 is driving the LEDs.

4. A 100pF capacitor, if used for coupling the BAT and SNS pins, must be placed close to those pins.
5. The compensation network on I_{COMP} and V_{COMP} must be placed close to their respective pins.
6. Minimize loop area in paths with high pulsating currents. In the example in Figure 15, this loop is fanned by D9, Q2, and C5.

Battery Removal Detection

The bq2031 interprets V_{BAT} rising past V_{HCO} or falling past V_{LCO} as battery removal, and the bq2031 enters the Fault state until a new battery insertion is seen. The battery removal transitions are precluded during periods of voltage regulation unless circuitry (e.g., a pull-up to VDC) is provided to pull V_{BAT} out of the 'battery present" range.

Voltage regulation occurs during phase 2 of the Two-Step Voltage fast charge algorithm and in battery qualification test 1 which precedes all three algorithms. The time-out period of this test (= 0.02 • MTO) is at least 1.2 minutes and may be as long as 28.8 minutes. Unless waiting through this period before detecting battery removal is acceptable, the pull-up is required in the purely current regulated algorithms as well. A diode should also be installed in the path of the pull-up to prevent the power supply from draining the battery when the supply is turned off. Refer to resistor R12 and diode D3 in the example design in Figure 15.

This pull-up creates a background trickle charge current to the battery that can be minimized by minimizing the voltage overhead; that is, the voltage difference between the VDC supply and the battery stack.

Load-Only Operation

The bq2031 supports the case in which the charger must supply the load in the absence of a battery, provided the load can pass the two pre-charge qualifications tests (draw current of at least I_{COND} when regulated at V_{FLT} + 0.25V and maintain voltage of at least V_{MIN} when regulated at I_{COND}). Further, the load must not create conditions that cause fast charge termination or it must be able to tolerate the conditions of maintenance regulation for the charge algorithm selected. This is regulation at V_{FLT} in the case of the Two-Step Voltage algorithm or constant or hysteretic pulsed current supply in the case of the Two-Step Current and Pulsed Current algorithms, respectively. This can be a problem for intermittent loads unless circuitry is provided to maintain these conditions during the low-load or no-load periods.

Back-up Supply Regulation

To protect the system from damage during periods of fast charge voltage regulation, the bq2031 regulates to I_{MAX} if the current tries to rise above that level, and has an absolute current limit of 1.25 • I_{MAX}. Similarly, during periods of fast charge current regulation, the bq2031 enforces a V_{BLK} upper limit on voltage, and regulates to V_{BLK} if the voltage tries to rise above this level. During the maintenance phase, the bq2031 regulates to V_{FLT} and I_{COND} during periods of current or voltage regulation, respectively.

Applications Example: Single-Ended Buck Charger

Charger Specifications:

- Charge Algorithm: Two-Step Voltage mode
- Charge Current: 2.76 A
- Battery Specifications: Yuaea 12V, 10Ah

The following information is derived from the battery specifications:

- Number of cells = 6 (divide battery voltage by 2, the SLA nominal V/cell)
- Capacity = 10 amp-hours
- V_{BLK} threshold = 2.4V per cell (from the cyclic voltage specification)
- V_{FLT} threshold = 2.2V per cell (from the float voltage specification)
- The safety timer (MTO) is set equal to the amp-hour capacity divided by the charge current:

Equation 13

$$\text{MTO} = \frac{10}{2.75} = \text{approximately 4 hours}$$

- The temperature window of operation from the Yuasa battery specifications is 0°C–45°C. This gives: LTF = 0°C and HTF = 45°C

Apply these parameters in equations 1 through 10 to determine values for the following:

- Battery divider network
- Sense resistor
- MTO time-out
- PWM frequency
- Temperature window network

The final schematic (see Figure 15) uses a low V_{CE} (sat), high-gain, high-bandwidth PNP transistor (Q2) as the switching device in a single-ended buck topology powered from a DC supply of 24 V.

The power filter inductor (L2) is a 78-turn powdered-iron toroidal core inductor from Micrometals. The capacitor

(C4) is used to suppress the inductive effect of long lead wires from the board to the battery. The low Q inductor (L1) causes transistor Q2 to turn off faster during the commutation period. See Table 7 for the parts list for the design.

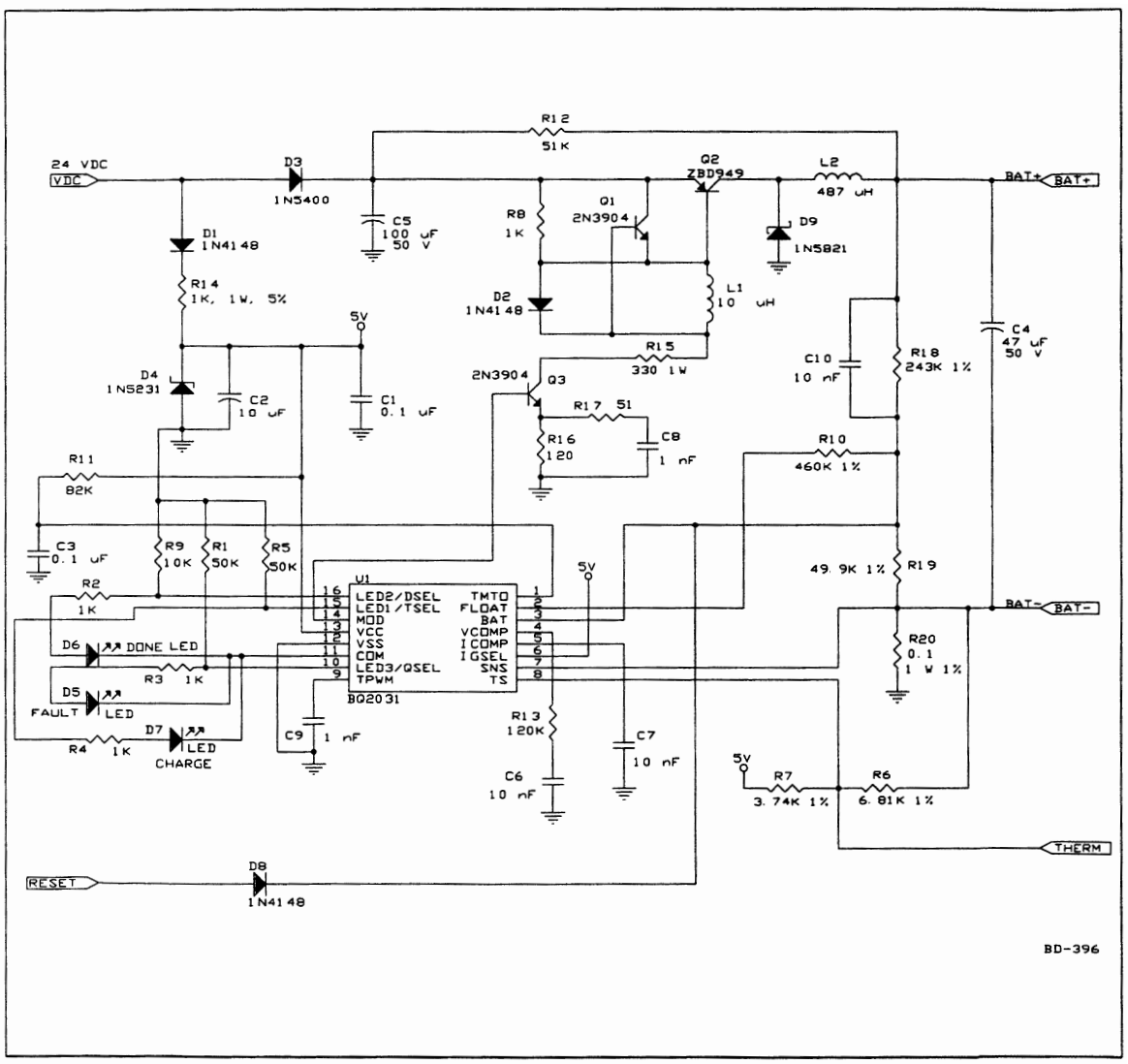


Figure 15. Example Schematic of a Single-Ended Buck Topology Charger Using the bq2031

Table 7. Parts List for a Single-Ended Buck Charger

Item	Quantity	Reference	Part
1	2	C1, C3	0.1µF
2	1	C2	10µF
3	1	C4	47µF
4	1	C5	100µF
5	2	C6, C7	10nF
6	2	C8, C9	1nF
7	3	D1, D2, D8	1N4148
8	1	D3	1N5400
9	1	D4	1N5231
10	3	D5, D6, D7	LED
11	1	D9	1N5821
12	1	L1	10µH
13	1	L2	487µH
14	2	Q1, Q3	2N3904
15	1	Q2	ZBD949
16	2	R9, RT1	10K
17	2	R1, R5	50K
18	4	R2, R3, R4, R8	1K
19	1	R6	6.81K 1%
20	1	R7	3.74K 1%
21	1	R10	460K 1%
22	1	R11	82K
23	1	R12	51K
24	1	R13	120K
25	1	R14	1K, 1W, 5%
26	1	R15	330 1W
27	1	R16	120
28	1	R17	51
29	1	R18	243K 1%
30	1	R19	49.9K 1%
31	1	R20	0.1
32	2	R21, R22	0.1Ω
33	1	U1	bq2031

Appendix A: Implementation Details of Pulsed Maintenance Charging

Two-Step Current Algorithm

Maintenance charging in the Two-Step Current Algorithm is implemented by varying the period (T_P) of a fixed current ($I_{COND} = I_{MAX}/5$) and duration (0.2 second) pulse to achieve the configured average maintenance current value. See Figure 16.

Maintenance current can be calculated by:

Equation 14

$$\text{Maintenance current} = \frac{((0.2) \cdot I_{COND})}{T_P} - \frac{((0.04) \cdot I_{MAX})}{T_P}$$

where T_P is the period of the waveform in seconds.

Table 8 gives the values of T_P programmed by IGSEL

Table 8. Fixed Pulse Period by IGSEL

IGSEL	T_P (sec.)
L	0.4
H	0.8
Z	1.6

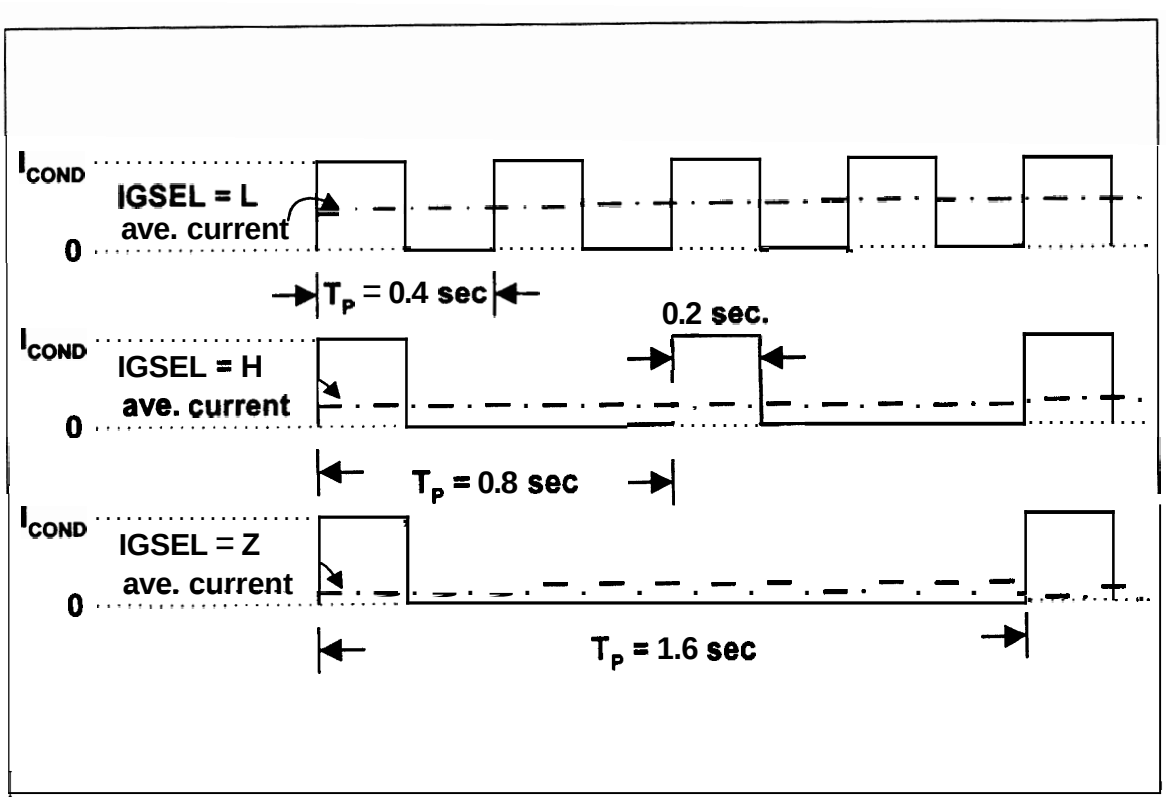


Figure 16. Implementation of Fixed-Pulse Maintenance Charge

BENCHMARQ

Preliminary Switch-Mode Power Conversion Using the bq2031

1

Introduction

The bq2031 incorporates the necessary PWM control circuitry to support switch-mode voltage and current regulation, as required by its charge control function block This application note describes how to configure the bq2031 in buck mode switching power supply topology. A methodology for phase compensation of the voltage and current feedback loops is recommended. A brief description of the PWM control circuitry and phase compensation criteria appears below, followed by a discussion dealing with topology specific issues.

The Pulse Width Modulator

The bq2031 incorporates two voltage mode direct duty cycle Pulse Width Modulators, one for each control loop (voltage and current). A block diagram is shown in Figure 1. Each PWM runs off a common saw-tooth waveform whose time-base is controlled by a capacitor, C_{PWM} on the **TPWM** pin.

The relationship of C_{PWM} to the switching frequency, **Fs** is given by:

Equation 1

$$F_S = \frac{0.1}{C_{PWM}} \text{ kHz}$$

where:

- C_{PWM} is in µF.

The **PWM** for either loop coneists of a comparator whose positive terminal is driven by the output of the sawtooth ramp signal, **Vs,** while the negative terminal is driven by the output of an Operational **Transconductance** Amplifier (OTA). The output is the control signal, **Vc.** The output of each **PWM** is logically ORed to generate a constant frequency pulse width modulated rectangular waveform at the MOD output. The relationship of the MOD output with **respect** to the OTA control signal, Vc, and the sawtooth ramp signal, **Vs,** is shown in Figure 2.

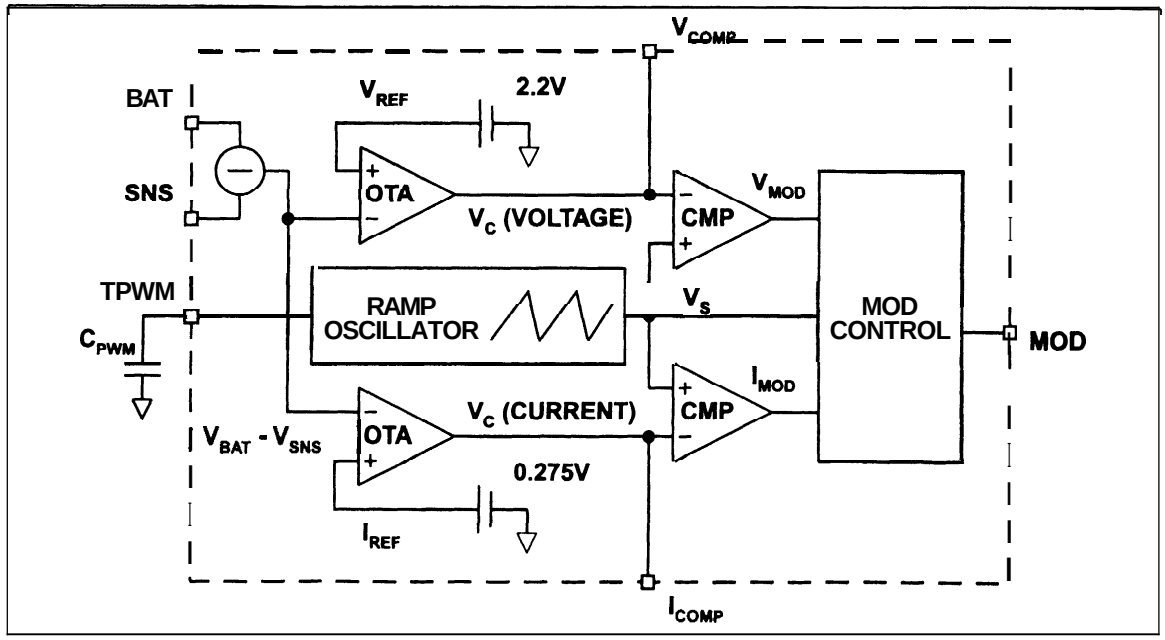


Figure 1. Block Diagram of the bq2031 PWM Control Circuitry

The MOD output swings rail-to-rail and can source and sink 10mA. It is used to control a switching transistor in a switch-mode application.

The pulse width modulated square wave signal on the MOD pin is synchronized to the internal sawtooth ramp signal. The ramp-down time (T_D) is fixed at approximately 20% of the total period (T_P). This condition limits the maximum duty-cycle to approximately 80%. For example, with a switching frequency F_S = 100kHz, T_D = 2µs.

Phase Compensation

As in any feedback control system, phase compensation is necessary to achieve both loop stability and dynamic line and load response. AS shown in the PWM block diagram (Figure 1) the bq2031 provides two high-impedance nodes, I_{COMP} and V_{COMP}, for current and voltage loop phase compensation. In a battery charger application the dynamic load response is not as much a concern as loop stability, especially during voltage regulation.

Voltage and Current Control Loops

Two independent PWM function blocks implement direct duty cycle control for current and voltage regulation. During current regulation the feedback signal is the voltage across the current sense resistor, R_{SNS}, as shown in the current feedback loop model of Figure 3.

The current regulation total open-loop transfer function, $I_{L(s)}$, may be expressed as:

Equation 2

$$I_{L(s)} = A(s) * P_{\omega}(s) * P_T(s)$$

where:

- A(s) is OTA error amplifier and compensation network transfer function, V_C/V_O
- $P_{\omega(s)}$ is the PWM transfer function. D/VC
- $P_T(s)$ is the power train transfer function, V_O/D
- D is the duty cycle of the PWM waveform

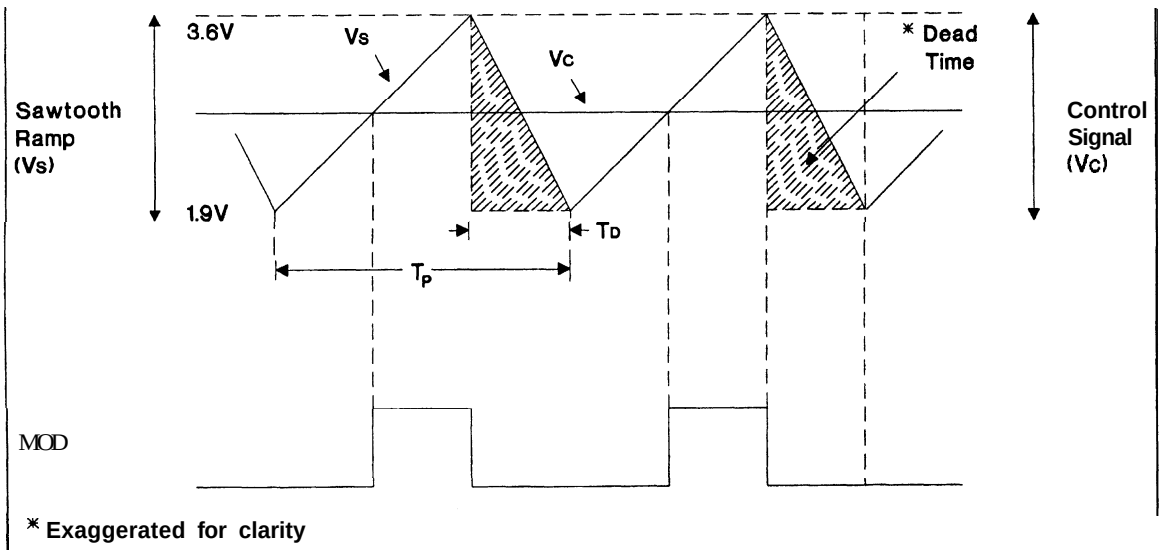


Figure 2. Relationship of MOD Output to Sawtooth Waveform Vs and Control Signal Vc

During voltage regulation, the feedback signal is the voltage sensed at the midpoint of the battery voltage divider (between RB1 and RB2). The voltage feedback control loop is modeled as shown in Figure 4.

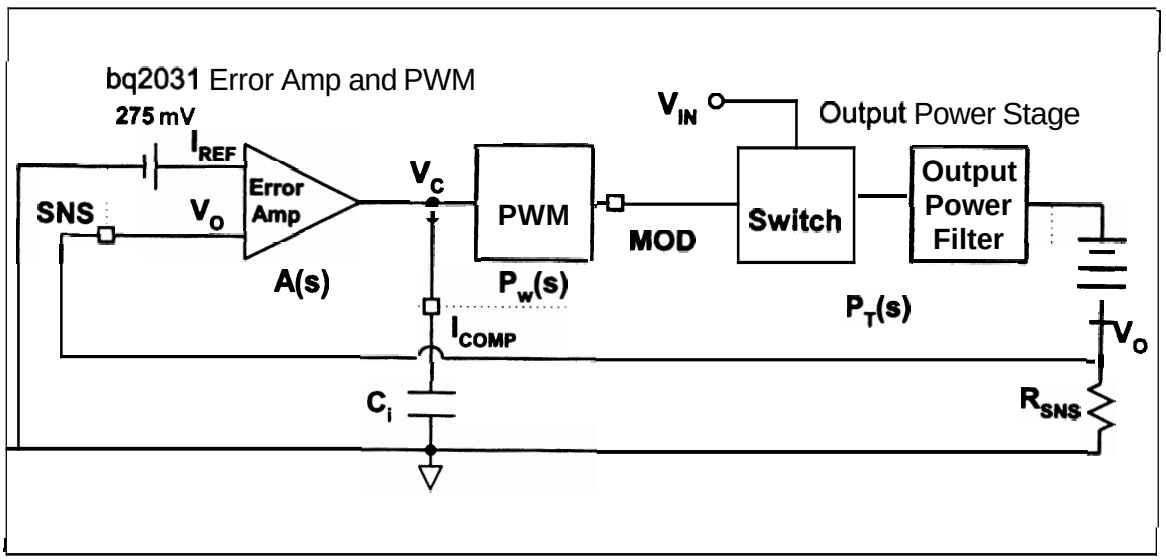


Figure 3. Model of Current Control Loop

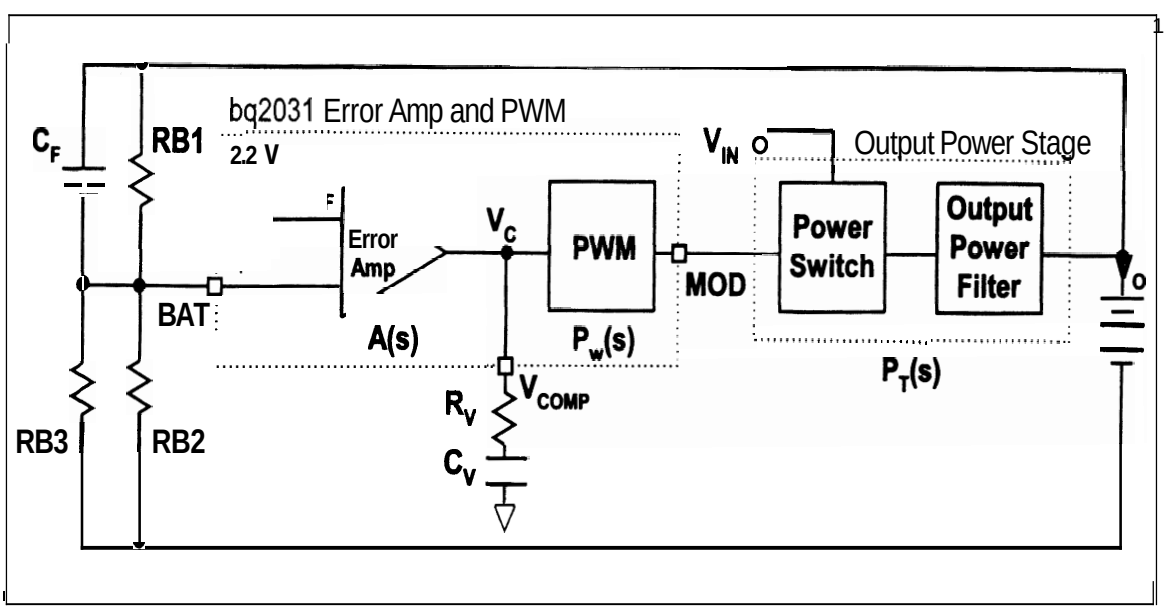


Figure 4. Model of Voltage Control Loop

For voltage regulation, the total open-loop transfer function, $V_L(s)$, may be expressed as:

Equation 3

$$V_L(s) = A(s) * P_\omega(s) * P_T(s)$$

where:

- $P_T(s)$ is the transfer function of the output power stage, V_O/D.

The switching frequency and circuit topology of the system dictate the gain-frequency characteristics of the output power stage. The PWM characteristics are fixed within the bq2031. This situation leaves the OTA and its associated compensation network as the only function block whose characteristics can be changed to achieve the desired loop stability and response.

The Error Amplifier

The bq2031 error amplifiers are the OTA (Operational Transconductance Amplifier) type. The parameters of interest (see Figure 6) are:

- Transconductance gain, g_m = 0.42 milli-mhos
- Output resistance of error amplifier, R = 250kΩ
- Gain Bandwidth product = 80MHz

This situation fixes the maximum voltage gain at 105 (g_m*R) or 40.4dB, which is good out to the 3dB corner frequency of 2MHz. Note that the 40dB gain is the maximum achievable, regardless of the impedance across the output to ground.

Criteria for Loop Stability

The gain and phase characteristics of the OTA and associated circuitry must be adjusted to meet the following three criteria for loop stability:

1. Total open-loop gain ($I_L(s)$ and $V_L(s)$ above) must be forced to 0dB at a crossover freauency (F_C) equal to at least 1/6 the switching frequency (F_S).
2. The phase of the total open-loop gain at F_C must be at least 45 degress less than 180 degrees.

The above criteria for loop stability can be easily achieved if the total loop-gain transfer function exhibits dominant pole characteristics as shown in Figure 5.

Stabilizing the Current Loop

From Equation 2, the total open-loop transfer function is expressed as:

$$I_L(s) = A(s) * P_\omega(s) * P_T(s)$$

$P_\omega(s)$ (the transfer function for the PWM) is given as:

$$P_\omega(s) = \frac{D_{MAX}}{V_S}$$

where:

- D_{MAX} is the maximum duty cycle of the PWM waveform
- Vs is the peak-tupeak amplitude of the sawtooth waveform

For the bq2031, Vs is fixed at 1.7V, and the maximum duty cycle is 80%. This condition reduces the PWM transfer function to:

Equation 4

$$P_\omega(s) = 0.47$$

$P_T(s)$ (the transfer function for the output power stage) is given as:

Equation 5

$$P_T(s) = \frac{V_{IN} * (1 + s * R_i * C_B) * R_{SNS}}{R_i + R_{SNS} + s[L + R_O R_L * C_B + R_{SNS} + R_i * C_B] + s^2 L * R_L * C_B}$$

where:

- s is the complex variable jω
- V_{IN} is DC input voltage
- C_B is the equivalent internal battery capacitance (see Figure 11)
- L is inductor value
- R_L is inductor resistance

  R_i is the equivalent internal battery resistance (see Figure 11)

- R_{SNS} is sense resistor value
- R_O is the equivalent battery load resistance (see Figure 11)

Stabilizing the current loop requires the compensation of the loop error amplifier to be such that the transfer function A(s) has dominant pole characteristics. This can be achieved by adding a capacitor, C_i, between ground and the output of the OTA error amplier as shown in Figure 6.

The transfer function A(s) is given as:

$$A(s) = \frac{V_C}{V_O} = \frac{(g_m * R)}{(1 + (s * R * C_i))}$$

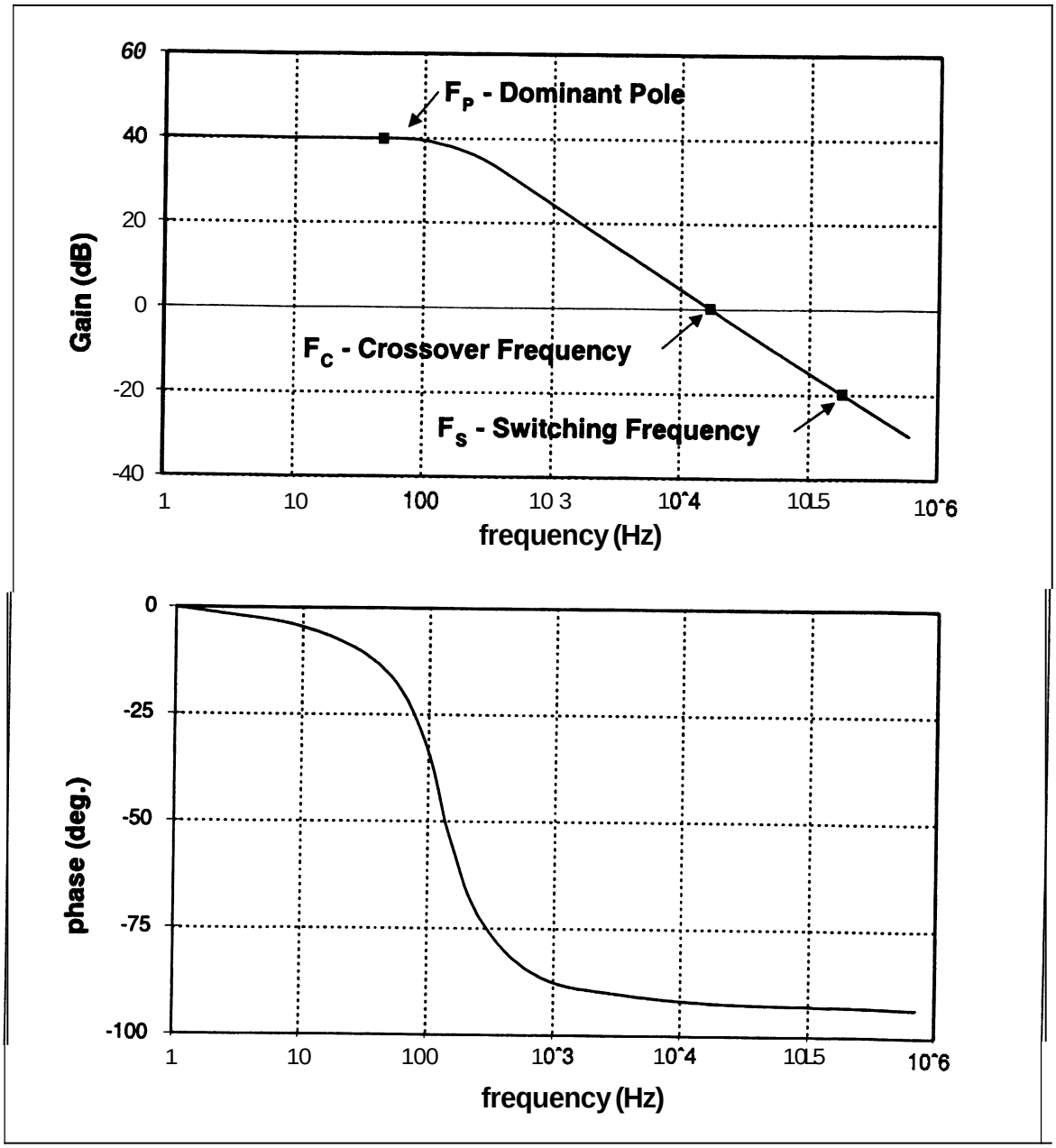


Figure 5. Target Gain and Phase Characteristics of a Stable Closed-Loop System

Substituting values for g_m and R, we get:

Equation 6

$$A(s) = \frac{105}{(1 + (s * 250000 * C_i))}$$

where:

- C_i is the output capacitance of the error amplifier (see Figure 6)

Substituting Equations 4 and 5 in Equation 2 gives the compensated total current loop gain transfer function:

Equation 7

$$I_L(s) = \frac{0.47 * V_{IN} * 105}{(1 + (s * 250000 * C_i))}$$

As shown in the bode plot for $I_L(s)$ (Figure 7), C_I can be varied to achieve the necessary phase and gain margin for different V_{IN} values.

Stabilizing the Voltage Loop

Recalling Equation 3, the voltage regulation open-loop transfer function can be expressed as:

$$V_L(s) = A(s) * P_m(s) * P_T(s)$$

The output power stage transfer function $P_T(s)$ depends on the inductor and battery impedances.

The components required to compensate the error amplifier for achieving voltage loop stability appear in Figure 8.

The resultant transfer function of the compensated error amplifier may be expressed as:

Equation 8

$$A(s) = \frac{D * 105 * (1 + s*RB1*C_F) * (1 + (s * R_V * C_V))}{(1 + s*D*RB_1*C_F) * (1 + s*(2.5*10^5 + R_V) * C_V)}$$

where:

- D = Battery voltage divider ratio during voltage regulation:

$$D = \frac{RB2 \;||\; RB3}{((RB2 \;||\; RB3) + RB1)}$$

  - Note: See the application note entitled 'Using the bq2031 to Charge Lead-Acid Batteries' for instructions on calculating RB1, RB2, and RB3.
- RB1 = the resistor value between the high side of the battery stack and the BAT pin in the battery voltage divider network
- C_F = the capacitance in parallel with RB1
- R_V = series resistance between V_{COMP} and ground
- C_V = series capacitance between V_{COMP} and ground

(see Figure 8 and Voltage Loop Error Amplifier Compensation below for calculating the values of C_F, R_V, and C_V.)

The above transfer function contributes two poles and two zeros.

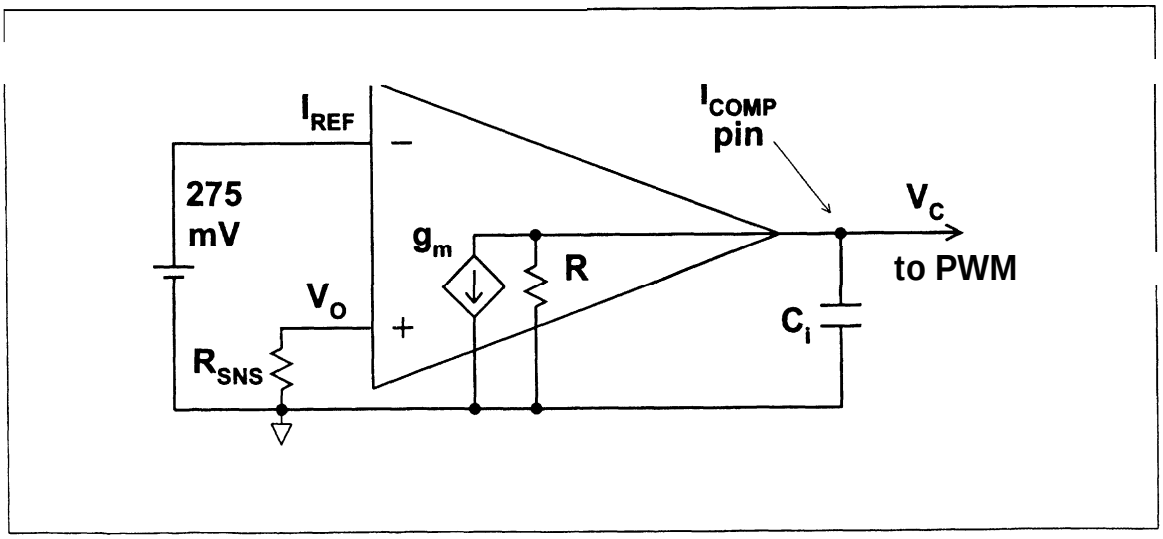


Figure 6. Compensation Network for the Current Loop

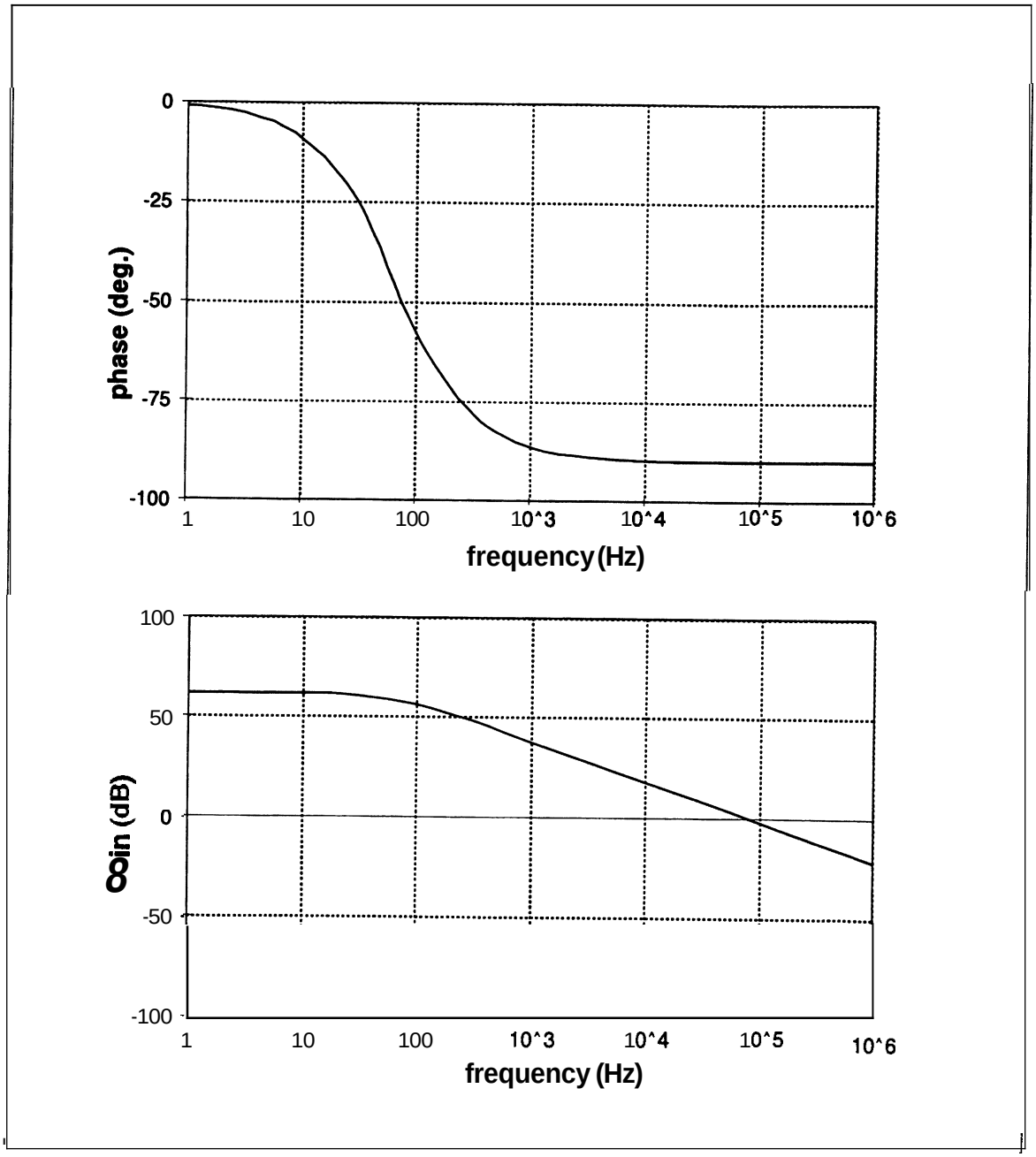


Figure 7. Bode Plot of the Current Loop-Gain

Transfer Function for V_{IN} = 24V

Poles (Equation 9)

$$fp1 = \frac{1}{(2\pi * (2.5 \bullet 10^5 + R_V) * C_V)}$$

$$fp2 = \frac{1}{(2\pi * D * RB1 * C_F)}$$

Zeroes (Equation 10)

$$fz1 = \frac{1}{(2\pi * RB1 \bullet C_F)}$$

$$fz2 = \frac{1}{(2\pi * R_V * C_V)}$$

The effect of this feedback and compensation network on the transfer function of A(s) is shown in Figure 9.

Voltage Loop Compensation for Buck Topology

Figure 10 shows a functional diagram of a switch-mode buck topology converter using the bq2031. The battery voltage is divided down to a per-cell equivalent value at the BAT pin. During voltage regulation, the voltage on the BAT pin (V_{BAT}) is regulated to the internal band-gap reference of 2.2V (with a temperature drift of -3.9mV/°C). The charge current through the inductor L is sensed across the resistor R_{SNS}. During current regulation, the bq2031 regulates the voltage on the SNS pin (V_{SNS}) to a temperature-compensated reference of 0.275V. This in turn regulates the current to I_{MAX}, provided that a properly designed resistor network is in use.

The passive component C on the I_{COMP} pin and R_V and C_V on the V_{COMP} pin form the phase compensation network for the current and voltage control loops, respectively. The diode (D_{b1}) prevents battery drain when VDC is absent, while the pull-up resistor (R) detects battery removal. The resistor R13, typically a few tens of mΩ, is optional and depends on the battery impedance and the resistance of the battery leads to and from the charger board.

The Output Power Stage

The output power stage in a buck topology charger comprises the inductor L and the parallel combination of the output capacitor, C_O, and impedance of the battery (see Figure 12). The output capacitor is electrolytic and in the range from 47µF to 100µF. It nullifies the inductive effect of long leads from the charger terminals to the battery.

Inductor Selection

The inductor selection criteria for a DC-DC buck converter vary depending on the charging algorithm used. For the Two-Step Current and Pulsed Current charge algorithms, the inductor equation is:

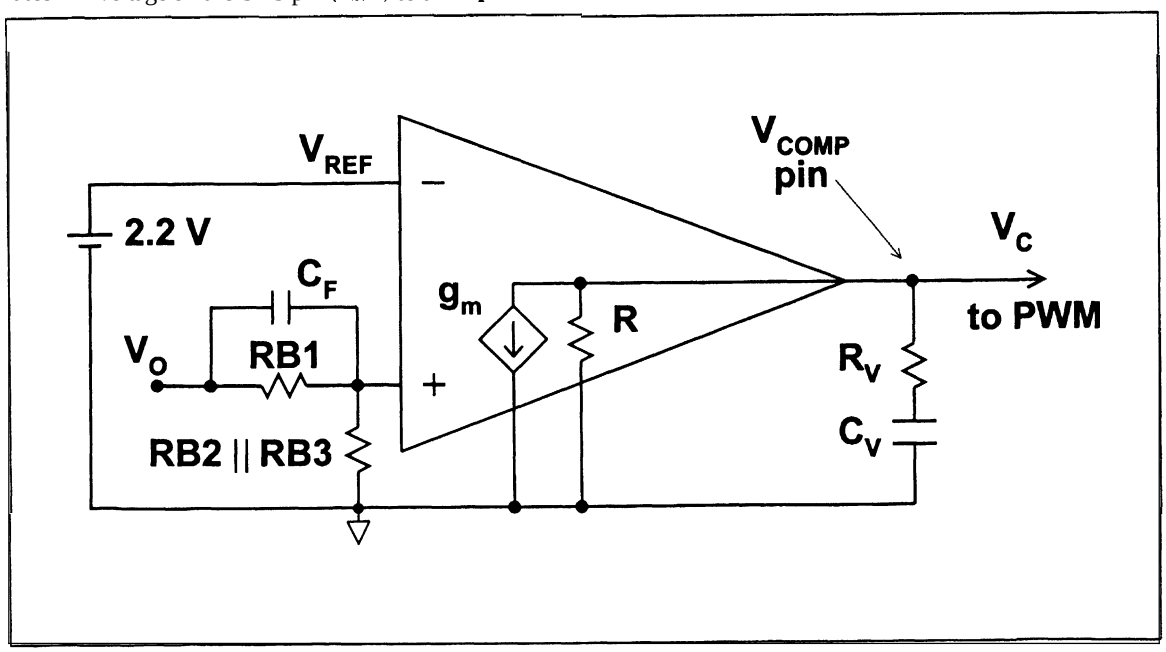


Figure 8. Compensation Network for the Voltage Loop

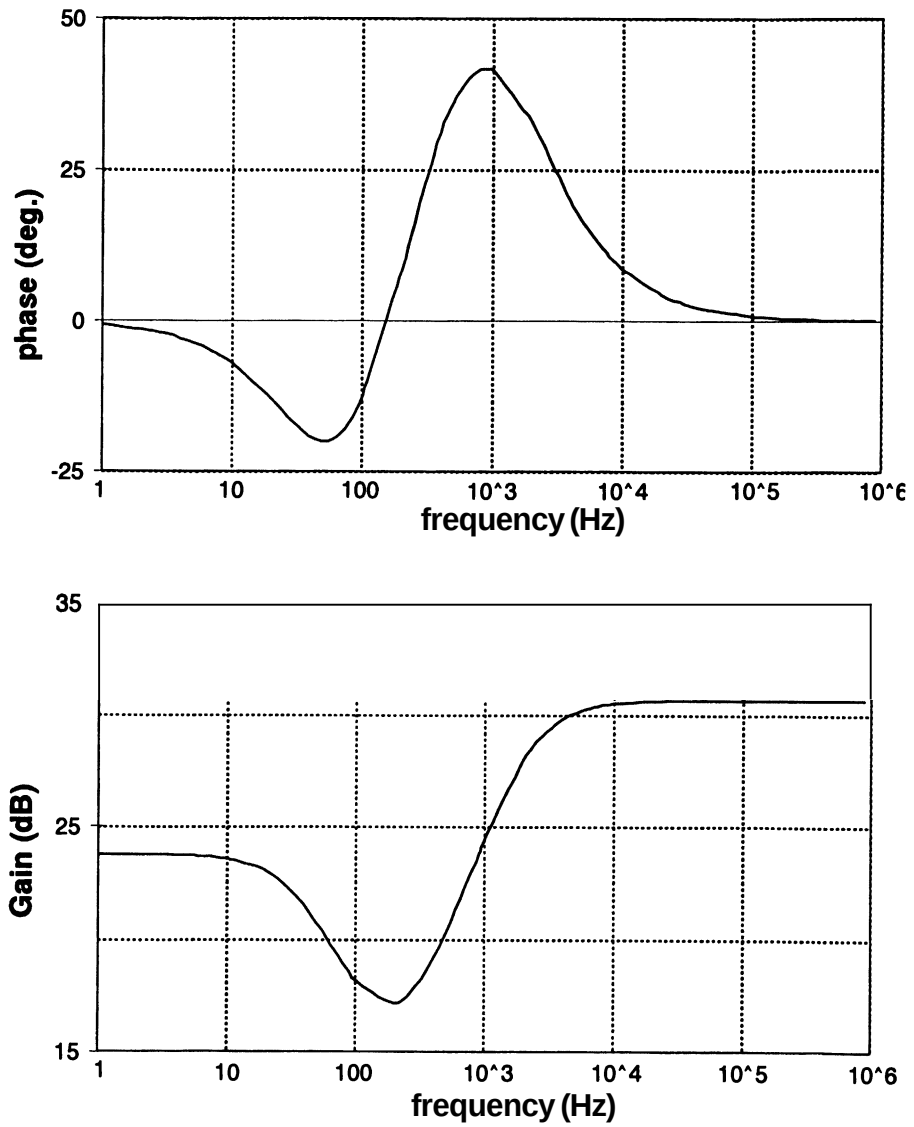


Figure 9. Effect of Compensation Network on Amplifier Transfer Function, A(s)

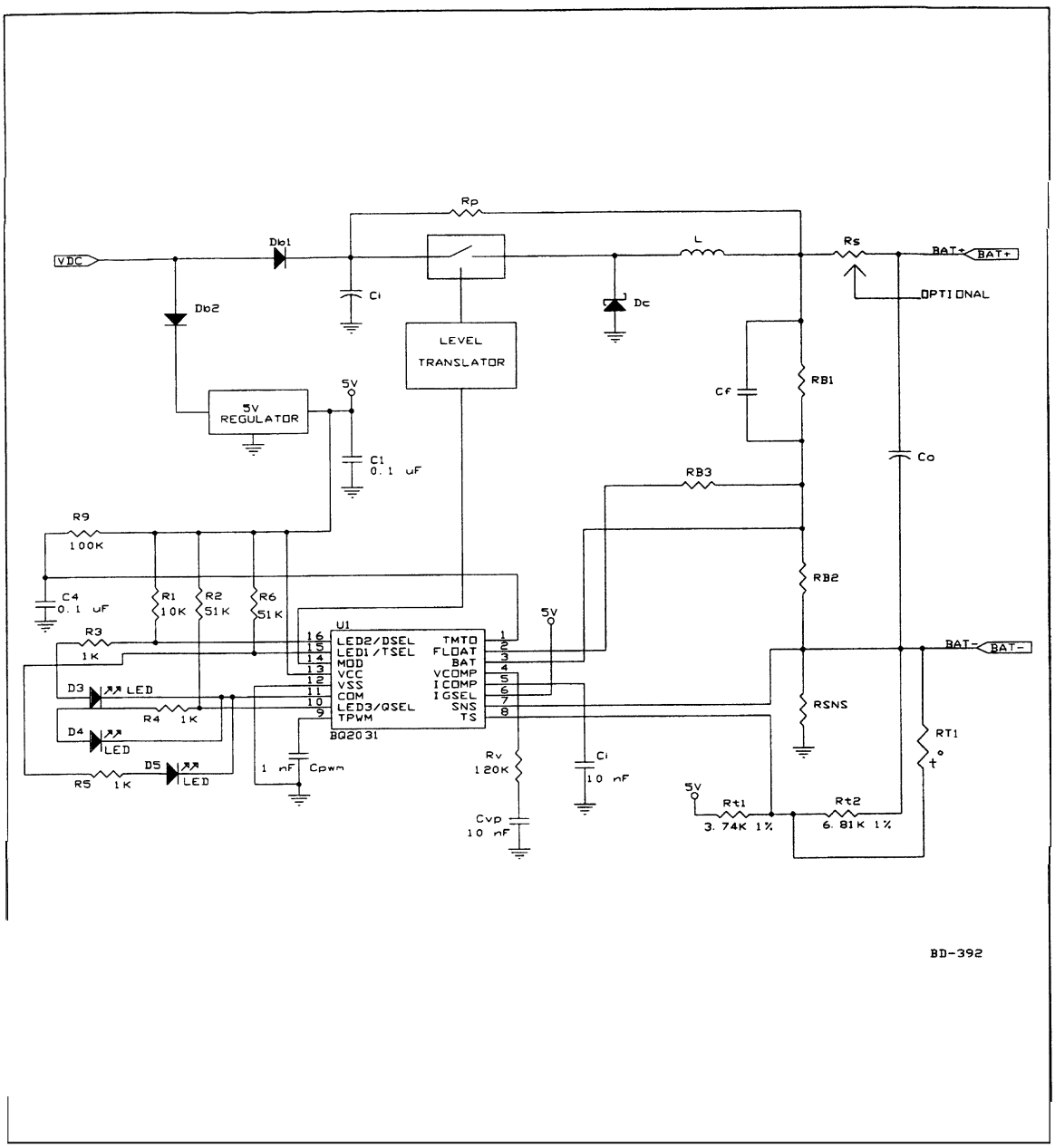


Figure 10. Functional Diagram of a Switch-Mode Buck Regulator Lead-Acid Charger Using the bq2031

Equation 11

$$L = \frac{(N * V_{BLK} * 0.5)}{F * \Delta I}$$

where:

- N = number of cells
- V_{BLK} = bulk voltage per cell, in volts
- Fs = switching frequency, in hertz
- ΔI = ripple current at I_{MAX}, in amps

The ripple current is usually set between 20–25% of I_{MAX}.

Example: A 6-cell SLA battery is to be charged at I_{MAX} = 2.75A in a buck topology running at 100kHz. The V_{BLK} threshold is set at 2.45V per cell and the charger is configured for Pulsed Current mode. Assuming a ripple = 25% of I_{MAX}, the inductor value required is:

$$L = \frac{(6 * 2.45 * 0.5)}{(10^5 * 0.6875)} = 107\mu H$$

The inductor current, which must remain continuous down to I_{MIN} during Fast Charge phase 2 (voltage regulation phase), dictates the inductor formula for the Two-Step Voltage charge algorithm.

Equation 12

$$L = \frac{N * V_{BLK} * 0.5}{F_S * 2 * I_{MIN}}$$

Example: A 6-cell SLA battery is to be charged at IMAX = 2.75A in a buck topology running at 100 kHz. The V_{BLK} threshold is set at 2.45V per cell and the charger is configured for Two-Step Voltage mode, with $I_{MIN} = I_{MAX/20}$. The inductor value required is:

$$L = \frac{6 * 2.45 * 0.5}{(10^5 * 2 * 0.1375)} = 267\mu H$$

Model of a Lead Acid Battery

The battery impedance can be represented as a capacitor (C_B) in series with its internal impedance (R) as shown in Figure 12. The capacitance can be empirically derived from the amp-hour rating of the battery. The rule of thumb is:

$$C_B = 100 * C$$

where C = the capacity of the battery in ampere-hours.

The internal resistance Ri of a lead-acid battery is dictated by:

- Number of cells, N
- Amp-hour capacity, C
- State of charge

Figure 12 shows the variation of the internal impedance of a Yuasa NP6-12 (12V, 6 amp-hrs) battery as a function of its state of charge.

An average value of the impedance swing is recommended for use in loop stability equations. For example, with the battery above we recommend using R = 0.0552.

The resistor R_O models the loading effects of the battery when a voltage equivalent to V_{BLK} (typically 2.45V/cell) is applied across the battery. The range of values R_O takes on depends on the bulk charge current, the bulk voltage, and the I_{MIN} to I_{MAX} ratio. For example: A 12V

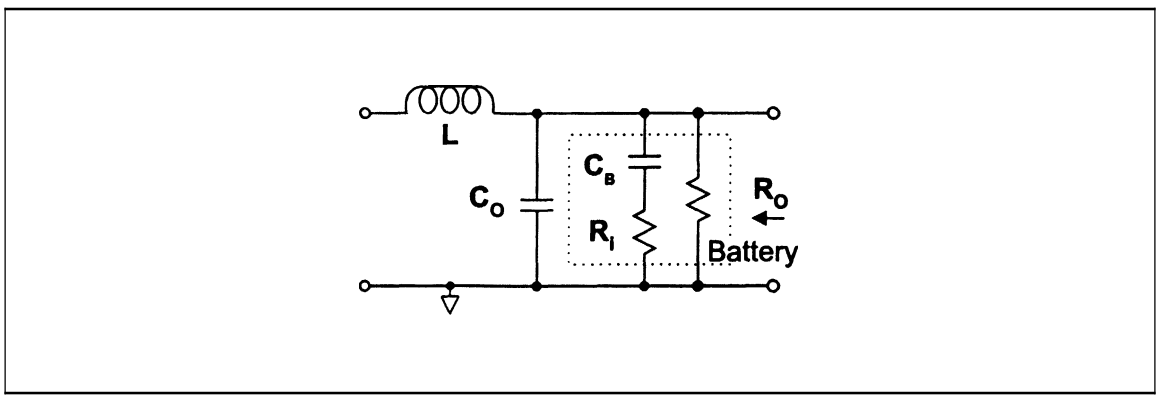


Figure 11. Model of Output LC Filter for Buck Topology

battery being charged at I_{MAX} = 3A will exhibit the following range with a I_{MIN}/I_{MAX} ratio of 1:20.

$$R_{L(min)} = 6 * \frac{2.45}{3} = 4.921$$

$$R_{L(max)} = 6 * \frac{2.45}{0.15} = 98\Omega$$

Use the minimum value for worst case scenario of loop stability.

The Power Stage Transfer Function

The transfer function of the output power stage, $P_T(s)$ can be expressed as:

Equation 13

$$P_T(s) = \frac{V_{IN} * (1 + (s * R * C_B))}{(1 + (s/\omega_0)^2 + (s * (R_i C_B + 1/R_O)))}$$

where:

$$\omega_0 = 1/\sqrt{L * C_B}$$

The poles and zeros of $P_T(s)$ are:

Equation 14

$$fzo = \frac{1}{(2\pi * R_i * C_B)}$$

$$fpo = 1/(2\pi * \sqrt{L * C_B})$$

A second pole is not used in these calculations:

$$\frac{1}{2\pi * (R_i C_B + 1/R_O)}$$

Typical Switch-Mode Buck Charger Specifications

The application specifications for a switch-mode buck topology charger are usually given as:

- DC input voltage, V_{IN} = 20 to 30V
- Switching frequency, F_S = 100kHz, T = 10µs
- Charge algorithm = Two-Step Voltage mode:
  - V_{BLK} = 2.45V/cell , Vflt = 2.2V/cell
  - I_{MAX} = 3A, I_{MIN} = I_{MAX}/30 = 300mA
- Battery specs: 12V, 10A-hr, Internal impedance: 0.02 to 0.07Ω

PWM and Output Power Stage Transfer Functions

Starting again from the basic voltage regulation loop-gain transfer function (Equation 3) is given as:

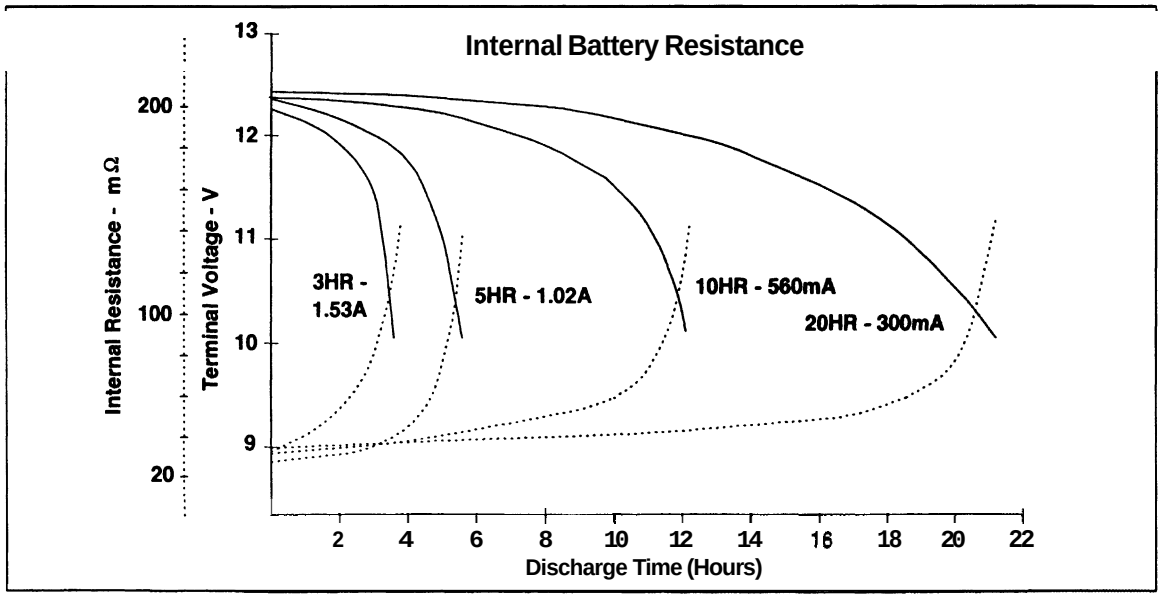


Figure 12. Internal Resistance of Yuasa NP6-12 Battery vs. State of Charge

$$V_L(s) = A(s) * P_w(s) * P_T(s)$$

This equation can be written as:

$$V_L(s) = A(s) * G(s)$$

where G(s) is the combined transfer function of $P_{w(s)}$ and $P_T(s)$

Combining Equations 4 and 13:

Equation 15

$$G(s) = \frac{0.47 * V_{IN} * (1 + (s * R * C_B))}{(1 + (s/\omega_0)^2 + (s * (R_i C_B + 1/R_O)))}$$

Based on the typical values in the section above, the worst case values for loop parameters are:

- V_{IN} = 30 V
- R_i = 0.05Ω
- C_B = 100 * 10 = 1000µF
- R_O = 4.9Ω

From Equation 12:

$$L = \frac{(6 * 2.45 * 0.5)}{(10^5 * 2 * 0.1)} = 367.5\mu H$$

The resulting bode plots for G(s) are shown below.

Since the plots exhibit similar characteristics to that of the output power filter, we can use Equation 14 to determine the poles and zeros:

- f_{po} = 263Hz
- f_{zo} = 3183Hz

Voltage Loop Error Amplifier Compensation

For this control loop, we must find appropriate values for Rv and Cv, the compensation components for the V_{COMP} pin. From Table 3 of "Using the bq2031 to Charge Lead-Acid Batteries" the values for the divider network components are:

- RB1=261K
- RB2=49.9K
- RB3= 475K

Therefore

$$D = \frac{(RB2 * RB3)}{(RB2 * RB3 + (RB1 * (RB2 + RB3)))} = 0.15$$

From the first criterion for loop stability, set the crossover frequency F_C (0 dB loop-gain) to 1/20th the switching frequency:

$$F_C = F_S/20 = 5kHz$$

Set the two zeros of A(s), fz1 and fz2, at 1/2 to cancel the second order poles of G(s) at f_{po}:

$$f_{z1} = f_{z2} = f_{po}/2 = 263/2 = 131.5\ Hz$$

From Equation 10's first zero, fz1:

$$C_F = \frac{1}{(2\pi * RB1 * f_{z1})} = \frac{1}{(2\pi * 2.61 * 10^5 * 131)} = 4.63nF$$

From Equation 9's second pole, fp2:

$$f_{p2} = 865\ Hz$$

In order to achieve 0 dB loop-gain at Fc the compensated amplifier gain at fp2 must be forced to the absolute gain of G(s) at the crossover frequency, which can determined from the Bode plot in Figure 13 to be -31dB = 35.48.

The value for Rv can be determined from the gain magnitude equation for A(s) at fp2

$$A(f_{p2}) = \frac{105 * D * R_V}{2.5 * 10^5 * R_V}$$

Using the value of 35.48 for A(fp2) in the above equation gives:

$$R_V = \frac{35.48 * 2.5 * 10^5}{35.48 - 15.75} = 450k\Omega$$

Plugging this value for Rv into equation 10 for fz2 yields:

$$C_V = \frac{1}{2\pi * 450 * 10^3 * 131} = 2.7nF$$

Substituting these values for Rv and Cv in equation 10 for fp2 gives:

$$f_{p2} = \frac{1}{2\pi * (450k\Omega + (2.5 * 10^5)) * 2.7nF} = 84.2Hz$$

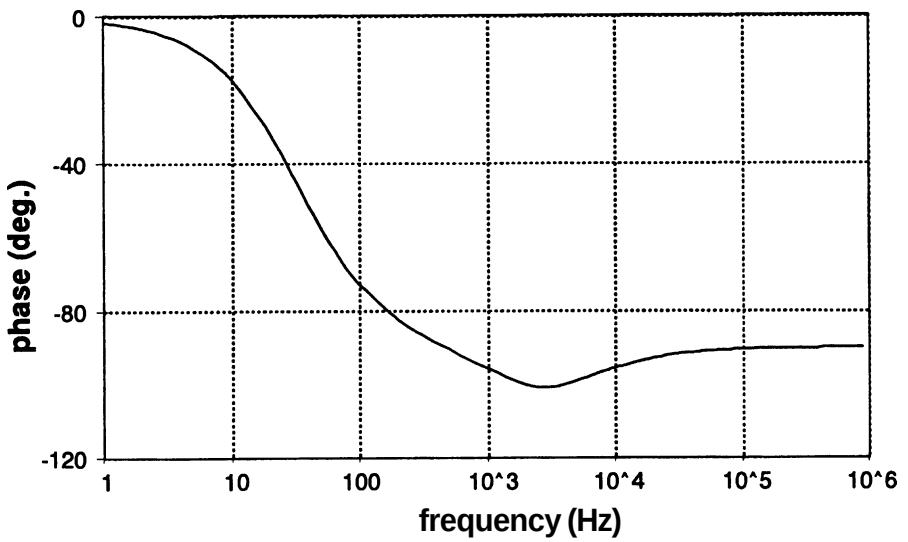
Figures 14 and 15 show the resultant Bode and loop gain plots for A(s), respectively.

Current Loop Error Amplifier Compensation

For this control loop, we must find the value for C_i, the compensation component for the I_{COMP} pin. The compensation network component Ci must be chosen such that the current loop gain transfer function has a dominant pole at 1/20th of the switching frequency, F(s).

$$\frac{1}{2\pi * (2.5 * 10^5) * C_i} = 131.5$$

$$C_i = \frac{1}{2\pi * (2.5 * 10^5) * 131.5} = 4.84nF$$



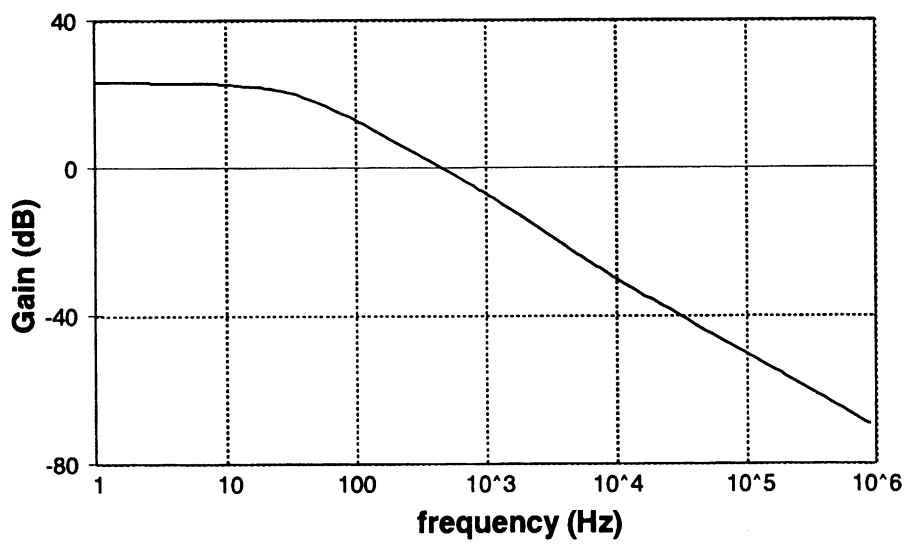


Figure 13. Bode Plot for G(s)

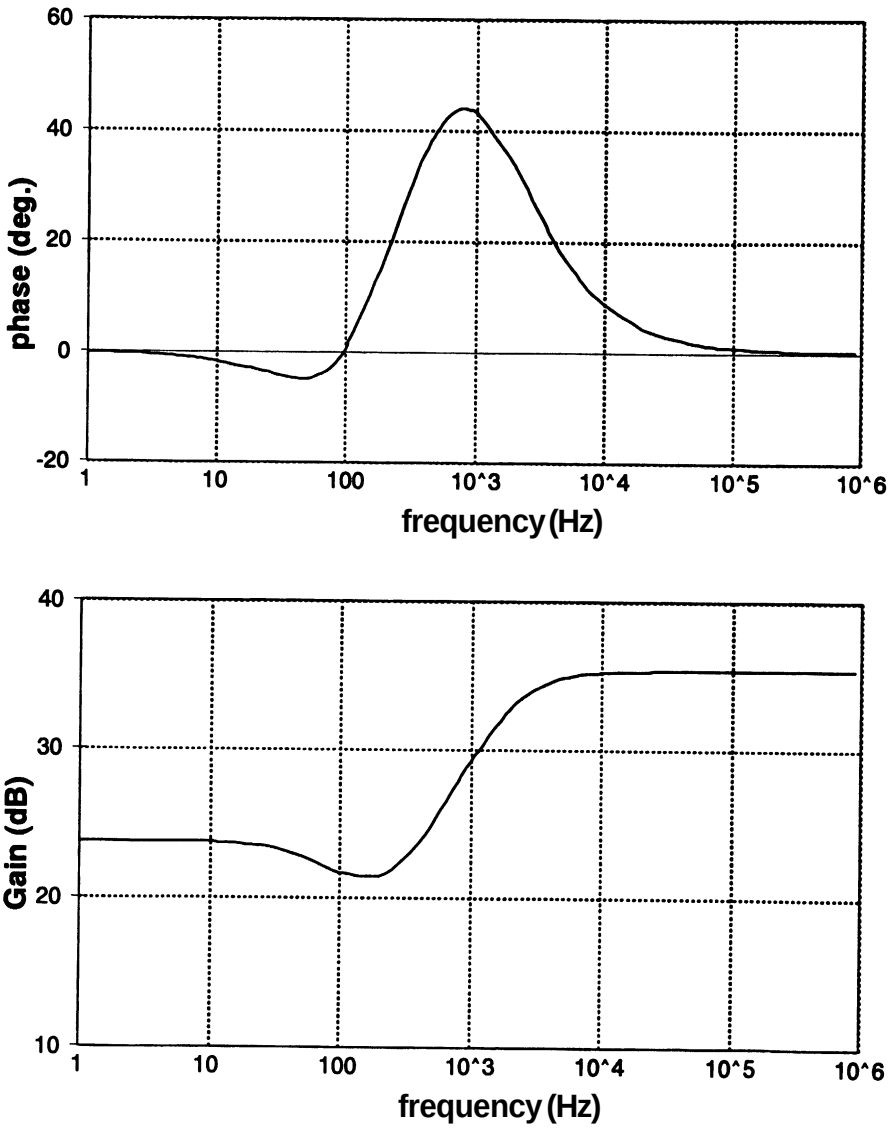


Figure 14. Bode Plot for Error Amplifier, A(s)

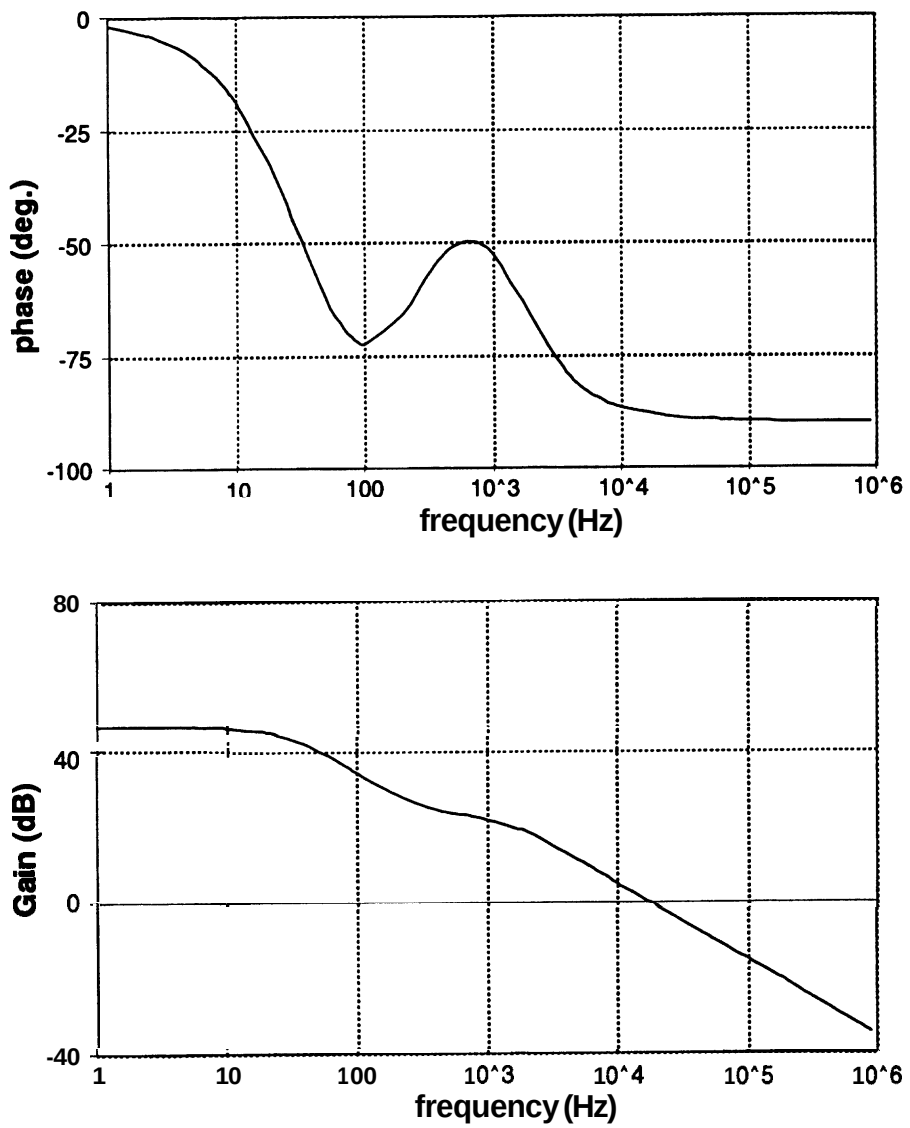


Figure 15. Loop Gain Bode/Example Buck Charger Design

bq2053x

Lithium Ion Pack Supervisor

Features

- Protects and individually monitors two to four Lithium Ion series cells from overvoltage, undervoltage, and overcurrent
- Designed for battery pack integration
  - Small outline package, minimal external components and space, and low cost
  - Drives external N-FET switches
- User-selectable thresholds mask programmable by Benchmarq
- Operates on very low current, <40µA for 4-cell, <20µA for 3-cell, and <15µA for 2-cell configuration
- Operates on very low standby current, < 1µA
- Available in 8-pin 150-mil narrow SOIC

General Description

The bq2053 Lithium Ion Pack Supervisors are designed to control the charge and discharge voltage safety limits for two to four lithium ion (Li-Ion) series cells, accommodating battery packs containing series/parallel configurations. The very low operating current does not overdischarge the cells during periods of storage, and does not significantly increase the system discharge load. The bq2053 can be part of a low-cost Li-Ion charge control system within the battery pack.

The bq2053 controls two external N-FETs to limit the charge and discharge potentials. Charging is allowed when the per cell voltage is below V_{CE} (charge enable voltage). When the voltage on any cell rises above V_{OV} (overvoltage limit), the CHG pin goes low, shutting off charge to the battery pack. This safety feature prevents overcharge of any cell within the battery pack.

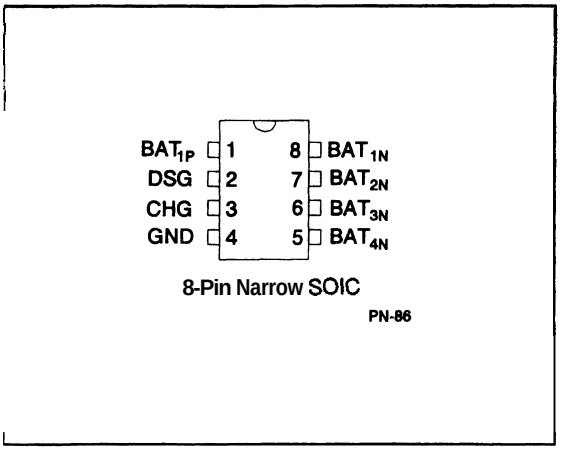
Discharge is allowed when the per-cell voltage is above V_{UV} (undervoltage limit).

If the voltage across any cell falls below V_{UV}, the DSG output goes low, shutting off the battery discharge. This safety feature prevents overdischarge of any cell within the battery pack.

Charging and discharging are allowed if the voltage across BAT_{4N} and GND is less than V_{OC} (overcurrent limit). This safety feature prevents excessive pack current.

V_{UV}, V_{CE}, and V_{OV} are programmed at Benchmarq. The default limits for V_{UV} and V_{CE} are 2.3V and V_{OV} - 100mV, respectively. Five V_{OV} limits are available (see Table 2). Contact Benchmarq for other options.

Pin Connections



8-Pin Narrow SOIC

PN-86

Pin Names

BAT_{1P}	Battery 1 positive input
BAT_{1N}	Battery 1 negative input
BAT_{2N}	Battery 2 negative input
BAT_{3N}	Battery 3 negative input
BAT_{4N}	Battery 4 negative input
DSG	Discharge control
CHG	Charge control
GND	Ground

Pin Descriptions

BAT_{1P} Battery 1 positive input

This input is connected to the positive terminal of the cell designated BAT_1 in Figure 2.

BAT_{1N} Battery 1 negative input

This input is connected to the negative terminal of the cell designated BAT_1 in Figure 2. This input is connected to BAT_{1P} for less than four cells in a series.

BAT_{2N} Battery 2 negative input

This input is connected to the negative tennInal of the cell designated BAT_2 in Figure 2. This input is connected to BAT_{1P} and BAT_{1N} for leas than three cells in a s e d .

BAT_{3N} Battery 3 negative input

This input is connected to the negative tennInal of the cell designated BAT3 in Figure 2.

BAT_{4N} Battery 4 negative input

This input is connected to the negative terminal of the cell designated BAT4 in Figure 2

CHG Charge control output

This output controls the charge path to the battery pack. This output is internally connected to BAT_{1P} when charging is allowed (CHG = High). CHG is internally connected to GND when charging is prohibited (CHG = Low).

DSG Discharge control output

This output controls the discharge path to the battery pack. This output is internally connected to BAT_{1P} when discharging is allowed (DSG = High). DSG is internally connected to BAT_{4N} when discharging is prohibited (DSG = Low).

GND System Ground

Battery pack return.

Functional Description

Figure 1 is a block diagram outlining the major components of the bq2053. Figure 2 shows a typical application example. The various functional aspects of the bq2053 are detailed in the following sections.

Configuration

The bq2053 may be configured to supervise two-, three-, or four-series cell packs. For two-series cell configurations, BAT_{1N} and BAT_{2N} are connected to BAT_{1P}. For three-series cell configurations, BAT_{1N} is connected to BAT_{1P}. See Table 1. The bq2053 controls two external N-FETs connected for low-side control of the battery pack. Contact Benchmarq for application examples.

Table 1. Pin Configuration for 2-, 3-, and 4-Series Cells

Number of Cells	Configuration Pins	Battery Pins
2 cells	BAT_{1N}, BAT_{2N} tied to BAT_{1P}	BAT_{2N} – Negative terminal of second cell
		BAT_{3N} – Negative terminal of third cell
		BAT_{4N} – Negative terminal of fourth cell
3 cells	BAT_{1N} tied to BAT_{1P}	BAT_{1N} – Positive terminal of first cell
		BAT_{2N} – Negative terminal of first cell
		BAT_{3N} – Negative terminal of second cell
		BAT_{4N} – Negative terminal of third cell
4 cells	–	BAT_{1P} – Positive terminal of first cell
		BAT_{1N} – Negative terminal of first cell
		BAT_{2N} – Negative terminal of second cell
		BAT_{3N} – Negative terminal of third cell
		BAT_{4N} – Negative terminal of fourth cell

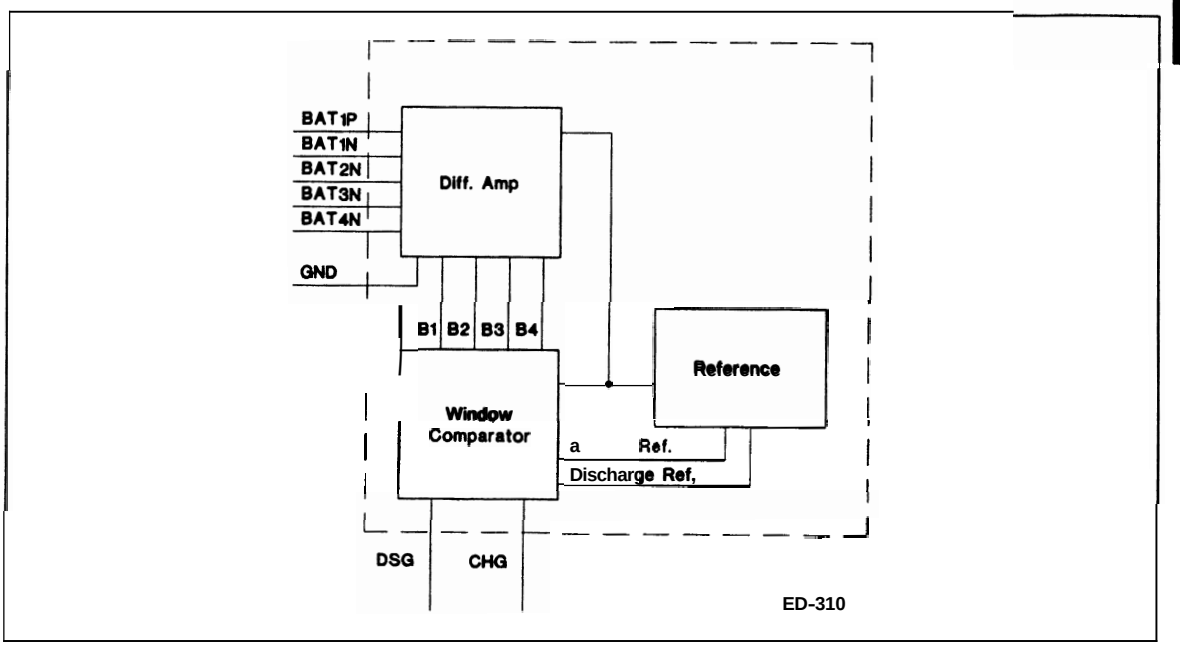


Figure 1. Block Diagram

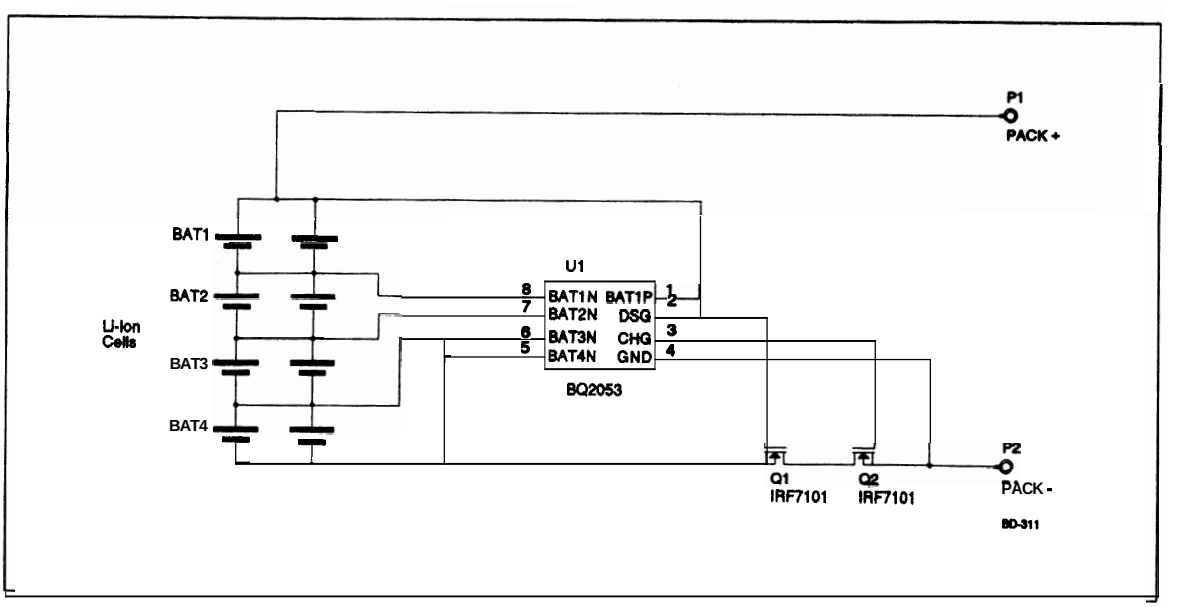


Figure 2. Application Diagram: 4x2 Cell Configuration

Thresholds

The bq2053 monitors four thresholds for overcharge, overdischarge, and overcurrent protection. The default values are listed below.

Overvoltage during charge:

Table 2. Overvoltage Threshold Options

Part #	V_{OV} Limit	Tolerance
bq2053M	4.15V	±1.5% (3, 4 cell) ±1.7% (2 cell)
bq2053F	4.20V	
bq2053	4.25V	
bq2053D	4.30V	
bq2053J	4.36V	

Charge enable voltage:

$V_{CE} = V_{OV} - 100mV \pm 50mV$

Undervoltage during discharge:

$V_{UV} = 2.3V \pm 100mV$

Overcurrent limit during charge and discharge:

±250mV ±25mV

These thresholds are programmed at Benchmarq. Please contact Benchmarq for other voltage threshold and tolerance options.

The bq2053 samples a cell every 25ms (typical) and each measurement is fully differential. During this sample period, the cell is checked for a Vov, V_{UV}, V_{OC}, V_{MIN}, and V_{CE} condition. Please refer to Figure 3 for the cell monitoring timing.

Initialization

During the initial connection of the bq2053 circuit to the battery pack, the bq2053 recognizes a low voltage condition, and disables the DSG output. A charging supply must be applied to the bq2053 circuit to enable the pack. The charging supply must produce a voltage of greater than 30mV between BAT_{4N} and GND for the bq2053 to recognize a valid charge condition, and enable the DSG output.

The bq2053 operating current is leas than 40µA in a 4-cell, 25µA in a 3-cell, and 15µA in a 2-cell configuration. This feature avoids possible cell damage due to overdischarging the battery pack and extends the storage time between recharge.

Discharge Supervision

Overdischarge protection is asserted when any cell voltages fall below the V_{UV} threshold. Once V w is reached, DSG goes low, disabling the discharge of the pack. The bq2053 then enters the low-power standby mode.

Low-Power Standby Mode

When the bq2053 enters the low-power mode, DSG is disabled and the device consumes less than 1µA. The differential signal between BAT_{4N} and GND is then continuously monitored to determine if a valid charge condition exists. If the condition exists, the output is enabled to allow charging of the lithium ion cells. The charging supply must produce a voltage greater than 30mV between BAT_{4N} and GND for the bq2053 to enable the DSG output. If charging is terminated while any cell is below the V_{UV} limit, DSG goes low, and the bq2053 returns to the low-power mode.

Charge Supervision

Overvoltage protection is asserted when any cell voltage exceeds the V_{OV} threshold. Once Vov is reached, the CHG pin goes low, disabling charge into the battery pack. Charging is disabled until all cell voltages fall below V_{CE}. This indicates that the overcharge has stopped and the pack is ready to accept further charge.

The bq2053 can be part of a cost-effective charge control system which utilizes the pack protection circuit to limit the charge voltage to the lithium ion cells. The hysteresis between V_{OV} and V_{CE} allows the lithium ion cell voltage to fall sufficiently before re-enabling the charge current.

Over-Current Supervision

The voltage across the BAT_{4N} and GND pins is sampled approximately every 25ms for an overcurrent condition. If the bq2053 determines an overcurrent condition exists (either charge or discharge), it disables the CHG and DSG outputs. After an overcurrent condition is detected, the bq2053 then re-enables the CHG and DSG outputs for approximately 6ms every 100ms to determine if the condition still exists. If the voltage between BAT_{4N} and GND is less than 250mV (typical), the bq2053 allows charging or discharging to continue, resets the overcurrent test, and once again begins sampling for an overcurrent situation.

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_T	Voltage applied on any pin relative to BAT_{1P}	-18 to +0.31	V	
T_{OPR}	Operating temperature	-30 to +85	°C	
T_{STG}	Storage temperature	-55 to +125	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

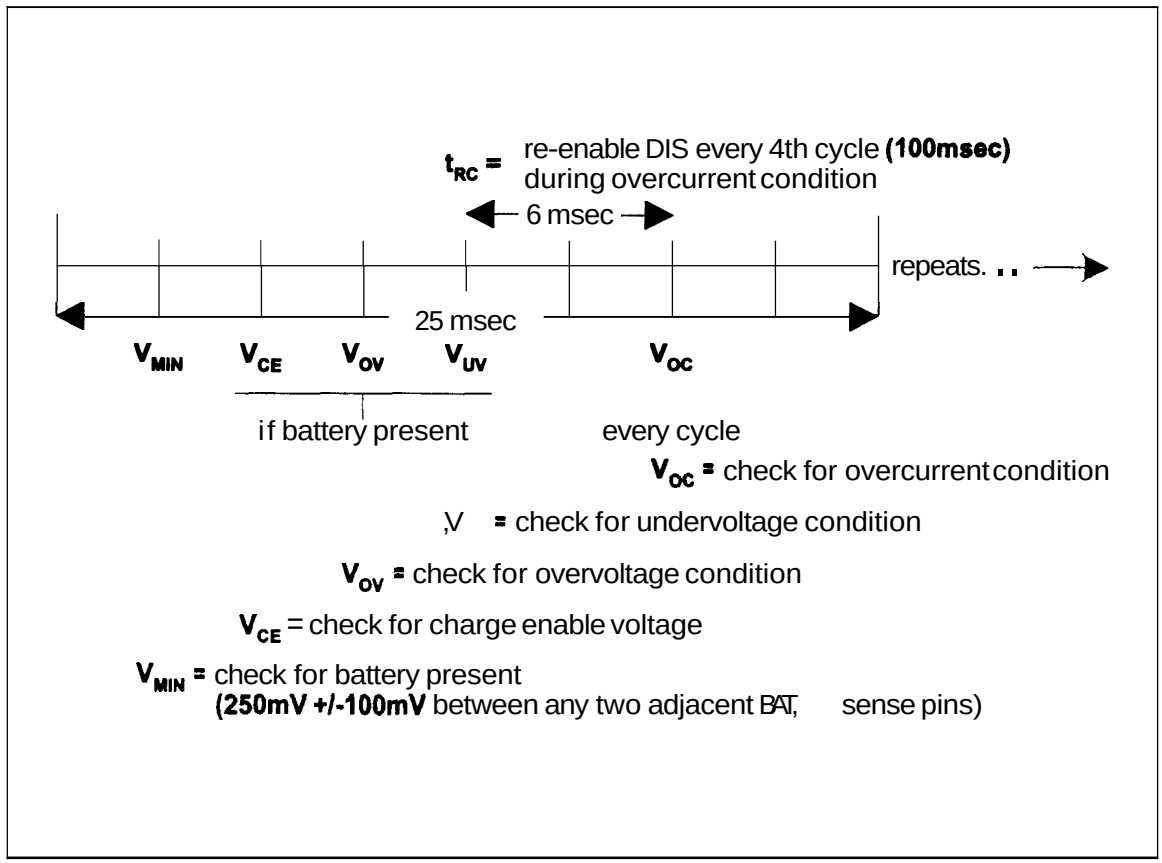


Figure 3. Cell Monitor Timing

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbd	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
V_{OH}	Output high voltage	BAT_{1P} - 0.5	-		V	I_{OH} = 50µA, CHG, DSG
V_{OP}	Operating voltage	3.0		18	V	
V_{OL}	Output low voltage			BAT_{4N} +0.5	V	I_{OL} = 50µA, DSG
				GND + 0.5	V	I_{OL} = 50µA, CHG
I_{CC}	Operating current 2-cell		7	15	µA	
	Operating current 3-cell		12	25	µA	
	Operating current 4-cell		25	40	µA	
I_{CCLP}	Low power current	-	-	1	µA	
$R_{BAT1N, 2N, 3N}$	Battery input impedance		10		MΩ	

DC Thresholds ($T_A = T_{OPR}$)

Symbol	Parameter	Value	Unit	Tolerance	Conditions/Notes
V_{OV}	Overvoltage limit	See Table 1	V	± 1.5%	3- or 4- cell
				±1.7%	2-cell
V_{CE}	Charge enable voltage	Vov - 100mV	V	± 50mV	
V_{UV}	Undervoltage limit	2.3	V	± 100mV	
Voc	Overcurrent limit	± 250	mV	± 25mV	

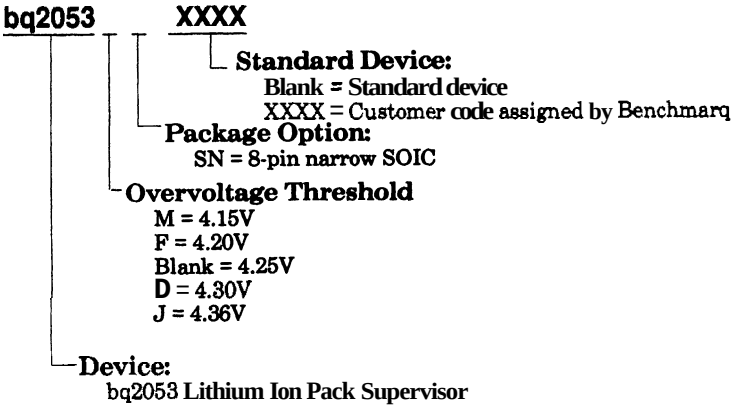
Note: Standard device. Contact Benchmarq for different threshold options.

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	1, 4	Modified CHG state during discharge	Was: CHG = Low when $V_{CELL} = V_{UV}$ Is: CHG = High when $V_{CELL} = V_{UV}$
1	4, 5	Overcurrent re-enable sample rate	Was: 12ms Is: 6ms
2	1, 2, 4, 6	2-cell configuration references removed	
2	4	Reworked Thresholds section with addition of Table 2	
2	5	New Cell Monitor Timing diagram (Figure 3)	

Note: Change 1 = Feb. 1996 B 'Final' changes from Dec. 1994 *Advanced Information.'
Change 2 = Sept. 1996 C changes from Feb. 1996 B.

Ordering Information



Using the bq2053 Lithium Ion Pack Supervisor

Description of Operation

The bq2053 Lithium Ion Pack Supervisors are a family of low-cost safety devices designed to enforce high and low battery voltage limits during charge and discharge plus short-circuit protection for two-, three-, or four-seriee cell Li-Ion battery packs.

The bq2053 individually monitors each cell in the pack to determine if either an overvoltage or an undervoltage condition exists. Tne bq2053 incorporates overvoltage and undervoltage protection, breaking the battery charge or discharge path, as appropriate, if any cell voltage becomes greater or less than predefined limits. In addition, the bq2053 includes an overcurrent feature designed to protect against an accidental pack short-circuit.

The bq2053 uses two external FETs to control the charge and discharge paths to the batteries. Their extremely low operating current does not overdischarge the cells during periods of storage and does not significantly increase the load on the battery. The chips are usable as part of a simple, low-cost, voltage hysteresis Li-Ion charge control system contained entirely within the battery pack.

The bq2053 family allows multiple cells in parallel in each aeries rank. This document will always refer to a single-cell per series rank. If multiple cells are configured in parallel in a single rank, careful matching of cells during pack assembly by state-of-charge, manufacturer, age, and lot number is recommended.

Overvoltage Protection

Charging can occur whenever the voltage of each pack cell is below V_{CE} (charge enable voltage). When any individual cell voltage rises above V_{OV} (overvoltage limit), the charge FET control pin (CHG) is driven to GND, disconnecting the charger from the pack This feature prevents overcharging on a cell-by-cell basis. CHG remains at GND until all cells are once again less than V_{CE}.

Undervoltage Protection

Discharge can occur whenever the voltage of each cell is above V_{UV} (undervoltage limit). If any individual cell voltage falls below V_{UV}, the discharge FET control pin (DSG) is driven to BAT_{4N}, disconnecting the load from the pack. The bq2053 is also placed in a sleep mode in which it consumes less than 1µA of current. This undervoltage protection feature prevents overdischarge on a cell-by-cell basis. DSG remains at BAT_{4N} and the chip remains in sleep mode until the voltage at GND becomes less than that at BAT_{4N} by the charge detect threshold value (V_{CD}). This condition indicates the presence of a charging source.

Table 1. Pin Configuration for 2-, 3-, and 4-Series Cells

Number of Cells	Configuration Pins	Battery Pins
2 cells	BAT_{1N}, BAT_{2N} tied to BAT_{1P}	BAT_{2N} – Negative terminal of second cell
		BAT_{3N} – Negative terminal of third cell
		BAT_{4N} – Negative terminal of fourth cell
3 cells	BAT_{1N} tied to BAT_{1P}	BAT_{1N} – Positive terminal of first cell
		BAT_{2N} – Negative terminal of first cell
		BAT_{3N} – Negative terminal of second cell
		BAT_{4N} – Negative terminal of third cell
4 cells	–	BAT_{1P} – Positive terminal of first cell
		BAT_{1N} – Negative terminal of first cell
		BAT_{2N} – Negative terminal of second cell
		BAT_{3N} – Negative terminal of third cell
		BAT_{4N} – Negative terminal of fourth cell

Overcurrent (Short-circuit) Protection

A short-circuit condition is detected if CHG and DSG are both active and the voltage between GND and BAT_{4N} is greater than the overcurrent detect threshold (V_{OC}).

Once these conditions are met, both CHG and DSG are driven low, disconnecting the load from the pack. The bq2053 will then re-enable CHG and DSG every 100ms until it finds the short-circuit condition above is false. CHG and DSG then remain enabled, and the chip returns to normal operation.

CHG and DSG States

Condition	CHG pin	DSG pin
Normal operation	BAT_{1P}	BAT_{1P}
Overvoltage	GND	BAT_{1P}
Undervoltage (Sleep Mode)	BAT_{1P}	BAT_{4N}
Overcurrent	GND	BAT_{4N}

Number of Cells

The user must configure the bq2053 for two-, three-, or four-series cell operation, as Table 1 specifies.

Mask Configurable Parameters

V_{OV} threshold and tolerance are configurable by Benchmarq during manufacturing. Contact the factory for availability.

Battery Monitor Timing

Battery monitoring operates on a 25ms time period (see Figure 1). At the beginning of each period, the bq2053 checks to see if more than 250mV (±100mV) potential is between any two sequential battery sense pins (BAT_{1P}, BAT_{1N}, BAT_{2N}, BAT_{3N}, and BAT_{4N}), indicating the presence of a battery. If a battery is present, the chip then checks the V_{CE}, V_{OV}, and V_{UV} thresholds, in that order and at 3.125ms intervals. The chip changes the state of CHG and DSG accordingly if it finds that an error condition has appeared or disappeared since the last cycle.

6.25 ms after the time for the V W check, the chip will check the V_{OC} threshold, regardless of Whether or not a battery was detected at the beginning of the cycle.

After an overcurrent condition has been detected (and the CHG and DSG outputs brought low), the bq2053 will bring the CHG and DSG outputs high during every fourth cycle (every 100ms) at the same time it performs the V_{UV} check. When the V_{OC} check is performed 6.25ms later, CHG and DSG will again be driven low if the overcurrent condition still exists.

These monitoring cycles repeat indefinitely, as long as the operating voltage (V_{OP}) is above 3.0V.

Auxiliary Circuits

A number of auxiliary circuits may be required in conjunction with the bq2053 depending upon the charac-

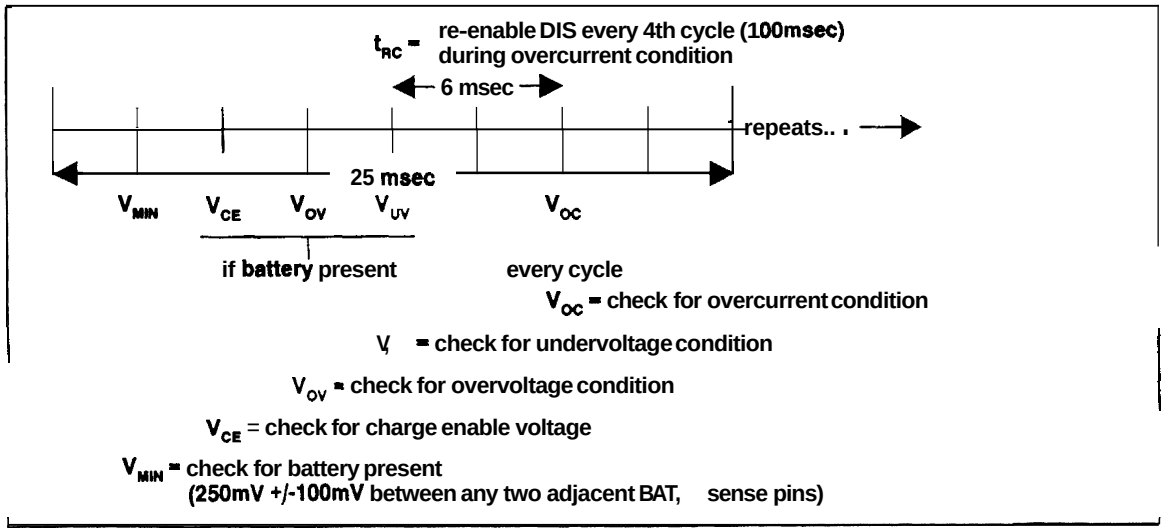


Figure 1. Battery Monitor Timing

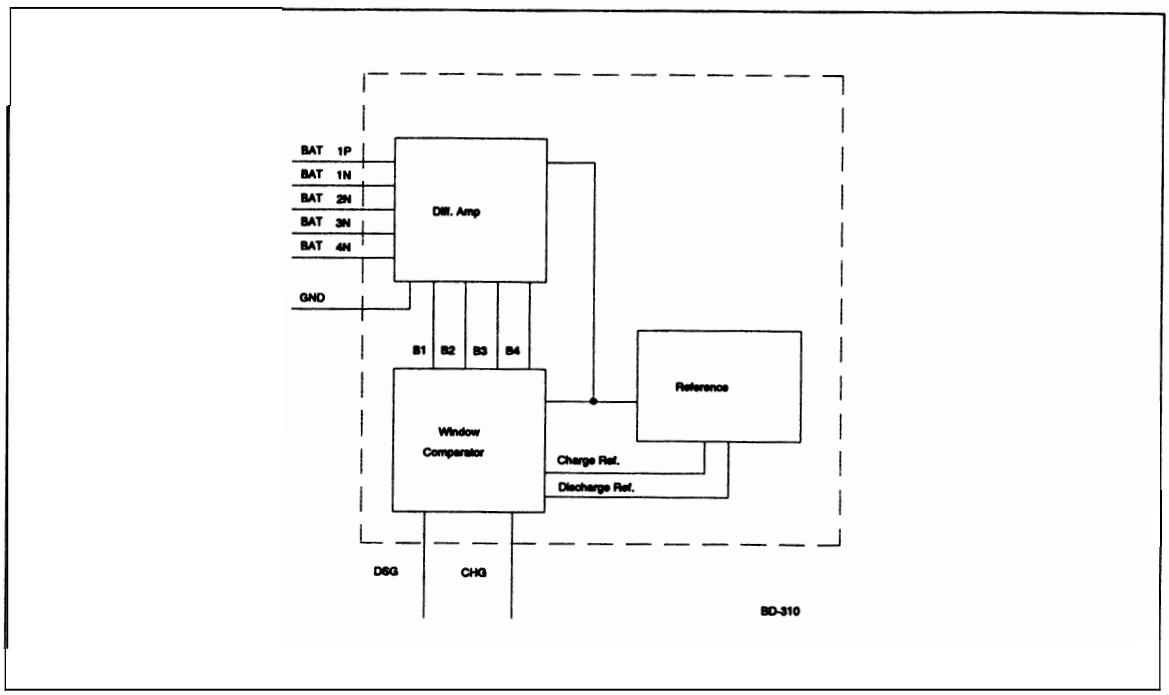


Figure 2. bq2053 Block Diagram

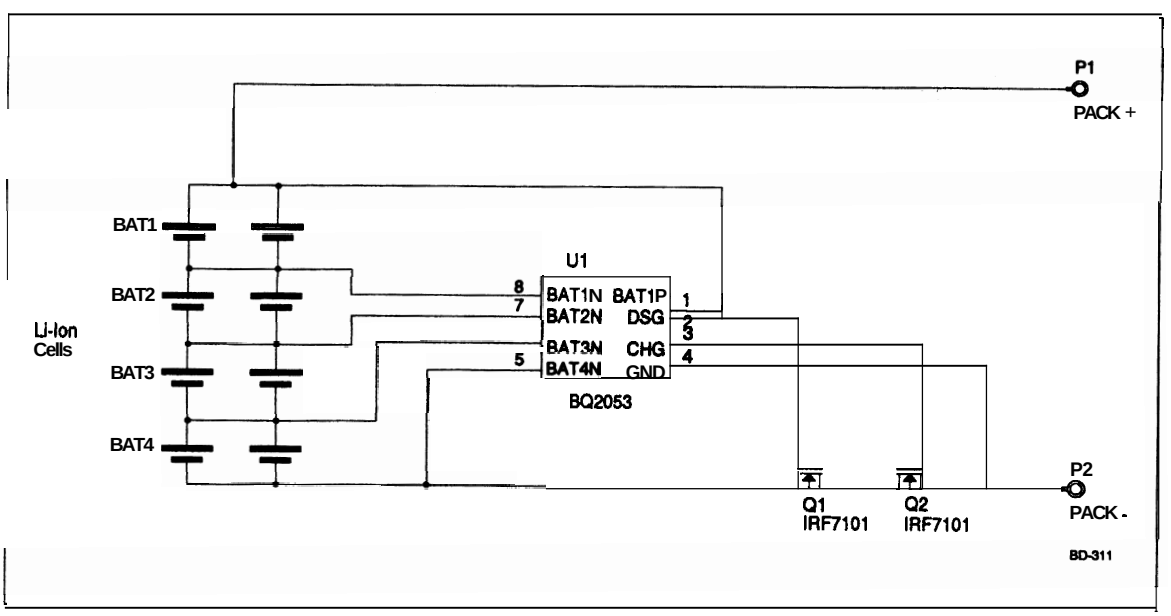


Figure 3. Basic Application Diagram: 4x2 Cell Configuration

Table 2. Ovewoltage Thresholds and Tolerance

	Vov		
		Tolerance	
Part No.	Value	3, 4 cell ±1.5%	2 cell ±1.7%
bq2053M	4.15V	Contact factory for higher tolerances	Contact factory for higher tolerances
bq2053F	4.20V		
bq2053	4.25V		
bq2053D	4.30V		
bq2053J	4.36V		

teristics of the application. These circuits are present in the bq2153 module design (see Figure 4).

ESD and Inductive Spike Protection

The bq2153 module uses a few components external to the bq2053 to provide ESD and inductive spike protection. These components should be present in all designs where applicable. The components are C1 to C4, R1 to R3, C6, and R10 or RE3 and R9.

Ovewoltage Supply Protection

The bq2153 has a circuit that is used to limit the voltage to bq2053. This circuit should be in place if the charging supply is capable of voltages greater than 18V. The circuit comprises R8, R9, D2, and D1.

Faster Short Circuit Protection

The bq2053 provides short circuit protection by monitoring the voltage across the control FETs. If the voltage is greater than |250±25| mv, then both control FETs are switched off. Once these FETs are off, the bq2053 will wait 100ms before testing the voltage drop again by turning the FETs back on. In cases where mechanical restrictions on the contacts make a short highly unlikely, this protection may be adequate.

If faster short circuit protection is required, then an external circuit must be used. The primary function of the external circuit is to switch off the FETs earlier. With only the bq2053 to detect the short circuit, the short circuit might be present for as long as 25ms prior to detection. This situation may cause heating of the MOSFETs. This heating will increase the on resistance of the MOSFETs, which in return will cause additional heating.

Method 1 is to use R12, Q3, R7, and C7 to detect the short circuit faster. In this case, R11 is removed. By detecting the short circuit faster, the heating of the discharge MOSFET will be reduced due to the shorter on-time of the MOSFET. When the drop across the MOSFETs exceeds O.W in the discharge diiion, Q3 will pull the gate of the discharge MOSFET low and turn the discharge off. By AC coupling the signal from the MOSFETs, the protection will only be activated by the transient and not the steady-state condition. Once the discharge MOSFET is off, the bq2053 will keep the MOSFET off for at least 100ms, because the voltage across MOSFETs is greater than the overcurrent threshold. After this time, the bq2053 will turn on the MOSFETs, and if the short circuit is still present, then the process will repeat. In many cases, this method of short circuit is adequate; however, in some cases where the short circuit provides less than O.W across the MOSFETs and yet more than the rated current, the MOSFETs may sustain damage eventually due to the retest of the short circuit.

Method 2 is similar to Method 1, but R12 is removed while R11 is installed. In this case, the circuit detects a 0.7V drop across the MOSFETs and then pulls the BAT_{3N} line low. This action causes the bq2053 to enter a low battery state with the discharge MOSFET off. The MOSFET will remain off until a charge is applied to the battery. In this method, the retest of the short is not done, and the MOSFETs are protected to a much greater degree. R7 and C7 should be adjusted if the battery is plugged into a power supply where a large input capacitor may look like a short circuit. In this case, the time constant of R7 and R8 should be increased to prevent this problem.

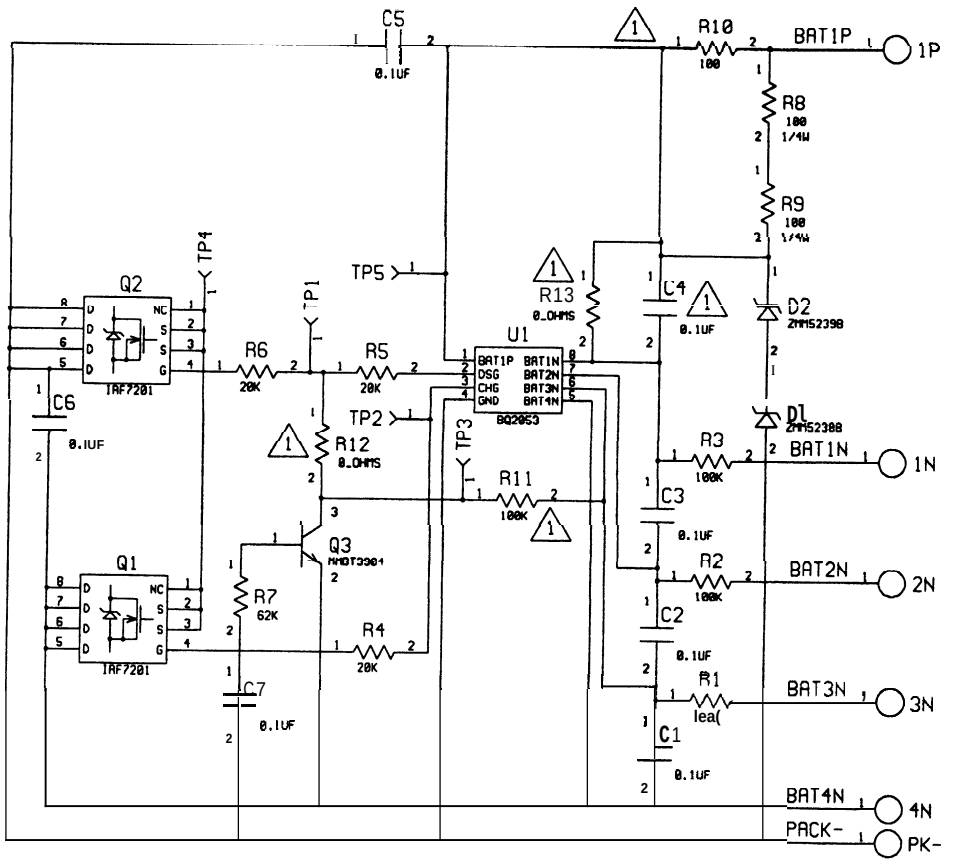
Series Element Selection

Configure the number of series cells using Table 3.

bq2153 Connection Sequence

Use precaution not to short any terminals of the battery to each other or any part of the PCB during assembly.

1. Connect the most positive terminal of the battery pack to BAT_{1P}.
2. In the case of a four-cell pack, connect the second most positive terminal to BAT_{1N}. In the case of a three-cell pack, connect the second most positive terminal to BAT_{2N}. In the case of a two-cell pack, connect the second most positive terminal to BAT_{3N}.
3. In the case of a four-cell pack, connect the third most positive terminal to BAT_{2N}. In the case of a three-cell pack, connect the third most positive terminal to BAT_{3N}. In the case of a two-cell pack, connect the negative terminal to BAT_{4N}.



Note: 1. Component may or may not be placed depending on the configuration.

BD-2153b

Figure 4. bq2153 Schematic

4. In the case of a four-cell pack, connect the fourth most positive terminal to BAT_{3N}. In the case of a three-cell pack, connect the negative terminal to BAT_{4N}.
5. In the case of a four-cell pack, conned the negative terminal to BAT_{4N}.
6. Connect the negative PACK conductor to PK-.

bq2053 Test Procedure

The following procedure verifies functionality of a bq2053 Lithium Ion protector circuit and refers to the test circuit shown in Figure 5.

Setup

1. Set voltage supply to 3.6V • the number of series cells, current limit to low setting (100mA), turn power off.
2. Set current supply to +0.25A, voltage limit to -5V, turn power off. For unipolar supply, connect for positive current.
3. Attach resistor string to BAT_{1P}, BAT_{1N}, BAT_{2N}, BAT_{3N}, BAT_{4N}.
4. Connect voltage supply.
5. Conned current supply and current meter.
6. Conned voltage meters.
7. Turn voltage supply on.
8. Turn current supply on.
9. Check for current flow through FETs and voltage drop across them.
10. If unit passing charge current with ~0.0125V across FETs, increase current to 1A.

V_{OV} Overvoltage Limit

Increase voltage supply until current through FETs is interrupted. I_{CHG} = 0 and V_{FETS} = 5V. Check that voltage where current interrupted falls within limits for cell count in the following table:

Number of cells	2	3	4
Lower limit (V)	8.37	12.56	16.75
Upper Limit (V)	8.63	12.94	17.26

V_{CE} Charge Enable Voltage

Once the Vov value is determined, decrease the voltage supply until the charge current is re-enabled. The voltage at which this occurs should be 50mV to 150mV below the Vov value.

V_{UV} Undervoltage Limit

Reverse the polarity of the current supply so that a discharge is simulated. Lower the voltage supply to 2.5V per cell, then continue to lower it very slowly. The current flow will be interrupted at VUV. Verify that the voltage at which the discharge current was interrupted is within the following table:

Number of cells	2	3	4
Lower limit (V)	4.4	6.6	8.8
Upper Limit (V)	4.8	7.2	9.6

Note that the unit will enter a sleep mode and will not wake up until the current supply is reversed to the charge direction.

V_{OC} Overcurrent Limit

Set the voltage supply to 3.6V per cell. Increase the current supply in the charge direction to 4A. Monitor the voltmeter across the FETs. Slowly increase the current supply. The current will be periodically interrupted when the voltage across the FETs is near 0.250V. The voltage across the FETs at the time just prior to being turned off is the value for V_{OC}. Note that unless the voltmeter is across pins 4 and 5 of the bq2053 chip, the measurement will have error due to the large currents involved. The V_{CH} procedure can be repeated for the discharge direction.

Table 3. bq2153 Circuit Configuration Options

Option	R8	R9	R10	R11	R12	R13	C3	C4	D1	D2
Accelerated short-circuit protection method 1	-	-	-	N	Y	-	-	-	-	-
Accelerated short-circuit protection method 2	-	-	-	Y	N	-	-	-	-	-
No accelerated short-circuit detection	-	-	-	N	N	-	-	-	-	-
Overvoltage supply protection	N	N	Y	-	-	-	-	-	N	N
No overvoltage supply protection	Y	Y	N	-	-	-	-	-	Y	Y
2-cell configuration	-	-	-	-	-	Y	*	N	-	-
3-cell configuration	-	-	-	-	-	Y	Y	N	-	-
4-cell configuration	-	-	-	-	-	N	Y	Y	-	-

* Replace with zero ohm resistor.

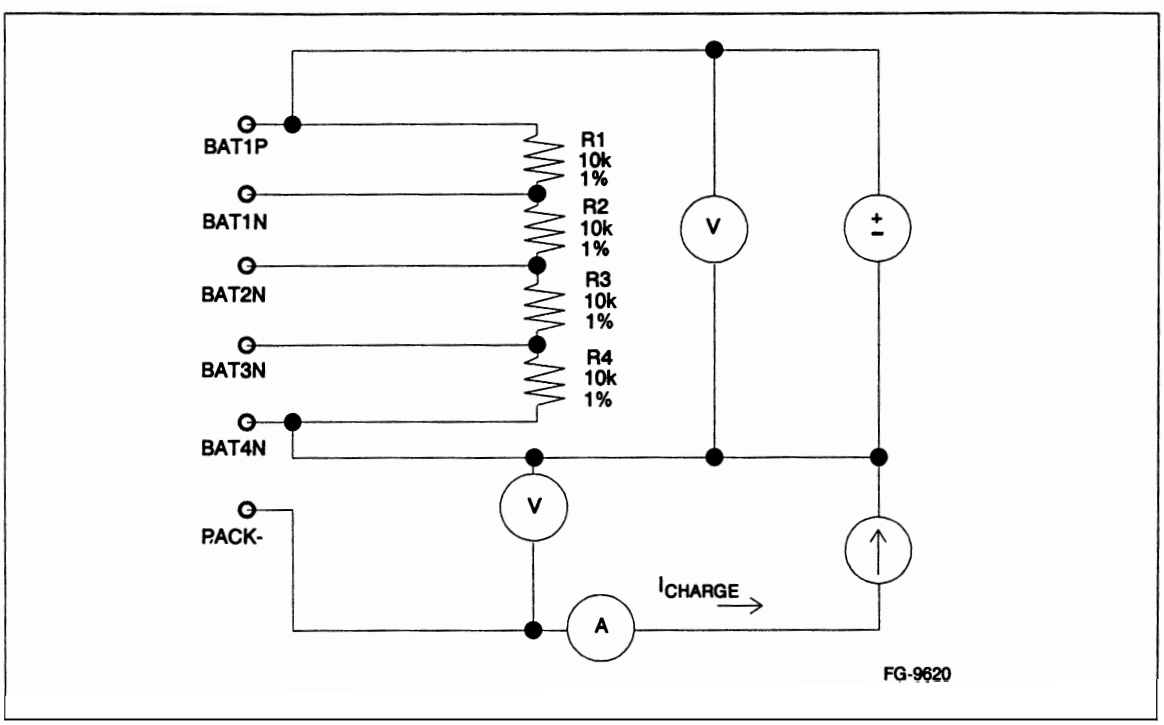


Figure 5. bq2053 Test Circuit

Notes

bq2054

Lithium Ion Fast Charger

1

Features

- Safe charge of Lithium Ion battery packs
- Voltage-regulated current-limited charging
- Fast charge terminated by selectable minimum current; safety backup termination on maximum time
- Charging continuously qualified by temperature and voltage limit.
- Pulse-width modulation control ideal for high-efficiency switch-mode power conversion
- Direct LED control outputs display charge statue and fault conditions

General Description

The bq2054 Lithium Ion Fast Charge IC is designed to optimize charging of lithium ion (Li-Ion) chemistry batteries. A flexible pulse-width modulation regulator allows the bq2054 to control voltage and current during charging. The regulator frequency is set by an external capacitor for design flexibility. The switch-mode design keeps power dissipation to a minimum.

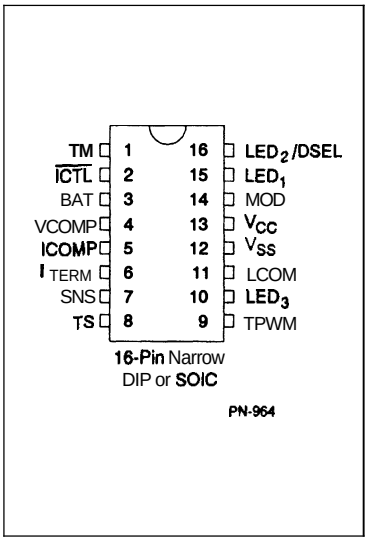
The bq2054 measures battery temperature using an external thermistor for charge qualification. Charging begins when power is applied or on battery insertion.

For safety, the bq2054 inhibits charging until the battery voltage and temperature are within configured limits. If the battery voltage is less than the low-voltage threshold, the bq2054 provides low-current conditioning of the battery.

A constant current-charging phase replenishes up to 70% of the charge capacity, and a voltage-regulated phase returns the battery to full. The charge cycle terminates when the charging current falls below a user-selectable current limit. For safety, charging terminates after maximum time and is suspended if the temperature is outside the preconfigured limits.

The bq2054 provides status indications of all charger states and faults for accurate determination of the battery and charge system conditions.

Pin Connections



16-Pin Narrow DIP or SOIC

PN-964

Pin Names

TM	Time-out programming input	TPWM	Regulator timebase input
$\overline{ICTL}$	Inrush current control output	LED3	Charge status output 3
BAT	Battery voltage input	LCOM	Common LED output
VCOMP	Voltage loop comp input	V_{SS}	System ground
ICOMP	Current loop comp input	V_{CC}	5.0V±10% power
ITERM	Minimum current termination select input	MOD	Modulation control output
SNS	Sense resistor input	LED1	Charge status output 1
TS	Temperature sense input	LED2/ DSEL	Charge status output 2/ Display select input

Pin Descriptions

TM — Time-out programming input

This input sets the maximum charge time. The resistor and capacitor values are determined using Equation 5. Figure 7 shows the resistor/capacitor connection.

$\overline{\text{ICTL}}$ — Inrush current control output

$\overline{\text{ICTL}}$ is driven low during the fault or charge-complete states of the chip. It is used to disconnect the capacitor across the battery pack terminals, preventing inrush currents from tripping overcurrent protection features in the pack when a new battery is inserted.

BAT — Battery voltage input

BAT is the battery voltage sense input. This potential is generally developed using a high-impedance resistor divider network connected between the positive and the negative terminals of the battery. See Figure 4 and Equation 1.

VCOMP — Voltage loop compensation input

This input uses an external R-C network for voltage loop stability.

I_{TERM} — Minimum current termination select

This three-state input is used to set I_{MIN} for fast charge termination. See Table 2.

ICOMP — Current loop compensation input

This input uses an external R-C network for current loop stability.

SNS — Charging current sense input

Battery current is sensed via the voltage developed on this pin by an external sense resistor, R_{SNS}, connected in series with the negative terminal of the battery pack. See Equation 6.

TS — Temperature sense input

This input is used to monitor battery temperature. An external resistor divider network sets the lower and upper temperature thresholds. See Figure 6 and Equations 3 and 4.

TPWM — Regulation timebase input

This input uses an external timing capacitor to ground to set the pulse-width modulation (PWM) frequency. See Equation 7.

LCOM — Common LED output

Common output for LED_{1-3}. This output is in a high-impedance state during initialization to read programming input on DSEL.

MOD — Current-switching control output

MOD is a pulse-width modulated push/pull output that is used to control the charging current to the battery. MOD switches high to enable current flow and low to inhibit current flow.

LED_{1-3} — Charger display status 1–3 outputs

These charger status output drivers are for the direct drive of the LED display. Display modes are shown in Table 1. These outputs are tri-stated during initialization so that DSEL can be read.

DSEL — Display select input

This three-level input controls the LED_{1-3} charge display modes. See Table 1.

V_{CC} — **V_{CC} supply**

5.0V, ± 10% power

V_{SS} — **Ground**

Charge Algorithm

The bq2054 uses a two-phase fast charge algorithm. In phase 1, the bq2054 regulates constant current (I_{SNS} = I_{MAX}) until V_{CELL} (= V_{BAT} - V_{SNS}) rises to V_{REG}. The bq2054 then transitions to phase 2 and regulates constant voltage (V_{CELL} = V_{REG}) until the charging current falls below the programmed I_{MIN} threshold. The charging current must remain below I_{MIN} for 120 ± 40ms before a valid fast charge termination is detected. Fast charge then terminates, and the bq2054 enters the Charge Complete state. See Figures 1 and 2.

Charge Qualification

The bq2054 starts a charge cycle when power is applied while a battery is present or when a battery is inserted. Figure 2 shows the state diagram for pre-charge qualification and temperature monitoring. The bq2054 first checks that the battery temperature is within the allowed, user-configurable range. If the temperature is out of range, the bq2054 enters the Charge Pending state and waits until the battery temperature is within the allowed range. Charge Pending is enunciated by LED_3 flashing.

Thermal monitoring continues throughout the charge cycle, and the bq2054 enters the Charge Pending state when the temperature out of range. (There is one exception; if the bq2054 is in the Fault state—see below—the out-of-range temperature is not recognized until the bq2054 leaves the Fault state.) *All* timers are suspended (but not reset) while the bq2054 is in Charge Pending. When the temperature comes back into range, the bq2054 returns to the point in the charge cycle where the out-of-range temperature was detected.

When the temperature is valid, the bq2054 then regulates current to I_{COND} ($=I_{MAX}/5$). After an initial holdoff period t_{HO} (which prevents the chip from reacting to transient voltage spikes that may occur when charge current ie first applied), the chip begins monitoring V_{CELL}. If V_{CELL} does not rise to at least V_{MIN} before the expiration of time-out limit t_{TO} (e.g. the chip has failed short), the bq2054 enters the Fault state. If V_{MIN} is achieved before expiration of the time limit, the chip begins fast charging.

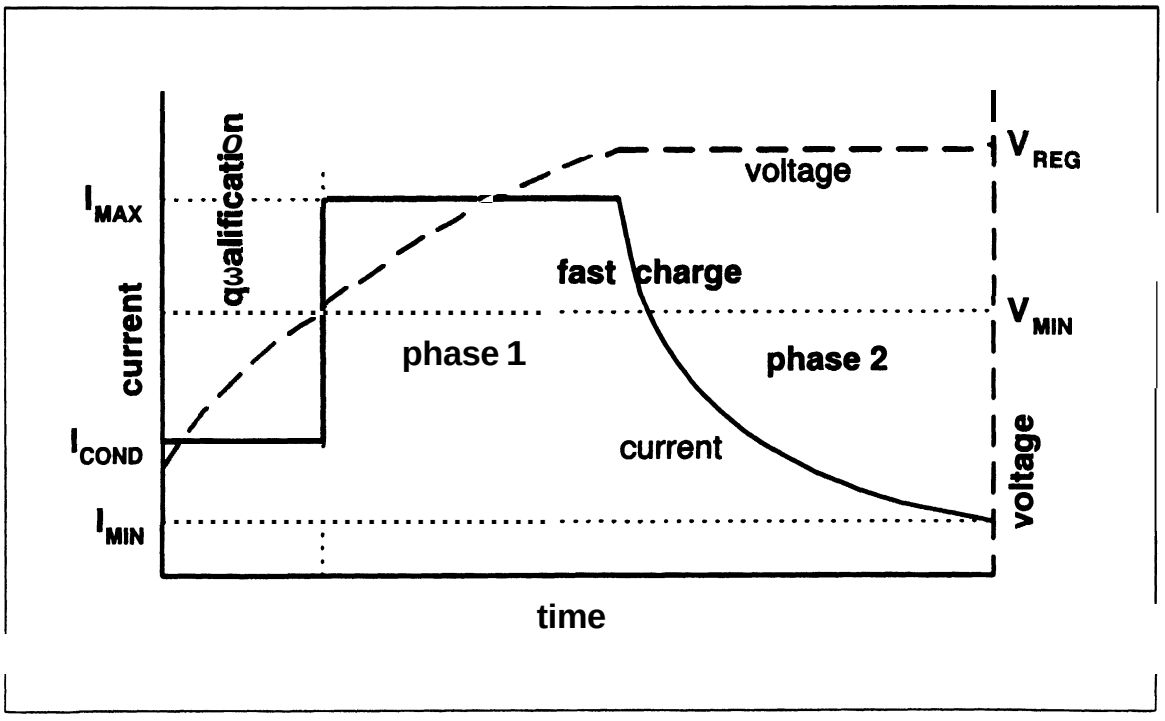


Figure 1. bq2054 Charge Algorithm

Once in the Fault state, the bq2054 waits until V_{CC} is cycled or a new battery insertion is detected. It then starts a new charge cycle and begins the qualification process again.

Charge Status Display

Charge status is enunciated by the LED driver outputs LED_1–LED_3. Three display modes are available in the bq2054; the user selects a display mode by configuring pin DSEL. Table 1 shows the three display modes.

The bq2054 does not distinguish between an over-voltage fault and a "battery absent" condition. The bq2054 enters the Fault state, enunciated by turning on LED_3, whenever the battery is absent. The bq2054, therefore, gives an indication that the charger is on even when no battery is in place to be charged.

Configuring the Display Mode and I_{MIN}

DSEL/LED_2 is a bi-directional pin with two functions; it is an LED driver pin as an output and a programming pin as an input. The selection of pull-up, pull-down, or no pull resistor programs the display mode on DSEL per Table 1. The bq2054 latches the programming data sensed on the DSEL input when any one of the following three events occurs:

1. V_{CC} rises to a valid level.
2. The bq2054 leaves the Fault state.
3. The bq2054 detects battery insertion.

The LEDs go blank for approximately 750ms (typical) while new programming data is latched.

Table 1. bq2054 Display Output Summary

Mode	Charge Action State	LED_1	LED2	LED3
DSEL = 0 (Mode 1)	Battery absent or over-voltage fault	Low	Low	High
	Pre-charge qualification	Flash	Low	Low
	Fast charging	High	Low	Low
	Charge complete	Low	High	Low
	Charge pending (temperature out of range)	X	X	Flash
	Charging fault	X	X	High
DSEL = 1 (Mode 2)	Battery absent or over-voltage fault	Low	Low	High
	Pre-charge qualification	High	High	Low
	Fast charge	Low	High	Low
	Charge complete	High	Low	Low
	Charge pending (temperature out of range)	X	X	Flash
	Charging fault	X	X	High
DSEL = Float (Mode 3)	Battery absent or over-voltage fault	Low	Low	High
	Pre-charge qualification	Flash	Flash	Low
	Fast charge: current regulation	Low	High	Low
	Fast charge: voltage regulation	High	High	Low
	Charge complete	High	Low	Low
	Charge pending (temperature out of range)	X	X	Flash
	Charging fault	X	X	High

Note: 1 = V_{CC}; 0 = V_{SS}; X = LED state when fault occurred; Flash = 1/6 sec. low, 1/6 sec high.

Fast charge terminates when the charging current drops below a minimum current threahold programmed by the value of I_{TERM} (see Table 2) and remains below that level for 120 ± 40ms.

Table 2. I_{MIN} Termination Thresholds

I_{TERM}	I_{MIN}
0	$I_{MAX}/10$
1	$I_{MAX}/20$
Z	$I_{MAX}/30$

Figure 3 shows the bq2054 configured for display mode 2 and $I_{MIN} = I_{MAX}/10$.

Voltage and Current Monitoring

The bq2054 monitors battery pack voltage at the BAT pin. The user must implement a voltage divider between the positive and negative terminals of the battery pack to present a scaled battery pack voltage to the BAT pin. The bq2054 also uses the voltage across a sense resistor (R_{SNS}) between the negative terminal of the battery pack and ground to monitor the current into the pack. See Figure 4 for the configuration of this network.

The resistor values are calculated from the following:

Equation 1

$$\frac{RB1}{RB2} = \frac{N * V_{REG}}{2.05V} - 1$$

where:

V_{CELL} = Manufacturer specified charging cell voltage
N = Number of cells in series

The current sense resistor, R_{SNS} (see Figure 6), determines the fast charge current. The value of R_{SNS} is given by the following:

Equation 2

$$I_{MAX} = \frac{0.250V}{R_{SNS}}$$

where:

- N = Number of cells
- V_{REG} = Desired fast-charging voltage
- I_{MAX} = Desired maximum charge current

These parameters are typically specified by the battery manufacturer. The total resistance presented across the battery pack by RB1 + RB2 should be between 150kΩ and 1MΩ. The minimum value ensures that the divider network does not drain the battery excessively when the power source is disconnected. Exceeding the maximum value increases the noise susceptibility of the BAT pin.

Hold-Off Period

Both V_{HCO} and I_{MIN} terminations are ignored during the first 1.33 ± 0.19 seconds of both the Charge Qualification and Fast Charge phases. This condition prevents premature termination due to voltage spikes which may occur when charge is first applied.

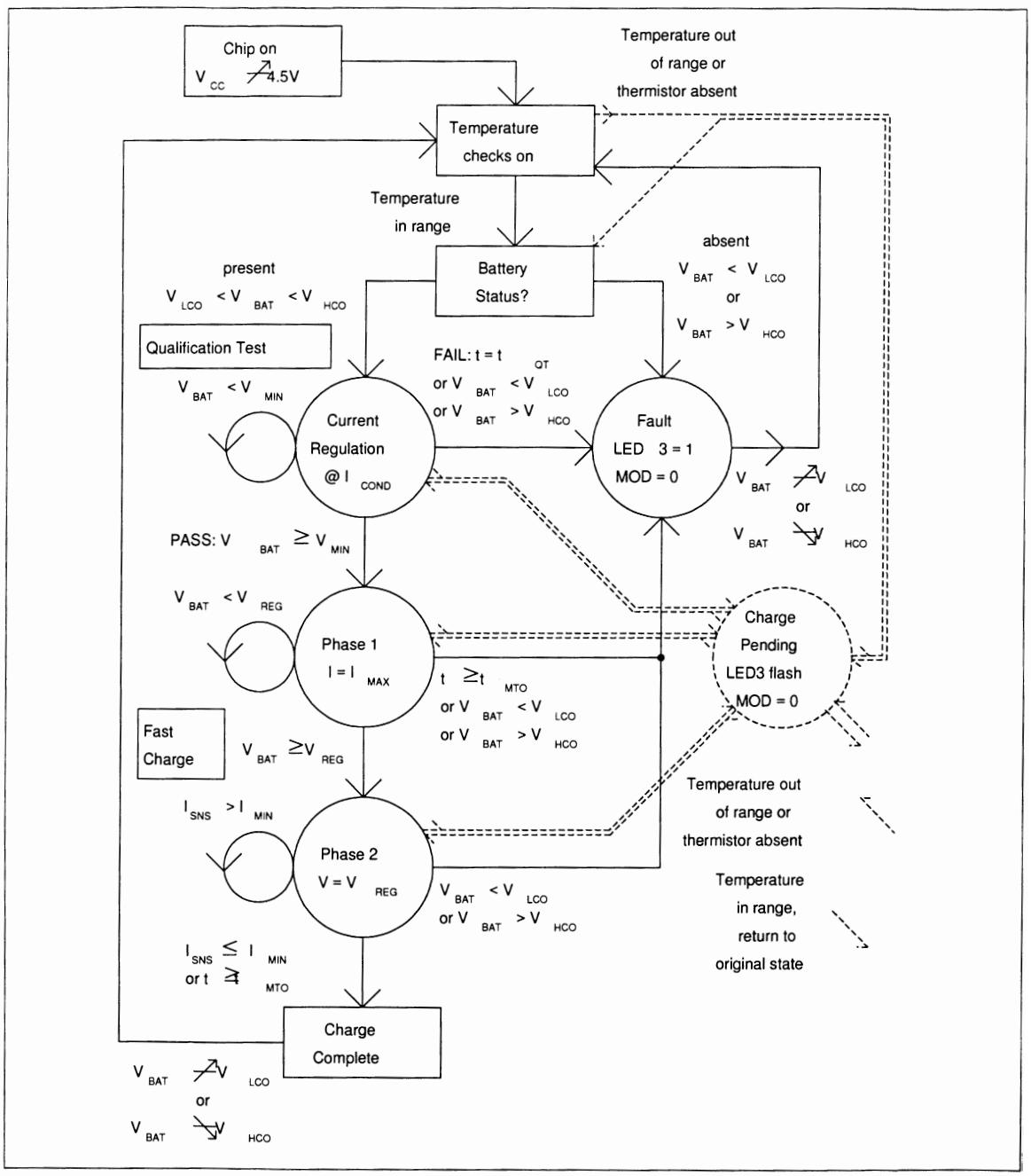


Figure 2. bq2054 State Diagram

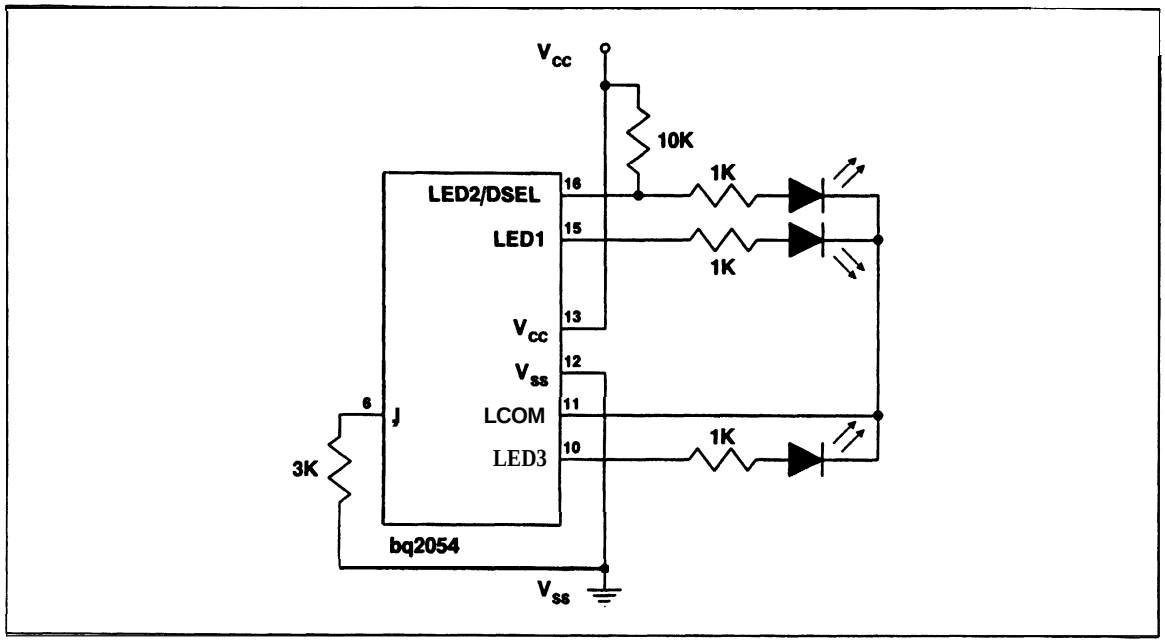


Figure 3. Configured Display Mode/I_{MIN} Threshold

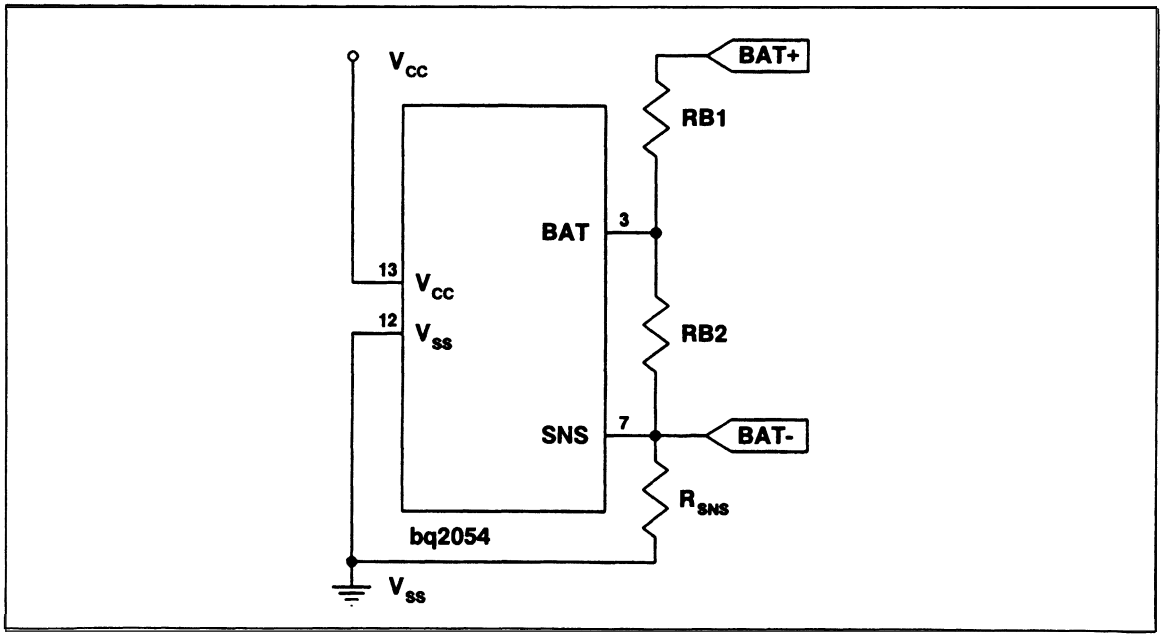


Figure 4. Configuring the Battery Divider

Battery Insertion and Removal

V_{CELL} is interpreted by the bq2054 to detect the presence or absence of a battery. The bq2054 determines that a battery is present when V_{CELL} is between the High-Voltage Cutoff (V_{HCO} = V_{REG} + 0.25V) and the Low-Voltage Cutoff (V_{LCO} = 0.8V). When V_{CELL} is outside this range, the bq2054 determines that no battery is present and transitions to the Fault state. Transitions into and out of the range between V_{LCO} and V_{HCO} are treated as battery insertions and removals, respectively. The V_{HCO} limit also implicitly serves as an over-voltage charge termination.

Inrush Current Control

Whenever the bq2054 is in the fault or charge-complete state, the $\overline{ICTL}$ output is driven low. This output can be used to disconnect the capacitor usually present in the charger across the positive and negative battery terminals, preventing the cap from supplying large inrush currents to a newly inserted battery. Such inrush currents may trip the overcurrent protection circuitry usually present in Li-Ion battery packs.

Temperature Monitoring

The bq2054 monitors temperature by examining the voltage presented between the TS and SNS pins by a resistor network that includes a Negative Temperature Coefficient (NTC) thermistor. Resistance variations around that value are interpreted as being proportional to the battery temperature (see Figure 5).

The temperature thresholds used by the bq2054 and their corresponding TS pin voltage are:

- TCO (Temperature Cutoff): Higher limit of the temperature range in which charging is allowed. V_{TCO} = 0.4 • Vcc
- HTF (High-Temperature Fault): Threshold to which temperature must drop after temperature cutoff is exceeded before charging can begin again. V_{HTF} = 0.44 • V_{CC}
- LTF (Low-Temperature Fault): Lower limit of the temperature range in which charging is allowed. V_{LTF} = 0.6 • Vcc

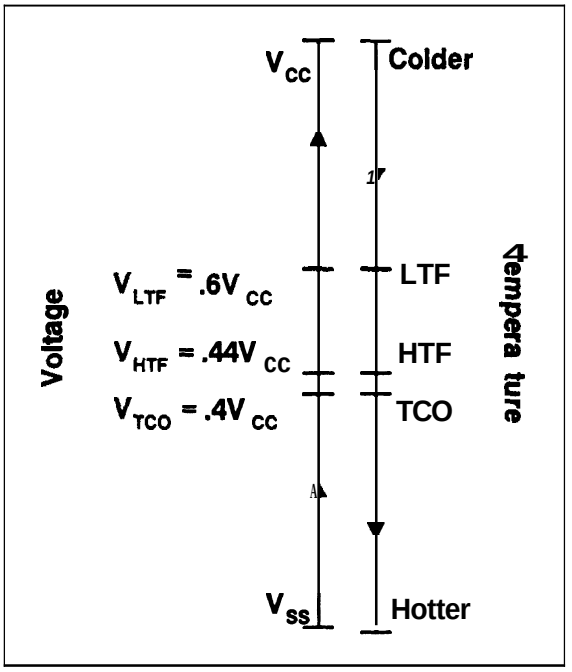


Figure 5. Voltage Equivalent of Temperature

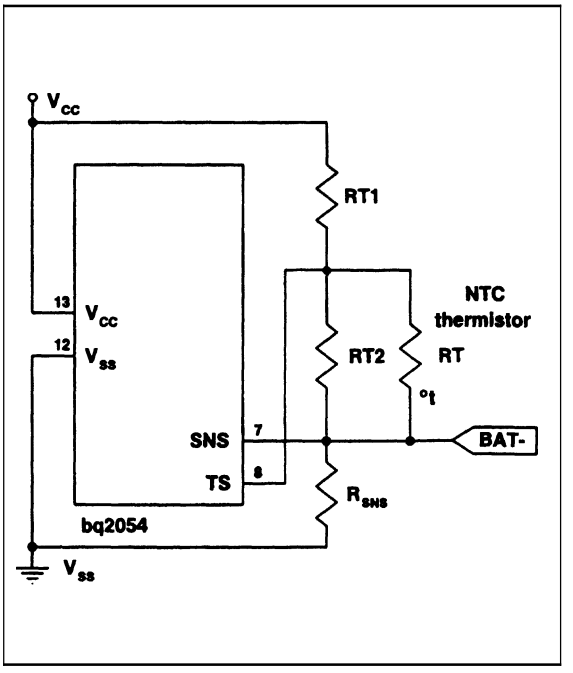


Figure 6. Configuring Temperature Sensing

A resistor divider network can be implemented that presents the defined voltage levels to the TS pin at the desired temperatures (see Figure 6).

The equations for determining RT1 and RT2 are:

Equation 3

$$0.6 * V_{CC} = \frac{(V_{CC} - 0.250)}{1 + \frac{RT1 * (RT2 + R_{LTF})}{(RT2 * R_{LTF})}}$$

Equation 4

$$0.44 = \frac{1}{1 + \frac{RT1 * (RT2 + R_{HTF})}{(RT2 * R_{HTF})}}$$

where:

- R_{LTF} = thermistor resistance at LTF
- R_{HTF} = thermistor resistance at HTF

TCO is determined by the values of RT1 and RT2. 1% resistors are recommended.

Disabling Temperature Sensing

Temperature sensing can be disabled by placing 10kΩ resistors between TS and SNS and between SNS and vcc.

Maximum Time-Out

MTO is programmed from 1 to 24 hours by an R-C network on the TM pin (see Figure 7) per the equation:

Equation 5

$$t_{MTO} = 0.5 * R * C$$

Where R is in kΩ and C is in µF, t_{MTO} is in hours. The maximum value for C (0.1µF) is typically used.

The MTO timer is reset at the beginning of fast charge and when fast charge transitions from the current regulated to the voltage regulated mode. If MTO expires during the current regulated phase, the bq2054 enters the Fault state and terminates charge. If the MTO timer expires during the voltage regulated phase, fast charging terminates and the bq2054 enters the Charge Complete state.

The MTO timer is suspended (but not reset) during the out-of-range temperature (Charge Pending) state.

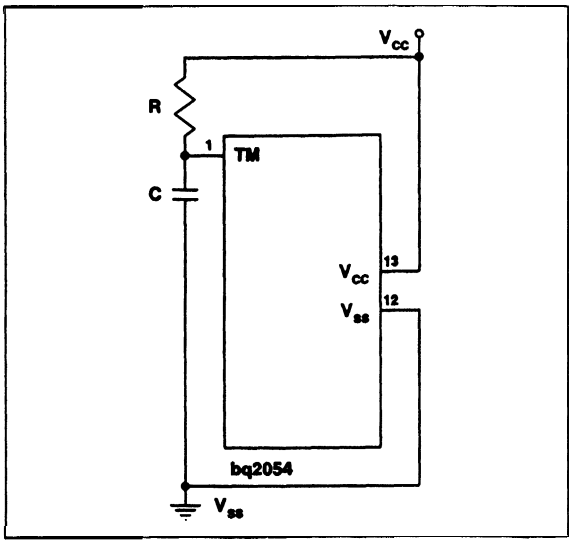


Figure 7. R-C Network for Setting MTO

Charge Regulation

The bq2054 controls charging through pulse-width modulation of the MOD output pin, supporting both constant-current and constant-voltage regulation. Charge current is monitored at the SNS pin, and charge voltage is monitored at the BAT pin. These voltages are compared to an internal reference, and the MOD output modulated to maintain the desired value.

Voltage at the SNS pin is determined by the value of resistor R_{SNS}, so nominal regulated current is set by

Equation 6

$$I_{MAX} = 0.250V/R_{SNS}$$

The switching frequency of the MOD output is determined by an external capacitor (CPWM) between the pin TPWM and ground, per the following:

Equation 7

$$F_{PWM} = 0.1/C_{PWM}$$

Where C is in µF and F is in kHz. A typical switching rate is 100kHz, implying C_{PWM} = 0.001µF. MOD pulse width is modulated between 0 and 80% of the switching period.

To prevent oscillation in the voltage and current control loops, frequency compensation networks (C or R-C) are typically required on the V_{COMP} and I_{COMP} pins (respectively).

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	U n	Notes
V_{CC}	V_{CC} relative to V_{SS}	-0.3	+7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3	+7.0	V	
T_{OPR}	Operating ambient temperature	-20	+70	°C	Commercial
		-40	+85	"C	Industrial "N"
T_{STG}	Storage temperature	-55	+125	°C	
T_{SOLDER}	Soldering temperature		+260	°C	10 sec. max.

Note: Permanent device damage may occur if **Absolute Maximum** Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds (TA = TOPR; VCC = 5V ±10%)

Symbd	Parameter	Rating	Unit	Tolerance	Note8
V_{REF}	Internal reference voltage	2.05	V	1%	T_A = 25°C
	Temperature coefficient	-0.5	mV/°C	1046	
V_{LTF}	TS maximum threshold	0.6 • Vcc	V	±0.03V	Low-temperature fault
V_{HTF}	TS hysteresis threshold	0.44 • Vcc	V	±0.03V	High-temperature fault
V_{TCO}	TS minimum threshold	0.4 • Vcc	V	±0.03V	Temperature cutoff
V_{HCO}	High cutoff voltage	V_{REG} • 0.25V	V	±0.03V	
V_{MIN}	Under-voltage threshold at BAT	0.2 * V_{CC}	V	±0.03V	
V_{LCO}	Low cutoff voltage	0.8	V	±0.03V	
V_{SNS}	Current sense at SNS	0.250	V	1046	I_{MAX}
		0.050	V	10%	I_{COND}

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	
V_{TEMP}	Temperature sense voltage	0		V_{CC}	V	V_{TS} - V_{SNS}
V_{CELL}	Per cell battery voltage input	0		V_{CC}	V	V_{BAT} - V_{SNS}
I_{CC}	Supply current		2	4	mA	Outputs unloaded
I_{IZ}	DSEL tri-state open detection	-2		2	µA	Note2
	I_{TERM} tri-state open detection	-2		2	µA	
V_{IH}	Logic input high	Vcc-0.3	-		V	DSEL, I_{TEM}
V_{IL}	Logic input low		-	V_{SS}+0.3	V	DSEL, I_{TERM}
V_{OH}	LED_{1-3}, $\overline{ICTL}$, output high	Vcc-0.8	-		V	$I_{OH} \leq 10mA$
	MOD output high	Vcc-0.8	-		V	$I_{OH} \leq 10mA$
V_{OL}	LED_{1-3}, $\overline{ICTL}$, output low		-	V_{SS}+0.8V	V	$I_{OL} \leq 10mA$
	MOD output low		-	V_{SS}+0.8V	V	$I_{OL} \leq 10mA$
	LCOM output low		-	V_{SS}+0.5	V	$I_{OL} \leq 30mA$
I_{OH}	LED_{1-3}, $\overline{ICTL}$, source	-10			mA	V_{OH} =V_{CC}-0.5V
	MOD source	-5.0			mA	V_{OH} =V_{CC}-0.5V
I_{OL}	LED_{1-3}, $\overline{ICTL}$, sink	10			mA	V_{OL} = V_{SS}+0.5V
	MOD sink	5			mA	V_{OL} = V_{SS}+0.8V
	LCOM sink	30			mA	V_{OL} = V_{SS}+0.5V
I_{IL}	DSEL logic input low source			+30	µA	V = V_{SS} to V_{SS}+ 0.3V, Note 2
	I_{TERM} logic input low source			+70	µA	V = V_{SS} to V_{SS}+ 0.3V
I_{IH}	DSEL logic input high source	-30			µA	V = V_{CC} - 0.3V toV_{CC}
	I_{TERM} logic input high source	-70			µA	V = V_{CC} - 0.3V toV_{CC}

Notes:
1. All voltages relative to V_{SS} except where noted.
2. Conditions during initialization after V_{CC} applied.

1

Impedance

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
R_{BATZ}	BAT pin input impedance	50			MΩ	
R_{SNSZ}	SNS pin input impedance	60			MΩ	
R_{TSZ}	TS pin input impedance	60			MΩ	
R_{PROG1}	Soft-programmed pull-up or pull-down resistor value (for programming)			10	kΩ	DSEL
R_{PROG2}	Pull-up or pull-down resistor value			3	kΩ	I_{TERM}
R_{MTO}	Charge timer resistor	20		480	kΩ	

Timing (TA = TOPR; VCC = 5V ±10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{MTO}	Charge time-out range	1		24	hours	See Figure 7
t_{QT}	Pre-charge qual test time-out period		$0.16t_{MTO}$			
t_{HO}	Termination hold-off period	1.14		1.52	sec.	
t_{IMIN}	Min. current detect filter period	80		160	msec.	
F_{PWM}	PWM regulator frequency range		100		kHz	C_{PWM} = 0.001µF

Capacitance

Symbol	Parameter	Minimum	Typical	Maximum	Unit
C_{MTO}	Charge timer capacitor			0.1	µF
C_{PWM}	PWM R-C capacitance		0.001		µF

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	5, 7, 8, 10	Value Change	Changed V_{SNS} and I_{MAX}
2	5, 10	Value Change	Changed V_{REF}
3	10	Coefficient Addition	Temperature coefficient added
4	5	New state diagram	Diagram inserted
4	1, 2, 8, 12	NC pin replaced with $\overline{ICTL}$	
4	3, 5, 13	Termination hold-off period added I_{MIN} detect filtering added	

Note: Change 3 = April 1996 C changes from Dec. 1995 B.
Change 4 = Sept. 1996 D changes from April 1996 C.

Ordering Information

bq2054

Temperature:
blank = Commercial (-20 to +70°C)
N = Industrial (-40 to +85°C)*

Package Option:
PN = 16-pin plastic DIP
SN = 16-pin narrow SOIC

Device:
bq2054 Li-Ion Charge IC

* Contact factory for availability.

BENCHMARQ

Preliminary **DV2054S1**

Fast Charge Development System

Control of On-Board PNP Switch-Mode Regulator

Features

- bq2054 fast charge control evaluation and development
- Accepts 24 VDC (max.) input supply
- On-board configuration for fast charge of 1, 2, 3, or 4 Li-Ion cells
- Constant current (up to 3.5A) and constant voltage (up to 15V) provided by on-board switch mode regulator
- Charge termination by maximum voltage, selectable minimum current, or maximum time-out
- Direct connections for battery, thermistor, and reset signal
- Jumper configurable three-LED display

General Description

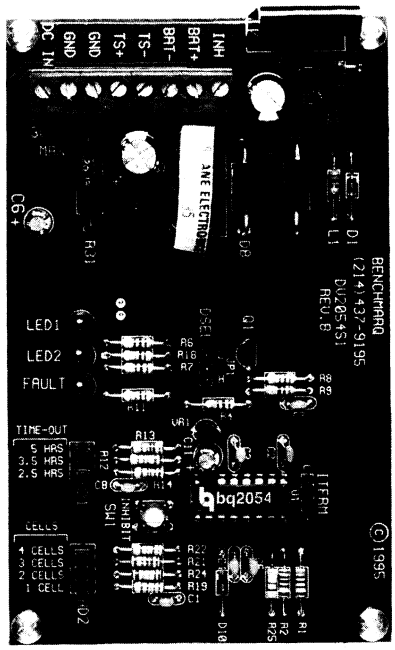
The DV2054S1 Development System provides a development environment for the bq2054 Lithium Ion Fast Charge IC. The DV2054S1 incorporates a bq2054 and a buck-type switch-mode regulator to provide fast charge control for 1 through 4 Li-Ion cells.

Fast charge is preceded by a pre-charge qualification period.

Fast charge termination occurs on:

- Maximum voltage
- Minimum current – I_{MAX} divided by 10, 20, or 30
- Maximum time-out

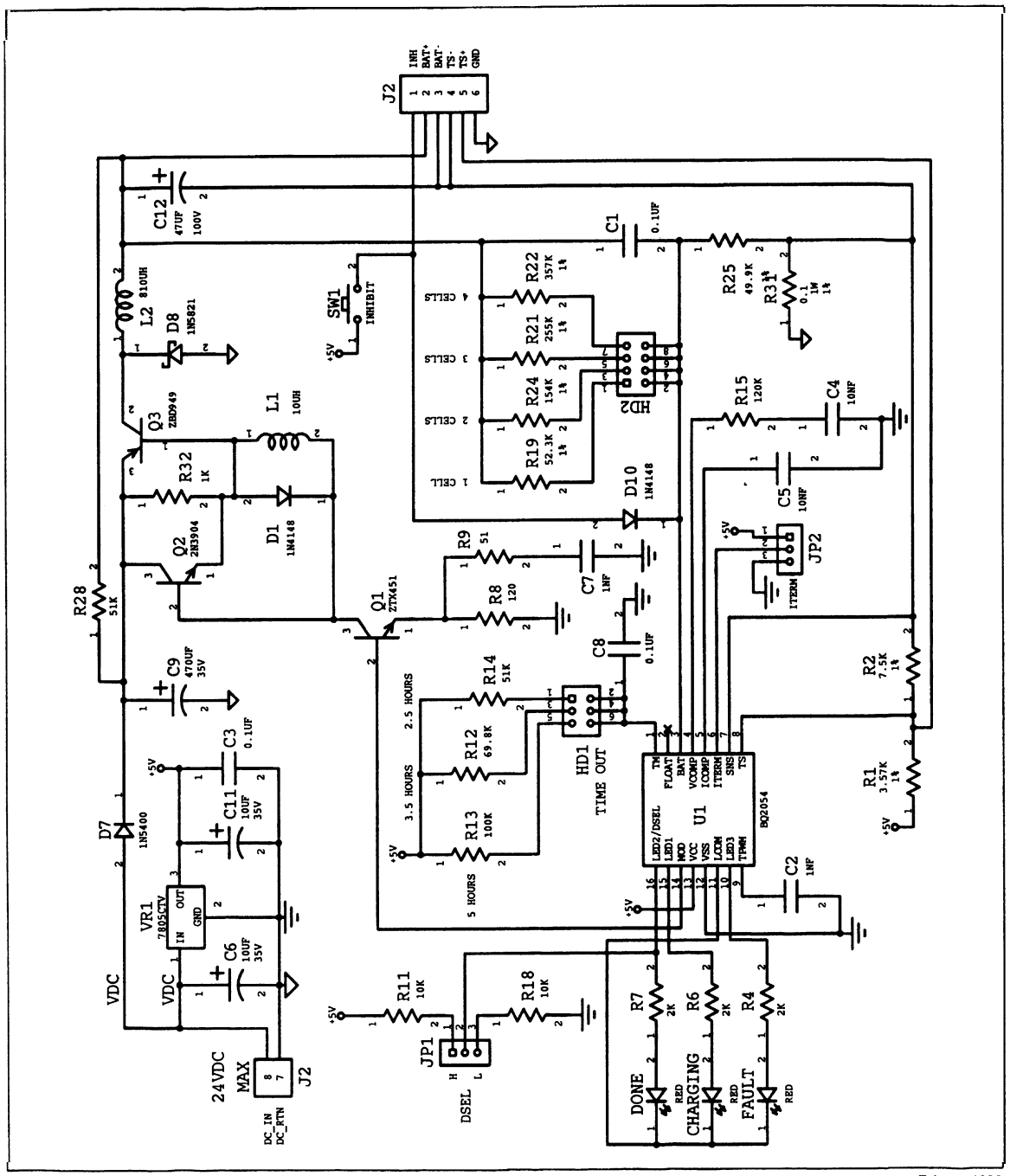
The bq2054 can be reset and a new charge cycle started with either the momentary on-board switch (SW1) or via the INH input on connector J2. The reset signal simulates a "Battery Absent" condition. Charging is inhibited as long as the reset signal is active; once it is released, the charge cycle re-starts at pre-charge qualification.



The user provides a DC power supply and batteries and configures the board for the number of cells, the maximum time-out period, the minimum current threshold, and the LED display mode. The board has direct connections for the battery and the provided thermistor.

Before using the DV2054S1 board, please review the bq2054 data sheet.

DV2054S1 Board Schematic



Rev. C Board

Feb. 13, 1996

bq2050, bq2053, and bq2054 Li-Ion Evaluation System

Features

- bq2050 Gas Gauge IC, bq2053 Lithium Ion Pack Supervisor, and bq2054 Fast Charge control evaluation and development system for 2 to 4 cells
- Conservative and repeatable measurement of available capacity compensated for charge/discharge rates. Capacity and self-discharge estimation also temperature-compensated using thermal sensor internal to the bq2050
- Overvoltage, undervoltage, and short-circuit protection provided by the bq2053
- On-board frequency-modulated current regulation with Minimum Current and Maximum Time-Out fast charge termination using the bq2054 Fast Charge IC. Also features pre-charge qualification for temperature and voltage faults
- Programmable LED outputs display battery and charge status, plus on-board data logging by the bq2050

General Description

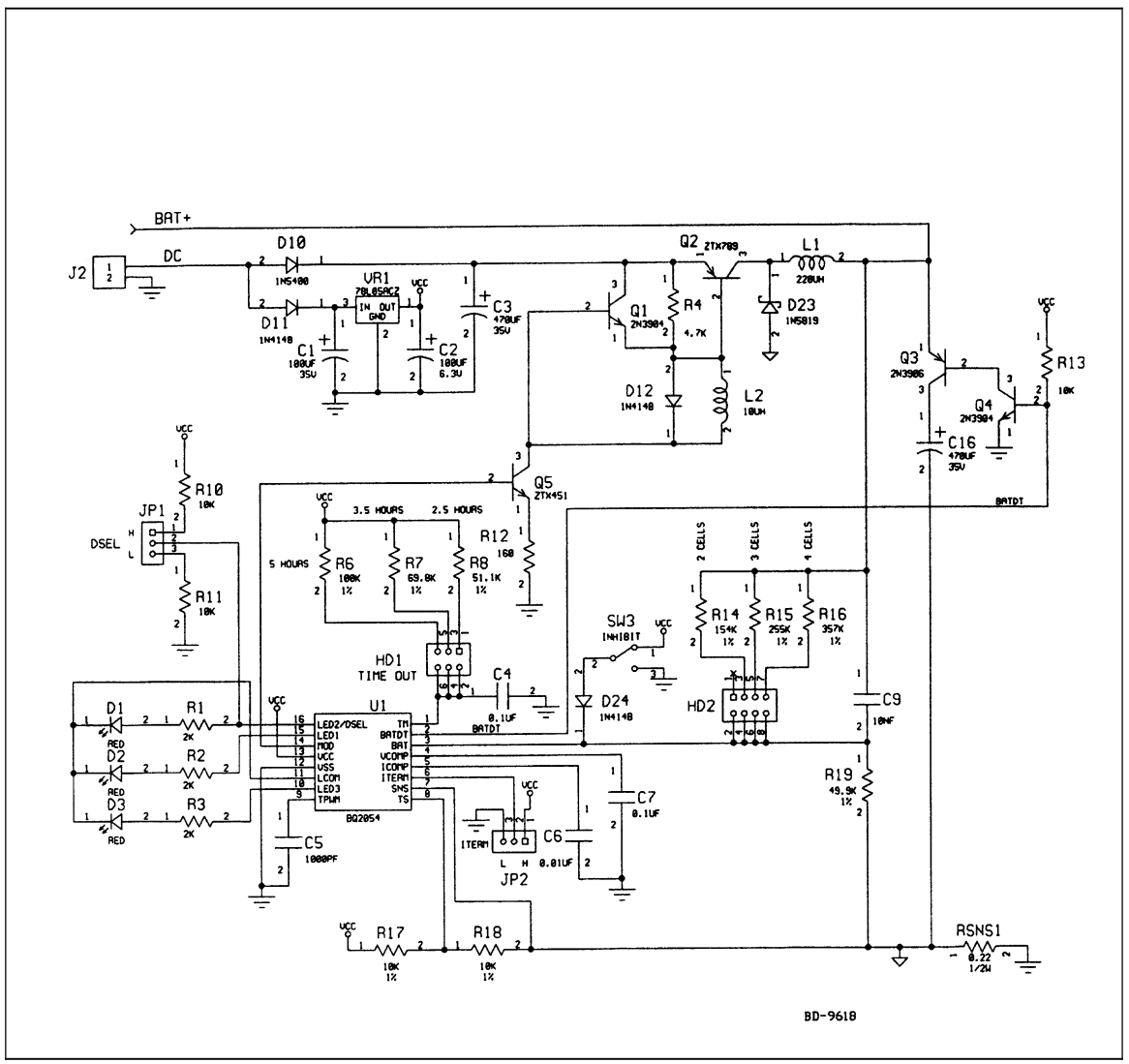
The EV205x provides a development and evaluation environment for the bq2050 Lithium Ion Power Gauge and the bq2053 Lithium Ion Pack Supervisor ICs. The bq2053 provides overvoltage, undervoltage, and short circuit protection for two to four lithium ion cells. The bq2050 reports conservative and repeatable measurement of the available capacity in those cells. The board incorporates a bq2054 Fast Charge IC to provide frequency modulated constant current regulation with minimum current and maximum time out (MTO) termination to fast charging, plus two FETs for charge and discharge control.

The V_{UV}, V_{CE}, and V_{OV} thresholds in the bq2053 are set to 2.3V, 4.15V, and 4.25V, respectively. Other voltage settings are mask programmable at Benchmarq. Please refer to the bq2050, bq2053, and bq2054 data sheets for device descriptions.

Hardware for the RS-232 interface is included on the EV205x to provide easy access to the bq2050 data logging function. The menu-driven software accesses data *logging* and displays charge/discharge activity on any standard DOS PC.

The user provide%a DC power supply and batteries. The user configures the EV205x for the number of cells, battery capacity, maximum charge time, and coke or graphite anode technology.

EV205x Schematic



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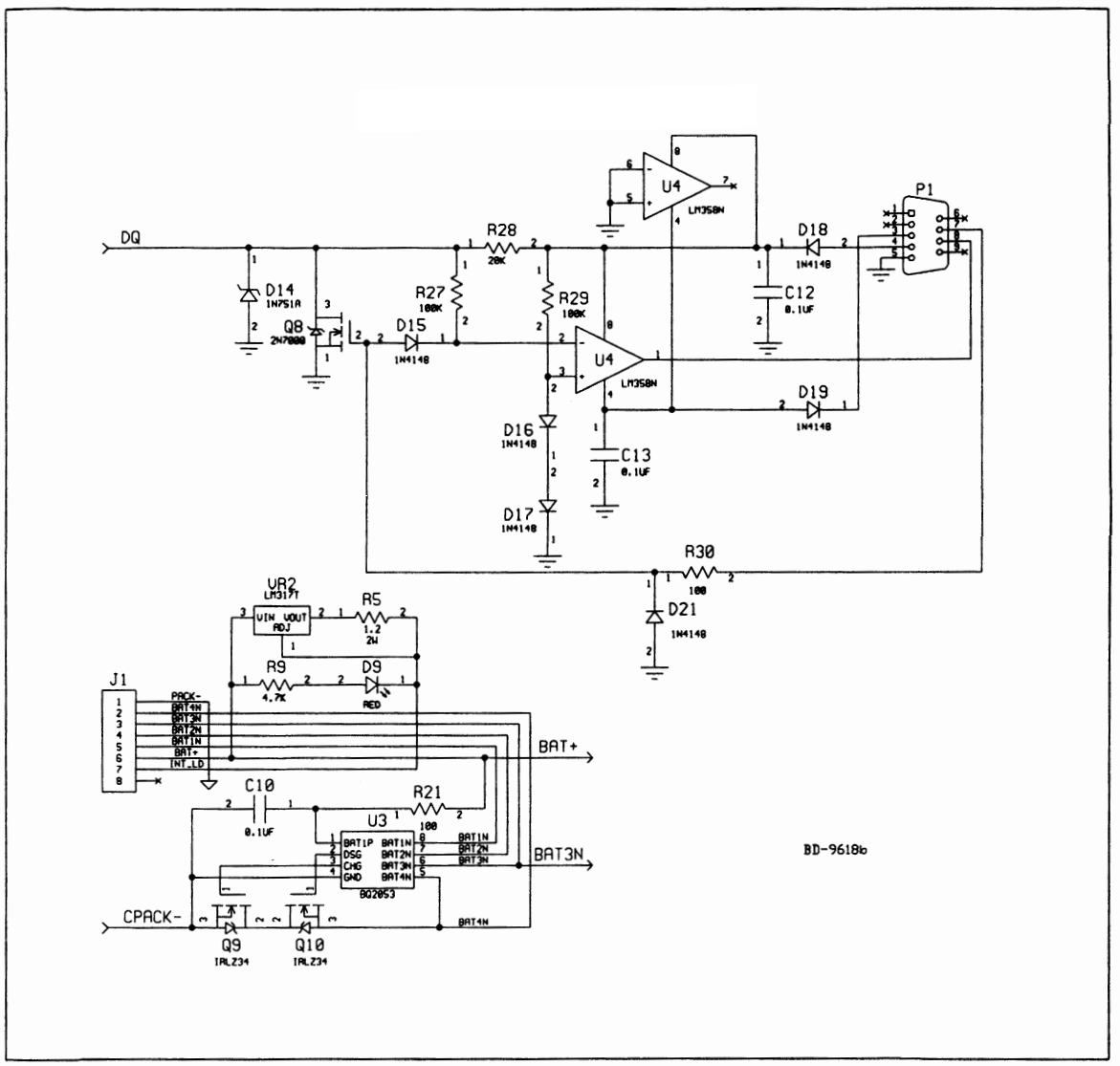
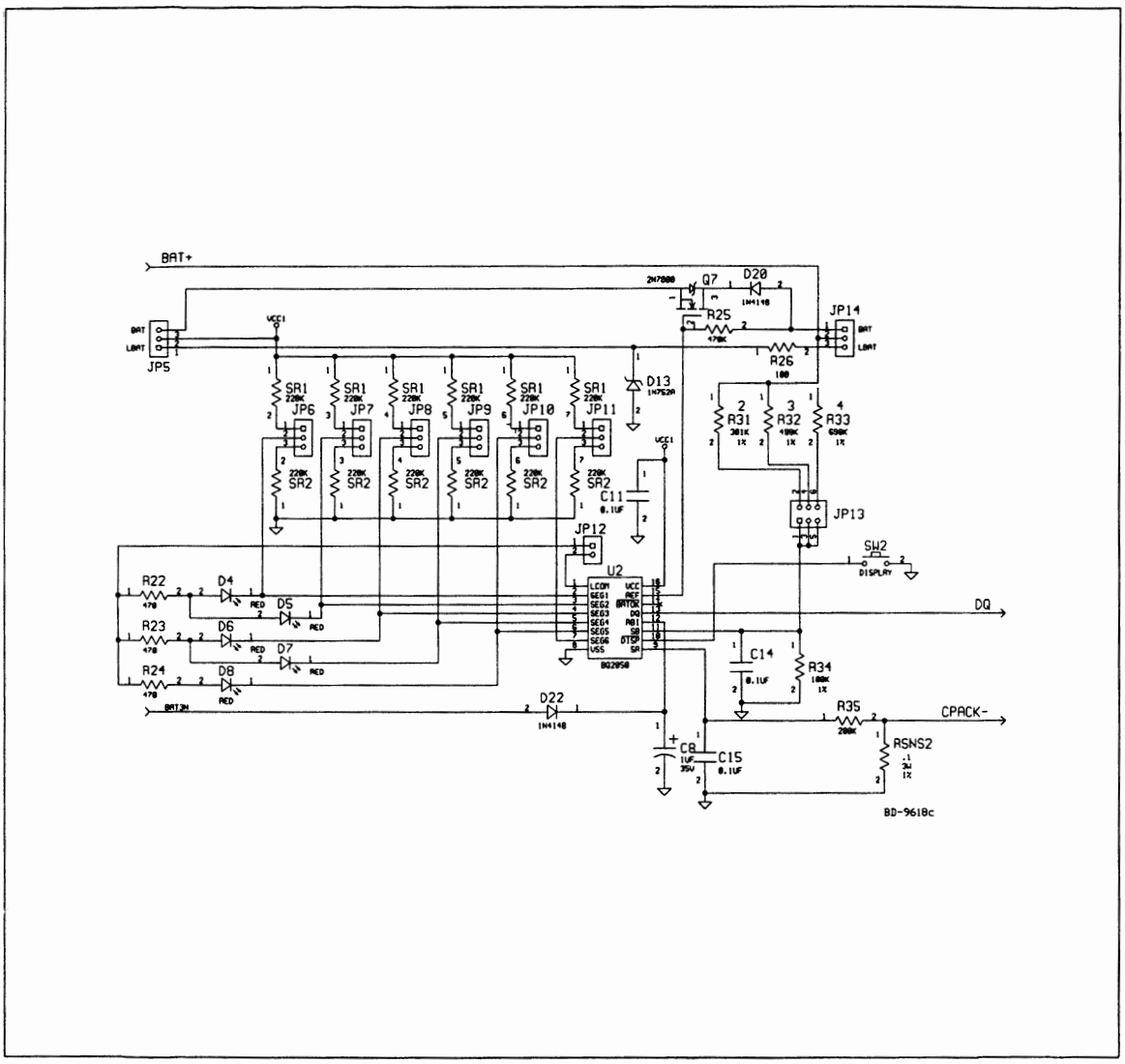
EV205x Schematic (Continued)



EV205x Schematic (Continued)



Preliminary bq2058x

Lithium Ion Pack Supervisor

Features

- Protects and individually monitors three or four Lithium Ion series cells for ovewoltage, undewoltage, and overcurrent
- Designed for battery pack integration
  - Small outline package, minimal external components and space, and low cost
  - Drives external N-FET switches
- User-selectable thresholds mask programmable by Benchmarq
- Operates on <40µA
- <1.5µA standby current
- Available in 16-pin 150-mil narrow SOIC

General Description

The bq2058 Lithium Ion Pack Supervisors are designed to control the charge and discharge voltage safety limits for three or four lithium ion (Li-Ion) series cells, accommodating battery packs containing series/ parallel configurations. The very low operating current does not overdischarge the cells during **periods** of storage and does not significantly increase the system discharge load. The bq2058 can be part of a low-cost Li-Ion charge control system within the battery pack.

The bq2058 controls two external N-FETs to limit the charge and discharge potentials. The bq2058 allows charging when each individual cell voltage is below V_{CE} (charge enable voltage). If the voltage on any cell exceeds V_{OV} (overvoltage limit) for a user-configurable delay **period** (t_{OVD}), the CHG pin is driven inactive, shutting off charge to the battery pack This safety feature prevents overcharge of any cell within the battery pack

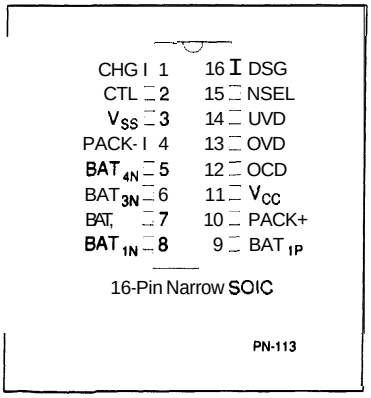
The bq2058 allows discharge when each individual cell voltage exceeds V_{UV} (undervoltage limit). If the voltage on any cell falls below V_{UV} for a user-configurable delay **period** (t_{UVD}), the DSG output becomes inactive, shutting off the battery discharge. This safety feature prevents overdischarge of **any** cell within the battery pack

The bq2058 also prevents discharging upon detection of an overcurrent condition. Overcurrent occurs in either of the following instances: when the voltage between BAT_{4N} and PACK- is greater than V_{OCL} or when the voltage between BAT_{1P} and PACK+ is greater than V_{OCH}.

Vov, V_{CE}, and V_{UV} are trimmed during manufacturing at Benchmarq. Default values are 4.25, 4.15, and 2.25V. Six different Vov limits are available (see Table 2).

The polarities of the CTL input and the CHG and DSG outputs are programmed at Benchmarq.

Pin Connections



16-Pin Narrow SOIC

PN-113

Pin Names

CHG	Charge control output	DSG	Discharge control output
CTL	Pack disable input	NSEL	3- or 4-cell selection
V_{SS}	Low potential input	UVD	Undervoltage delay input
PACK-	Pack negative input	OVD	Overvoltage delay input
BAT_{4N}	Banery 4 negative input	OCD	Overcurrent delay input
BAT_{3N}	Battery 3 negative input	V_{CC}	High potential input
BAT_{2N}	Battery 2 negative input	PACK+	Pack positive input
BAT_{1N}	Battery 1 negative input	BAT_{1P}	Banery 1 positive input

Pin Descriptions

CHG **Charge control output**

This output controls the charge path to the battery pack.

CTL **Pack disable input**

When active, this input allows an external source to disable the pack by making both DSG and CHG inactive.

V_{SS} **Low potential input**

PACK- **Battery pack negative terminal sense input**

BAT_{4N} **Battery 4 negative input**

This input is connected to the negative terminal of the cell designated BAT4 in Figure 2.

BAT_{3N} **Battery 3 negative input**

This input is connected to the negative terminal of the cell designated BAT3 in Figure 2.

BAT_{2N} **Battery 2 negative input**

This input is connected to the negative terminal of the cell designated BAT2 in Figure 2.

BAT_{1N} **Battery 1 negative input**

This input is connected to the negative terminal of the cell designated BAT1 in Figure 2. This input is connected to BAT_{1P} in a 3-cell configuration.

DSG **Discharge control output**

This output controls the discharge path to the battery pack.

NSEL **Number of cells input**

This input selects the number of series cells in the pack. NSEL should connect to V_{CC} for four cells and to V_{SS} for three cells.

UVD **Undervoltage delay input**

This input uses an external capacitor to V_{CC} to set the undervoltage delay timing.

OVD **Overvoltage delay input**

This input uses an external capacitor to Vcc to set the overvoltage delay timing.

OCD **Overcurrent delay input**

This input uses an external capacitor to V_{CC} to set the overcurrent delay timing.

V_{CC} **High potential input**

PACK+ **Battery pack positive terminal sense input**

BAT_{1P} **Battery 1 positive input**

This input is connected to the positive terminal of the cell designated BAT1 in Figure 2.

Table 1. Pin Configuration for 3- and 4-Series Cells

Number of Cells	Confiauration Pins	Battery Pins
3 cells	BAT_{1N} tied to BAT_{1P} NSEL = V_{SS}	BAT_{1N} – Positive terminal of first cell
		BAT_{2N} – Negative terminal of first cell
		BAT_{3N} – Negative terminal of second cell
		BAT_{4N} – Negative terminal of third cell
4 cells	NSEL = Vcc	BAT_{1P} – Positive terminal of first cell
		BAT_{1N} – Negative terminal of first cell
		BAT_{2N} – Negative terminal of second cell
		BAT_{3N} – Negative terminal of third cell
		BAT_{4N} – Negative terminal of fourth cell

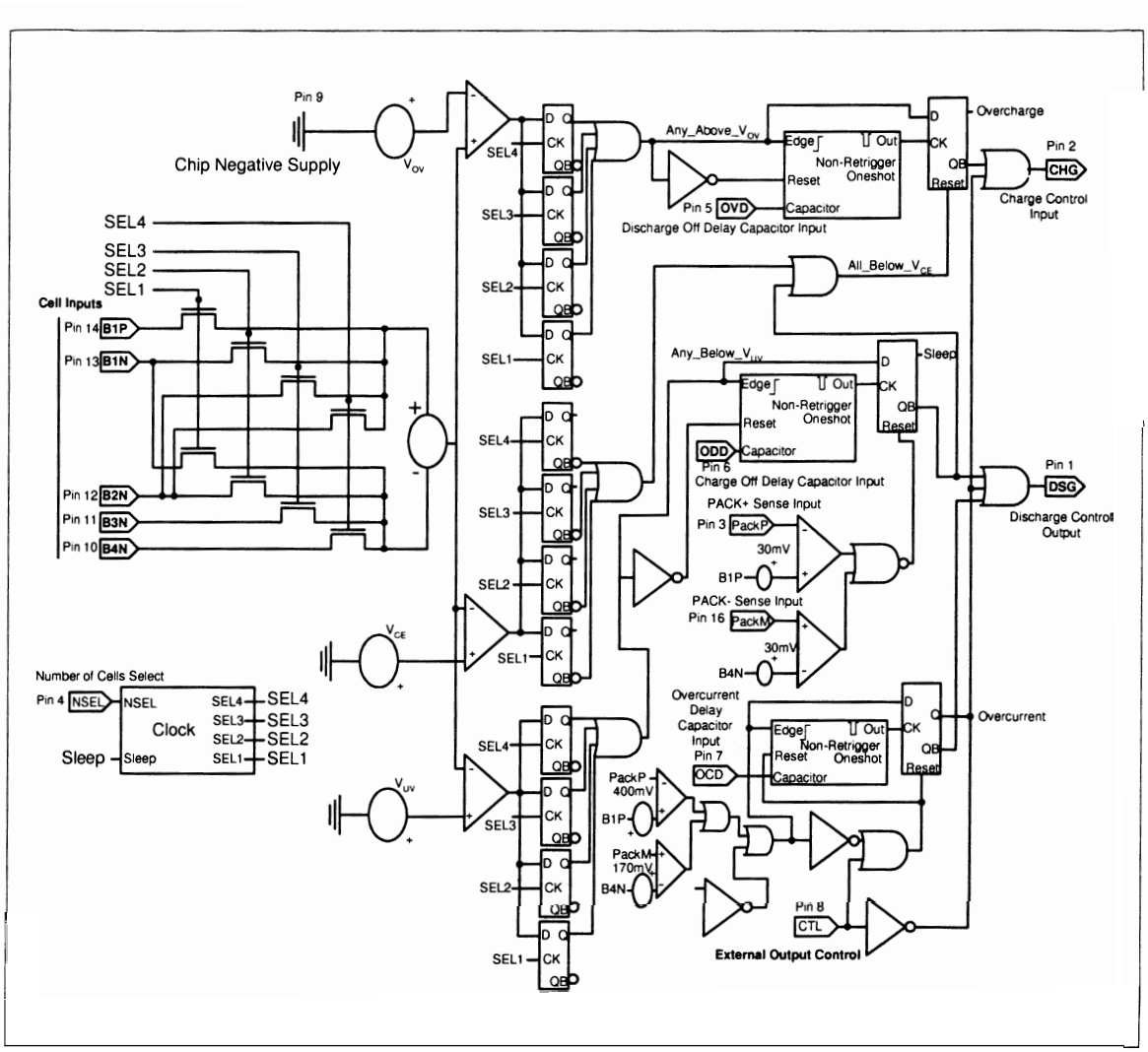


Figure 1. Block Diagram

Functional Description

Figure 1 is a block diagram outlining the major components of the bq2058. Figure 2 shows a typical application example. The following sections detail the various functional aspects of the bq2058.

Configuration

The bq2058 may be configured to supervise three- or four-series cell packs. For three-series cell configurations, BAT_{1N} is connected to BAT_{1P}. See Table 1. The bq2058 controls two external N-FETs connected for low-side control of the battery pack. Please contact Benchmarq for other application examples.

Thresholds

The bq2058 monitors four thresholds for overcharge (overvoltage), charge enable, overdischarge (undervoltage), and overcurrent protection. The following are the default values.

Overvoltage (V_{OV}) during charge:

Table 2. Overvoltage Threshold Options

Part #	V_{OV} Limit	Tolerance
bq2058M	4.15V	±50mV, ±42mV, or ±25mV
bq2058F	4.20V	
bq2058K	4.225	
bq2058	4.25V	
bq2058D	4.30V	
bq2058J	4.36V	

Charge enable voltage:

$$V_{CE} = V_{OV} - 150mV \pm 50mV$$

Undervoltage during discharge:

$$V_{UV} = 2.3V \pm 100mV$$

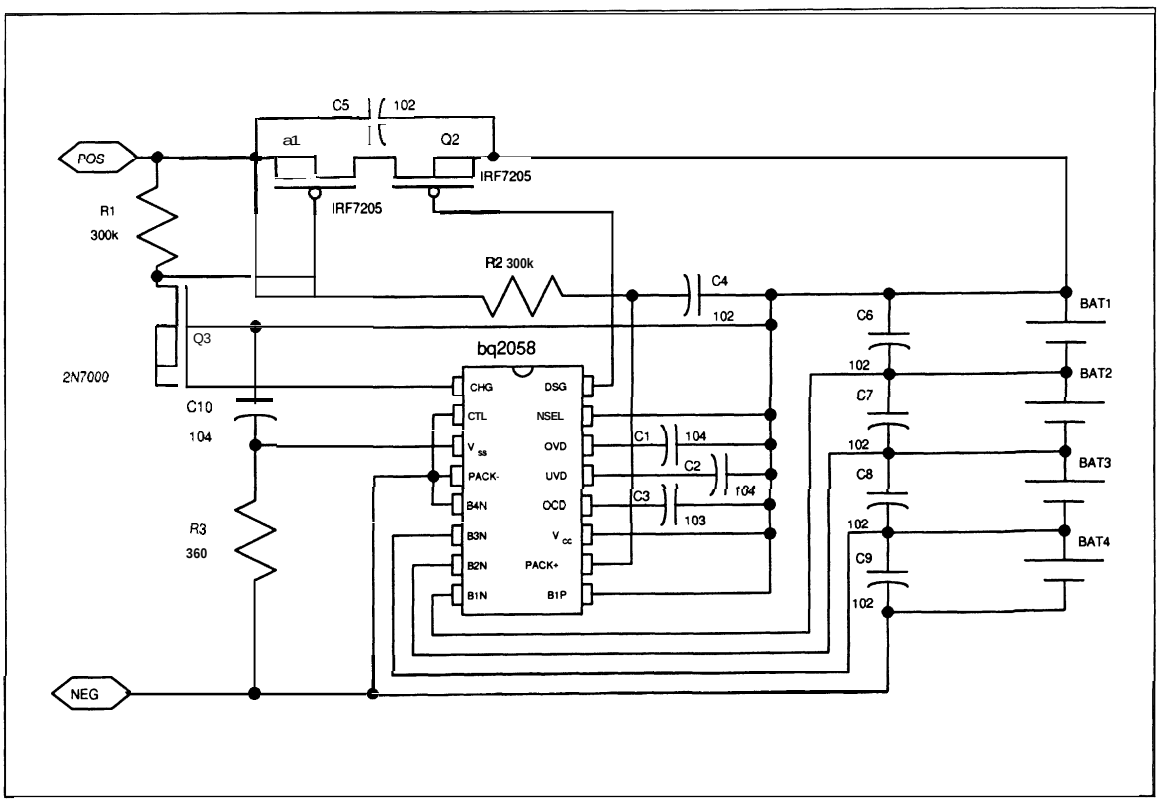


Figure 2. Typical Application Circuit

Overcurrent limit during discharge:

V_{OCH} = 400mV ± 30mV (high-side detect)

V_{OCL} = 170mV ± 30mV (low-side detect)

These thresholds are programmed at Benchmarq. Please contact Benchmarq for other voltage threshold and tolerance options.

The bq2058 samples a cell every 37.5ms (typical), and each measurement is fully differential. During this sample period, the bq2058 checks for a Vov, Vw, and V_{CE} condition. V_{OCH}, V_{OCL}, and V_{CD} (charge detect) are continuously monitored, not sampled.

Initialization

During the initial connection of the bq2058 circuit to the battery pack, the bq2058 recognizes a low voltage condition and enters the low-power mode, disabling the DSG output. A charging supply must be applied to the bq2058 circuit to enable the pack. See Low-Power Standby Mode below.

Discharge Supervision

Overdischarge protection is asserted after a user-configurable delay (t_{UVD}) when any cell voltages fall below the V_{UV} threshold. If the cell voltage remains below V_{UV} and t_{UVD} expires, DSG becomes inactive, disabling the discharge of the pack. The bq2058 then enters the low-power standby mode.

Low-Power Standby Mode

When the bq2058 enters the low-power mode, DSG is disabled, and the device consumes less than 1.5µA. The differential signal between BAT_{4N} and PACK- and PACK+ and BAT_{1P} is then continuously monitored to determine if a valid charge condition exists. If the condition exists, the output is enabled to allow charging of the lithium ion cells. The charging supply must produce a voltage greater than V_{CD} between BAT_{4N} and PACK- or PACK+ and BAT_{1P} for the bq2058 to enable the DSG output. If charging is terminated while any cell is below the V_{UV} limit, DSG again goes low after t_{UVD}, and the bq2058 returns to the low-power mode.

Charge Supervision

Overvoltage protection is asserted after a user-configurable delay (t_{OVD}) when any cell voltage exceeds the Vov threshold. If the cell voltage remains above Vov and t_{OVD} expires, the CHG pin becomes inactive, disabling charge into the battery pack. Charging is disabled until all cell voltages fall below V_{CE}. This indicates that an overcharge condition no longer exists and that the pack is ready to accept further charge.

The bq2058 can be part of a cost-effective charge control system which utilizes the pack protection circuit to limit the charge voltage to the lithium ion cells. The hysteresis between V_{OV} and V_{CE} allows the lithium ion cell voltage to fall sufficiently before re-enabling the charge current.

Overcurrent Supervision

The bq2058 monitors the voltage across the BAT_{4N} and PACK- and PACK+ and BAT_{1P} pins for an overcurrent condition. It detects an overcurrent condition if CHG and DSG are both active and either the voltage at PACK+ is V_{OCH} greater than BAT_{1P} or the voltage at PACK- is V_{OCL} less than BAT_{4N} for the entirety of the delay period.

Once these conditions are met, the discharge FET control pin (DSG) is driven inactive after a user-configurable time delay (t_{OCD}), disconnecting the load from the pack. DSG remains inactive until both of the voltage conditions listed above are false, indicating removal of the short-circuit condition. The user can facilitate clearing these conditions by inserting the battery pack into a charger or connecting a high-value resistor directly between the high side of the battery stack to PACK+ or from the low side to PACK-. In the case of a catastrophic short, the delay period t_{OCD} may be shortened due to the collapse of the battery voltage.

CHG and DSG States

Condition	CHG pin	DSG pin
Normal operation	active	active
Overvoltage	inactive	active
Undervoltage	active	inactive
Overcurrent	active	inactive

Number of Cells

The user must configure the bq2058 for three- or four-series cell operation. For a three-cell pack, NSEL should be tied directly to V_{SS}. For a four-cell pack, NSEL should be connected directly to Vcc.

In three-cell operation, BAT_{1N} is tied to BAT_{1P}.

Number of Series Cells	NSEL
3-cell	Tied to V_{SS}
4-cell	Tied to V_{CC}

Protection Delay Timers

The delay timers for all three protection parameters are reset any time the condition that started them is removed. The fault condition must therefore persist through the entire delay period, or the bq2058 will not deactivate either FET control output.

The delay time between the detection of an overcurrent, overvoltage, or undervoltage condition and the deactivation of the CHG and/or DSG outputs is user-configurable by the selection of capacitor values between the OCC, OVD, UVD pins (respectively) and V_{CC}. See Table 3 below.

Note that delay time versus capacitance is approximately linear around the typical points.

Mask Configurable Parameters

The parameters shown in Table 4, as well as the V_{OV} and other voltage thresholds and tolerances (see Table 2), are selectable by Benchmarq when the parts are manufactured. Contact the factory for availability.

Figure 3 shows a step-by-step event cycle for the bq2058.

Table 3. Protection Delay Timers

Protection Feature	Delay Period	Cap. from VCC to:	Minimum		Typical		Maximum	
			Cap.	Time	Cap.	Time	Cap.	Time
Overcurrent	t_{OCD}	OCD	0.007µF	7ms	0.010µF	10ms	0.013µF	13ms
Overvoltage	t_{OVD}	OVD	0.070µF	560ms	0.100µF	800ms	0.130µF	1040ms
Undervoltage	t w o	UVD						

Table 4. Other Mask Configurable Parameters

CHG		DSG		CTL		
Polarity	Type	Polarity	Type	Polarity	Type	FET Location
CHG	Push-pull	DSG	Push-pull	CTL	Push-pull	High-side
$\overline{CHG}$	Open drain to GND	$\overline{DSG}$	Open drain to GND	$\overline{CTL}$	Open drain to GND	Low-side
	Open drain to V_{CC}		Open drain to V_{CC}		Open drain to V_{CC}	

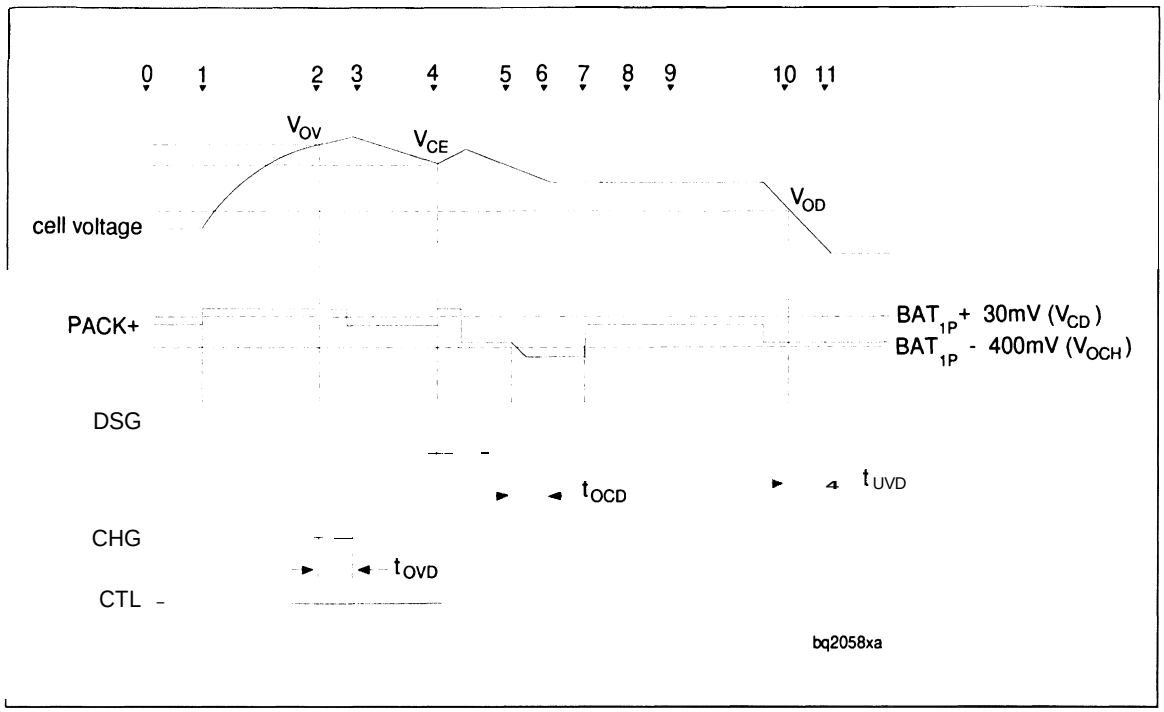


Figure 3. Example High-Side Protector Event Diagram

Event Definition:

0: The bq2058 is in the low-power sleep mode because one or more of the cell voltages are below V_{UV}.

1: A charger is applied to the pack causing the difference between PACK+ and V_{CC} to become greater than 30mV. This awakens the bq2058 and enables the discharge pin DSG.

2: One or more cells charge to a voltage equal to V_{OV} initiating the overvoltage delay timer.

3: The overvoltage delay time expires, causing CHG to go inactive.

4: All cell voltages fall below V_{CE}, re-enabling the CHG output.

5: An overcurrent condition is detected, initiating the overcurrent delay timer.

6: The overcurrent delay time expires, causing DSG to go inactive.

7: The overcurrent condition is no longer present; DSG is re-enabled.

8: Pin CTL is driven high, disabling both DSG and CHG.

9: Pin CTL is driven low, allowing DSG and CHG to resume their normal function.

10: One or more cells fall below V_{UV}, initiating the overdischarge delay timer.

11: Once the overdischarge delay timer expires, if any of the cells are below V_{UV}, the bq2058 disables DSG and goes into the low-power sleep mode.

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_T	Voltage applied on any pin relative to BAT_{1P}	-18 to +0.31	V	
T_{OPR}	Operating temperature	-30 to +70	°C	
T_{STG}	Storage temperature	-55 to +125	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Electrical Characteristics ($T_A = T_{OPR}$)

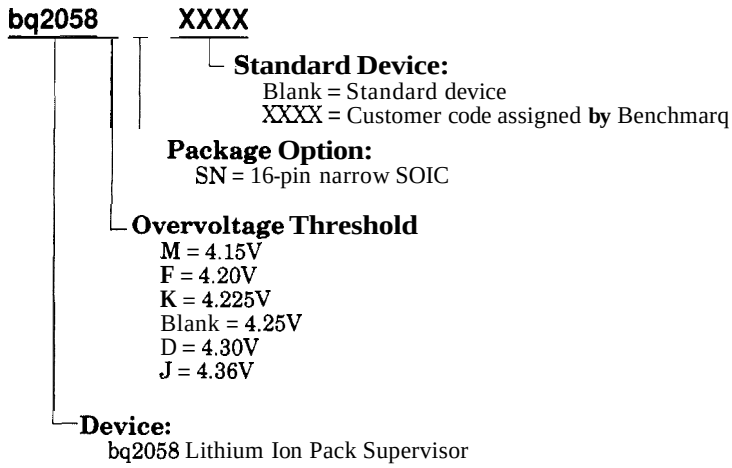
Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
V_{OH}	Output high voltage	VCC - 0.5	-	-	V	I_{OH} = 10µA
V_{OL}	Output low voltage			V_{SS} + 0.5	V	I_{OL} = 10µA
V_{OP}	V_{CC} - V_{SS}	0		18	V	
V_{IL}	Input low voltage			0.5	V	Pin CTL
V_{IH}	Input high voltage	2.0			V	Pin CTL
V_{IL}	Input low voltage			0.5	V	Pin NSEL
V_{IH}	Input high voltage	Vcc-0.5	-		-	Pin NSEL
I_{CCA}	Active current	-	25	40	µA	
I_{CCS}	Sleep current	-	.7	1.5	µA	
R_{CELL}	Input impedance	-	10		MΩ	Pins BAT4N, BAT_{3N}, BAT_{2N}, BAT_{1N}, and BAT_{1P}

DC Thresholds ($T_A = T_{OPR}$)

Symbol	Parameter	Value	Unit	Tolerance	Conditions
V_{OV}	Overvoltage threshold	4.25	V	± 50mV	See note
		Table 2			Customer option
V_{CE}	Charge enable threshold	V_{OV} - 150mV	V	± 1.75%	See note
V_{UV}	Undervoltage threshold	2.25	.V	± 100mV	See note
V_{OCH}	Overcurrent detect high-side	400	mV	± 30mV	See note
V_{OCL}	Overcurrent detect low-side	170	mV	± 30mV	See note
V_{CD}	Charge detect threshold	30	mV	+100%, -50%	See note
t_{OVD}	Overvoltage delay threshold	800	ms	±30%	C_{OVD} = 0.100µF T_A = 30°C
t_{UVD}	Undervoltage delay threshold	800	ms	±30%	C_{UVD} = 0.100µF T_A = 30°C
t_{OCD}	Overcurrent delay threshold	10	ms	±30%	C_{OCD} = 0.010µF T_A = 30°C

Note: Standard device. Contact Benchmarq for different threshold options.

Ordering Information



Notes

BENCHMARQ

Preliminary **bq2902**

Rechargeable Alkaline Charge/Discharge Controller IC

1

Features

- Safely charges two rechargeable alkaline batteries such as Renewal@from **Rayovac®**
- Terminates **pulsed** charge with maximum voltage **limit**
- Contains LED charge **status** output
- ➤ Features a pin-selectable low-battery cut-off
- **Pre-charge qualification indicates** fault **condition**
- Available in **8-pin** 300-mil **DIP** or 150-mil SOIC

General Description

The bq2902 is a **low-cost** charger for rechargeable alkaline batteries **such** as Renewal@ batteries from **Rayovac®.** The **bq2902** combines sensitive, full-charge detection for two rechargeable alkaline cells, with a low-battery cut-off for over-discharge protection.

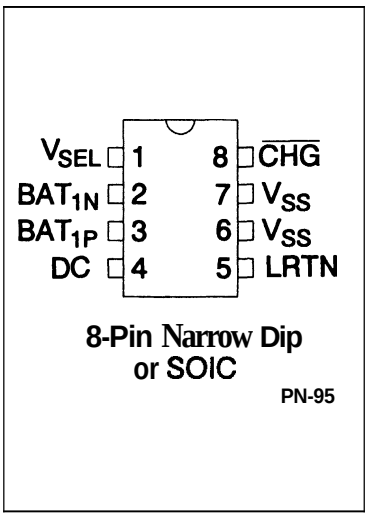
Designed for system integration into a two-cell system, the **bq2902** can improve the **service** life of the rechargeable alkaline cells by properly managing the charge and discharge. The **bq2902** requires a voltage limited current source to generate the proper charge **pulses** for the **Renewal®** cell. Each cell is individually monitored to ensure full charge without a damaging overcharge.

Charge completion is indicated when the average charge **rate** falls below approximately 3% of the fast charge rate. A **statue** output is provided to indicate charge in **progress,** charge complete, or fault indication.

The **bq2902** avoids over-depleting the battery by using the internal end-of-discharge control circuit. The **bq2902** also eliminates the external power switching transistors needed to eeparately charge individual Renewal cells.

For safety, charging is inhibited if the per-cell voltage is greater than **3.0V** during charge (closed-circuit voltage), or if the cell voltage is lees than **0.4V** (open-circuit voltage).

Pin Connections



8-Pin Narrow Dip or SOIC

PN-95

Pin Names

DC	Charging supply input
$\overline{CHG}$	Battery **status** output
BAT_{1P}	Battery 1 positive input
BAT_{1N}	Battery 1 negative input
V_{SS}	Battery 2 negative input **IC ground**
LRTN	**System load return**
V_{SEL}	**End-of-discharge** voltage select input

Pin Descriptions

DC **DC supply input**

This input is used to charge the rechargeable alkaline cells and power the bq2902 during charge. To charge the batteries, this input should be connected to a current-source limited to 300 mA. If the DC input current is greater than 300mA, the power dissipation limits of the package may be exceeded. The DC input should also be capable of supplying a minimum of 3.3V and should not exceed 5.5V.

$\overline{CHG}$ **Charge** status

This open-drain output is used to signify the battery charging status and is valid only when DC is applied.

V_{SEL} **End—f-discharge select input**

This three-level input selects the desired end-of-discharge cut-off voltage for the bq2902. V_{SEL} = BAT_{1P} selects an EDV of 1.10V. V_{SEL} floating selects EDV = 1.0V. V_{SEL} = BAT_{2N} selects EDV = 0.9.V

BAT_{1P} **Battery 1 positive input**

This input connects to the positive terminal of the battery designated BAT_1 (see Figure 3). This pin also provides power to the bq2902 when DC is not present.

BAT_{1N} **Battery 1 negative input**

This input connects to the negative terminal of the battery designated BAT_1 (see Figure 3).

V_{SS} **Battery 2 negative input/IC ground**

This input connects to the negative terminal of the battery designated BAT_2 (see Figure 3).

LRTN **Load return**

This input is the system load return.

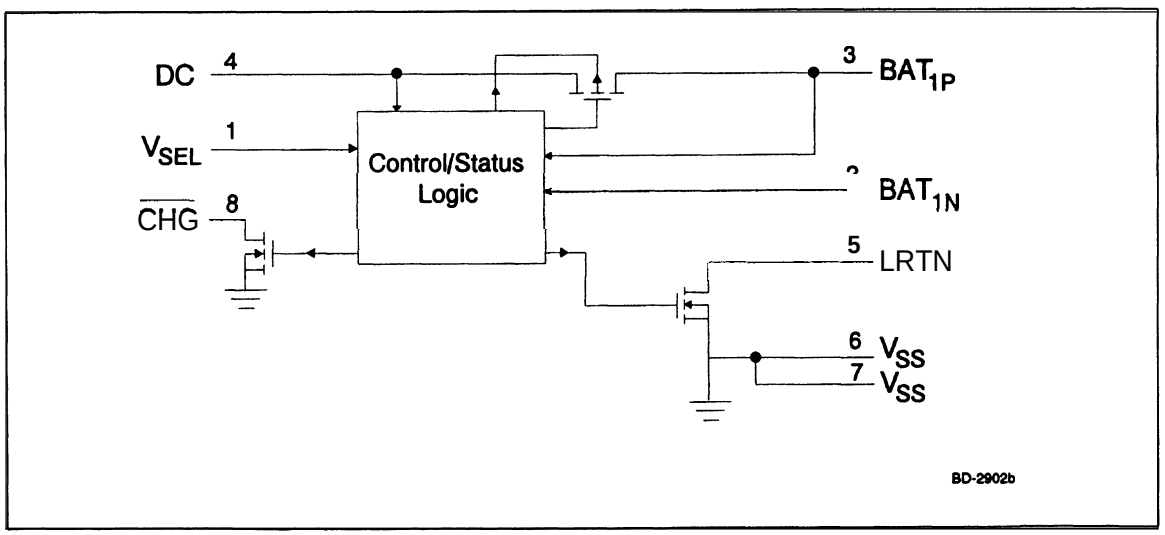


Figure 1. Functional Block Diagram

Functional Description

Figure 2 illustrates the charge control and display status during a bq2902 cycle. Table 1 outlines the various operational states and their associated conditions which are described in detail in the following section.

Charge Initiation

The bq2902 always initiates and performs a charge cycle whenever a valid DC input is applied. A charge cycle consists of pulse charging the battery and then checking for a termination condition. The charging section explains charging in greater detail.

Charge Pre-Qualification

After DC is applied, the bq2902 checks the open-circuit voltage (Vocv) of each cell for an undervoltage condition (V_{MIN} 0.4V) and begins a charge cycle when the Vocv of all cells is above V_{MIN}. If Vocv of any cell is below V_{MIN}, the bq2902 enters a charge-pending mode and indicates a fault condition (see Table 1). The bq2902 remains in a charge-pending mode until Vocv of each cell is above V_{MIN}.

Charge Termination

Once a charge cycle begins, the bq2902 terminates charge when the average charge rate falls below 3% of the maximum charge rate. The bq2902 also terminates charge when the closed-circuit voltage (Vccv) of any cell exceeds 3.0V (V_{FLT}) during charge and indicates a fault condition on the $\overline{CHG}$ output (see Table 1).

Charge Re-Initiation

If DC remains valid, the bq2902 will suspend all charge activity after full-charge termination. A charge cycle is re-initiated when all cell potentials fall below 1.4V. The rechargeable alkaline cells, unlike other rechargeable chemistries, do not require a maintenance charge to keep the cells in a fully charged state. The self-discharge rate for the Renewal cells is typically 4% per year at room temperature.

Charge Status Indication

Table 1 and Figure 2 outline the various charge action states and the associated BAT_{1P}, and $\overline{CHG}$ output states. The charge status output is designed to work with an LED indicator. In all cases, if DC is not present at the DC pin, or if the DC supply is less than the voltage at the BAT_{1P} pin, the CHG output is held in a high-impedance condition.

Charging

The bq2902 controls charging by periodically connecting the DC current-source to the battery stack, not to the individual battery cells. The charge current is pulsed from the internal clock at approximately a 100Hz rate on the BAT_{1P} pin.

Table 1. bq2902 Operational Summary

Charge Action State	Conditions	BAT_{1P} Input	$\overline{CHG}$ Output
DC absent	$V_{DC} < V_{BAT1P}$	Low battery detection per V_{SEL}	Z
Charge initiation	DC applied		
Charge pending/ fault	Vocv < 0.4V[1] or Vccv > 3.0V[2]		2/3 sec = Low 2/3 sec = Z
Charge pulse	Vocv ≤ 1.63V before pulse	Charge pulsed @ 100Hz per Figure 2	1/6 sec = Low 1/6 sec = Z
Pulse skip	Vocv > 1.63V before pulse	Pulse skipped per Figure 2	1/6 sec = Low 1/6 sec = Z
Charge complete	Average charge rate falls below 3% of the fast charge rate	Charge complete	Low

Notes: 1. Vocv = Open-circuit voltage of each cell between positive and negative leads.

2. Vccv = Closed-circuit voltage.

The bq2902 pulse charges the battery for approximately 7.5ms of every 10ms, when conditions warrant. The bq2902 measures the open-circuit voltage (Vocv) of each battery cell during the idle period. If a single-cell potential of any battery is above the maximum open-circuit voltage (V_{MAX} = 1.63V ±3%), the following pulses are skipped until all cell potentials fall below the V_{MAX} limit. Charging is terminated when the average charge rate falls below approximately 3% of the maximum charge rate. Once charging is terminated, the internal charging FET remains off, and the $\overline{CHG}$ output becomes active per Table 1 and Figure 2. With DC applied, the internal discharge FET will always remain on.

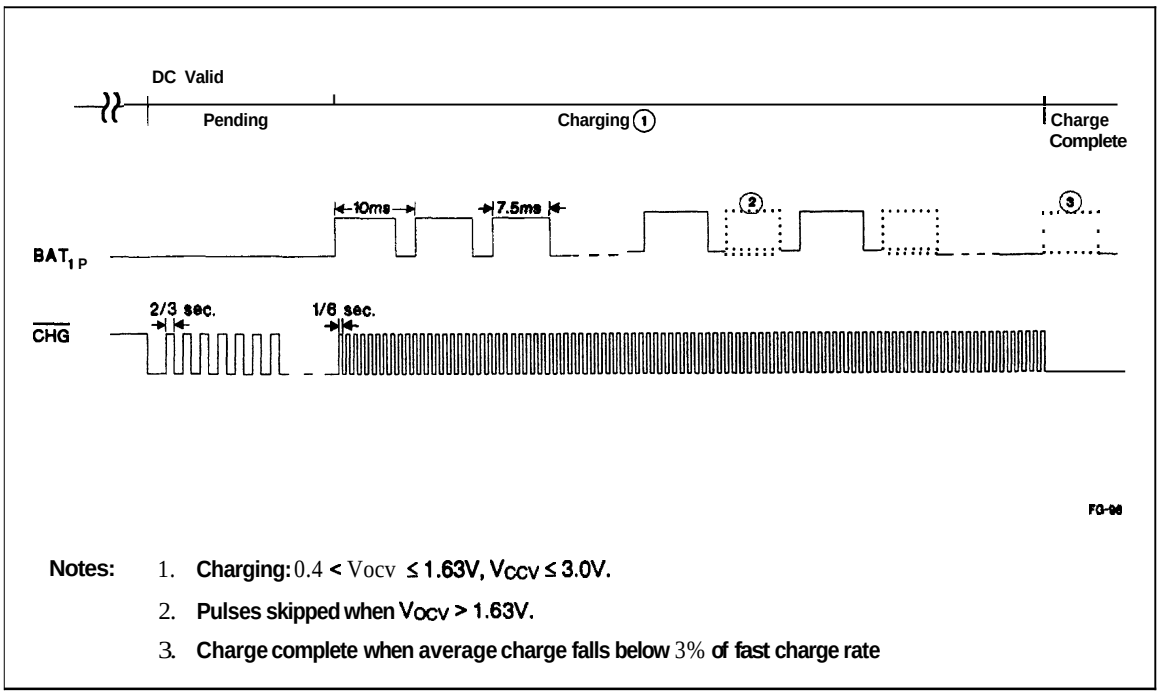
End-of-Discharge Control

When DC is not present or less than the voltage present on the BAT_{1P} pin, the bq2902 power is supplied by the voltage present at the BAT_{1P} pin. In this state, the batteries discharge down to the level determined by the V_{SEL} pin. The bq2902 monitors the cell voltage of the rechargeable alkaline cells.

If the voltage across any cell is below the voltage specified by the V_{SEL} input, the bq2902 disconnects the battery stack from the load by turning the internal discharge FET off. The discharge FET remains off until either the batteries are replaced or DC is reapplied, initiating a new charge cycle. After disconnecting the battery stack from the load, the standby current in the bq2902 is reduced to less than 1µA. The end-of-discharge voltage (V_{EDV}) is selectable by connecting the V_{SEL} pin as outlined in Table 2. After disconnecting the battery stack from the load, the standby current in the bq2902 is reduced to less than 1µA. Typically, higher discharge loads (>200mA) should use a lower discharge voltage cut-off to maximize battery capacity.

Table 2. bq2902 EDV Selections

End-of-Discharge Voltage	Pin Connection
1.10V	$V_{SEL} = BAT_{1P}$
1.00V	V_{SEL} = Z
0.90V	$V_{SEL} = BAT_{2N}$



Notes:
1. **Charging:** 0.4 < Vocv ≤ 1.63V, V_{CCV} ≤ 3.0V.
2. **Pulses skipped when Vocv > 1.63V.**
3. **Charge complete when average charge falls below 3% of fast charge rate**

Figure 2. bq2902 Application Diagram

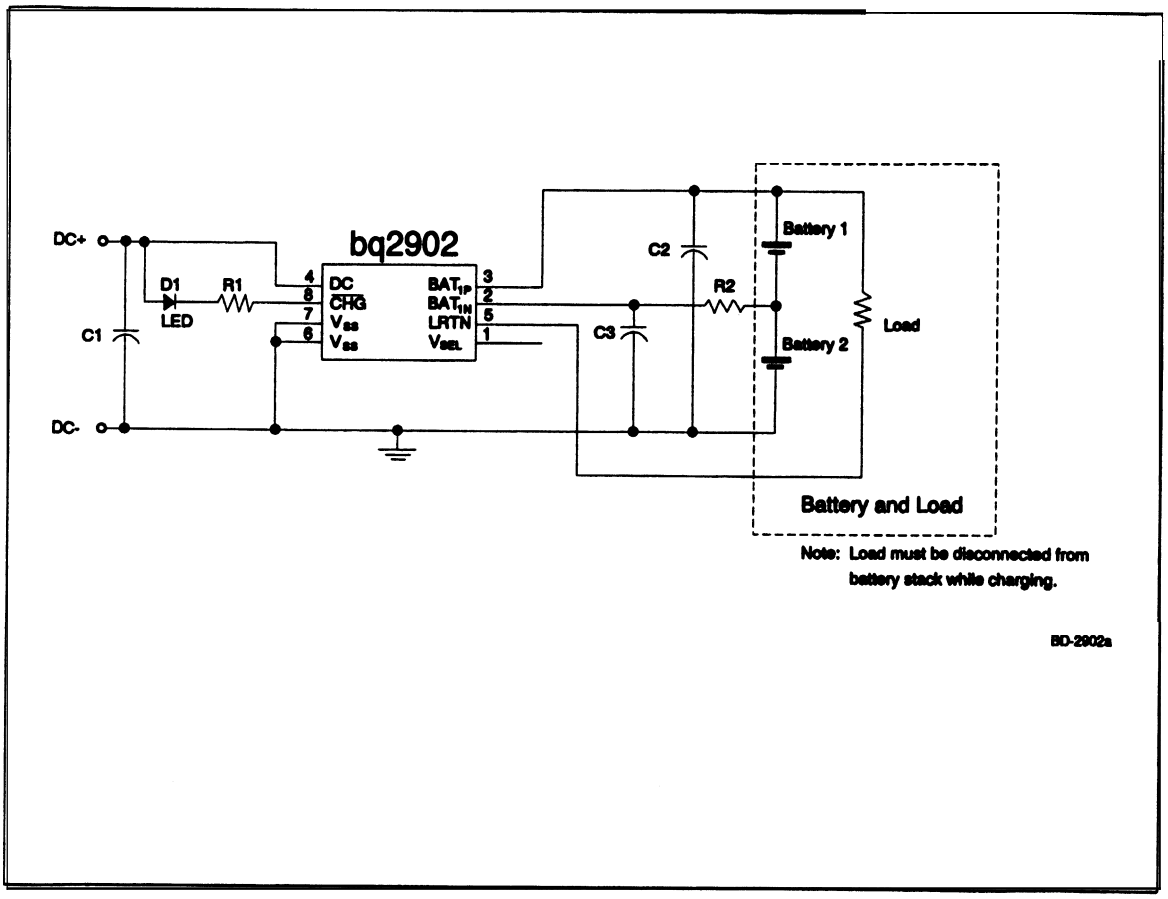


Figure 3. bq2902 Application Example, 1.0V EDV

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
DC_{IN}	V_{DC} relative to GND	-0.3	7.0	V	
V_T	DC threshold voltage applied on any pin, excluding the DC pin, relative to GND	-0.3	7.0	V	
T_{OPR}	Operating ambient temperature	0	+70	°C	Commercial
		-40	+85	°C	Industrial
T_{STG}	Storage temperature	-40	+85	°C	
T_{SOLDER}	Soldering temperature		+260	°C	10 sec max.
I_{DC}	DC charging current		400	mA	
I_{LOAD}	Discharge current		500	mA	
I_{OL}	Output current			mA	$\overline{CHG}$

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the **Recommended** DC Operating **Conditions** detailed in this data sheet. **Exposure** to conditions beyond the operational limits for extended periods of time may *affect* device reliability.

DC Thresholds (T_A = 25°C; V_{DC} = 5.5V)

Symbol	Parameter	Rating	Tolerance	Unit	Notes
V_{MAX}	Maximum open-circuit voltage	1.63	±3%	V	$V_{OCV} > V_{MAX}$ inhibits/terminates charge pulses
V_{EDV}	End-of-discharge voltage	0.90	±5%	V	$V_{SEL} = BAT_{2N}$
		1.00	±5%	V	$V_{SEL} = Z$
		1.10	±5%	V	$V_{SEL} = BAT_{1P}$
V_{FLT}	Maximum open-circuit voltage	3.00	±5%	V	$V_{CCV} > V_{FLT}$ terminates charge, indicates fault
V_{MIN}	Minimum battery voltage	0.40	±5%	V	$V_{OCV} < V_{MIN}$ inhibits charge
V_{CE}	Charge enable	1.40	±5%	V	$V_{OCV} < V_{CE}$ on both cells re-initiates charge

Note: Each DC threshold parameter above has a temperature coefficient associated with it. To determine the coefficient for each parameter, use the following formula:

$$\text{Tempco} = \frac{\text{ParameterRating}}{1.63} * -0.5\text{mV/°C}$$

The tolerance for these temperature coefficients is 10%.

1

Timing FA = TOPR)

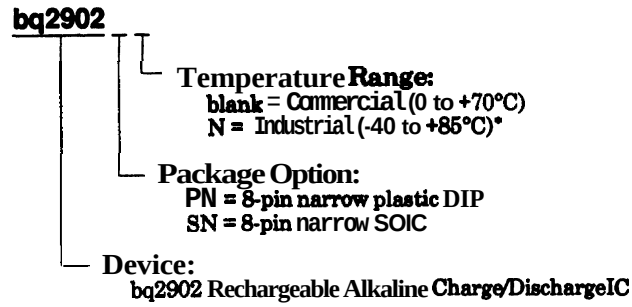
Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
tP	Pulse period		10		me	See Figure 2
tPW	Pulse width		7.5		me	See Figure 2

Note: Typical is at T_A = 25°C.

DC Electrical Characteristics (TA = TOPR)

Symbol	Parameter	inimum	Typical	Maximum	Unit	Notes
V_{IH}	Logic input high	V_{BAT1P} - 0.1		V_{BAT1P}	V	V_{SEL}
V_{IL}	Logic input low	V_{SS}		V_{SS} + 0.1	V	V_{SEL}
V_{OL}	Logic output low			0.8	V	I_{OL} = 10mA
I_{OL}	Output current	10			mA	@V_{OL} = V_{SS} + 0.8V
I_{CC}	Supply current			250	µA	Outputs unloaded, V_{DC} = 5.5V
I_{SB1}	Standby current			25	µA	V_{DC} = OV, V_{OCV} > V_{EDV}
I_{SB2}	End-of-discharge standby current			1	µA	VDC = 0V
I_L	Input leakage			±1	µA	V_{SEL}
I_{OZ}	Output leakage in high-Z state	-5			µA	$\overline{CHG}$
R_{DSON}	On resistance		0.5		Ω	Discharge FET; V_{BAT1P} = 1.8V
I_{IL}	Logic input low	-	-	70	µA	V_{SEL}
I_{IH}	Logic input high	-70	-	-	µA	V_{SEL}
I_{IZ}	Logic input float	-2	-	2	µA	V_{SEL}
I_{DC}	DC charging current	-	-	300	mA	
V_{DC}	DC charging voltage	3.3V	-	5.5	V	
I_{LOAD}	Discharge current			400	mA	
V_{OP}	Operating voltage				V	DC, BAT_{1P}

Ordering Information



* Contact factory for availability.

BENCHMARQ

bq2903

Rechargeable Alkaline Charge/Discharge Controller IC

Features

- Safe charge of three or four rechargeable alkaline batteries such as Renewal® from Rayovac®
- Pulsed charge terminated with maximum voltage limit
- LED outputs indicate charge status
- Selectable end-of-discharge voltage prevents overdischarge and improves cycle life
- Optional external FET drive allows high current loads
- Pre-charge qualification indicates fault conditions
- Automatic charge control simplifies charger design
- Available in 14-pin 300-mil DIP or 150-mil SOIC

General Description

The bq2903 is a cost-effective charge controller for rechargeable alkaline batteries such as Renewal batteries from Rayovac. The bq2903 combines sensitive, full-charge detection for three to four rechargeable alkaline cells, with a low-battery cut-off for over-discharge protection.

Designed for integration into a three- or four-cell system, the bq2903 *can* improve the service life of the rechargeable alkaline cells by properly managing the charge and discharge. The bq2903 requires a voltage-limited current source to generate the proper charge pulses for the Renewal cell. Each cell is individually monitored to ensure full charge without a damaging overcharge.

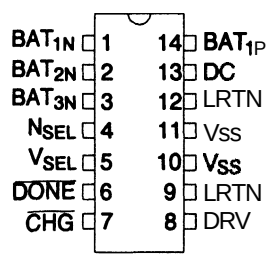
Charge completion is indicated when the average *charge* rate falls below approximately 6% of the fast charge rate. Statue outputs are provided to indicate charge in progress, charge complete, *or* fault condition.

The bq2903 avoids over-depleting the battery by using the internal end-of-discharge control circuitry. The bq2903 also eliminates the external power switching transistors needed to separately charge individual Renewal cells.

To reduce external component count, the discharge and charge control FETs are internal to the bq2903; however, if the discharge load is greater than 400mA, a DRV pin is provided to drive an external N-FET, reducing the effective *discharge* path resistance for the system.

For safety, charging is inhibited if the voltage of any cell is greater than 3.0V during charge or if the voltage of any cell is leas than 0.4V when not *charging* (open-circuit voltage).

Pin Connections



14-Pin Narrow DIP or SOIC

PN-116

Pin Names

DC	Charging supply input	BAT_{1N}	Battery 1 negative input
$\overline{CHG}$	Battery status output 1	BAT_{2N}	Battery 2 negative input
DONE	Battery status output 2	BAT_{3N}	Battery 3 negative input
N_{SEL}	Number of cells input	V_{SS}	Battery 4 negative input/ IC ground
V_{SEL}	End of discharge voltage select input	LRTN	System load return
BAT_{1P}	Battery 1 positive input	DRV	External FET drive output

Pin Descriptions

DC **DC supply input**

This input is used to recharge the rechargeable alkaline cells and power the bq2903 during charge. This input must be connected to a voltage-limited current source.

$\overline{CHG}$ **Charge status**

This open-drain output is used to signify the battery charging status and is valid only when DC is applied. See Figure 4 and Table 1.

$\overline{DONE}$ **Charge done**

This open-drain output is used to signify charge completion and is valid only when DC is applied.

N_{SEL} **Number of cells input**

This input selects whether the bq2903 charges 3 or 4 cells. N_{SEL} = BAT_{1P} selects 4 cells, and N_{SEL} = V_{SS} selects 3 cells.

V_{SEL} **End-of-discharge select input**

This three-level input selects the desired end-of-discharge cut-off voltage for the bq2903. V_{SEL} = BAT_{1P} selects an EDV of 1.10V. V_{SEL} floating selects EDV = 1.0V. V_{SEL} = V_{SS} selects EDV = 0.9V.

BAT_{1P} **Battery 1 positive input**

This input connects to the positive terminal of the battery designated BAT_1 (see Figure 3). This pin also provides power to the bq2903 when DC is not present.

BAT_{1N} **Battery 1 negative input**

This input connects to the negative terminal of the battery designated BAT_1 (see Figure 3).

BAT_{2N} **Battery 2 negative input**

This input connects to the negative terminal of the battery designated BAT_2 (see Figure 3).

BAT_{3N} **Battery 3 negative input**

Thie input connects to the negative terminal of the battery designated BAT_3 (see Figure 3).

V_{SS} **Battery 4 negative input/IC ground**

This input connects to the negative terminal of the battery designated BAT4 (see Figure 3).

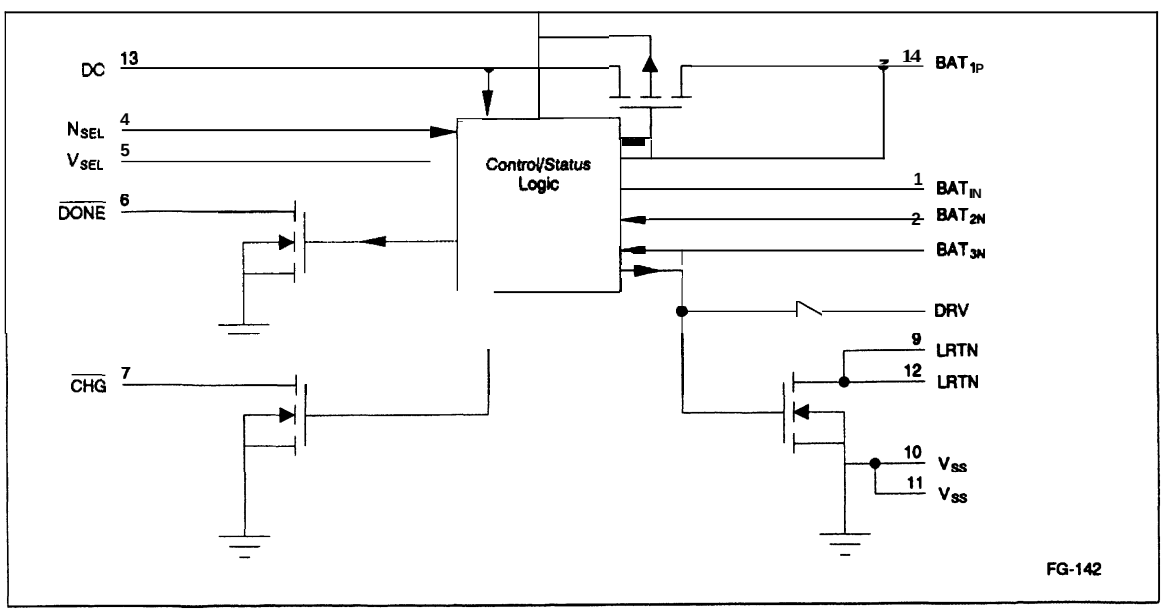


Figure 1. Functional Block Diagram

LRTN **Load** return

This input is the **system** load return.

DRV **External FET drive output**

This push-pull output drives an optional **external N-FET (see** Figure 4**). The DRV pin** should not be connected if the external FET is not used. **See** page 5 for a full **description.**

Functional Description

Figure 2 illustrates the charge **control and display status** during a **bq2903** cycle. Table **1** outlines the various operational states and their associated conditions which are described in detail in the following section.

DC Input

This input is **used** to charge the rechargeable **alkaline** cells and **power** the **bq2903 during a charge. To** charge **the** batteries, this input should be connected to a current source limited to 800mA. If the DC input current is **greater** than **300mA, the power dissipation** limits of the package will be **exceeded.** The DC input should **also** be capable of supplying a minimum of **2.0V*N,** where N **is** the number of cells to be charged. The DC input should not **exceed 10V.**

Charge Pre-Qualification

After DC is applied, the **bq2903 checks** the open-circuit voltage (**Vocv**) of each cell for an undervoltage condition (**Vocv<0.4V**). **If the Vocv of any cell is below V_{MIN}, the bq2903 enters** a charge-pending mode and **indicates** a fault **(see** Table **1).**

If all **cells are** above **V_{MIN}** and the **minimum** operating voltage **$V_{OP(min)}$=2.7V** at the **DC** pin is met, the bq2903 will initiate a charge cycle. A charge cycle **consists** of **pulse charging the battery and then checking for a nation condition.**

Charge Termination

Once a charge cycle begins, the bq2903 terminates charge when the average charge rate **falls below** 696 of the **maximum** charge rate. The **bq2903** also **terminates charge when the closed-circuit voltage (Vccv) of any cell exceeds 3.0V (V_{FLT}) during charge and indicates a fault condition on the CHG output (see Table 1).**

Charge Re-Initiation

If DC remains valid, the bq2903 will suspend all charge activity after full-charge termination. A charge cycle is re-initiated when all cell potentials fall below 1.4V. The rechargeable alkaline cells, unlike other rechargeable chemistries, do not require a maintenance charge to keep the cells in a fully charged state. The self-discharge rate for the Renewal cells is typically 4% per year at room temperature.

Charge Status Indication

Table **1** and Figure **2 outline the various charge** action states and the associated **BAT_{1P},** $\overline{CHG}$, and $\overline{DONE}$ output states. **The charge status outputs are designed work with individual or tri-color LED indicators. In cases, if the voltage at the DC pin is less than the voltage at the BAT_{1P} pin, $\overline{CHG}$ and $\overline{DONE}$ outputs are held in a** high-impedance condition.

Table 1. bq2903 Operational Summary

Charge Action State	Conditions	BAT_{1P} Input	$\overline{CHG}$ Output	$\overline{DONE}$ Output
DC absent	$V_{DC} < V_{BAT1P}$		Z	Z
Charge initiation	DC applied			
Charge pending/ fault	$V_{OCV} < 0.4V$[1] or $V_{CCV} > 3.0V$[2]		1/8 sec = Low 1/8 sec = Z	Z
Charge pulse	Vocv ≤ 1.63V before pulse	Charge pulsed @ 100Hz per Figure 1	Low	Z
Pulse skip	Vocv > 1.63V before pulse	Pulse skipped per Figure 1	Low	Z
Charge complete	Average charge rate falls below 6% of the fast charge rate	Charge complete	Z	Low

Notes: 1. **Vocv =** Open-circuit voltage of each cell between positive and negative leads.

2. **Vccv =** Closed-circuit voltage.

Charging

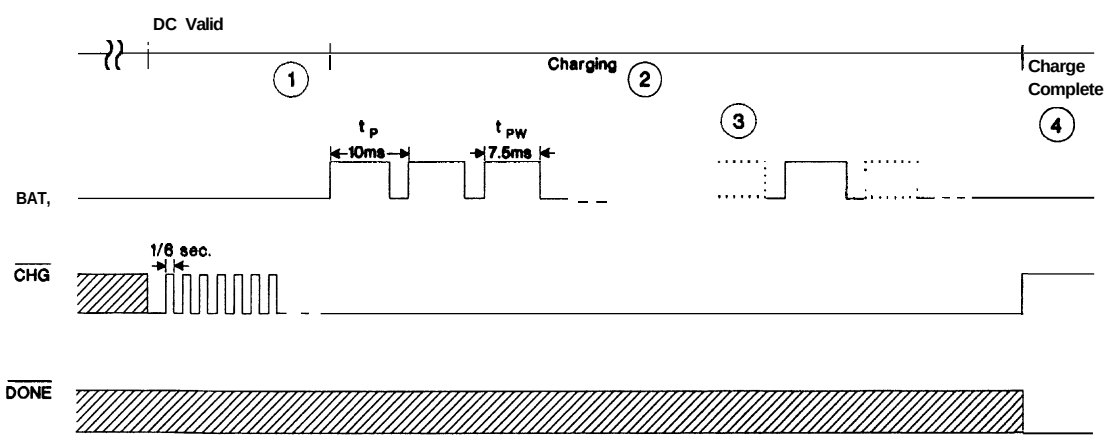
The bq2903 controls charging by periodically connecting the DC current source to the battery stack, not to the individua! battery cells. The charge current is pulsed from the internal clock at approximately a 100 Hz rate on the BAT_{1P} pin.

The bq2903 pulse charges the battery for approximately 7.5ms of every 10ms, when conditions warrant. The bq2903 measures the open circuit voltage (Vocv) of each battery cell during the idle period. If a single-cell potential of any battery is above the maximum open-circuit voltage (V_{MAX} = 1.63V ±3%), the following pulses are skipped until all cell potentials fall below the V_{MAX} limit. Charging is terminated when the average charge rate falls below approximately 6% of the maximum charge rate. Once charging is terminated, the internal charging FET remains off, and the DONE output becomes active per Table 1 and Figure 2. With DC applied, the internal discharge FET will always remain on, and the DRV output will remain high.

Endof-Discharge Control

When DC is less than the voltage on BAT_{1P}, the bq2903 is powered by the battery at BAT_{1P}. In this state, the batteries discharge down to the level determined by the V_{SEL} pin The end-of-discharge voltage (V_{EDV}) is selectable by connecting the V_{SEL} pin as outlined in Table 2. If the voltage across any cell is below the voltage specified by the V_{SEL} input, the bq2903 disconnects the battery stack from the load by turning the internal discharge FET off. The DRV output is also driven low, disabling the external FET. After disconnecting power (the battery stack) to the load, the standby current in the bq2903 is reduced to less than 1µA. Typically, higher discharge loads (>200mA) should use a lower discharge voltage cutoff to maximize battery capacity.

After disconnecting the battery stack from the load, the internal discharge FET remains off, and the DRV output remains low until the batteries are replaced or DC is reapplied, initiating a new charge cycle.



Notes:
1. Charge Pending = V_{OCV} < 0.4V per cell, Vccv > 3.0V per cell.
2. Charging: 0.4 < Vocv ≤ 1.63V, Vccv ≤ 3.0V.
3. Pulses skipped when Vocv > 1.63V.
4. Charge complete when average charge rate falls below approximately 6% of the fast charge rate.

Figure 2. bq2903 Example of Charge Action Events

Table 2. **bq2903** EDV Selections

End-of-Discharge Voltage	Pin Connection
1.10V	$V_{SEL} = BAT_{1P}$
1.00V	$V_{SEL} = Z$
0.90V	$V_{SEL} = V_{SS}$

Numberof-Cell Selection

N_{SEL} is used to select whether the bq2903 will charge 3 or 4 cells. Figure 3 shows the proper connection for a 3- or 4-cell system. For 4 cell operation, $N_{SEL} = BAT_{1P}$. For 3 cell operation, $N_{SEL} = V_{SS}$ and the BAT_{2N} pin should be connected to the BAT_{3N} pin.

DRV Pin

The bq2903 controls battery discharge with an internal FET between LRTN and Vss. The current through this switch should be limited to 400mA. To reduce the effective discharge switch resistance, or for high current loads, the DRV pin can control an external N-FET, as shown in Figure 4. DRV is "high" when a valid charging voltage is applied to the DC pin and remains "high" during discharge. DRV goes "low" during discharge to turn off the external FET when an end-of-discharge condition is met. This pin should not be connected if the external FET option is not used.

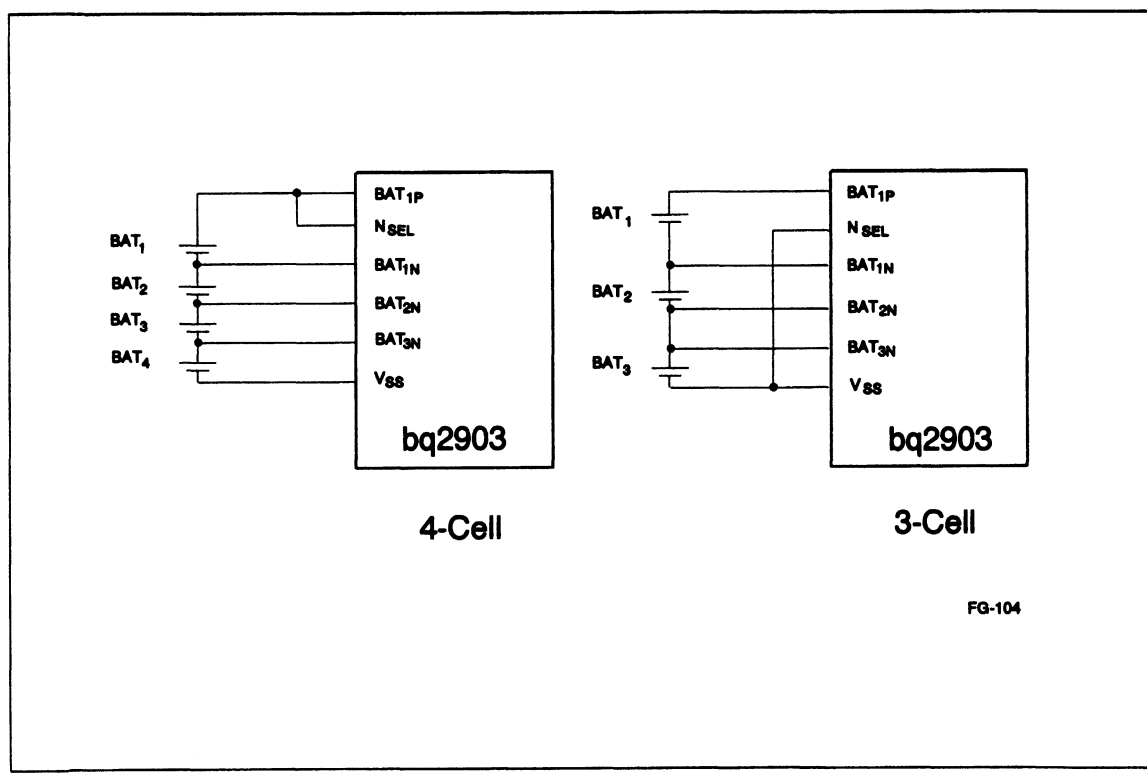


Figure 3. N_{SEL} Connection Diagram

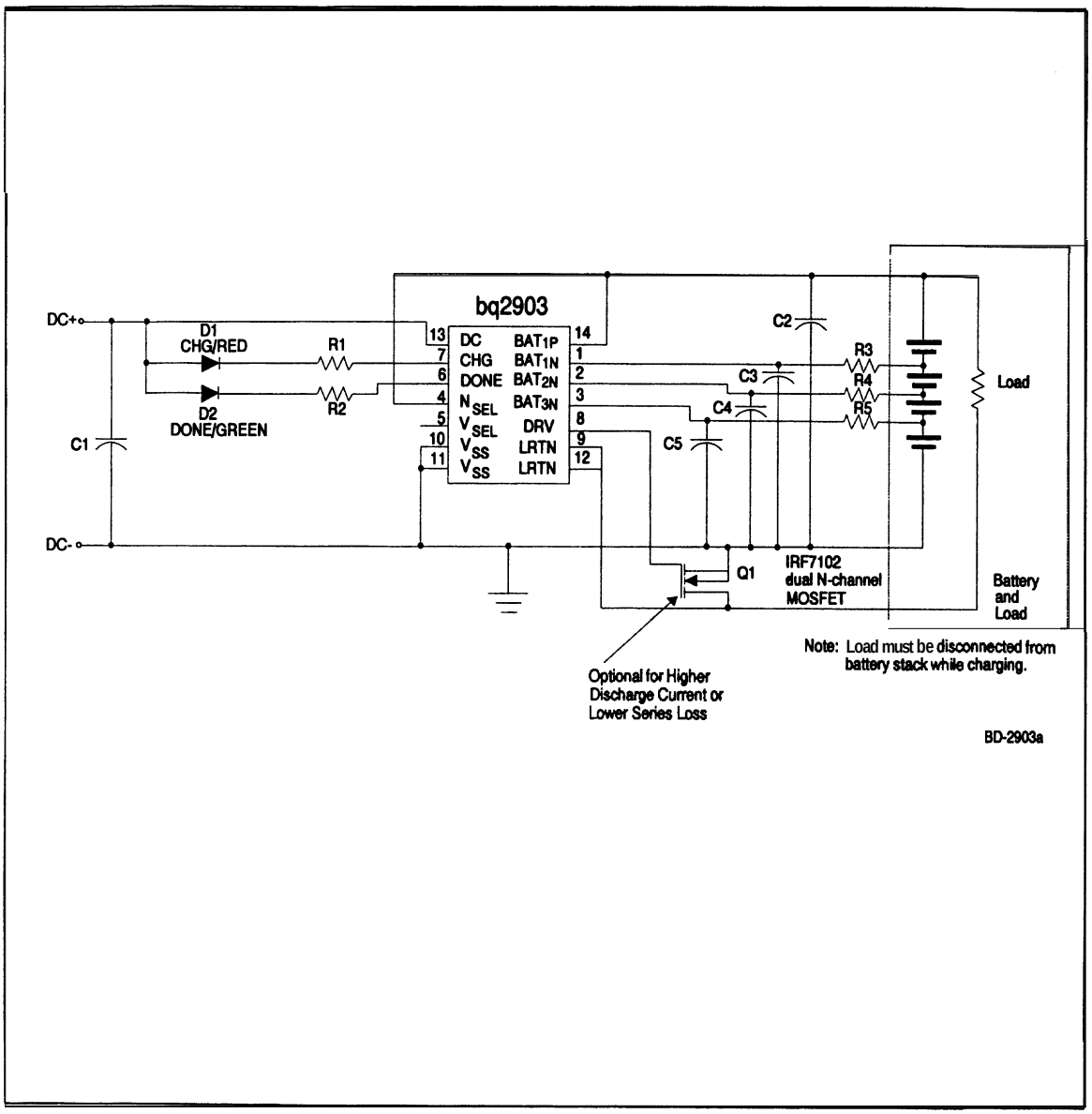


Figure 4. bq2903 Application Example, 4–Cell and 1.0V EDV

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
DC_{IN}	V_{DC}	-0.3	11.0	V	
V_T	DC threshold voltage applied on any pin, excluding DC pin	-0.3	11.0	V	
T_{OPR}	Operating ambient temperature	0	+70	°C	Commercial
		-40	+86	°C	Industrial
T_{STG}	Storage temperature	-40	+85	°C	
T_{SOLDER}	Soldering temperature		+260	°C	10 sec max.
I_{DC}	DC charging current		400	mA	
I_{LOAD}	Discharge current		500	mA	No external FET
I_{OL}	Output current		20	mA	$\overline{CHG}$, $\overline{DONE}$

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds (T_A = 25°C; V_{DC} = 10V)

Symbol	Parameter	Rating	Tolerance	Unit	Notes
V_{MAX}	Maximum open-circuit voltage	1.63	±3%	V	$V_{OCV} > V_{MAX}$ inhibits or terminates charge pulses
V_{EDV}	End-of-discharge voltage	0.90	±5%	V	$V_{SEL} = V_{SS}$
		1.00	±5%	V	V_{SEL} = Z
		1.10	±5%	V	$V_{SEL} = BAT_{1P}$
V_{FLT}	Maximum closed-circuit voltage	3.00	±5%	V	$V_{CCV} > V_{FLT}$ terminates charge, indicates fault
V_{MIN}	Minimum battery voltage	0.40	±5%	V	$V_{OCV} < V_{MIN}$ inhibits charge
V_{CE}	Charge enable	1.40	±5%	V	$V_{OCV} < V_{CE}$ on all cells re-initiates charge

Note: Each parameter above has a temperature coefficient associated with it. To determine the coefficient for each parameter, use the following formula:

$$\text{Tempco} = \frac{\text{ParameterRating}}{1.63} * -0.5\text{mV/°C}$$

The tolerance for these temperature coefficients is 10%.

Timing (T_A = 25°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_P	Pulse period	-	10	-	ms	See Figure 2
t_{PW}	Pulse width		7.5		ms	See Figure 2

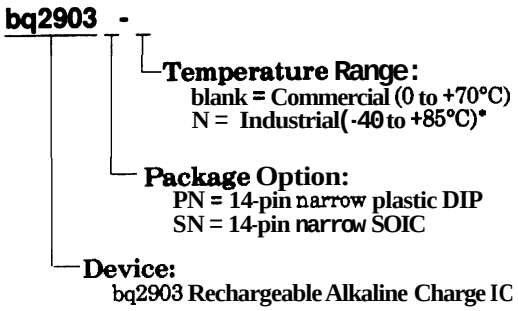
1

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
Vm	Logic input high	V_{BAT1P} - 0.1		V_{BAT1P}	V	V_{SEL}, N_{SEL}
V_{IL}	Logic input low	V_{SS}		V_{SS} + 0.1	V	V_{SEL}, N_{SEL}
V_{OL}	Logic output low			1.0	V	$\overline{DONE}$, $\overline{CHG}$, I_{OL} = 5mA
				0.4	V	I_{OL} = 1.0mA, DRV
V_{OH}	Gate drive output	(Greater of V_{BAT1P} or V_{DC}) - 1.0			V	DRV, I_{OH} = -1.0mA
I_{OL}	Output current	5			mA	V_{OL} = V_{SS} + 1.0V, $\overline{CHG}$, $\overline{DONE}$
		1			mA	DRV = V_{SS} + 1.0V
I_{DC}	Supply current		35	250	µA	Outputs unloaded. V_{DC} = 10.0V
I_{SB1}	Standby current		25	40	µA	V_{DC} = 0, V_{OCV} > V_{EDV}, BAT_{1P-3N}
I_{SB2}	End-of-discharge standby current			1	µA	V_{DRV} = OV, V_{DC} = 0
I_L	Input leakage			±1	µA	NSEL
I_{OZ}	Output leakage in high-Z state			±5	µA	$\overline{CHG}$, $\overline{DONE}$
R_{DSON}	Discharge on resistance		0.5		Ω	Discharge FET; V_{BAT1P} = 2.7V
I_{LOAD}	Discharge current without external N-FET			400	mA	No external FET
I_{IL}	Logic input low			70	µA	V= GND to GND + 0.5V, V_{SEL}
I_{IH}	Logic input high	-70			µA	V = V_{DC} -0.5 to V_{DC}, V_{SEL}
I_{IZ}	Logic input float	-2		2	µA	V_{SEL}
I_{DC}	DC charging current			300	mA	
V_{OP}	Operating voltage	2.7		10	V	

Note: All voltages relative to V_{SS}.

Ordering Information



* Contact factory for availability

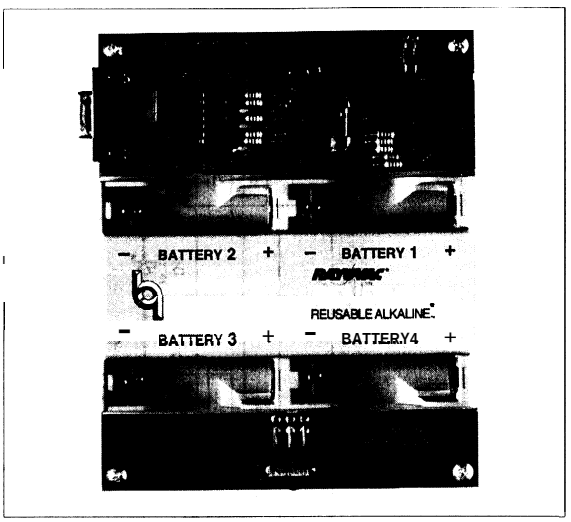
BENCHMARQ

Product Brief **EV2903**

bq2903 Evaluation System

Features

- ➤ bq2903 fast charge control evaluation and development system for rechargeable alkaline batteries such as Renewal® from Rayovac®
- Optional on-board 300mA current-limited charge supply
- Fast charge of three or four alkaline cells
- Pulsed charge terminated by minimum current and backed up by a maximum voltage safety termination
- Selectable end-of-discharge voltage
- Charge status indicator LEDs
- Datalog capability for charge and discharge currents through an RS-232 port to a PC



The user provides batteries and DC power supply. The user configures the EV2903 for the number of cells (three or four), end-of-discharge voltage, and on-board or off-board current regulation.

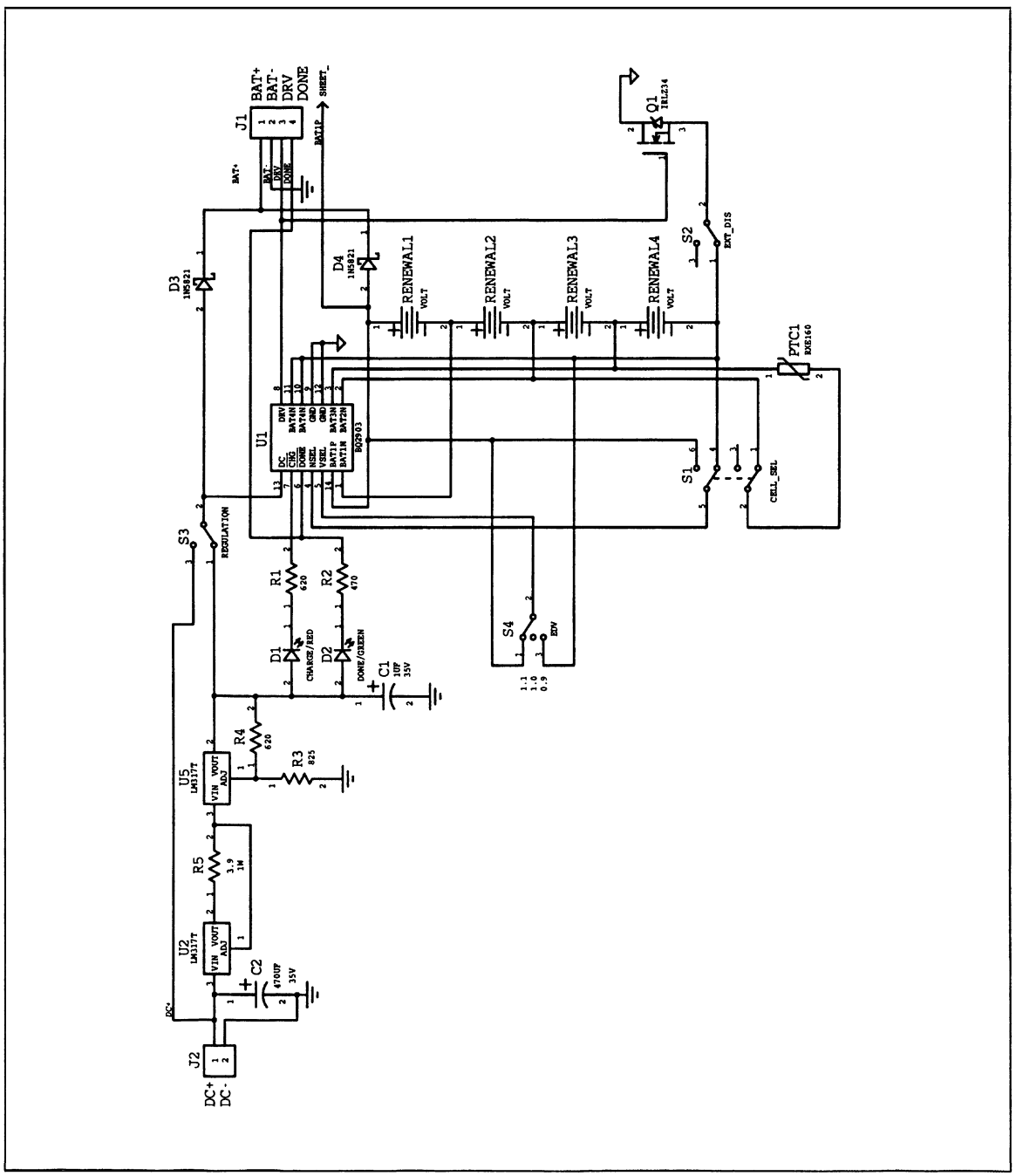
A full data sheet of this product is available on our web site (http://www.benchmarq.com), or you may contact the factory for one.

General Description

The EV2903 Evaluation System provides a development and evaluation environment for the bq2903 Rechargeable Alkaline Charge/Discharge Controller IC. The EV2903 incorporates a bq2903, a bq2014 Gas Gauge IC, an on-board discharge N-FET, and all other hardware needed to charge three or four rechargeable alkaline batteries, such as Renewal from Rayovac.

Fast charge is terminated when the average charge rate falls below approximately 3% of the fast charge rate. For safety, charging is inhibited if the voltage of any cell is greater than 3.0V during charge or if the voltage of any cell is less than 0.4V when not charging (open-circuit voltage).

EV2903 Schematic



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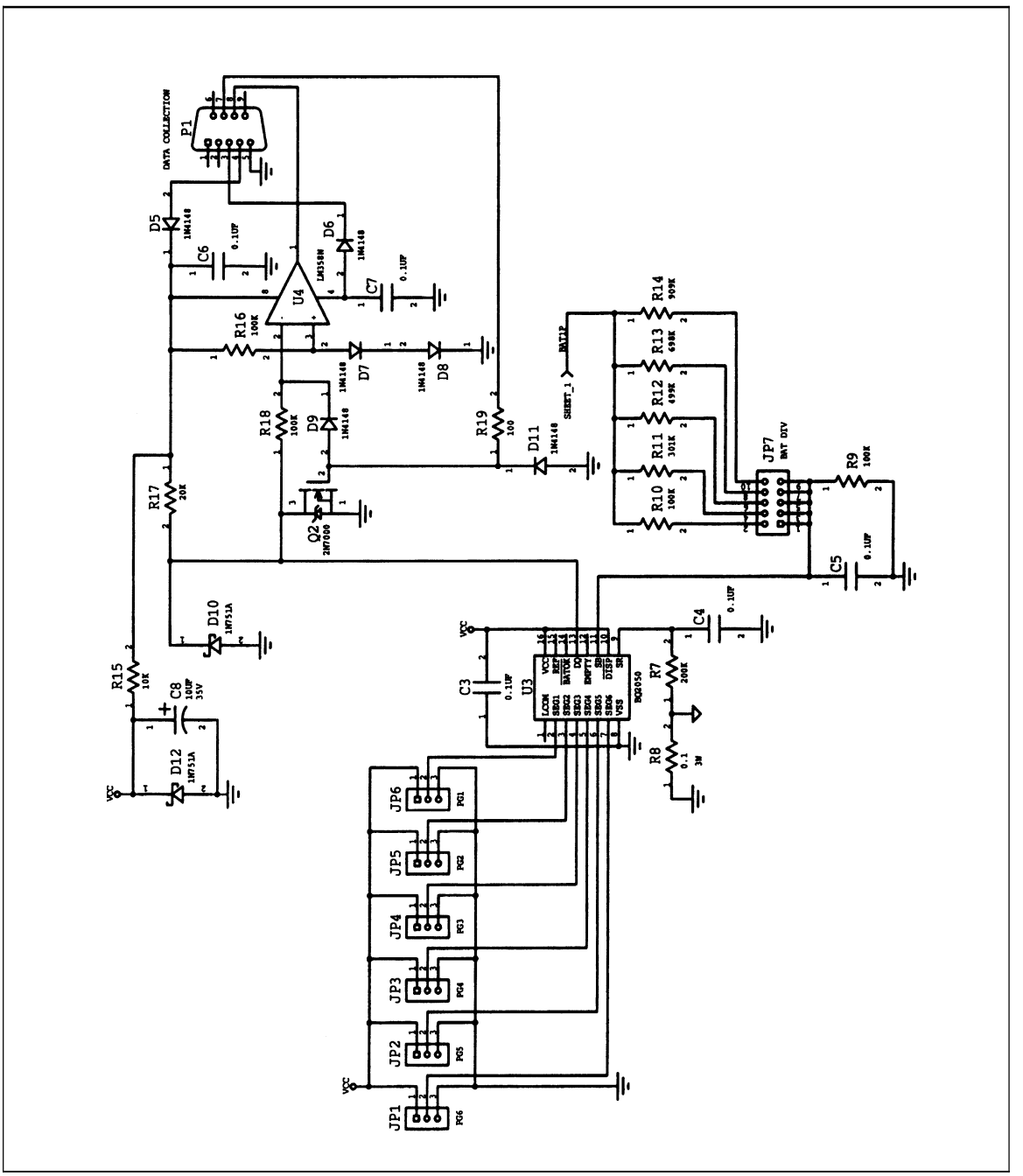
EV2903 Schematic (Continued)



Notes

bq2010
Gas Gauge IC

Features

- Conservative and repeatable measurement of available charge in rechargeablebatteries
- Designed for battery pack integration
  - 120µA typical standby current
  - Small size enables implementations in as little as ½ square inch of PCB
- Integrate within a system or as a stand-alone device
  - Display capacity via single-wire aerial communication port or direct drive of LEDs
- Measurements compensated for current and temperature
- Self-discharge compensation using internal temperature sensor
- Accurate measurements across a wide range of current (> 500:1)
- 16-pin narrow SOIC

General Description

The bq2010 Gas Gauge IC is intended for battery-pack or in-system installation to maintain an accurate record of a battery's available charge. The IC monitors a voltage drop across a sense resistor connected in series between the negative battery terminal and ground to determine charge and discharge activity of the battery.

NiMH and NiCd battery self-discharge is estimated baaed on an inter nal timer and temperature sensor. Compensations for battery temperature and rate of charge or discharge are applied to the charge, discharge, and self-discharge calculations to provide available charge information across a wide range of operating conditions. Battery capacity is automatically recalibrated, or "learned," in the course of a discharge cycle from full to empty.

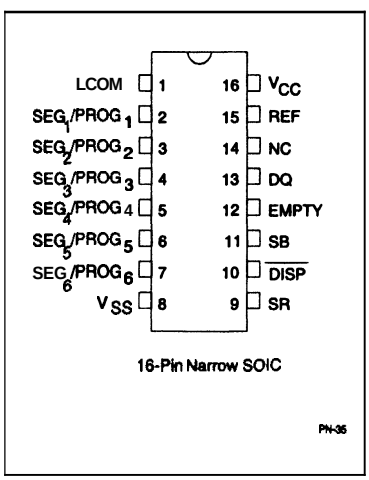
Nominal available charge may be directly indicated using a five- or six-segment LED display. Theae segments are used to indicate graphically the nominal available charge.

The bq2010 supports a simple single-line bidirectional aerial link to an external processor (common ground). The bq2010 outputs battery information in response to external commands over the serial link.

The bq2010 may operate directly from 3 or 4 cells. With the REF output and an external transistor, a simple, inexpensive regulator can be built to provide Vcc across a greater number of cells.

Internal registers include available charge, temperature, capacity, battery ID, battery status, and programming pin settings. To support subassembly testing, the outputs may also be controlled. The external processor may also overwrite some of the bq2010 gas gauge data registers.

Pin Connections



16-Pin Narrow SOIC

Pin Names

LCOM	LED common output	REF	Voltage reference output
$SEG_1/PROG_1$	LED segment 1/ program 1 input	NC	No connect
$SEG_2/PROG_2$	LED segment 2/ program 2 input	DQ	Serial communications input/output
$SEG_3/PROG_3$	LED segment 3/ program 3 input	EMPTY	Empty battery indicator output
$SEG_4/PROG_4$	LED segment 4/ program 4 input	SB	Battery sense input
$SEG_5/PROG_5$	LED segment 5/ program 5 input	$\overline{DISP}$	Display control input
$SEG_6/PROG_6$	LED segment 6/ program 6 input	SR	Sense resistor input
		Vcc	3.0-6.5V
		Vss	System ground

Pin Descriptions

LCOM LED common output

Open-drain output switches V_{CC} to source current for the LEDs. The switch is off during initialization to allow reading of the soft pull-up or pull-down program resistors. LCOM is also high impedance when the display is off.

SEG_1–SEG_6 LED display segment outputs (dual function with $PROG_1$–$PROG_6$)

Each output may activate an LED to sink the current sourced from LCOM.

$PROG_1$–$PROG_2$ Programmed full count selection inputs (dual function with SEG_1–SEG_2)

These three-level input pins define the programmed full count (PFC) thresholds described in Table 2.

$PROG_3$–$PROG_4$ Gas gauge rate selection inputs (dual function with SEG_3–SEG_4)

These three-level input pins defiie the scale factor described in Table 2.

$PROG_5$ Self-discharge rate selection (dual function with SEG_5)

This three-level input pin defines the selfdischarge compensation rate shown in Table 1.

$PROG_6$ Display mode selection (dual function with SEG_6)

This three-level pin defines the display operation shown in Table 1.

NC No connect

SR Sense resistor input

The voltage drop (V_{SR}) across the sense resistor R_S is monitored and integrated over time to interpret charge and discharge activity. The SR input is tied to the high side of the sense resistor. $V_{SR} < V_{SS}$ indicates discharge, and $V_{SR} > V_{SS}$ indicates charge. The effective voltage drop, V_{SRO}, as seen by the bq2010 is $V_{SR} + V_{OS}$ (see Table 4).

$\overline{DISP}$ Display control input

$\overline{DISP}$ high disables the LED display. $\overline{DISP}$ tied to V_{CC} allows $PROG_X$ to connect directly to Vcc or Vss instead of through a pull-up or pull-down resistor. $\overline{DISP}$ floating allows the LED display to be active during discharge or charge if the NAC registers update at a rate equivalent to $|V_{SRO}| \geq 4mV$. $\overline{DISP}$ low activates the display. See Table 1.

SB Secondary battery input

This input monitors the single-cell voltage potential through a high-impedance resistive divider network for end-of-discharge voltage (EDV) thresholds, maximum charge voltage (MCV), and battery removed.

EMPTY Battery empty output

This open-drain output becomes high-impedance on detection of a valid end-of-discharge voltage (V_{EDVF}) and is low following the next application of a valid charge.

DQ Serial I/O pin

This is an open-drain bidirectional pin.

REF Voltage reference output for regulator

REF provides a voltage reference output for an optional micro-regulator.

V_{CC} Supply voltage input

V_{SS} Ground

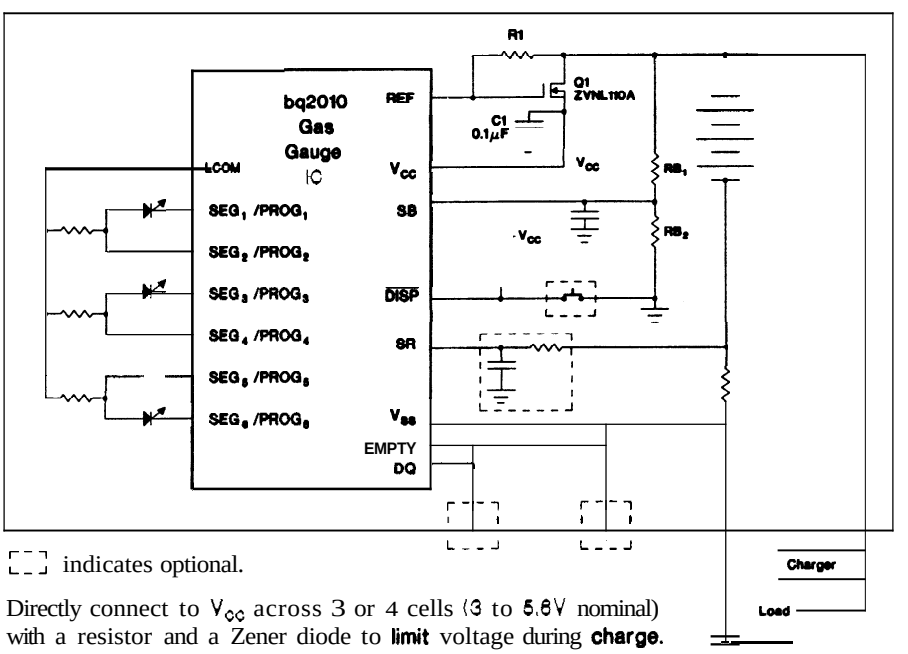
Functional Description

General Operation

The bq2010 determines battery capacity by monitoring the amount of charge input to or removed from a rechargeable battery. The bq2010 measures discharge and charge currents, estimates self-discharge, monitors the battery for low-battery voltage thresholds, and compensates for temperature and charge/discharge rates. The charge measurement derives from monitoring the voltage acmes a small-value series sense resistor between the negative battery terminal and ground. The available battery charge is determined by monitoring this voltage over time and correcting the measurement for the environmental and operating conditions.

Figure 1 shows a typical battery pack application of the bq2010 using the LED display capability as a charge-state indicator. The bq2010 can be configured to display capacity in either a relative or an absolute display mode. The relative display mode uses the last measured discharge capacity of the battery as the battery 'full' reference. The absolute display mode uses the programmed full count (PFC) as the full reference, forcing each segment of the display to represent a fixed amount of charge. A push-button display feature is available for momentarily enabling the LED display.

The bq2010 monitors the charge and discharge currents as a voltage across a sense resistor (see R_S in Figure 1). A filter between the negative battery terminal and the SR pin may be required if the rate of change of the battery current is too great.



[ ] indicates optional.

Directly connect to V_{CC} across 3 or 4 cells (3 to 5.6V nominal) with a resistor and a Zener diode to limit voltage during charge. Otherwise, R1, C1, and Q1 are needed for regulation of > 4 cells. The value of R1 depends on the number of cells.

Programming resistors (6 max.) and ESD-protection diodes are not shown.

R-C on SR may be required, application-specific.

SD-179

Figure 1. Battery Pack Application Diagram—LED Display

Voltage Thresholds

In conjunction with monitoring V_{SR} for charge/discharge currents, the bq2010 monitors the single-cell battery potential through the SB pin. The single-cell voltage potential is determined through a resistor/divider network according to the following equation:

$$\frac{RB_1}{RB_2} = N - 1$$

where N is the number of cells, RB_1 is connected to the positive battery terminal, and RB_2 is connected to the negative battery terminal. The single-cell battery voltage is monitored for the end-of-discharge voltage (EDV) and for maximum cell voltage (MCV). EDV threshold levels are used to determine when the battery has reached an 'empty" state, and the MCV threshold is used for fault detection during charging.

Two EDV thresholds for the bq2010 are fixed at:

V_{EDV1} (early warning) = 1.05V

V_{EDVF} (empty) = 0.95V

If V_{SB} is below either of the two EDV thresholds, the associated flag is latched and remains latched, independent of V_{SB}, until the next valid charge. EDV monitoring may be disabled under certain conditions as described in the next paragraph.

During discharge and charge, the bq2010 monitors V_{SR} for various thresholds. These thresholds are used to compensate the charge and discharge rates. Refer to the count compensation section for details. EDV monitoring is disabled if $V_{SR} \leq -250mV$ typical and resumes ½ second after $V_{SR} > -250mV$.

EMPTY Output

The EMPTY output switches to high impedance when $V_{SB} < V_{EDVF}$ and remains latched until a valid charge occurs. The bq2010 also monitors V_{SB} relative to V_{MCV}, 2.25V. V_{SB} falling from above V_{MCV} resets the device.

Reset

The bq2010 recognizes a valid battery whenever V_{SB} is greater than 0.1V typical. Vse rising from below 0.25V or falling from above 2.25V resets the device. Reset can also be accomplished with a command over the serial port as described in the Reset Register section.

Temperature

The bq2010 internally determines the temperature in 10°C steps centered from -35°C to +85°C. The temperature steps are used to adapt charge and discharge rate compensations, self-discharge counting, and available charge display translation. The temperature range is available over the aerial port in 10°C increments as shown below:

TMPGG (hex)	Temperature Range
0x	< -30°C
1x	-30°C to -20°C
2x	-20°C to -10°C
3x	-10°C to 0°C
4x	0°C to 10°C
5x	10°C to 20°C
6x	20°C to 30°C
7x	30°C to 40°C
8x	40°C to 50°C
9x	50°C to 60°C
Ax	60°C to 70°C
Bx	70°C to 80°C
Cx	> 80°C

Layout Considerations

The bq2010 measures the voltage differential between the SR and Vss pins. V_{OS} (the offset voltage at the SR pin) is greatly affected by PC board layout. For optimal results, the PC board layout should follow the strict rule of a singlepoint ground return. Sharing high-current ground with small signal ground causes undesirable noise on the small signal nodes. Additionally:

- The capacitors (SB and V_{CC}) should be placed as close as possible to the SB and V_{CC} pins, respectively, and their paths to V_{SS} should be as short as possible. A high-quality ceramic capacitor of 0.1µf is recommended for Vcc.
- The sense resistor capacitor should be placed as close as possible to the SR pin.
- The sense resistor (R_{SNS}) should be as close as possible to the bq2010.

Gas Gauge Operation

The operational overview diagram in Figure 2 illustrates the operation of the bq2010. The bq2010 accumulates a measure of charge and discharge currents, as well as an estimation of sell-discharge. Charge and discharge currents are temperature and rate compensated, whereas self-discharge is only temperature compensated.

The main counter, Nominal Available Charge (NAC), represents the available battery capacity at any given time. Battery charging increments the NAC register, while battery discharging and self-discharge decrement the NAC register and increment the DCR (Discharge Count Register).

The Discharge Count Register (DCR) is used to update the Last Measured Discharge (LMD) register only if a complete battery discharge from full to empty occurs without any partial battery charges. Therefore, the bq2010 adapts its capacity determination based on the actual conditions of discharge.

The battery's initial capacity is equal to the Programmed Full Count (PFC) shown in Table 2. Until LMD is updated, NAC counts up to but not beyond this threshold during subsequent charges. This approach allows the gas gauge to be charger-independent and compatible with any type of charge regime.

1. **Last Measured Discharge (LMD) or learned battery capacity:**

   LMD is the last measured discharge capacity of the battery. On initialization (application of Vcc or battery replacement), LMD = PFC. During subsequent discharges, the LMD is updated with the latest measured capacity in the Discharge Count Register (DCR) representing a discharge from full to below EDV1. A qualified discharge is necessary for a capacity transfer from the DCR to the LMD register. The LMD also serves as the 100% reference threshold used by the relative display mode.

2. **Programmed Full Count (PFC) or initial battery capacity:**

   The initial LMD and gas gauge rate values are programmed by using $PROG_1$-$PROG_4$. The PFC also provides the 100% reference for the absolute display mode. The bq2010 is configured for a given application by selecting a PFC value from Table 2. The correct PFC may be determined by multiplying the rated battery capacity in mAh by the sense resistor value:

   Battery capacity (mAh) • sense resistor (Ω) =

   PFC (mVh)

   Selecting a PFC slightly less than the rated capacity for absolute mode provides capacity above the full reference for much of the battery's life.

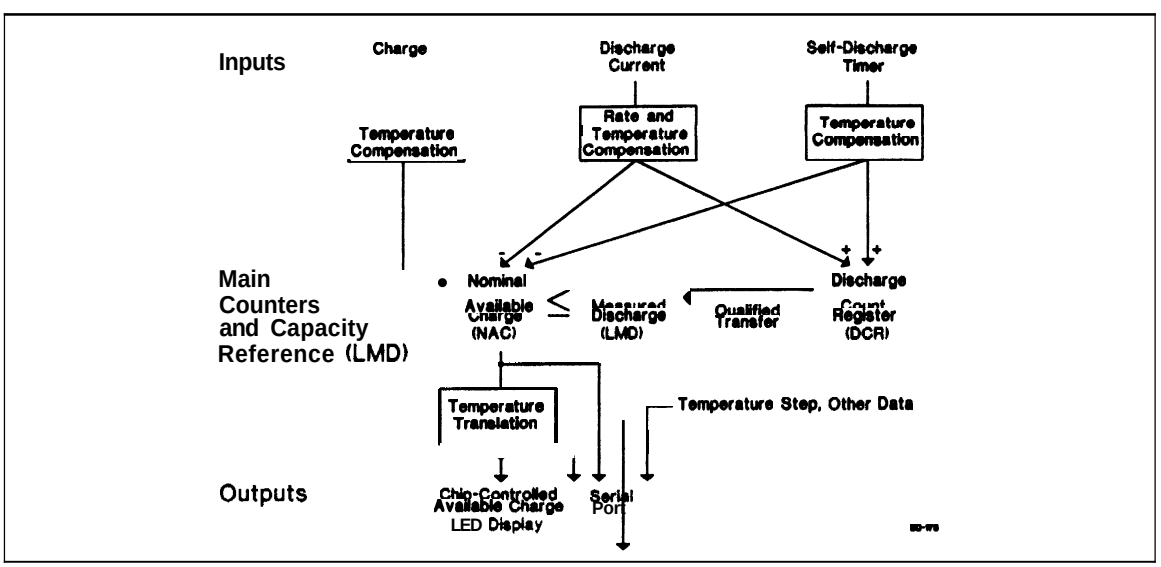


Figure 2. Operational Overview

Example: Selecting a PFC Value

Given:

Sense resistor = 0.1Ω
Number of cells = 6
Capacity = 2200mAh, NiCd battery
Current range = 50mA to 2A
Absolute display mode
Serial port only
Self-discharge = C/64
Voltage drop over sense resistor = 5mV to 200mV

Therefore:

2200mAh • 0.1Ω = 220mVh

Select:

PFC = 33792 counts or 211mVh
$PROG_1$ = float
$PROG_2$ = float
$PROG_3$ = float
$PROG_4$ = low
$PROG_5$ = float
$PROG_6$ = float

The initial full battery capacity is 211mVh (2110mAh) until the bq2010 "learns" a new capacity with a qualified discharge from full to EDV1.

Table 1. bq2010 Programming

Pin Connection	$PROG_5$ Self-Discharge Rate	$PROG_6$ Display Mode	$\overline{DISP}$ Display State
H	Disabled	Absolute NAC = PFC on reset	LED disabled
Z	NAC/64	Absolute NAC = 0 on reset	LED-enabled on discharge or charge when equivalent $\lvert V_{SRO} \rvert \geq 4mV$
L	NAC/47	Relative NAC = 0 on reset	LED on

Note: $PROG_5$ and $PROG_6$ states are independent.

Table 2. bq2010 Programmed Full Count mVh Selections

$PROG_x$		Programmed Full Count (PFC)	$PROG_4$ = L			$PROG_4$ = Z			Units
1	2		PROG3 = H	PROG3 = Z	PROG3 = L	PROG3 = H	PROG3 = Z	PROG3 = L	
-	-	-	Scale = 1/80	Scale = 1/160	Scale = 1/320	Scale = 1/640	Scale = 1/1280	Scale = 1/2560	mVh/ count
H	H	49152	614	307	154	76.8	38.4	19.2	mVh
H	Z	45056	563	282	141	70.4	35.2	17.6	mVh
H	L	40960	512	256	128	64.0	32.0	16.0	mVh
Z	H	36864	461	230	115	57.6	28.8	14.4	mVh
Z	Z	33792	422	211	106	53.0	26.4	13.2	mVh
Z	L	30720	384	192	96.0	48.0	24.0	12.0	mVh
L	H	27648	346	173	86.4	43.2	21.6	10.8	mVh
L	Z	25600	320	160	80.0	40.0	20.0	10.0	mVh
L	L	22528	282	141	70.4	35.2	17.6	8.8	mVh
VSR equivalent to 2 counts/sec. (nom.)			90	45	22.5	11.25	5.6	2.8	mV

3. Nominal Available Charge **(NAC):**

   NAC counts up during charge to a maximum value of LMD and down during discharge and **self-discharge** to **0.** NAC is reset to **0** on initialization ($PROG_8$ = Z or low) and on the first valid **charge** following discharge to **EDV1.** NAC is set to PFC on initialization if $PROG_8$ = high. To prevent overstatement of charge during **periods** of overcharge, NAC stops incrementing when NAC = LMD.

4. Discharge **Count** Register (DCR):

   The DCR counts up during discharge independent of NAC and could continue increasing **after** NAC has decremented to **0.** Prior to NAC = **0** (empty battery), both discharge and self-discharge increment the DCR. After NAC = **0,** only discharge increments the DCR The DCR resets to **0** when NAC = LMD. The DCR does not roll over but stops counting when it reaches FFFFh.

   The DCR value becomea the new LMD value on the **first** charge after a valid discharge to V_{EDV1} if:

   No valid charge initiations (charges greater than 256 NAC counts, where $V_{SRO} > V_{SRQ}$) occurred during the period between NAC = LMD and EDV1 detected.

   The self-discharge count is not more than 4096 counts (8% to 18% of PFC, specific percentage threshold determined by PFC).

   The temperature is ≥ **0°C** when the EDV1 level is reached during discharge.

   The valid discharge flag **(VDQ)** indicates whether the present **discharge** is valid for LMD update.

Charge Counting

Charge activity is detected based on a positive voltage on the V_{SR} input. If charge activity is **detected,** the bq2010 increments NAC at a rate proportional to V_{SRO} and, if enabled, activates an LED display if the **rate** is equivalent to V_{SRO} > 4mV. Charge actions increment the NAC after **compensation** for charge rate and temperature.

The **bq2010** determines charge activity **sustained** at a continuous rate equivalent to $V_{SRO} > V_{SRQ}$. A valid charge equates to sustained charge activity greater than 256 NAC counts. **Once** a valid charge is detected, charge counting continues until V_{SRO} (V_{SR} + V_{OS}) **falls** below V_{SRQ}. V_{SRQ} is a programmable threshold as described in the Digital Magnitude **Filter** section. The default value for V_{SRQ} is **375µV.**

Discharge Counting

All **discharge counts** where $V_{SRO} < V_{SRD}$ **cause** the NAC register to decrement and the DCR to increment. Exceeding the **fast** discharge threshold **(FDQ)** if the rate is equivalent to $V_{SRO} < -4mV$ activates the display, if enabled. The display becomes inactive after V_{SRO} rises above -4mV. V_{SRD} is a **programmable** threshold as described in the Digital Magnitude Filter section. The default value for V_{SRD} is -300µV.

Self-Discharge Estimation

The **bq2010** continuously **decrements** NAC **and** increment8 DCR for **self-discharge based** on time and temperature. **The self-discharge** count rate is **programmed** to be a nominal **1/64** • NAC, **1/47** • NAC per day, or disabled **as selected** by **$PROG_5$.** This is **the** rate for a battery **whose** temperature **is** between **20°–30°C. The** NAC register cannot be decremented **below** 0.

Count Compensations

The **bq2010** determines fast charge when the NAC updates at a rate of 2 2 **counts/sec.** Charge and discharge activity is **compensated** for temperature and **charge/discharge** rate before updating the NAC **and/or DCR. Self-discharge** estimation **is compensated** for temperature before updating the NAC **or** DCR.

Charge Compensation

Two charge **efficiency** compensation factors **are** used for trickle **charge** and **fast** charge. Fast charge is **defined** as a rate of **charge resulting** in ≥ 2 **NAC counts/sec (≥ 0.15C** to **0.32C** depending on PFC **selections;** see Table 2). The compensation default8 **to** the fast charge factor until the actual **charge** rate **is** determined.

Temperature **adapts** the charge rate **compensation** factors over three ranges between nominal, warm, and hot temperatures. The compensation factors are shown below.

Charge Temperature	Trickle Charge Compensation	Fast Charge Compensation
<30°C	**0.80**	**0.96**
30–40°C	0.75	0.90
> 40°C	**0.65**	0.80

Discharge Compensation

Corrections for the rate of discharge are made by adjusting an internal discharge compensation factor. The discharge compensation factor is based on the **dynamically measured** V_{SR}.

The compensation factors during discharge are:

Approximate V_{SR} Threshold	Discharge Compensation Factor	Efficiency
V_{SR} > -150 mV	1.00	100%
V_{SR} < -150 mV	1.05	95%

Temperature compensation during discharge also takes place. At lower temperatures, the compensation factor increases by 0.05 for each 10°C temperature step below 10°C.

Comp. factor = 1.0 + (0.05 • N)

Where N = Number of 10°C steps below 10°C and -150mV < V_{SR} < 0.

For example:

T > 10°C: Nominal compensation, N = 0

0°C < T < 10°C: N = 1 (i.e., 1.0 becomes 1.05)

-10°C < T < 0°C: N = 2 (i.e., 1.0 becomes 1.10)

-20°C < T < -10°C: N = 3 (i.e., 1.0 becomes 1.15)

-20°C < T < -30°C: N = 4 (i.e., 1.0 becomes 1.20)

Self-Discharge Compensation

The self-discharge compensation is programmed for a nominal rate of 1/64 • NAC, 1/47 • NAC per day, or disabled. This is the rate for a battery within the 20–30°C temperature range (TMPGG = 6x). This rate varies across 8 ranges from <10°C to >70°C, doubling with each higher temperature step (10°C). See Table 3.

Table 3. Self-Discharge Compensation

Temperature Range	Typical Rate	
	$PROG_5$ = 7	$PROG_5$ = L
< 10°C	NAC/256	NAC/188
10–20°C	NAC/128	NAC/94
20–30°C	NAC/64	NAC/47
30–40°C	NAC/32	NAC/23.5
40–50°C	NAC/16	NAC/11.8
50–60°C	NAC/8	NAC/5.88
60–70°C	NAC/4	NAC/2.94
> 70°C	NAC/2	NAC/1.47

Digital Magnitude Filter

The bq2010 has a programmable digital filter to eliminate charge and discharge counting below a set threshold. The default setting is -0.30mV for V_{SRD} and +0.38mV for V_{SRQ}. The proper digital filter setting can be calculated using the following equation. Table 4 shows typical digital filter settings.

$$V_{SRD}\ (mV) = -45 / DMF$$

$$V_{SRQ}\ (mV) = -1.25 \bullet V_{SRD}$$

Table 4. Typical Digital Filter Settings

DMF	DMF Hex.	V_{SRD} (mV)	V_{SRQ} (mV)
75	4B	-0.60	0.75
100	64	-0.45	0.56
150 (default)	96	-0.30	0.38
175	AF	-0.26	0.32
200	C8	-0.23	0.28

Error Summary

Capacity Inaccurate

The LMD is susceptible to error on initialization or if no updates occur. On initialization, the LMD value includes the error between the programmed full capacity and the actual capacity. This error is present until a valid discharge occurs and LMD is updated (see the DCR description on page 7). The other cause of LMD error is battery wear-out. As the battery ages, the measured capacity must be adjusted to account for changes in actual battery capacity.

A Capacity Inaccurate counter (CPI) is maintained and incremented each time a valid charge occurs (qualified by NAC; see the CPI register description) and is reset whenever LMD is updated from the DCR. The counter does not wrap around but stops counting at 255. The capacity inaccurate flag (CI) is set if LMD has not been updated following 64 valid charges.

Current-Sensing Error

Table 5 illustrates the current-sensing error as a function of V_{SR}. A digital filter eliminates charge and discharge counts to the NAC register when V_{SRQ} (V_{SR} + V_{OS}) is between V_{SRQ} and V_{SRD}.

Communicating With the bq2010

The bq2010 includes a simple single-pin (DQ plus return) serial data interface. A host processor uses the interface to access various bq2010 registers. Battery characteristics may be easily monitored by adding a single contact to the battery pack. The open-drain DQ pin on the bq2010 should be pulled up by the host system or may be left floating if the serial interface is not used.

Table 5. bq2010 Current-Sensing Errors

Symbol	Parameter	Typical	Maximum	Units	Notes
V_{OS}	Offset referred to V_{SR}	± 50	± 150	µV	$\overline{DISP}$ = Vcc.
INL	Integrated non-linearity error	± 2	± 4	%	Add 0.1% per °C above or below 25°C and 1% per volt above or below 4.25V.
INR	Integrated non-repeatability error	± 1	± 2	%	Measurement repeatability given similar operating conditions.

The interface uses a command-based protocol, where the host processor sends a command byte to the bq2010. The command directs the bq2010 either to store the next eight bits of data received to a register specified by the command byte or to output the eight bits of data specified by the command byte.

The communication protocol is asynchronous return-to-one. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 333 bits/sec. The least-significant bit of a command or data byte is transmitted first. The protocol is simple enough that it can be implemented by most host processors using either polled or interrupt processing. Data input from the bq2010 may be sampled using the pulse-width capture timers available on some microcontrollers.

Communication is normally initiated by the host processor sending a BREAK command to the bq2010. A BREAK is detected when the DQ pin is driven to a logic-low state for a time, t_B or greater. The DQ pin should then be returned to its normal ready-high logic state for a time, t_{BR}. The bq2010 is now ready to receive a command from the host processor.

The return-bone data bit frame consists of three distinct sections. The first section is used to start the transmission by either the host or the bq2010 taking the DQ pin to a logic-low state for a period, $t_{STRH,B}$. The next section is the actual data transmission, where the data should be valid by a period, t_{DSU}, after the negative edge used to start communication The data should be held for a period, t_{DV}, to allow the host or bq2010 to sample the data bit.

The final section is used to stop the transmission by returning the DQ pin to a logic-high state by at least a period, t_{SSU}, after the negative edge used to start communication. The final logic-high state should be held until a period, t_{SV}, to allow time to ensure that the bit transmission was stopped properly. The timings for data and break communication are given in the serial communication timing specification and illustration sections.

Communication with the bq2010 is always performed with the least-significant bit being transmitted first. Figure 3 shows an example of a communication sequence to read the bq2010 NAC register.

bq2010 Registers

The bq2010 command and status registers are listed in Table 6 and described below.

Command Register (CMDR)

The write-only CMDR register is accessed when eight valid command bits have been received by the bq2010. The CMDR register contains two fields:

- W/$\overline{R}$ bit
- Command address

The W/$\overline{R}$ bit of the command register is used to select whether the received command is for a read or a write function.

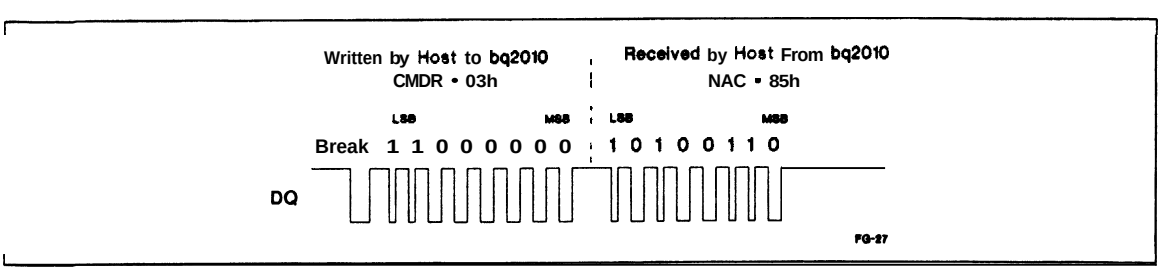


Figure 3. Typical Communication With the bq2010

Table 6. bq2010 Command and Status Registers

Symbol	Register Name	Loc. (hex)	Read/ Write	Control Field							
				7(MSB)	6	5	4	3	2	1	0(LSB)
CMDR	Command register	00h	Write	W/$\overline{R}$	AD6	AD5	AD4	AD3	AD2	AD1	AD0
FLGS1	Primary status flags register	Olh	Read	CHGS	BRP	BRM	CI	VDQ	n/u	EDV1	EDVF
TMPGG	Temperature and gas gauge register	02h	Read	TMP3	TMP2	TMP1	TMP0	GG3	GG2	GG1	GG0
NACH	Nominal available charge high byte register	03h	R/W	NACH7	NACH6	NACH5	NACH4	NACH3	NACH2	NACH1	NACHO
NACL	Nominal available charge low byte register	17h	Read	NACL7	NACL6	NACL5	NACL4	NACL3	NACL2	NACL1	NACL0
BATID	Battery identification register	04h	R/W	BATID7	BATID6	BATID5	BATID4	BATID3	BATID2	BATID1	BATID0
LMD	Last measured discharge register	05h	R/W	LMD7	LMD6	LMD5	LMD4	LMD3	LMD2	LMD1	LMD0
FLGS2	Secondary status flags register	06h	Read	CR	DR2	DR1	DRO	n/u	n/u	n/u	OVLD
PPD	Program pin pull-down register	07h	Read	n/u	n/u	PPD6	PPD5	PPD4	PPD3	PPD2	PPD1
PPU	Program pin pull-up register	08h	Read		n/u	PPU6	PPU5	PPU4	PPU3	PPU2	PPU1
CPI	Capacity inaccurate count register	09h	Read	CP17	CPI6	CP15	CP14	CP13	CP12	CPI1	CPIO
DMF	Digital magnitude filter register	0ah	R/W	DMF7	DMF6	DMF5	DMF4	DMF3	DMF2	DMF1	DMF0
RST	Reset register	39h	Write	RST	0	0	0	0	0	0	0

Note: n/u = not used

The W/$\overline{R}$ values are:

CMDR Bits							
7	6	5	4	3	2	1	0
W/$\overline{R}$	-	-	-	-	-	-	-

Where W/$\overline{R}$ is:

0 The bq2010 outputs the requested register contents specified by the address portion of CMDR.

1 The following eight bits should be written to the register specified by the address portion of CMDR.

The lower seven-bit field of CMDR contains the address portion of the register to be accessed. Attempts to write to invalid addresses are ignored.

CMDR Bits							
7	6	5	4	3	2	1	0
-	AD6	AD5	AD4	AD3	AD2	AD1	AD0 (LSB)

Primary Status Flags Register (FLGS1)

The read-only FLGSl register (address=01h) contains the primary bq2010 flags.

The charge *status* flag (CHGS) is asserted when a valid charge rate is detected. Charge rate is deemed valid when $V_{SRO} > V_{SRQ}$. A V_{SRO} of less than V_{SRQ} or discharge activity clears CHGS.

The CHGS values are:

FLGSl Bits							
7	6	5	4	3	2	1	0
CHGS	-	-	-	-	-	-	-

Where CHGS is:

0 Either discharge activity detected or $V_{SRO} < V_{SRQ}$

1 $V_{SRO} > V_{SRQ}$

The *battery* replaced flag (BRP) is asserted whenever the potential on the SB pin (relative to V_{SS}), V_{SB}, falls from above the maximum cell voltage, MCV (2.25V), or rises above 0.1V. The BRP flag is also set when the bq2010 is reset (see the RST register description). BRP is reset when either a valid charge action increments NAC to be equal to LMD, or a valid charge action is detected after the EDVl flag is asserted. BRP = 1 signifies that the device has been reset.

The BRP values are:

FLGSl Bits							
7	6	5	4	3	2	1	0
-	BRP	-				-	-

Where BRP is:

0 Battery is charged until NAC = LMD or discharged until the EDV1 flag is asserted

1 V_{SB} dropping from above MCV, V_{SB} rising from below 0.1V, or a serial part initiated reset has occurred

The *battery removed* flag (BRM) is asserted whenever the potential on the SB pin (relative to V_{SS}) rises above MCV or falls below 0.1V. The BRM flag is asserted until the condition causing BRM is removed.

The BRM values are:

FLGSl Bits							
7	6	5	4	3	2	1	0
	-	BRM	-				

Where BRM is:

0 $0.1V < V_{SB} < 2.25V$

1 $0.1 V > V_{SB}$ or $V_{SB} > 2.25V$

The *capacity inaccurate* flag (CI) is used to warn the user that the battery has been charged a substantial number of times since LMD has been updated. The CI flag is asserted on the 64th charge after the last LMD update or when the bq2010 is reset. The flag is cleared after an LMD update.

The CI values are:

FLGSl Bits							
7	6				2	1	0
-	-	-	CI	-	-	-	-

Where CI is:

0 When LMD is updated with a valid full discharge

1 After the 64th valid charge action with no LMD updates or the bq2010 is reset

The valid *discharge* flag (VDQ) is asserted when the bq2010 is discharged from NAC=LMD. The flag remains set until either LMD is updated or one of three actions that can clear VDQ occurs:

- The self-discharge count register (SDCR) has exceeded the maximum acceptable value (4096 counts) for an LMD update.
- A valid charge action sustained at $V_{SRO} > V_{SRQ}$ for at least 256 NAC counts.
- The EDV1 flag was set at a temperature below 0°C

The VDQ values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	VDQ	-	-	-

Where VDQ is:

0 SDCR ≥ 4096, subsequent valid charge action detected, or EDV1 is asserted with the temperature less than 0°C

1 On first discharge after NAC = LMD

The firet *end-of-discharge warning* flag (EDV1) warns the user that the battery is almost empty. The first segment pin, SEG_1, is modulated at a 4Hz rate if the display is enabled once EDV1 is asserted, which should warn the user that loss of battery power is imminent. The EDV1 flag is latched until a valid charge has been detected.

The EDV1 values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	EDV1	-

Where EDV1 is:

0 Valid charge action detected, $V_{SB} \geq 1.05V$

1 $V_{SB} < 1.05V$ providing that OVLD=0 (see FLGS2 register description)

The final *end-of-discharge warning* flag (EDVF) is used to warn that battery power is at a failure condition. All segment drivers are turned off. The EDVF flag is latched until a valid charge has been detected. The EMPTY pin is also forced to a high-impedance state on assertion of EDVF. The host system may pull EMPTY high, which may be used to disable circuitry to prevent deep-discharge of the battery.

The EDVF values are:

FLGSI Bits							
7	6	5					
-	-	-				-	EDVF

Where EDVF is:

0 Valid charge action detected, $V_{SB} \geq 0.95V$

1 $V_{SB} < 0.95V$ providing that OVLD=0 (see FLGS2 regieter description)

Temperature and Gas Gauge Register (TMPGG)

The read-only TMPGG register (address=02h) contains two data fields. The first field contains the battery temperature. The second field contains the available charge from the battery.

TMPGG Temperature Bits							
7	6	5	4	3	2	1	0
TMP3	TMP2	TMP1	TMP0	-	-	-	

The bq2010 contains an internal temperature sensor. The temperature is used to set charge and discharge efficiency factors as well as to adjust the self-discharge coefficient.

The temperature register contents may be translated as shown below.

TMP3	TMP2	TMP1	TMPO	Temperature
0	0	0	0	T < -30°C
0	0	0	1	-30°C < T < -20°C
0	0	1	0	-20°C < T < -10°C
0	0	1	1	-10°C < T < 0°C
0	1	0	0	0°C < T < 10°C
0	1	0	1	10°C < T < 20°C
0	1	1	0	20°C < T < 30°C
0	1	1	1	30°C < T < 40°C
1	0	0	0	40°C < T < 50°C
1	0	0	1	50°C < T < 60°C
1	0	1	0	60°C < T < 70°C
1	0	1	1	70°C < T < 80°C
1	1	0	0	T > 80°C

The bq2010 calculates the available charge as a function of NAC, temperature, and a full reference, either LMD or PFC. The results of the calculation are available via the display port or the gas gauge field of the TMPGG register. The register is used to give available capacity in 1/16 increments from 0 to 15/16.

TMPGG Gas Gauge Bits							
7	6	5	4	3	2	1	0
-	-	-	-	GG3	GG2	GG1	GG0

The gas gauge display and the gas gauge portion of the TMPGG register are adjusted for cold temperature dependencies. A piece-wise correction is performed as follows:

Temperature	Available Capacity Calculation
> 0°C	NAC / "Full Reference"
-20°C < T < 0°C	0.75 • NAC / "Full Reference"
< -20°C	0.5 • NAC / "Full Reference"

The adjustment between > 0°C and -20°C < T < 0°C has a 10°C hysteresis.

Nominal Available Charge Registers (NACH/NACL)

The read/write NACH high-byte register (address=03h) and the read-only NACL low-byte register (address=17h) are the main gas gauging register for the bq2010. The NAC registers are incremented during charge actions and decremented during discharge and self-discharge actions. The correction factors for charge/discharge efficiency are applied automatically to NAC.

On reset, if $PROG_6$ = Z or low, NACH and NACL are cleared to 0; if $PROG_6$ = high, NACH = PFC and NACL = 0. When the bq2010 detects a valid charge, NACL resets to 0. *Writing to the NAC registers affects the available charge counts and, therefore, affects the bq2010 gas gauge operation. Do not write the NAC registers to a value greater than LMD.*

Battery Identification Register (BATID)

The read/write BATID register (address=04h) is available for use by the system to determine the type of battery pack. The BATID contents are retained as long as V_{CC} is greater than 2V. The contents of BATID have no effect on the operation of the bq2010. There is no default setting for this register.

Last Measured Discharge Register (LMD)

LMD is a read/write register (address=05h) that the bq2010 uses as a measured full reference. The bq2010 adjusts LMD based on the measured discharge capacity of the battery from full to empty. In this way the bq2010 updates the capacity of the battery. LMD is set to PFC during a bq2010 reset.

Secondary Status Flags Register (FLGS2)

The read-only FLGS2 register (address=06h) contains the secondary bq2010 flags.

The ***charge rate*** flag (CR) is used to denote the fast charge regime. Fast charge is assumed whenever a charge action is initiated. The CR flag remains asserted if the charge rate does not fall below 2 counts/sec.

The CR values are:

FLGS2 Bits							
7	6	5	4	3	2	1	0
CR	-	-	-	-	-	-	-

Where CR is:

0 When charge rate falls below 2 counts/sec

1 When charge rate is above 2 counts/sec

The fast charge regime efficiency factors are used when CR = 1. When CR = 0, the trickle charge efficiency factors are used. The time to change CR varies due to the user-selectable count rates.

The ***discharge rate*** flags, DR2–0, are bits 6–4.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	DR2	DR1	DR0	-	-	-	

They are used to determine the current discharge regime as follows:

DR2	DR1	DR0	V_{SR} (V)
0	0	0	V_{SR} > -150mV
0	0	1	V_{SR} < -150mV

The ***overload*** flag (OVLD) is asserted when a discharge overload is detected, V_{SR} < -250mV. OVLD remains asserted as long as the condition persists and is cleared 0.5 seconds after V_{SR} > -250mV. The overload condition is used to stop sampling of the battery terminal characteristics for end-of-discharge determination. Sampling is re-enabled 0.5 secs after the overload condition is removed.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	OVLD

DR2–0 and OVLD are set based on the measurement of the voltage at the SR pin relative to Vss. The rate at which this measurement is made varies with device activity.

Program Pin Pull-Down Register (PPD)

The read-only PPD register (address=07h) contains some of the programming pin information for the bq2010. The segment drivers, SEG_{1-6}, have a corresponding PPD register location, PPD_{1-6}. A given location is eat if a pull-down resistor has been detected on its corresponding segment driver. For example, if SEG_1 and SEG_4 have pull-down resistors, the contents of PPD are xx001001.

PPD/PPU Bits							
7	6	5	4	3	2	1	0
	-	PPU_6	PPU_5	PPU_4	PPU_3	PPU_2	PPU_1
	-	PPD_6	PPD_5	PPD_4	PPD_3	PPD_2	PPD_1

Program Pin Pull-Up Register (PPU)

The read-only PPU register (address=08h) contains the rest of the programming pin information for the bq2010. The segment drivers, SEG_{1-6}, have a corresponding PPU register location, PPU_{1-6}. A given location is set if a pull-up resistor has been detected on its corresponding segment driver. For example, if SEG_3 and SEG_6 have pull-up resistors, the contents of PPU are xx100100.

Capacity Inaccurate Count Register (CPI)

The read-only CPI register (address=09h) is used to indicate the number of times a battery has been charged without an LMD update. Because the capacity of a rechargeable battery varies with age and operating conditions, the bq2010 adapts to the changing capacity over time. A complete discharge from full (NAC=LMD) to empty (EDV1=1) is required to perform an LMD update assuming there have been no intervening valid charges, the temperature is greater than or equal to 0°C, and the self-discharge counter is leas than 4096 counts.

The CPI register is incremented every time a valid charge is detected. When NAC > 0.94 • LMD, however, the CPI register increments on the f i i valid charge; CPI does not increment again for a valid charge until NAC < 0.94 • LMD. This prevents continuous trickle charging from incrementing CPI if self-discharge decrements NAC. The CPI register increments to 255 without rolling over. When the contents of CPI are incremented to 64, the capacity inaccurate flag, CI, is asserted in the FLGS1 register. The CPI register is reset whenever an update of the LMD register is performed, and the CI flag is also cleared.

Digital Magnitude Filter (DMF)

The read-write DMF register (address = 0ah) provides the system with a means to change the default settings of the digital magnitude filter. By writing different values into this register, the limits of V_{SRD} and V_{SRQ} can be adjusted.

Note: Care should be taken when writing to this register. A V_{SRD} and V_{SRQ} below the specified V_{OS} may adversely affect the accuracy of the bq2010. Refer to Table 4 for recommended settings for the DMF register.

Reset Register (RST)

The reset register (address=39h) provides the means to perform a software-controlled reset of the device. By writing the RST register contents from 00h to 80h, a bq2010 reset is performed. Setting any bit other than the most-significant bit of the RST register *is not allowed,* and results in improper opemtwn of the *bq2010.*

Resetting the bq2010 sets the following:

- LMD = PFC

  CPI, VDQ, NACH, and NACL = 0
- CI and BRP = 1

Note: NACH = PFC when $PROG_6$ = H. Self-discharge is disabled when $PROG_5$ = H

Display

The bq2010 can directly display capacity information using low-power LEDs. If LEDs are used, the program pins should be resistively tied to V_{CC} or Vss for a program high or program low, respectively.

The bq2010 displays the battery charge state in either absolute or relative mode. In relative mode, the battery charge is represented as a percentage of the LMD. Each LED segment represents 20% of the LMD. The sixth segment, SEG_6, is not used.

In absolute mode, each segment represents a fixed amount of charge, based on the initial PFC. In absolute mode, each segment represents 20% of the PFC, with SEG_6 representing "overfull" (charge above the PFC). As the battery wears out over time, it is possible for the LMD to be below the initial PFC. In this case, all of the LEDs may not turn on in absolute mode, representing the reduction in the actual battery capacity.

The capacity display is also adjusted for the present battery temperature. The temperature adjustment reflects the available capacity at a given temperature but does not affect the NAC register. The temperature adjustments are detailed in the TMPGG register description.

When $\overline{DISP}$ is tied to V_{CC}, the SEG_{1-6} outputs are inactive. When $\overline{DISP}$ is left floating, the display becomes active whenever the NAC registers are counting at a rate equivalent to $|V_{SRO}| \geq 4mV$. When pulled low, the segment outputs become active immediately. A capacitor tied to $\overline{DISP}$ allows the display to remain active for a short period of time after activation by a push-button switch.

The segment outputs are modulated as two banks of three, with segments 1, 3, and 5 alternating with segments 2, 4, and 6. The segment outputs are modulated at approximately 100Hz with each segment bank active for 30% of the period.

SEG_1 blinks at a 4Hz rate whenever V_{SB} has been detected to be below V_{EDV1} (EDV1 = 1), indicating a low-battery condition. V_{SB} below V_{EDVF} (EDVF = 1) disables the display output.

Microregulator

The bq2010 can operate directly from 3 or 4 cells. To facilitate the power supply requirements of the bq2010, an REF output is provided to regulate an external low-threshold n-FET. A micropower source for the bq2010 can be inexpensively built using the FET and an external resistor; see Figure 1.

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to V_{SS}	-0.3	+7.0	V	
All other pins	Relative to Vss	-0.3	+7.0	V	
REF	Relative to Vss	-0.3	+8.5	V	Current limited by R1 (see Figure 1)
V_{SR}	Relative to V_{SS}	-0.3	+7.0	V	Minimum 100Ω series resistor should be used to protect SR in case of a shorted battery (see the bq2010 application note for details).
T_{OPR}	Operating temperature	0	+70	°C	Commercial
		-40	+85	°C	Industrial

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation

DC Voltage Thresholds ($T_A = T_{OPR}$; V = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDVF}	Final empty warning	0.93	0.95	0.97	V	SB
V_{EDV1}	First empty warning	1.03	1.05	1.07	V	SB
V_{SR1}	Discharge compensation threshold	-120	-150	-180	mV	SR, $V_{SR} + V_{OS}$
V_{SRO}	SR sense range	-300	-	+2000	mV	SR, $V_{SR} + V_{OS}$
V_{SRQ}	Valid charge	375	-	-	µV	$V_{SR} + V_{OS}$ (see note)
V_{SRD}	Valid discharge			-300	µV	$V_{SR} + V_{OS}$ (see note)
V_{MCV}	Maximum single-cell voltage	2.20	2.25	2.30	V	SB
V_{BR}	Battery removed/replaced		0.1	0.25	V	SB pulled low
		2.20	2.25	2.30	V	SB pulled high

Note: Default value; value set in DMF register. V_{OS} is affected by PC board layout. Proper layout guidelines should be followed for optimal performance. See "Layout Considerations."

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	3.0	4.25	6.5	V	V_{CC} excursion from < 2.0V to ≥ 3.0V initializes the unit.
V_{REF}	Reference at 25°C	5.7	6.0	6.3	V	I_{REF} = 5µA
	'Reference at -40°C to +85°C	4.5		7.6	V	I_{REF} = 5µA
R_{REF}	Reference input impedance	2.0	5.0		MΩ	V_{REF} = 3V
I_{CC}	Normal operation		90	136	µA	V_{CC} = 3.0V, DQ = 0
			120	180	µA	V_{CC} = 4.25V, DQ = 0
			170	250	µA	Vcc = 6.5V, DQ = 0
V_{SB}	Battery input	0		V_{CC}	V	
R_{SBmax}	SB input impedance	10			MR	0 < V_{SB} < V_{CC}
I_{DISP}	$\overline{DISP}$ input leakage			5	µA	V_{DISP} = V_{SS}
I_{LCOM}	LCOM input leakage	-0.2		0.2	µA	$\overline{DISP}$ = V_{CC}
R_{DQ}	Internal pulldown	500			KΩ	
V_{SR}	Sense resistor input	-0.3		2.0	V	V_{SR} < V_{SS} = discharge; V_{SR} > V_{SS} = charge
R_{SR}	SR input impedance	10			MΩ	-200mV < V_{SR} < Vcc
V_{IH}	Logic input high	V_{CC} - 0.2	-		V	$PROG_1$–$PROG_6$
V_{IL}	Logic input low		-	V_{SS} + 0.2	V	$PROG_1$–$PROG_6$
V_{IZ}	Logic input Z	float		float	V	$PROG_1$–$PROG_6$
V_{OLSL}	SEG_X output low, low V_{CC}		0.1		V	V_{CC} = 3V, I_{OLS} ≤ 1.75mA SEG_1–SEG_6
V_{OLSH}	SEG_X output low, high Vcc		0.4		V	V_{CC} = 6.5V, I_{OLS} ≤ 11.0mA SEG_1–SEG_6
V_{OHLCL}	LCOM output high, low Vcc	Vcc - 0.3	-		V	V_{CC} = 3V, I_{OHLCOM} = -5.25mA
V_{OHLCH}	LCOM output high, high Vcc	Vcc - 0.6	-		V	V_{CC} = 6.5V, I_{OHLCOM} = -33.0mA
I_{IH}	$PROG_{1-6}$ input high current		1.2		µA	V_{PROG} = V_{CC}/2
I_{IL}	$PROG_{1-6}$ input low current		1.2		µA	V_{PROG} = V_{CC}/2
I_{OHLCOM}	LCOM source current	-33			mA	At V_{OHLCH} = Vcc - 0.6V
I_{OLS}	SEG_X sink current			11.0	mA	At V_{OLSH} = 0.4V
I_{OL}	Open-drain sink current			5.0	mA	At V_{OL} = V_{SS} + 0.3V DQ, EMPTY
V_{OL}	Open-drain output low			0.5	V	I_{OL} 5 5mA, DQ, EMPTY
V_{IHDQ}	DQ input high	2.5			V	DQ
V_{ILDQ}	DQ input low			0.8	V	DQ
R_{PROG}	Soft pull-up or pull-down resistor value (for programming)			200	KΩ	$PROG_1$–$PROG_6$
R_{FLOAT}	Float state external impedance	-	5	-	MΩ	$PROG_1$–$PROG_6$

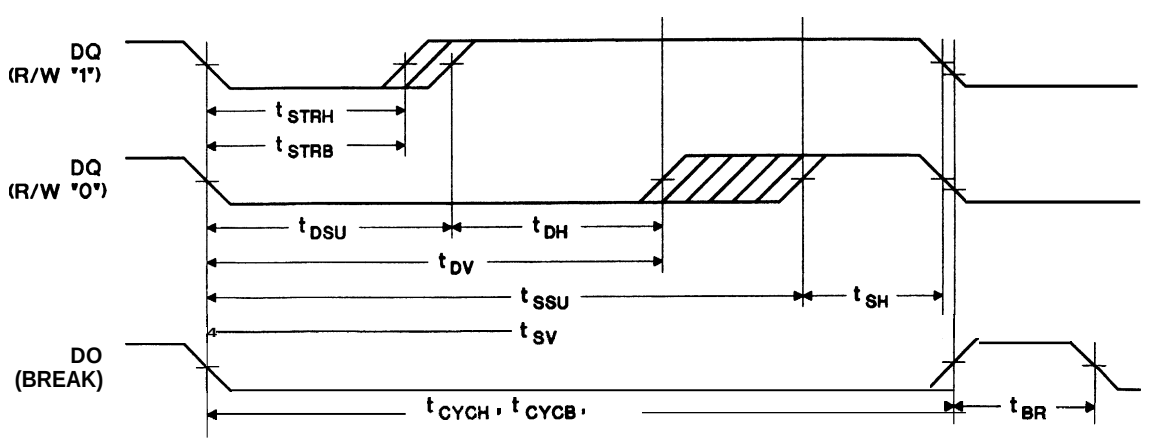
Note: All voltages relative to V_{SS}.

Serial Communication Timing Specification ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYCH}	Cycle time, host to bq2010	3			ms	See note
t_{CYCB}	Cycle time, bq2010 to host	3		6	me	
t_{STRH}	Start hold, host to bq2010	5			ns	
t_{STRB}	Start hold, bq2010 to host	500			µs	
t_{DSU}	Data setup			750	µs	
t_{DH}	Data hold	750			µs	
t_{DV}	Data valid	1.50			me	
tssu	Stop setup			2.26	me	
t_{SH}	Stop hold	700			µs	
t_{SV}	Stop valid	2.95			me	
t_B	Break	3			me	
t_{BR}	Break recovery	1			me	

Note: The open-drain DQ pin should be pulled to at least Vcc by the host system for proper DQ operation. DQ may be left floating if the serial interface is not used.

Serial Communication Timing Illustration



RC-34

Data Sheet Revision History

Chanae No.	Page No.	Description	Nature of Change
3	4	EDV monitoring	Was: EDV monitoring is disabled if $V_{SR} \leq$ -150mV; Is: EDV monitoring is disabled if $V_{SR} \leq$ -250mV
3	6	Table 1, $PROG_5$	Was: $PROG_5$ = H = Reserved; Is: $PROG_5$ = H = Disable self-discharge
3	7,8	Self-discharge	Add: or disabled as selected by $PROG_5$
3	11	Capacity inaccurate	Correction: CI is asserted on the 64th charge after the last LMD update or when the bq2010 is reset
3	13	Nominal available charge register	NACL stops counting when NACH reaches zero
3	13	Overload flag	Was: $V_{SR} <$ -150mV Is: $V_{SR} <$ -250mV

Note: Changes 1 and 2; please refer to the 1995 Data Book.
Change 3 = Apr. 1995 D changes from Mar. 1994 C.

Ordering Information

bq2010

Temperature Range:
blank = Commercial (0 to +70°C)
N = Industrial (-40 to +85°C)*

Package option:
SN = 16-pin narrow SOIC

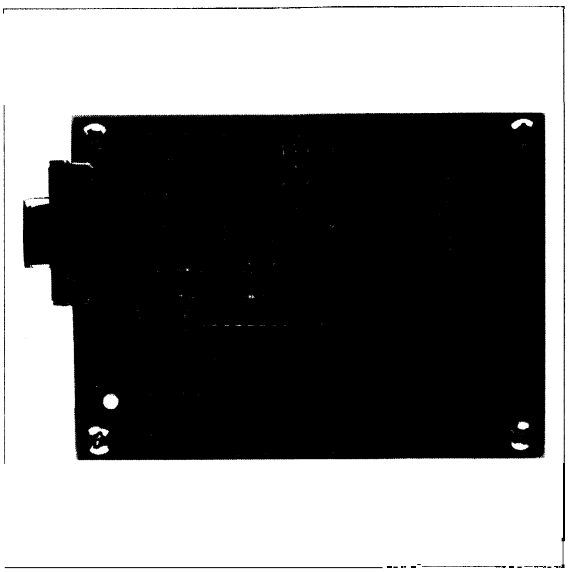
Device:
bq2010 Gas Gauge IC

* Contact factory for availability.

bq2010/H Evaluation System

Features

- bq2010/H Gas Gauge IC evaluation and development system
- ➤ RS-232 interface hardware for easy access to state-of-charge information via the serial port
- ➤ Alternative terminal block for direct connection to the serial port
- ➤ Battery state-of-charge monitoring for 5- to 10-cell (series) applications (2 user-selectable options for 3, 4, or greater than 10 cells)
- ➤ On-board regulator for greater than 4-cell applications
- ➤ State-of-charge information displayed on bank of 6 LEDs
- Nominal capacity jumper-configurable
- Cell chemistry jumper-configurable
- Display mode jumper-configurable



General Description

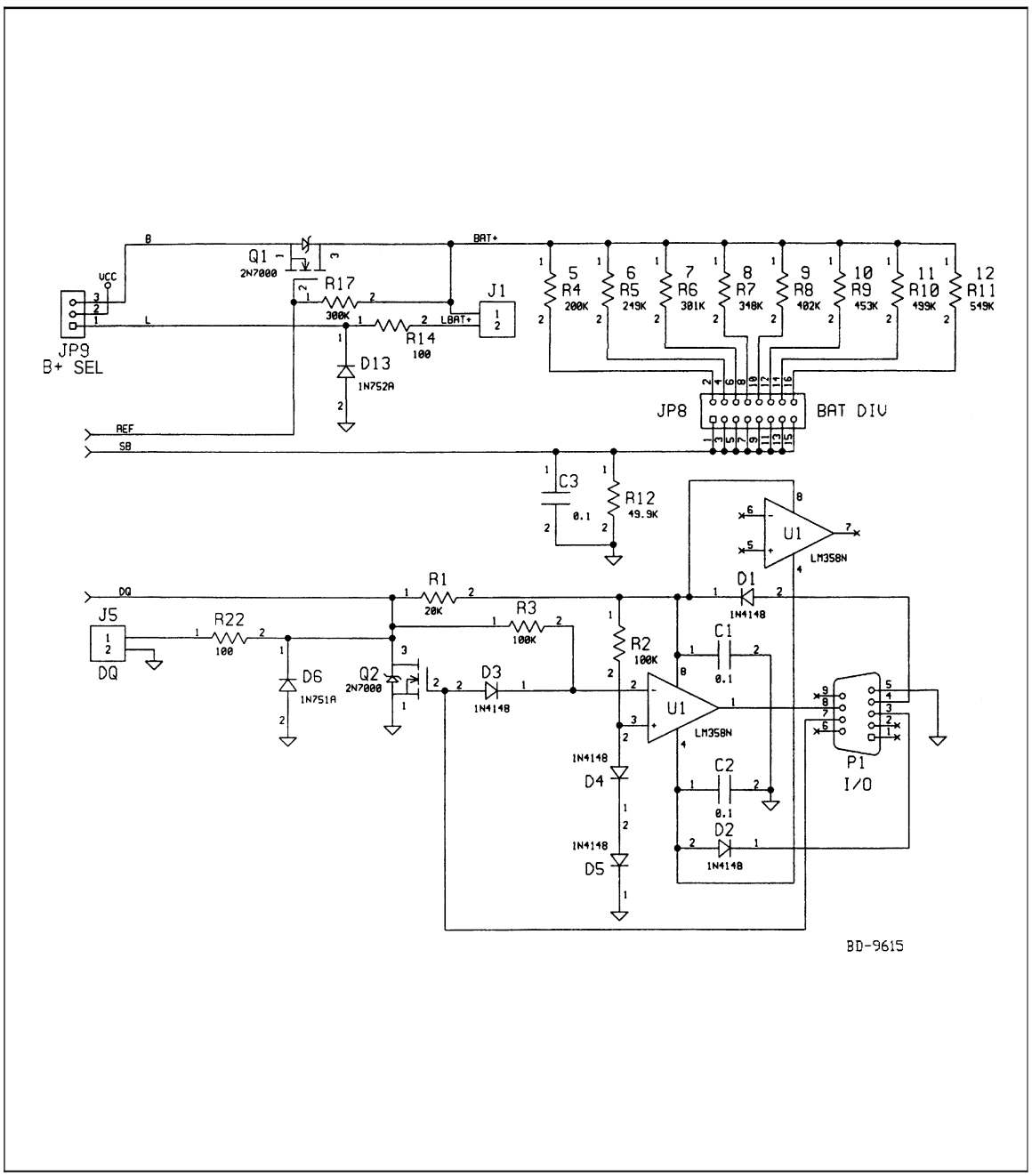
The EV2010/H Evaluation System provides a development and evaluation environment for the bq2010/H Gas Gauge IC. The EV2010/H incorporates a bq2010/H, a sense resistor, and all other hardware necessary to provide a capacity monitoring function for 3 to 12 series NiCd or NiMH cells.

Hardware for an RS-232 interface is included on the EV2010/H so that easy access to the state-of-charge information can be achieved via the serial port of the bq2010/H. Direct connection to the serial port of the bq2010/H is also made available for check-out of the final hardware/software implementation.

The menu-driven software provided with the EV2010/H displays charge/discharge activity and allows user interface to the bq2010/H from any standard DOS PC.

A full data sheet for this product is available on our web site (http://www.benchmarq.com),or you may contact the factory for one.

EV2010 Board Schematic



BENCHMARQ

Using the bq2010

A Tutorial for Gas Gauging

Introduction

This tutorial introduces the bq2010 Gas Gauge IC (secondary battery available charge monitor). The tutorial is intended to be used with the bq2010 data sheet by engineera and managers designing with or evaluating the bq2010.

The bq2010 Gas Gauge IC is a complete battery monitoring product for N i and N i d batteries. The bq2010 16-pin SOIC provides significant advantages:

- A complete single-chip system solution for in-the-pack monitoring of a battery's available charge
- No battery technology expertise required; the bq2010 is already optimized for NiMH or NiCd use, based on Benchmarq's extensive research on battery characteristics
- Minimal s eer n required, a single PCB layout specific to the application
- No software required for stand-alone battery-pack applications
- Single-wire serial interface for communication with an external processor to implement a customized display
- Direct LED display drive

This tutorial describes capacity monitoring, compares Benchmarq's gas gauge solutions to microprocessor-based implementations, describes device operation in general terms, and addressee implementation issues.

Available Charge Monitoring

Rechargeable batteries are used in many different applications, from cellular phones, portable computers, and medical equipment to power tools. The operating environment of these batteries covers a wide range of temperatures; therefore, battery efficiency changes due to battery temperature and rate of charge or discharge. The bq2010 compensates for both temperature and charge/discharge rate continuously.

The battery available charge can be displayed on LEDs and is also available via the serial port. The calculated available charge of the battery is also compensated according to battery temperature because the actual available *charge* is reduced at lower temperatures. For example, if the bq2010 indicates that the battery is 60% full at a temperature of 25°C, then the bq2010 indicates 40% full when cooled to 0°C, which is the predicted available *charge* at that temperature. When the temperature returns to 25°C, the displayed capacity returns to 60%. This ensures that the indicated capacity is always conservatively representative of the charge available for use under the given conditions.

The bq2010 also adjusts the available charge for the approximate internal self-diecharge that occurs in NiCd or NiMH batteries. The self-discharge adjustment is based on the selected rate, elapsed time, battery charge level, and temperature. This adjustment provides a conservative estimate of self-discharge that occurs naturally and that is a significant source of discharge in systems that are not charged often or are stored at elevated temperatures.

Comparing bq2010 Solution With MCU-Based Implementations

Low-power, single-chip microprocessors such as those available from Motorola, Toshiba, NEC, and others have been used to implement gas gauges in battery-powered equipment, notably camcorders and laptop computers. Although adequate, these implementations require extensive development efforts to be suitable for use in a battery pack, and even then, require significant space in the pack because of the high component count.

The bq2010 by comparison offers efficiency, ease of use, simplicity of design, and low component count. With careful PCB layout, the bq2010 *system* can fit in the space between AA batteries. Table 1 compares the bq2010 and a typical MCU gas gauge implementation.

bq2010 Operation

Gas gauging is accomplished by measuring the charge input to and subsequently removed from a battery. This is done by monitoring the voltage drop across a low-value resistor (typically 20 to 100mΩ) during charge and discharge. This voltage is integrated over time, scaled, and used to drive two 16-bit internal counters:

- Nominal Available Charge (NAC) counter-represents the amount of charge available from the battery.
- Discharge Count Register (DCR)—represents the amount of charge removed from the battery since it was last full.

Also, the Last Measured Discharge (LMD) register is an eight-bit register used to store the most recent count value representing "battery full."

In a typical situation, the Benchmarq Gas Gauge ICs are installed in a battery pack containing unconditioned batteries with an unknown charge state.

On application of power to the bq2010, the following assumptions are made:

- The battery is empty; therefore, the NAC is zero.
- The battery's storage capacity is the Programmed Full Count (PFC) as specified by the programming inputs, which are loaded into the LMD.

The actual storage capacity of the battery has yet to be determined. The battery capacity can be learned by charging the battery until NAC = LMD (LMD = PFC on initialization) and then discharging the battery until the cell voltage reaches the End-of-Discharge Voltage (EDV1) threshold (1.05V for the bq2010). As discharge occurs, the bq2010 tracks the amount of charge removed from the battery in the DCR. The new battery capacity (DCR) is transferred to the LMD if no partial charges have occurred, the temperature is above 10°C, and self-discharge accounts for less than 8 to 18% of the DCR when EDV1 waa reached. The valid discharge flag (VDQ) in the bq2010 indicates whether the present discharge is valid for LMD update.

Table 1. Comparing bq2010 and MCU Implementations

Feature	MCU Implementation	bq2010 Solution
Small size	>> 1 square inch; requires extra battery pack space	≤ 1 square inch; fits between batteries
Operating current (not including LEDs)	Typically ≥ 1mA awake; as low as 10µA asleep	125µA typical
LED display	Yea	Yes
Serial I/O	Depends on programming	Yes
Programmable capacity	Depends on programming	Yes
Self-discharge	Generally not implemented	Yes, with temperature compensations
Charge, discharge rate compensations	Generally not available but depends on programming	Yes
Charge, discharge temperature compensations	Generally not available but depends on programming; requirea a thermistor	Yes, uses internal temperature sensor
Programming requirements	Extensive MCU programming required for gas gauge functions; possible host programming, algorithm development, and software testing	No programming for stand-alone applications; small host code for serial I/O applications
Hardware design requirements	Extensive low-power-design, op amp, analog switch, MCU, resonator, low-power regulator, LEDs, sense resistor; component count = 56 typical	No engineering required; component count = 23 typical: bq2010, nFET, LEDs, sense resistor, programming resistors and capacitors

Discharging Before the First Charge

Most battery pack manufacturers will assemble their packs with the bq2010 and ship them without charging. When the customer receives a new pack, the pack indicates EMPTY, and the customer then charges the pack until it indicates full. Because chargers terminate fast charge on voltage (-AV) or temperature (ΔT/Δt) conditions, it is possible that fast charge will terminate before the gas gauge shows full because the available capacity of the battery was not zero.

The battery pack manufacturer may want to instruct the user to discharge the battery to EDVF before charging. Once this condition is reached, the battery can be fast-charged until termination—allowing NAC to count up to LMD. Now, the gas gauge is synchronized with the battery and learns the true battery capacity on the next valid discharge cycle.

For applications with LED displays, the complete discharge of the battery pack is indicated by all LEDs going off. For applications using the serial I/O port, complete discharge is indicated when the final end-of-discharge voltage (EDVF) flag is set.

To ensure that the bq2010 accurately predicts the amount of available charge, battery pack manufacturers should instruct their end-users to completely discharge a new battery pack and then charge it until the charger terminates.

Alternatively, the NAC can be written with an estimated battery capacity during pack assembly or testing. While this may alleviate the problem of fast charge terminating before NAC = LMD, it may give the user a false indication of battery capacity if the value written was inaccurate. Under this scenario, users should fully charge a new battery pack. The actual capacity is 'learned' on the next valid discharge.

Using the bq2010

The bq2010 IC is simple to use and implement into a system. Figure 1 shows the bq2010 configured for full functionality. Almost all of the external connections and components are *optional*, as indicated by the dotted lines. For example, most stand-alone applications do not need the EMPTY pin connection or the DQ port (except p s i - bly for testing).

All the external components except perhaps the sense resistor can be surface-mounted. The sense resistor could fit in the space between most battery cells, and the populated PCB may also fit in that space with the correct layout. A bq2010 Gas Gauge IC could, therefore, be added to existing product battery packs with little re-tooling of plastics.

Monitoring the Battery

To determine and track the charge state of the battery, the bq2010 monitors both the divided battery voltage and the voltage drop across the sense resistor.

The divided battery voltage (V_{SB}) is provided by a resistor-divider that divides the battery pack voltage down to a single-cell voltage. V_{SB} is primarily used to determine when the battery has reached the EDV1 threshold so that the new battery capacity determined during discharge may be saved in the LMD. V_{SB} is also used for EDVF determination, battery-removed indication, and battery-replacedindication.

The battery current is monitored using a low-value sense resistor attached to the negative terminal of the battery. The current through the resistor generates a proportional voltage drop, V_{SR}, which is provided to the SR input of the bq2010.

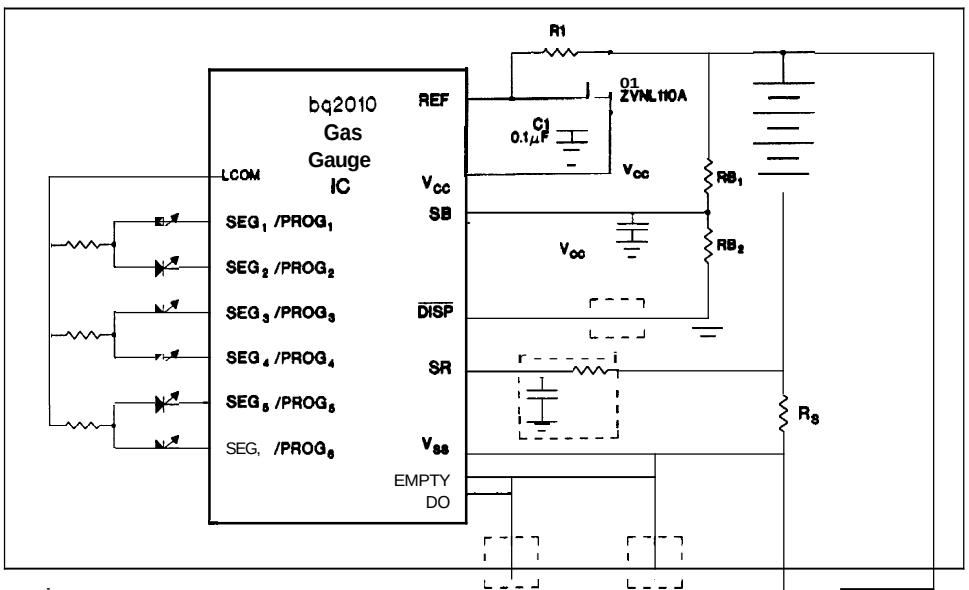
Picking a Sense Resistor

The sense resistor is used to measure the current flowing into or out of the battery. The sense resistor value depends on the currents being measured. The bq2010 specification for V_{SR} ranges from a maximum of 2.0V for charging to -300mV for discharging. The offset error for the bq2010 relative to V_{SR} is ± 150μV.

In general, a sense resistor should be selected so that: (a) the voltage drop across that resistor exceeds 5 to 7mV for the lowest current representing the majority of the battery drain, and (b) the lowest practical V_{SR} voltage drop is achieved to maximize the useful voltage available from the battery pack.

For example, Table 2 summarizes the approximate current requirements for a laptop computer application. The majority of the battery capacity is used in run (no disks) mode. The next largest amount of battery capacity is used in run (with disks) mode, with suspend mode consuming the least amount of battery capacity, even though it makes up the largest block of time.

If a 0.1Ω sense resistor is used, the voltage input to SR is as shown. This means that for both run modes, the integrator repeatability error is a maximum of 2% because $|V_{SR}|$ is well above 30mV. Although the repeatability error associated with suspend mode is approximately 5%, its total error contribution is only 0.5% because suspend mode is responsible for only 10% of the total consumption.



[ ] indicates optional.

Directly connect to V_{CC} across 3 or 4 cells (3 to 5.6V nominal) with a resistor and a Zener diode to limit voltage during charge. Otherwise, R1, C1, and Q1 are needed for regulation of > 4 cells. The value of R1 depends on the number of cells.

Programming resistors (6 max.) and ESD-protection diodes are not shown.

R-C on SR may be required, application-specific.

SD-179

Figure 1. bq2010 Application Diagram—LED Display

Table 2. Approximate Laptop Computer Current Requirements

Mode	Current (A)	0.1Ω Voltage Drop (mV)	Time (min.)	% of Battery Usage
Run (with disks)	1	100.0	20	16.7
Run (no disks)	0.5	50.0	175	72.9
Suspend	0.05	5	250	10.4

Selecting PFCs

When the bq2010 is first connected to the battery pack, a Programmed Full Count (PFC) representing the initial full battery capacity is loaded into the LMD. To select this PFC, determine the initial full battery capacity value in mVh by multiplying the manufacturer's battery capacity rating in mAh by the sense resistor value:

$$mVh = mAh \cdot R_{SNS}$$

Find the nearest corresponding value in Table 3 that is *less* than the calculated mVh value, and then set the programming pin levels to select the Programmed Full Count (PFC), scale, and scale multiplier associated with that value.

Nine PFC settings are available using $PROG_1$ and $PROG_2$, which together with scale ($PROG_3$ and $PROG_4$) settings provide a wide range of initial full battery values. ($PROG_5$ is used to select the self-discharge compensations for either NiMH or NiCd batteries; $PROG_6$ is used to determine the display mode of the bq2010 as described on page 6.)

For example, if a 0.1Ω sense resistor is being used, and the battery is rated at 1100mAh, then the initial full battery value is 110mVh. The nearest available value that is leas than 110mVh from Table 3 is 106mVh, which corresponds to $PROG_1$ = Z, $PROG_2$ = Z, $PROG_3$ = L, and $PROG_4$ = L.

Note that some cells in Table 3 have identical initial full battery values. For example, 141mVh can be found two places:

- Example 1: $PROG_1$ = L, $PROG_2$ = L, $PROG_3$ = Z, $PROG_4$ = L = 141mVh
- Example 2: $PROG_1$ = H, $PROG_2$ = Z, $PROG_3$ = L, $PROG_4$ = L = 141mVh

Example 1 corresponds to a PFC of 22528 of 65535 possible counts (34.4%). This means that, in all likelihood, a majority of the counter range will remain unused. Counter resolution could be increased by using the settings in example 2. In this case, the PFC is 45056 of 65535 counts (68.8% of range). In general, when faced with a choice, it is better to pick the finer resolution (that is, a larger PFC).

$PROG_3$ and $PROG_4$ inputs determine the scale to be used by the bq2010. Together these two pins determine the mVh value of a single NAC count. Thus, for any given PFC selected by $PROG_1$ and $PROG_2$, the capacity represented by that PFC (in mVh) is given by:

$$PFC \cdot scale$$

Note that the scale value is given for a $PROG_3$, $PROG_4$ pair at the top of each column in Table 3.

Table 3. bq2010 Programmed Full Count mVh Selections

$PROG_x$		Programmed Full Count (PFC)	$PROG_4$ = L			$PROG_4$ = Z			Units
1	2		$PROG_3$ = H	$PROG_3$ = Z	$PROG_3$ = L	$PROG_3$ = H	$PROG_3$ = Z	$PROG_3$ = L	
-	-		Scale = 1/80	Scale = 1/160	Scale = 1/320	Scale = 1/640	Scale = 1/1280	Scale= 1/2560	mVh/ count
H	H	49152	614	307	154	76.8	38.4	19.2-	mVh
H	Z	45056	563	282	141	70.4	35.2	17.6	mVh
H	L	40960	512	256	128	64.0	32.0	16.0	mVh
Z	H	36864	461	230	115	57.6	28.8	14.4	mVh
Z	Z	33792	422	211	106	53.0	26.4	13.2	mVh
Z	L	30720	384	192	96.0	48.0	24.0	12.0	mVh
L	H	27648	346	173	86.4	43.2	21.6	10.8	mVh
L	Z	25600	320	160	80.0	40.0	20.0	10.0	mVh
L	L	22528	282	141	70.4	35.2	17.6	8.8	mVh
VSR equivalent to 2 counts/sec. (nom.)			90	45	22.5	11.25	5.6	2.8	mV

Using the Programming Pins

The bq2010 is programmed through the LED display pins during a special programming cycle that occurs during power-up or during a device reset.

Programming Without LED Display

In applications where the LED display is not used. programming is very simple. The bq2010 may be programmed by tying each programming pin directly to the appropriate level:

H = V_{CC}

Z = open

L = V_{SS}

LED outputs must be disabled by tying $\overline{DISP}$ to V_{CC}. LCOM may remain open.

Programming With LED Display

When the LED display is used, it is necessary to provide programming information with either a pull-up resistor to V_{CC}, a pull-down resistor to V_{SS} (200KΩ value in either case), or no resistor at all. The logic states are set as follows:

H ≤ 200K to V_{CC}

Z = no resistor

L ≤ 200K to V_{SS}

LCOM must be used to provide power to the LEDs so that they may be disabled during reading of the programming resistors (see Figure 1).

Selecting Battery Chemistry

$PROG_5$ is used during power-up to select self-discharge compensations for either NiMH or NiCd batteries. $PROG_5$ = Z for NiCd and L for NiMH batteries.

Using the LED Display

The bq2010 supports 6 LEDs that display a gauge of available battery charge. LEDs 1 through 5 provide 20% step indication of charge, while the sixth *LED* indicates 'overfull' when the display is operating in absolute mode ($PROG_6$ = Z).

Selecting Display Mode

$PROG_6$ is used during power-up to determine the display mode of the bq2010. The bq2010 uses either absolute or relative battery *charge* state as described below ($PROG_6$ = Z or L, respectively).

The display indicates available battery charge as a percentage of "battery full.' This is based on the current LMD value ("relative" mode) or on the PFC value (the initial battery capacity value programmed, "absolute" mode). Relative mode is for applications where the customer does not want to see on the display the decline in battery capacity following many charge/discharge cycles. Absolute mode ie for applications when the customer wanta each segment to represent a fiied amount of charge.

Dispiay Activation

The LED display is normally maintained in the OFF state to conserve battery power. It is activated during a high rate of battery charge and discharge if $\overline{DISP}$ is floating, or continuously if the $\overline{DISP}$ pin is pulled to V_{SS}. When the display is not used, the DISP pin can be tied to V_{CC} to disable the display and allow the pins to be used strictly as programming pins.

LED Supply

The current source for the LEDs is provided through the LCOM pin in all applications, because the programming inputs and the LED outputa share common pins. When the bq2010 is initially powered-up, the LCOM output is disabled, thus allowing the pins to be sensed for the presence of programming resistors tied to V_{CC} or V_{SS} (see Figure 1).

Standard LEDs such as the Sharp PR series should provide adequate performance at low cost. For better results, customers could use a high-brightness LED (low current) such as the more expensive Sharp LR or UR series. The suitability of any particular LED depends not only on its luminosity at rated current, but also the packaging and lensing technique used (very important in concentrating viewable energy, eepecially for high-ambient-light conditions).

Using the DQ Serial Port

The bq2010 is also equipped with a bidirectional single-line serial I/O port (DQ) that allows it to conveniently communicate with a hoet processor.

Data Interface

The DQ serial port allows the implementation of gas gauge functions without the need for the LED display. For example, in cellular telephone and laptop computer applications, the LED display is not needed because an LCD is available. The host processor in these cases can simply obtain the gas gauge display step and the temperature over the serial port and use these to indicate available charge. The gas gauge step data is a 4-bit value that represents 1 of 16 possible steps (6.25% of full per step), giving a greater possible display accuracy than is possible with the LED display.

In a more sophisticated approach, the hoet may obtain the NAC, LMD, temperature, and operational status flags, and then use these to customize and display functions and features.

Battery Pack Testing

The DQ serial port is also useful for final testing of assembled battery packs. The bq2010 can be exercised from a hoet processor over the DQ serial port—allowing the host to directly control the state of the LED output pins and the EMPTY pin. The state of the programming pins may also be checked. A battery ID byte (stored in on-chip RAM) allows the manufacturer to identify battery types.

Using the EMPTY Pin

The EMPTY pin provides external control for automatic load disconnection on low battery, preventing deep discharge. It activates when V_{SB} drops below the EDVF threshold.

Supplying Power to the Part

The V_{CC} specification for the bq2010 is:

$$3.0V \leq V_{CC} \leq 6.5V$$

This may be achieved in several ways under various battery configurations.

Direct Battery Power

The bq2010 may be powered diitly from the batteries in configurations of 3 or 4 cells. When using unregulated direct battery power, ensure that the battery voltage does not exceed the maximum of 6.5V or fall below the minimum operational value of 3.0V.

Direct unregulated power supply should be limited to situations where varying or pulsed load conditions during discharge or charge do not cause battery voltage spikes. Such spikes typically result when batteries drive switching power supplies that use inductive storage, or when start-up transients in motors produce si cant voltage spikes on the battery,

Low-Cost nFET Regulator

Most applications require some kind of voltage regulator to supply V_{CC} within specifications over a broad range of battery voltage conditions. The bq2010 provides support for a low-cost regulator circuit consisting of an nFET and the on-chip reference voltage V_{REF}.

Across temperature, V_{REF} ranges from 4.5V to 7.5V, given an I_{REF} of 5µA, where:

$$V_{CC} = V_{REF} - V_{GS}$$

where V_{GS} is the gate-source voltage of the nFET, Q1. When the battery voltage drops below V_{REF}, the $R1/R_{REF}$ divider determines V_{CC}. A low-threshold nFET exhibiting a maximum V_{GS} of 0.8 to 1.5V may be adequate for this circuit. An example is the BSS138ZX from Zetex. The correct choice for R_1 is a function of the number of cells in the battery pack. Table 4 lists different values for R_1 for various battery packs.

Table 4. Reference Bias Resistor R_1 Selection

Assuming a Nominal Q1 V_{GS} = 1.5V

Number of Cells	R1 (Ω)
5	33K
6	100K
7	180K
8	240K
9	300K
10	390K
11	430K
12	510K

Split Battery Configurations

When a battery pack contains a large number of cells, the bq2010 may be operated from a small number of cells inside the larger pack. This is possible as long as the current required for LED operation does not significantly reduce the available charge of the small cell cluster relative to the available charge of the other cells in the pack. Generally, it is best not to use the bq2010 display in this configuration.

Notes

BENCHMARQ

bq2011

Gas Gauge IC

Features

- Conservative and repeatable measurement of available charge in rechargeable batteries
- Designed for portable equipment such ae power tools with high discharge rates
- Designed for battery pack integration
  - 120µA typical standby current (self-discharge estimation mode)
  - Small size enables implementations in as little as ½ square inch of PCB
- Direct drive of LEDs for capacity display
- Self-discharge compensation using internal temperature sensor
- Simple single-wire serial communications port for subassembly testing
- 16-pin narrow SOIC

General Descriptton

The bq2011 Gas Gauge IC is intended for battery-pack installation to maintain an accurate ≪ of available battery charge. The IC monitors a voltage drop across a sense resistor connected in eeriee between the negative battery terminal and ground to determine charge and discharge activity of the battery. The bq2011 is designed for systems *such* as power tools with very high discharge rates.

Battery self-discharge is estimated baaed on an internal timer and temperature sensor. Compensations for battery temperature and rate of charge or discharge are applied to the charge, discharge, and self-diecharge calculations to provide available charge information across a wide range of operating conditions. Initial battery capacity is set using the PFC and MODE pine. Actual battery capacity is automatically 'learned" in the course of a discharge cycle from full to empty and *may* be displayed depending on the display mode.

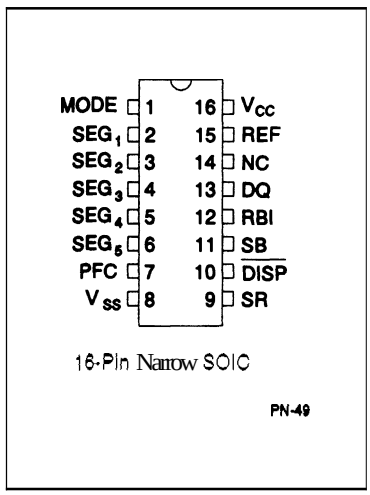
Nominal available charge may be directly indicated using a five-segment LED display. These segments are used to indicate graphically the nominal available charge.

The bq2011 supports a simple single-line bidirectional serial link to an external processor (common ground). The bq2011 outputs battery information in response to external commands over the aerial link. To support subassembly testing, the outputs may also be controlled by command. The external processor may also overwrite some of the bq2011 gas gauge data registers.

The bq2011 may operate directly from four cells. With the REF output and an external transistor, a simple, inexpensive regulator can be built to provide Vcc from a greater number of cells.

Internal registers include available *charge,* temperature, capacity, battery ID, and battery status.

Pin Connections



16-Pin Narrow SOIC

PN-49

Pin Names

MODE	Display mode output	NC	No connect
SEG_1	LED segment 1	DQ	Serial communications input/output
SEG_2	LED segment 2	RBI	Register backup input
SEG_3	LED segment 3	SB	Battery sense input
SEG_4	LED segment 4	$\overline{DISP}$	Display control input
SEG_5	LED segment 5	SR	Sense resistor input
PFC	Programmed full count selection input	V_{CC}	3.0-6.5V
REF	Voltage reference output	V_{SS}	Negative battery terminal

Pin Descriptions

MODE — Display mode output

When left floating, this output selects relative mode for capacity display. If connected to the anode of the LEDs to source current, absolute mode is selected for capacity display. See Table 1.

SEG_1-SEG_5 — LED display segment outputs

Each output may activate an LED to sink the current sourced from MODE, the battery, or V_{CC}.

PFC — Programmed full count selection input

This three-level input pin defines the programmed full count (PFC) thresholds and scale selections described in Table 1. The state of the PFC pin is only read immediately after a reset condition.

SR — Sense resistor input

The voltage drop (V_{SR}) across the sense resistor R_S is monitored and integrated over time to interpret charge and discharge activity. The SR input is tied to the low side of the sense resistor. $V_{SR} > V_{SS}$ indicates discharge, and $V_{SR} < V_{SS}$ indicates charge. The effective voltage drop, V_{SRO}, as seen by the bq2011 is $V_{SR} + V_{OS}$ (see Table 3).

NC — No connect

$\overline{DISP}$ — Display control input

$\overline{DISP}$ floating allows the LED display to be active during charge and discharge if $V_{SRO} < -1mV$ (charge) or $V_{SRO} > 2mV$ (discharge). Transitioning $\overline{DISP}$ low activates the display for 4 ± 0.5 seconds.

SB — Secondary battery input

This input monitors the single-cell voltage potential through a high-impedance resistive divider network for the end-of-discharge voltage (EDV) threshold and maximum cell voltage (MCV).

RBI — Register backup input

This input is used to provide backup potential to the bq2011 registers *during* periods when $V_{CC} \leq$ 3V. A storage capacitor should be connected to RBI.

DQ — Serial I/O pin

This is an open-drain bidirectional pin.

REF — Voltage reference output for regulator

REF provides a voltage reference output for an optional micro-regulator.

V_{CC} — Supply voltage input

V_{SS} — Ground

Functional Description

General Operation

The bq2011 determines battery capacity by monitoring the amount of charge input to or removed from a rechargeable battery. The bq2011 measures discharge and charge currents, estimates sell-discharge, monitors the battery for low-battery voltage thresholds, and compensates for temperature and charge/discharge rates. The charge measurement is made by monitoring the voltage across a small-value series sense resistor between the negative battery terminal and ground. The available battery charge is determined by monitoring this voltage over time and correcting the measurement for the environmental and operating conditions.

Figure 1 shows a typical battery pack application of the bq2011 using the LED display with abeolute mode as a charge-state indicator. The bq2011 can be configured to display capacity in either a relative or an absolute display mode. The relative display mode uses the last measured discharge capacity of the battery as the battery 'full' reference. The absolute display mode uses the programmed full count (PFC) as the full reference, forcing each segment of the display to represent a fixed amount of charge. A push-button display feature is available for momentarily enabling the LED display.

The bq2011 monitors the charge and discharge currents as a voltage across a sense resistor (see R_S in Figure 1). A filter between the negative battery terminal and the SR pin may be required if the rate of change of the battery current is too great.

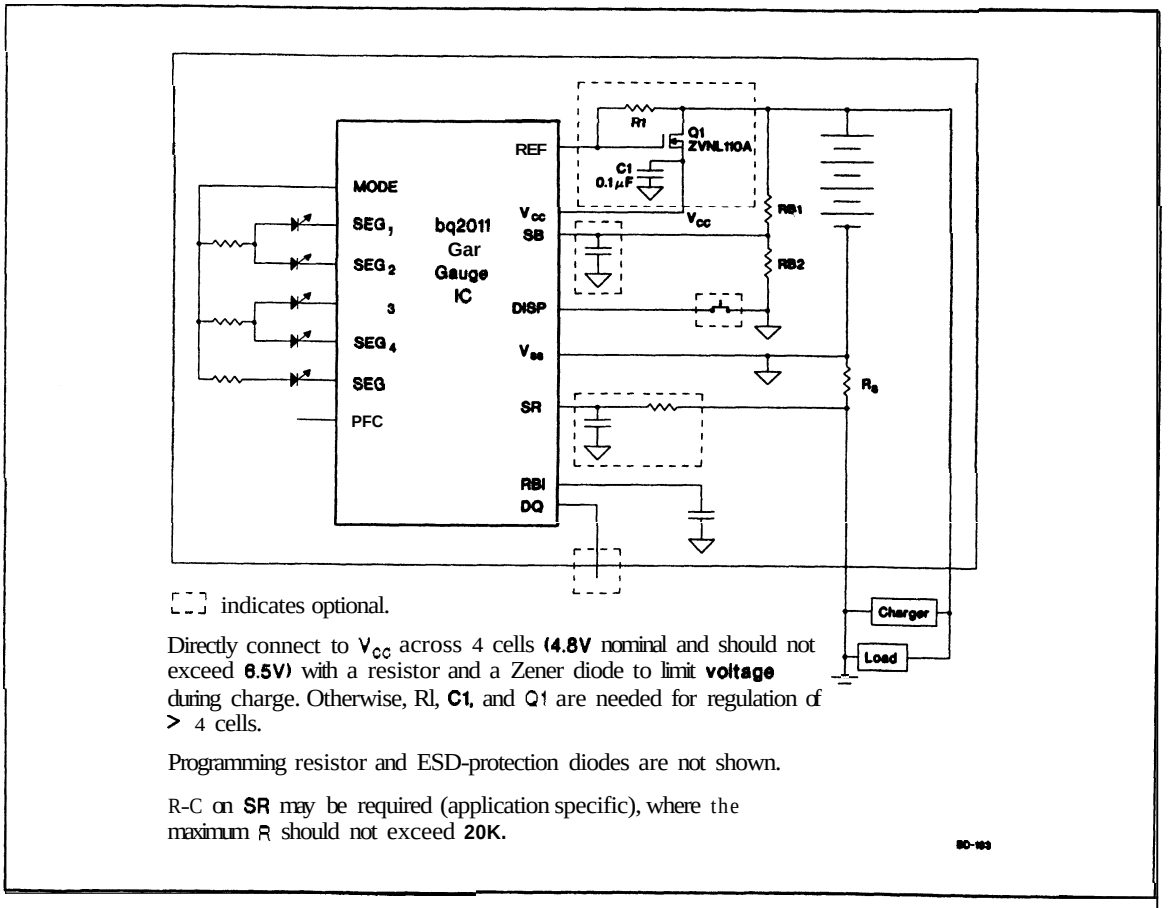


Figure 1. Battery Pack Application Diagram—LED Display, Absolute Mode

Register Backup

The bq2011 RBI input pin is intended to be used with a storage capacitor to provide backup potential to the internal bq2011 registers when Vcc momentarily drops below 3.0V. Vcc is output on RBI when Vcc is above 3.0V.

After Vcc rises above 3.0V, the bq2011 checks the internal registers for data loss or corruption. If data has changed, then the NAC and FULCNT registers are cleared, and the LMD register is loaded with the initial PFC.

Voltage Thresholds

In conjunction with monitoring VSR for charge/discharge currents, the bq2011 monitors the single-cell battery potential through the SB pin. The single-cell voltage potential is determined through a resistor-divider network per the following equation:

$$\frac{RB_1}{RB_2} = N - 1$$

where N is the number of cells, RB_1 is connected to the positive battery terminal, and RB2 is connected to the negative battery terminal. The eingle-cell battery voltage is monitored for the end-of-diacharge voltage (EDV) and for maximum cell voltage (MCV). The EDV threshold level is used to determine when the battery has reached an 'empty" state, and the MCV threshold is used for fault detection during charging. The EDV and MCV thresholds for the bq2011 are fixed at:

$$V_{EDV} = 0.90V$$
$$V_{MCV} = 2.00V$$

During discharge and charge, the bq2011 monitors VSR for various thresholds, V_{SR1}–V_{SR4}. These thresholds are used to compensate the charge and discharge rates. Refer to the diacharge compensation section for details. EDV monitoring is disabled if $V_{SR} \geq V_{SR1}$ (50mV typical) and resumes 1 second after VSR drops back below V_{SR1}.

Reset

The bq2011 recognizes a valid battery whenever VSB is greater than 0.1V typical. VSB rising from below 0.25V resets the device. Reset can also be accomplished with a command over the serial port as described in the Reset Register section.

Temperature

The bq2011 internally determines the temperature in 10°C steps centered from -35°C to +85°C. The temperature steps are used to adapt charge and discharge rate compensations, self-discharge counting, and available charge display translation. The temperature range is available over the serial port in 10°C increments as shown below:

TMPGG (hex)	Temperature Range
0x	< -30°C
1x	-30°C to -20°C
2x	-20°C to -10°C
3x	-10°C to 0°C
4x	0°C to 10°C
5x	10°C to 20°C
6x	20°C to 30°C
7x	30°C to 40°C
8x	40°C to 50°C
9x	50°C to 60°C
Ax	60°C to 70°C
Bx	70°C to 80°C
Cx	> 80°C

Layout Considerations

The bq2011 measures the voltage differential between the SR and Vss pins. Vos (the offset voltage at the SR pin) is greatly affected by PC board layout. For optimal results, the PC board layout should follow the strict rule of a single-point ground return. Sharing high-current ground with small signal ground caueea undesirable noise on the small signal nodes. Additionally:

- The capacitors (SB and Vcc) should be placed as close as possible to the SB and Vcc pins, respectively, and their paths to Vss should be as short as possible. A high-quality ceramic capacitor of 0.1µf is recommended for Vcc.
- The sense resistor (Rs) should be as close as possible to the bq2011.
- The R-C on the SR pin should be located as close as possible to the SR pin. The maximum R should not exceed 20K.

Gas Gauge Operation

The operational overview diagram in Figure 2 illustrates the operation of the **bq2011.** The **bq2011** accumulates a measure of charge and discharge currents, as well as an **estimation** of **self-discharge.** Charge and **discharge** currents are temperature and rate compensated, whereas sell-diecharge is only temperature compensated.

The main counter, Nominal Available Charge **(NAC), represents** the available battery capacity at any given time. Battery charging increments the NAC register, while battery discharging and self-discharge decrement the NAC regieter and increment the DCR (Discharge Count **Register).**

The Discharge Count **Register (DCR)** is used to update the Last Measured Discharge (LMD) register only if a complete battery discharge from full to empty occurs without any partial battery charges. Therefore, the **bq2011** adapts its capacity determination baeed on the **actual** conditions of **discharge.**

The battery's initial capacity is equal to the Programmed Full Count (PFC) shown in Table 1. Until LMD **is** updated, NAC counts up to but not beyond this threshold during subsequent charges. **This** approach allows the gas gauge to be charger-independent and compatible with any type of charge regime.

1. **Last Measured Discharge (LMD)** or **learned battery capacity:**

   LMD is the **last measured discharge** capacity of the battery. On initialization (application of Vcc or battery replacement), LMD = PFC. During **subsequent** discharges, the LMD is updated with the latest **measured** capacity in the Discharge Count Register (DCR) **representing** a discharge from **full** to below EDV. A qualified discharge is **necessary** for a capacity **transfer** from the DCR to the LMD **register.** The LMD **also** serves as the 100% reference **threshold** used by the relative **display** mode.

2. **Programmed** Full **Count (PFC)** or **initial** battery **capacity**

   The initial LMD and gas gauge rate values **are** programmed by using **PFC.** The **PFC** also provides the 100% reference for the **absolute** display mode. The **bq2011** is **configured** for a given application by **selecting** a PFC value **from** Table 1. The correct PFC may be determined by multiplying the rated battery capacity in mAh by the sense **resistor** value:

   Battery capacity (mAh) • **sense resistor (Ω) =**

   PFC (mVh)

   Selecting a PFC slightly less than the rated capacity for abeolute mode **provides** capacity **above** the full reference for much of the **battery's** life.

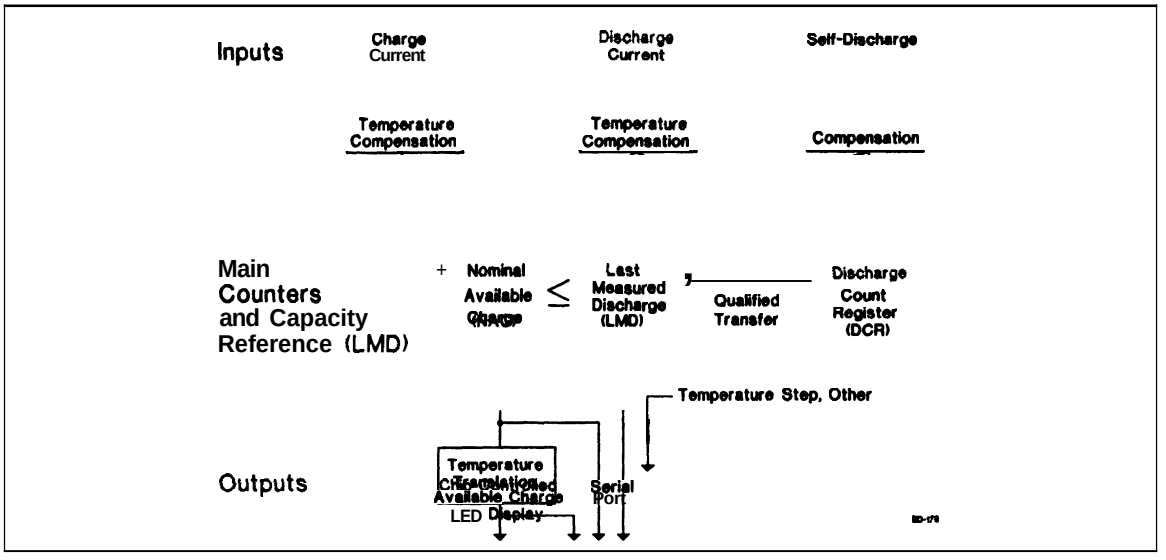


Figure 2. Operational Overview

Example: Selecting a *PFC* Value

Given:

Sense resistor = 0.005Ω
Number of cells = 6
Capacity = 1300mAh, NiCd cells
Current range = 1A to 80A
Relative display mode
Self-discharge = 6/64
Voltage drop over sense resistor = 5mV to 400mV

Therefore:

1300mAh • 0.00512 = 6.5mVh

Select:

PFC = 34304 counts or 6.5mVh
PFC = Z (float)
MODE = not connected

The initial full battery capacity is 6.5mVh (1300mAh) until the bq2011 learns' a new capacity with a qualified discharge from full to EDV.

Table 1. bq2011 Programmed Full Count mVh Selections

PFC	Programmed Full Count (PFC)	mVh	Scale	MODE Pin	Display Mode
H	27648	10.5	1/2640	Floating	Relative
Z	34304	6.5	1/5280		
L	44800	8.5	1/5280		
H	42240	8.0	1/5280	Connected to LEDs	Absolute
Z	31744	6.0	1/5280		
L	23808	4.5	1/5280		

3. Nominal Available Charge (NAC):

   NAC counts up during charge to a maximum value of LMD and down during discharge and selfdischarge to 0. NAC is reset to 0 on initialization and on the first valid charge following *discharge* to EDV. To prevent overstatement of charge during periods of overcharge, NAC stops incrementing when NAC = LMD.

   Note: NAC is set to the value in LMD when SEGs is pulled low during a reset.

4. Discharge Count Register (DCR):

   The DCR counts up during discharge independent of NAC and could continue increasing after NAC has decremented to 0. Prior to NAC = 0 (empty battery), both discharge and self-discharge increment the DCR After NAC = 0, only discharge increments the DCR. The DCR resets to 0 when NAC = LMD. The DCR does not roll over but stops counting when it reaches FFFFh.

   The DCR value becomes the new LMD value on the first charge after a valid discharge to V_{EDV} if:

   - No valid charge initiations (charges greater than 256 NAC counts; or 0.006 - 0.01C) occurred during the period between NAC = LMD and EDV detected.
   - The self-discharge count is not more than 4096 counts (8% to 18% of PFC, specific percentage threshold determined by PFC).
   - The temperature is ≥ 0°C when the EDV level is reached during discharge.

   The valid discharge flag (VDQ) indicates whether the present discharge is valid for LMD update.

Charge Counting

Charge activity is detected based on a negative voltage on the V_{SR} input. If charge activity is detected, the bq2011 increments NAC at a rate proportional to Vsm (V_{SR} + Vos) and, if enabled, activates an LED display if V_{SRO} < -1mV. Charge actions increment the NAC after compensation for charge rate and temperature.

The bq2011 determines a valid *charge* activity sustained at a continuous rate equivalent to V_{SRO} < -400µV. A valid charge equates to a sustained charge activity greater than 256 NAC counts. Once a valid charge is detected, charge counting continues until Vsm rises above -400µV.

Discharge Counting

All discharge counts where V_{SRO} > 500µV cause the NAC register to decrement and the DCR to increment. Exceeding the fast discharge threshold (FDQ) if the rate is equivalent to V_{SRO} > 2mV activates the display, if enabled. The display becomes inactive after V_{SRO} falls below 2mV.

Self-Discharge Estimation

The bq2011 continuously decrements NAC and increments DCR fa: self-discharge based an time and temperature. The self-discharge count rate is programmed to be a nominal 1/80 • NAC rate per day. This is the rate for a battery whose temperature is between 20°–30°C. The NAC register cannot be decremented below 0.

Count Compensations

The bq2011 determines fast charge when the NAC updates at a rate of ≥2 counts/sec. Charge and discharge activity is compensated for temperature and charge/discharge rate before updating the NAC and/or DCR Self-discharge estimation is compensated for temperature before updating the NAC or DCR.

Charge Compensation

Two charge efficiency factors are used for trickle charge and fast charge. Fast charge is defined as a rate of charge resulting in ≥ 2 NAC counts/sec (≥ 0.15C to 0.32C depending on PFC selections; see Table 2). The compensation defaults to the fast charge factor until the actual charge rate is determined.

Temperature adapts the charge rate compensation factors over three ranges between nominal, warm, and hot temperatures. The compensation factors are shown below.

Charge Temperature	Trickle Charge Compensation	Fast Charge Compensation
<40°C	0.80	0.95
≥ 40°C	0.75	0.90

Discharge Compensation

Corrections for the rate of discharge are made by adjusting an internal discharge compensation factor. The discharge factor is based on the dynamically measured V_{SR}. The compensation factors during discharge are:

Approximate V_{SR} Threshold	Discharge Compensation Factor	Efficiency
V_{SR} < 50 mV	1.00	100%
V_{SR1} > 50 mV	1.05	95%
V_{SR2} > 100 mV	1.15	85%
V_{SR3} > 150 mV	1.25	75%
V_{SR4} > 253 mV	1.25	75%

Temperature compensation during discharge also takes place. At lower temperatures, the compensation factor increases by 0.05 for each 10°C temperature step below 10°C.

Comp. factor = 1.00 + (0.05 • N)

Where N = number of 10°C steps below 10°C and V_{SR} < 50mV.

For example:

T > 10°C: Nominal compensation, N = 0

0°C < T < 10°C: N = 1 (i.e., 1.00 becomes 1.05)

-10°C < T < 0°C: N = 2 (i.e., 1.00 becomes 1.10)

-20°C < T < -10°C: N = 3 (i.e., 1.00 becomes 1.15)

-20°C < T < -30°C: N = 4 (i.e., 1.00 becomes 1.20)

Self-Discharge Compensation

The self-discharge compensation is programmed for a nominal rate of 1/80 • NAC per day. This is the rate for a battery within the 20–30°C temperature range (TMPGG = 6x). This rate varies across 8 ranges from <10°C to >70°C, doubling with each higher temperature step (10°C). See Table 2.

Table 2. Self-Discharge Compensation

Temperature Range	Self-Discharge Compensation Typical Rate/Day
< 10°C	NAC/320
10–20°C	NAC/160
20–30°C	NAC/80
30–40°C	NAC/40
40–50°C	NAC/20
50–60°C	NAC/10
60–70°C	NAC/5
> 70°C	NAC/2.5

Error Summary

Capacity Inaccurate

The LMD is susceptible to error on initialization or if no updates occur. On initialization, the LMD value includes the error between the programmed full capacity and the actual capacity. This error is present until a valid discharge occurs and LMD is updated (see the DCR description on page 7). The other cause of LMD error is battery wear-out. As the battery ages, the measured capacity must be adjusted to account for changes in actual battery capacity.

A Capacity Inaccurate counter (CPI) is maintained and incremented each time a valid charge occurs and is reset whenever LMD is updated from the DCR. The counter does not wrap around but stops counting at 255. The capacity inaccurate flag (CI) is set if LMD has not been updated following 64 valid charges.

Current-Sensing Error

Table 3 illustrates the current-sensing error as a function of V_{SR}. A digital filter eliminates charge and discharge counts to the NAC register when V_{SR0} (V_{SR} + V_{OS}) is between -400µV and 500µV.

Table 3. bq2011 Current-Sensing Errors

Symbol	Parameter	Typical	Maximum	Units	Notes
V_{OS}	Offset referred to V_{SR}	±50	±150	µV	$\overline{DISP}$ = V_{CC}.
INL	Integrated non-linearity error	±2	±4	%	Add 0.1% per °C above or below 25°C and 1% per volt above or below 4.25V.
INR	Integrated non-repeatability error	±1	±2	%	Measurement repeatability given similar operating conditions.

Communicating With the bq2011

The bq2011 includes a simple single-pin (DQ plus return) serial data interface. A hoet processor uses the interface to access various bq2011 registers. Battery characteristics may be easily monitored by adding a single contact to the battery pack. The open-drain DQ pin on the bq2011 should be pulled up by the hoet system, or may be left floating if the serial interface is not used.

The interface uses a command-based protocol, where the host processor sends a command byte to the bq2011. The command directs the bq2011 to either store the next eight bite of data received to a register specified by the command byte or output the eight bits of data specified by the command byte.

The communication protocol is asynchronous return-to-one. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 333 bits/sec. The least-significant bit of a command or data byte is transmitted first. The protocol is simple enough that it can be implemented by most host processors using either polled or interrupt processing. Data input from the bq2011 may be sampled using the pulse-width capture timers available on some microcontrollers.

Communication is normally initiated by the hoet processor sending a BREAK command to the bq2011. A BREAK is detected when the DQ pin is driven to a logic-low state for a time, t_B or greater. The DQ pin should then be returned to its normal ready-high logic state for a time, t_{BR}. The bq2011 is now ready to receive a command from the host processor.

The return-to-one data bit frame consists of three distinct sections. The first section is used to start the transmission by either the host or the bq2011 taking the DQ pin to a logic-low state for a period, $t_{STRH,B}$. The next section is the actual data transmission, where the data should be valid by a period, t_{DSU}, after the negative edge used to start communication. The data should be held for a period, t_{DV}, to allow the host or bq2011 to sample the data bit.

The final section is used to stop the transmission by returning the DQ pin to a logic-high state by at least a period, t_{SSU}, after the negative edge used to start communication. The final logic-high state should be held until a period, t_{SV}, to allow time to ensure that the bit transmission was stopped properly. The timings for data and break communication are given in the serial communication timing specification and illustration sections.

Communication with the bq2011 is always performed with the least-significantbit being transmitted first. Figure 3 shows an example of a communication sequence to read the bq2011 NAC register.

bq2011 Registers

The bq2011 *command* and statue registers are listed in Table 4 and described below.

Command Register (CMDR)

The write-only CMDR register is accessed when eight valid command bite have been received by the bq2011. The CMDR register contains two fields:

- W/$\overline{R}$ bit
- Command address

The W/$\overline{R}$ bit of the command register is used to select whether the received command is for a read or a write function.

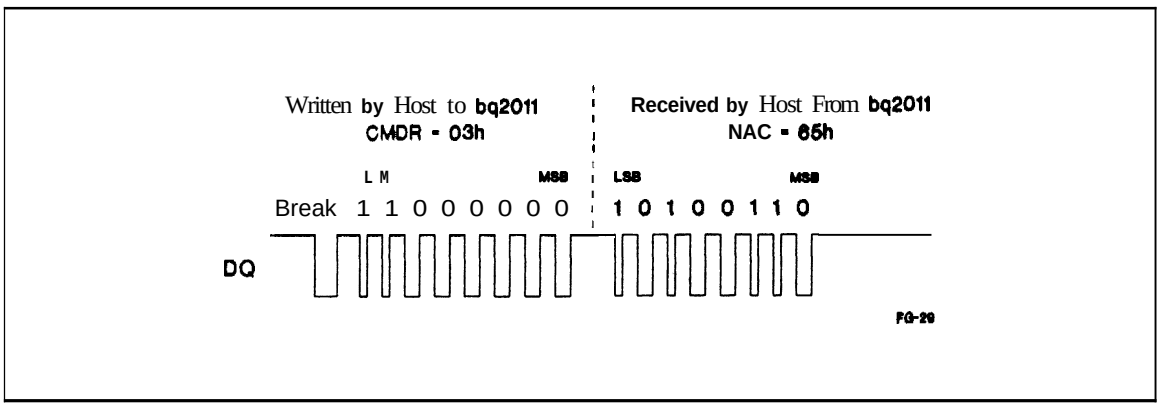


Figure 3. Typical Communication With the bq2011

Table 4. bq2011 Command and Status Registers

Symbol	Register Name	Loc. (hex)	Read/ Write	Control Field							
				7(MSB)	6	5	4	3	2	1	0(LSB)
CMDR	Command register	00h	Write	W	AD6	AD5	AD4	AD3	AD2	AD1	AD0
FLGS1	Primary status flags register	01h	Read	CHGS	BRP	MCV	CI	VDQ	n/u	EDV	n/u
TMPGG	Temperature and gas gauge register	02h	Read	TMP3	TMP2	TMP1	TMP0	GG3	GG2	GG1	GG0
NACH	Nominal available charge high byte register	03h	R/W	NACH7	NACH6	NACH5	NACH4	NACH3	NACH2	NACH1	NACHO
NACL	Nominal available charge low byte register	17h	Read	NACL7	NACL6	NACL5	NACL4	NACL3	NACL2	NACL1	NACL0
BATID	Battery identification register	04h	R/W	BATID7	BATID6	BATID5	BATID4	BATID3	BATID2	BATID1	BATID0
LMD	Last measured discharge register	05h	R/W	LMD7	LMD6	LMD5	LMD4	LMD3	LMD2	LMD1	LMD0
FLGS2	Secondary status flags register	06h	Read	CR	DR2	DR1	DR0	n/u	n/u	n/u	OVLD
CPI	Capacity inaccurate count register	09h	Read	CPI7	CPI6	CPIS	CPI4	CPI3	CPI2	CPI1	CPIO
OCTL	Output control register	Oah	Write	1	OC5	0C4	0C3	OC2	OC1	n/u	OCE
FULCNT	Full count register	Obh	Read	FUL7	FUL6	FUL5	FUL4	FUL3	FUL2	FUL1	FUL0
RST	Resetregister	39h	Write	RST	0	0	0	0	0	0	0

Note: n/u = not used

The $\overline{W/R}$ values are:

CMDR Bits							
7	6	5	4	3	2	1	0
$\overline{W/R}$	-	-	-	-	-	-	-

Where $\overline{W/R}$ is:

0 The bq2011 outputs the requested register contents specified by the address portion of CMDR

1 The following eight bits should be written to the register specified by the address portion of CMDR.

The lower eeven-bit field of CMDR contains the address portion of the register to be accessed. Attempts to write to invalid addresses are ignored.

CMDR Bits							
7	6	5	4	3	2	1	0
-	AD6	AD5	AD4	AD3	AD2	AD1	AD0 (LSB)

Primary Status Flags Register (FLGS1)

The read-only FLGS1 register (address=01h) contains the primary bq2011 flags.

The charge *status* flag (CHGS) is asserted when a valid charge rate is detected. Charge rate ia deemed valid when V_{SRO} < -400µV. A V_{SRO} of greater than- 400µV or discharge activity clears CHGS.

The CHGS values are:

FLGSI Bib			
	2	1	0
CHGS -	-	-	-

Where CHGS is:

0 Either discharge activity detected or V_{SRO} > -400µV

1 V_{SRO} < -400µV

The *battery* ***replaced*** flag (BRP) is asserted whenever the potential on the SB pin (relative to V_{SS}), V_{SB}, rises above 0.1V and determines the internal registers have been corrupted. The BRP flag is also set when the bq2011 is reset (see the RST register description). BRP is latched until either the bq2011 is charged until NAC = LMD or discharged until EDV is reached. BRP = 1 signifies that the device has been reset.

The BRP values are:

FLGS1 Bib							
7	6	5	4	9	2	1	0
-	BRP	-					

Where BRP is:

0 bq2011 is charged until NAC = LMD or discharged until the EDV flag is asserted

1 SB rising from below 0.1V, or a serial port initiated reset has occurred

The maximum all *voltage* flag (MCV) is asserted whenever the potential on the SB pin (relative to Vss) is above 2.0V. The MCV flag is asserted until the condition causing MCV is removed.

The MCV values are:

RGSI Bib							
7	6	5	4	3	2	1	0
-	-	MCV	-	-	-	-	-

Where MCV is:

0 V_{SB} < 2.0V

1 V_{SB} > 2.0V

The *capacity inaccurate* flag (CI) is used to warn the user that the battery has been charged a substantial number of times since LMD has been updated. The CI flag is asserted on the 64th charge after the last LMD update or when the bq2011 is reset. The flag is cleared after an LMD update.

The CI values are:

RGSI Bib							
7	6	5	4	3	2	1	0
-	-	-	CI	-	-	-	-

Where CI is:

0 When LMD is updated with a valid full discharge or the bq2011 is reset

1 After the 64th valid charge action with no LMD updates

The *valid discharge* flag (VDQ) is asserted when the bq2011 is discharged from NAC=LMD. The flag remains set until either LMD is updated or one of three actions that can clear VDQ occurs:

- The self-discharge count register (SDCR) has exceeded the maximum acceptable value (4096 counts) for an LMD update.
- A valid charge action equal to 256 NAC counts with $V_{SRO} < -400\mu V$.
- The EDV flag was set at a temperature below 0°C

The VDQ values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	VDQ	-	-	-

Where VDQ is:

0 SDCR ≥ 4096, subsequent valid charge action detected, or EDV is asserted with the temperature less than 0°C

1 On first discharge after NAC = LMD

The *end-of-discharge warning* flag (EDV) warns the user that the battery is empty. SEG1 blinks at a 4Hz rate. EDV detection is disabled if $V_{SR} > V_{SR1}$. The EDV flag is latched until a valid charge has been detected.

The EDV values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
					-	EDV	-

Where EDV is:

0 Valid charge action detected and $V_{SB} \geq 0.90V$

1 $V_{SB} < 0.90V$ providing that $V_{SR} < V_{SR1}$

Temperature and Gas Gauge Register (TMPGG)

The read-only TMPGG register (address=02h) contains two data fields. The first field contains the battery temperature. The second field contains the available charge from the battery.

TMPGG Temperature Bits							
7	6	5	4	3	2	1	0
TMP3	TMP2	TMP1	TMP0	-	-	-	

The bq2011 contains an internal temperature sensor. The temperature is used to set charge and discharge efficiency factors as well as to adjust the self-discharge coefficient. The temperature register contents may be translated as shown below.

TMP3	TMP2	TMP1	TMP0	Temperature
0	0	0	0	T < -30°C
0	0	0	1	-30°C < T < -20°C
0	0	1	0	-20°C < T < -10°C
0	0	1	1	-10°C < T < 0°C
0	1	0	0	0°C < T < 10°C
0	1	0	1	10°C < T < 20°C
0	1	1	0	20°C < T < 30°C
0	1	1	1	30°C < T < 40°C
1	0	0	0	40°C < T < 50°C
1	0	0	1	50°C < T < 60°C
1	0	1	0	60°C < T < 70°C
1	0	1	1	70°C < T < 80°C
1	1	0	0	T > 80°C

The bq2011 calculates the available charge as a function of NAC, temperature, and a full reference, either LMD or PFC. The results of the calculation are available via the display port or the gas gauge field of the TMPGG register. The register is used to give available capacity in 1/16 increments from 0 to 15/16.

TMPGG Gas Gauge Bits							
7	6	5	4	3	2	1	0
-	-	-	-	GG3	GG2	GG1	GG0

The gas gauge diaplay and the gas gauge portion of the TMPGG register are adjusted for cold temperature dependencies. A piece-wise correction is performed as follows:

Temperature	Available Capacity Calculation
> 0°C	NAC / "Full Reference"
-20°C < T < 0°C	0.75 • NAC / "Full Reference"
< -20°C	0.5 • NAC / "Full Reference"

The adjustment between > 0°C and -20°C < T < 0°C has a 4°C hysteresis.

Nominal Available Charge Register (NAC)

The read/write NACH register (address=03h) and the read-only NACL register (address=17h) are the main gas gauging registers for the bq2011. The NAC registers are incremented during charge actions and decremented during discharge and self-discharge actions. The correction factors for charge/discharge efficiency are applied automatically to NAC.

If SEG_5 = 0 on reset, then NACH = PFC and NACL = 0. If SEG_5 = Z or H, the NACH and NACL registers are cleared to zero, NACL stops counting when NACL reaches zero. When the bq2011 detects a valid charge. NACL resets to *zero; writing to the NAC* register *affects the available charge counts and, therefore, affects the bq2011 gas gauge operation.*

Battery Identification Register (BATID)

The read/write BATID register (address=04h) is available for use by the system to determine the type of battery pack. The BATID contents are retained as long as V_{CC} is greater than 2V. The contents of BATID have no effect on the operation of the bq2011. There is no default setting for this register.

Last Measured Discharge Register (LMD)

LMD is a read/write register (address=05h) that the bq2011 uses as a measured full reference. The bq2011 adjusts LMD based on the measured discharge capacity of the battery from full to empty. In this way the bq2011 updates the capacity of the battery. LMD is set to PFC during a bq2011 reset.

Secondary Status Flags Register (FLGS2)

The read-only FLGS2 register (address=06h) contains the secondary bq2011 flags.

The charge *rate* flag (CR) is used to denote the fast charge regime. Fast charge is assumed whenever a charge action is initiated. The CR flag remains asserted if the charge rate does not fall below 2 counts/sec.

The CR values *are:*

FLGS2 Bits							
7	6	5	4	3	2	1	0
CR	-						

Where CR is:

0 When charge rate falls below 2 counts/sec

1 When charge rate is above 2 counts/sec

The fast charge regime efficiency factors are used when CR = 1. When CR = 0, the trickle *charge* efficiency factors are used. The time to change CR varies due to the user-selectable count rates.

The *discharge rate* flags, DR2–0, *are* bits 6–4.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	DR2	DR1	DR0	-			

They are used to determine the present discharge regime as follows:

DR2	DR1	DR0	V_{SR} (V)
0	0	0	V_{SR} < 50mV
0	0	1	50mV < V_{SR} < 100mV (overload, OVLD=1)
0	1	0	100mV < V_{SR} < 150mV
0	1	1	150mV < V_{SR} < 253mV
1	0	0	V_{SRD} > 253mV

The *overload* flag (OVLD) is asserted when a discharge overload is detected, V_{SRD} > 50mV. OVLD remains asserted as long as the condition persists and ia cleared when V_{SRD} < 50mV.

FLGS2 Bits							
7	6	5					
-	-	-				-	OVLD

DR2–0 and OVLD are set based on the measurement of the voltage at the SR pin relative to Vss. The rate at which this measurement is made varies with device activity.

Full Count Register (FULCNT)

The read-only FULCNT register (address=0bh) provides the system with a diagnostic of the number of times the battery has been fully charged (NAC = LMD). The number of full occurrences can be determined by multiplying the value in the FULCNT register by 16. Any discharge action other than self-discharge allows detection of another full occurrence during the next valid charge action

Capacity Inaccurate Count Register (CPI)

The read-only CPI register (address=09h) is used to indicate the number of times a battery has been charged without an LMD update. Because the capacity of a rechargeable battery varies with age and operating conditions, the bq2011 adapts to the changing capacity over time. A complete discharge from full (NAC=LMD) to empty (EDV=1) is required to perform an LMD update assuming there have been no intervening valid charges, the temperature is greater than or equal to 0°C, and the self-discharge counter is less than 4096 counts.

The CPI register is incremented every time a valid charge is detected. The register increments to 255 without rolling over. When the contente of CPI are incremented to 64, the capacity inaccurate flag, CI, is asserted in the FLGS1 register. CPI is reset whenever an update of the LMD register is performed, and the CI flag is also cleared.

Output Control Register (OCTL)

The write-only OCTL register (address=0ah) provides the system with a means to check the display connections for the bq2011. The segment drivers may be overwritten by data from OCTL when the least-significant bit of OCTL, OCE, is set. The data in bits OC_{5-1} of the OCTL register (see Table 4 on page 10 for details) is output onto the segment pine, SEG_{5-1}, respectively if OCE=1. *Whenever OCE* is written to 1, the MSB of OCTL should be *set* to a 1. The OCE register location must be cleared to return the bq2011 to normal operation. OCE may be cleared by either writing the bit to a logic zero via the serial port or by resetting the bq2011 as explained below. **Note:** Whenever the OCTL register is written, the MSB of OCTL should be written to a logic one.

Reset Register (RST)

The reset register (address=39h) provides the means to perform a software-controlled reset of the device. A full device reset may be accomplished by first writing LMD (address = 05h) to 00h and then writing the RST register contents from 00h to 80h. Setting any bit other than the most-significant bit of the RST register is *not* allowed, and results in *improper operation* of the *bq2011*.

Resetting the bq2011 sets the following:

- LMD = PFC
- CPI, VDQ, NAC, and OCE = 0 or NAC = LMD when SEG5 = L
- CI and BRP = 1

Display

The bq2011 can directly display capacity information using low-power LEDs. If LEDs *are* used, the segment pins should be tied to V_{CC}, the battery, or the MODE pin for programming the bq2011.

The bq2011 displays the battery charge state in either absolute or relative mode. In relative mode, the battery charge is represented as a percentage of the LMD. Each LED segment represents 20% of the LMD.

In absolute mode, each segment represents a fixed amount of charge, based on the initial PFC. In absolute mode, each segment represents 20% of the PFC. As the battery wears out over time, it is possible for the LMD to be below the initial PFC. In this case, all of the LEDs may not turn on, representing the reduction in the actual battery capacity.

The capacity display is also adjusted for the present battery temperature. The temperature adjustment reflects the available capacity at a given temperature but does not affect the NAC register. The temperature adjustments *are* detailed in the TMPGG register description.

When $\overline{DISP}$ is tied to Vcc, the SEG_{1-5} outputs are inactive. When $\overline{DISP}$ is left floating, the display becomes active during charge if the NAC registers are counting at a rate equivalent to $V_{SRO} < -1mV$ or fast discharge if the NAC registers are counting at a rate equivalent to $V_{SRO} > 2mV$. When pulled low, the segment output becomes active for 4 seconds, ±0.5 seconds.

The segment outputs are modulated as two banks, with segments 1, 3, and 5 alternating with segments 2 and 4. The segment outputs are modulated at approximately 320Hz, with each bank active for 30% of the period.

SEG_1 blinks at a 4Hz rate whenever V_{SB} has been detected to be below V_{EDV} to indicate a low-battery condition or NAC is less than 10% of the LMD or PFC, depending on the display mode.

Microregulator

The bq2011 *can* operate directly from 4 cells. To facilitate the power supply requirements of the bq2011, an REF *output* is provided to regulate an external low-threshold n-FET. A micropower source for the bq2011 can be inexpensively built using the FET and an external resistor.

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to V_{SS}	-0.3	+7.0	V	
All other pins	Relative to V_{SS}	-0.3	+7.0	V	
V_{SR}	Relative to V_{SS}	-0.3	+7.0	V	Minimum 100Ω series resistor should be used to protect SR in case of a shorted battery (see the bq2011 application note for details).
T_{OPR}	Operating temperature	0	+70	°C	Commercial
		-40	+85	°C	Industrial

Note: Permanent device damage may occur if **Absolute Maximum Ratings are** exceeded. Functional operation should be limited to the Recommended DC Operating **Conditions** detailed in **this** data sheet. Exposure to conditions beyond the operational **limits** for extended periods of time may ***affect*** device reliability.

DC Voltage Thresholds ($T_A = T_{OPR}$; V = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDV}	End-of-discharge warning	0.87	0.90	0.93	V	SB
V_{SR1}	Discharge compensation threshold	20	50	75	mV	SR (see note)
V_{SR2}	Discharge compensation threshold	70	100	125	mV	SR (see note)
V_{SR3}	Discharge compensation threshold	120	150	175	mV	SR (see note)
V_{SR4}	Discharge compensation threshold	220	253	275	mV	SR (see note)
V_{SRQ}	Valid charge	-	-	-400	µV	$V_{SR} + V_{OS}$
V_{SRD}	Valid discharge	500			µV	$V_{SR} + V_{OS}$
V_{MCV}	Maximum single-cell voltage	1.95	2.0	2.05	V	SB
V_{BR}	Battery removed/replaced		0.1	0.25	V	SB

Note: For proper operation of the threshold detection circuit, V_{CC} must be at least 1.5V greater than the voltage being measured.

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	3.0	4.25	6.5	V	V_{CC} excursion from < 2.0V to ≥ 3.0V initializes the unit.
V_{REF}	Reference at 25°C	5.7	6.0	6.3	V	I_{REF} = 5µA
	Reference at -40°C to +85°C	4.5	-	7.5	V	I_{REF} = 5µA
R_{REF}	Reference input impedance	2.0	5.0	-	MΩ	V_{REF} = 3V
I_{CC}	Normal operation	-	90	135	µA	V_{CC} = 3.0V, DQ = 0
		-	120	180	µA	V_{CC} = 4.25V, DQ = 0
		-	170	250	µA	V_{CC} = 6.5V, DQ = 0
V_{SB}	Battery input	0	-	V_{CC}	V	
R_{SBmax}	SB input impedance	10	-	-	MΩ	0 < V_{SB} < V_{CC}
I_{DISP}	$\overline{DISP}$ input leakage	-	-	5	µA	V_{DISP} = V_{SS}
I_{MODE}	MODE input leakage	-0.2	-	0.2	µA	$\overline{DISP}$ = V_{CC}
I_{RBI}	RBI data-retention current	-	-	100	nA	V_{RBI} > V_{CC} < 3V
R_{DQ}	Internal pulldown	500	-	-	KΩ	
V_{SR}	Sense resistor input	-0.3	-	2.0	V	V_{SR} > V_{SS} = discharge; V_{SR} < V_{SS} = charge
R_{SR}	SR input impedance	10	-	-	MΩ	-200mV < V_{SR} < V_{CC}
V_{IHPFC}	PFC logic input high	V_{CC} - 0.2	-	-	V	PFC
V_{ILPFC}	PFC logic input low	-	-	V_{SS} + 0.2	V	PFC
V_{IZPFC}	PFC logic input Z	float	-	float	V	PFC
I_{IHPFC}	PFC input high current	-	1.2	-	µA	V_{PFC} = V_{CC}/2
I_{ILPFC}	PFC input low current	-	1.2	-	µA	V_{PFC} = V_{CC}/2
V_{OLSL}	SEG_X output low, low V_{CC}	-	0.1	-	V	V_{CC} = 3V, I_{OLS} ≤ 1.75mA SEG_1–SEG_5
V_{OLSH}	SEG_X output low, high V_{CC}	-	0.4	-	V	V_{CC} = 6.5V, I_{OLS} ≤ 11.0mA SEG_1–SEG_5
V_{OHML}	MODE output high, low V_{CC}	V_{CC} - 0.3	-	-	V	V_{CC} = 3V, I_{OHMODE} = -5.25mA
V_{OHMH}	MODE output high, high V_{CC}	V_{CC} - 0.6	-	-	V	V_{CC} = 6.5V, I_{OHMODE} = -33.0mA
I_{OHMODE}	MODE source current	-33	-	-	mA	At V_{OHMODE} = V_{CC} - 0.6V
I_{OLS}	SEG_X sink current	11.0	-	-	mA	At V_{OLSH} = 0.4V, V_{CC} = 6.5V
I_{OL}	Open-drain sink current	5.0	-	-	mA	At V_{OL} = V_{SS} + 0.3V, DQ
V_{OL}	Open-drain output low	-	-	0.5	V	I_{OL} ≤ 5mA, DQ
V_{IHDQ}	DQ input high	2.5	-	-	V	DQ
V_{ILDQ}	DQ input low	-	-	0.8	V	DQ
R_{FLOAT}	Float state external impedance	-	5	-	MΩ	PFC

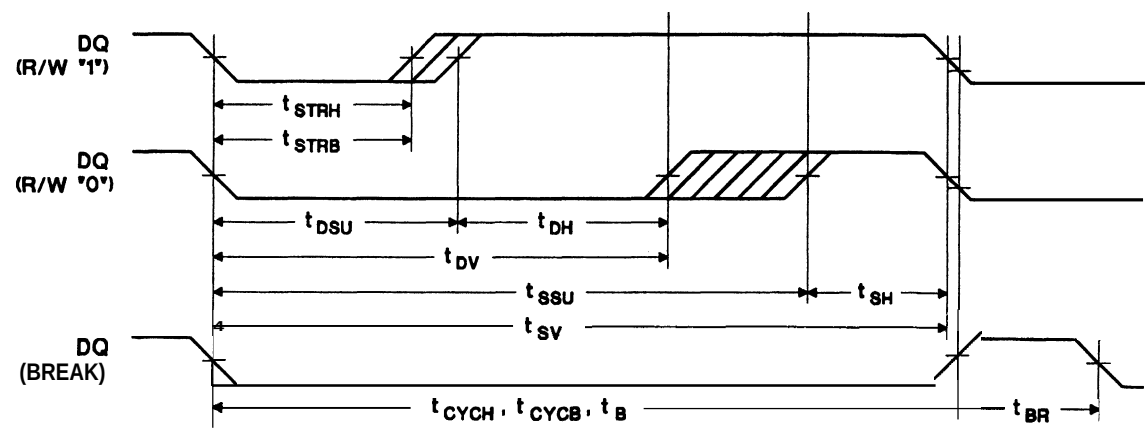
Note: All voltages relative to V_{SS}.

Serial Communication Timing Specification ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYCH}	Cycle time, host to bq2011	3			ma	See note
t_{CYCB}	Cycle time, bq2011 to host	3		6	ma	
t_{STRH}	Start hold, host to bq2011	5			ns	
t_{STRB}	Start hold, bq2011 to host	500			µs	
t_{DSU}	Data setup			750	µs	
t_{DH}	Data hold	750			µs	
t_{DV}	Data valid	1.60			ma	
t_{SSU}	Stop setup			2.26	ma	
t_{SH}	Stop hold	700			µs	
t_{SV}	Stop valid	2.96			ms	
t_B	Break	3			ms	
t_{BR}	Break recovery	1			ma	

Note: The open-drain DQ pin should be pulled to at least V_{CC} by the host system for proper DQ operation DQ *may* be left floating if the serial interface is not used.

Serial Communication Timing Illustration



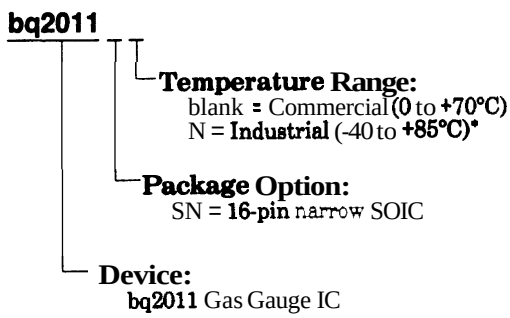
RC-34

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
3	7	Self-discharge count rate	Wae: 1/64 * NAC rate per day Is: 1/80 * NAC rate per day
3	7	Compeneation factor 30–40°C	Was: 0.90 Is: 0.96
3	7	Compensation factor >40°C	Was: 0.80 Is: 0.90
4	7	Charge compensation	(Changedcompensation factor variation with temperature
4	8	Self-discharge compensation	Changed self-discharge compensation rate variation with temperature

Note: Changes 1 and 2 = See the 1995 *Data* Book.
Change 3 = Jan. 1996 C changes from July 1994 C.
Change 4 = Feb. 1996 C changes from Jan. 1996 C.

Ordering Information

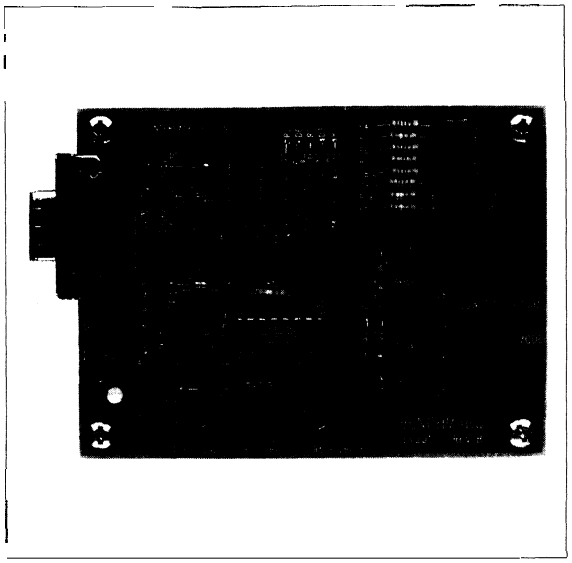


* Contact factory for availability.

bq2011 Evaluation System

Features

- ➤ bq2011 Gas Gauge IC evaluation and development system
- ➤ RS-232 interface hardware for easy access to state-of-charge information via the serial port
- ➤ Alternative terminal block for direct connection to the serial port
- ➤ Battery state-of-charge monitoring for 5- to 10-cell (series) applications (2 user-selectable options for 3, 4, or greater than 10 cells)
- ➤ On-board regulator for greater than 4-cell applications
- ➤ State-of-charge information displayed on bank of 5 LEDs
- ● Nominal capacity jumper-configurable
- ● Display mode jumper-configurable



General Description

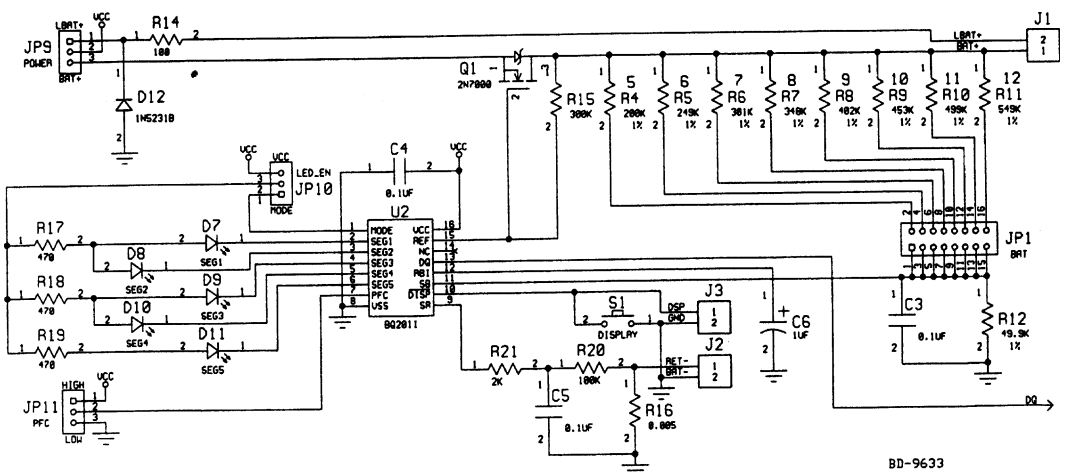
The EV2011 Evaluation System provides a development and evaluation environment for the bq2011 Gas Gauge IC. The EV2011 incorporates a bq2011, a sense resistor, and all other hardware necessary to provide a capacity monitoring function for 3 to 12 series NiCd cells.

Hardware for an RS-232 interface is included on the EV2011 so that easy access to the state-of-charge information can be achieved via the serial port of the bq2011. Direct connection to the serial port of the bq2011 is also made available for check-out of the final hardware1 software implementation.

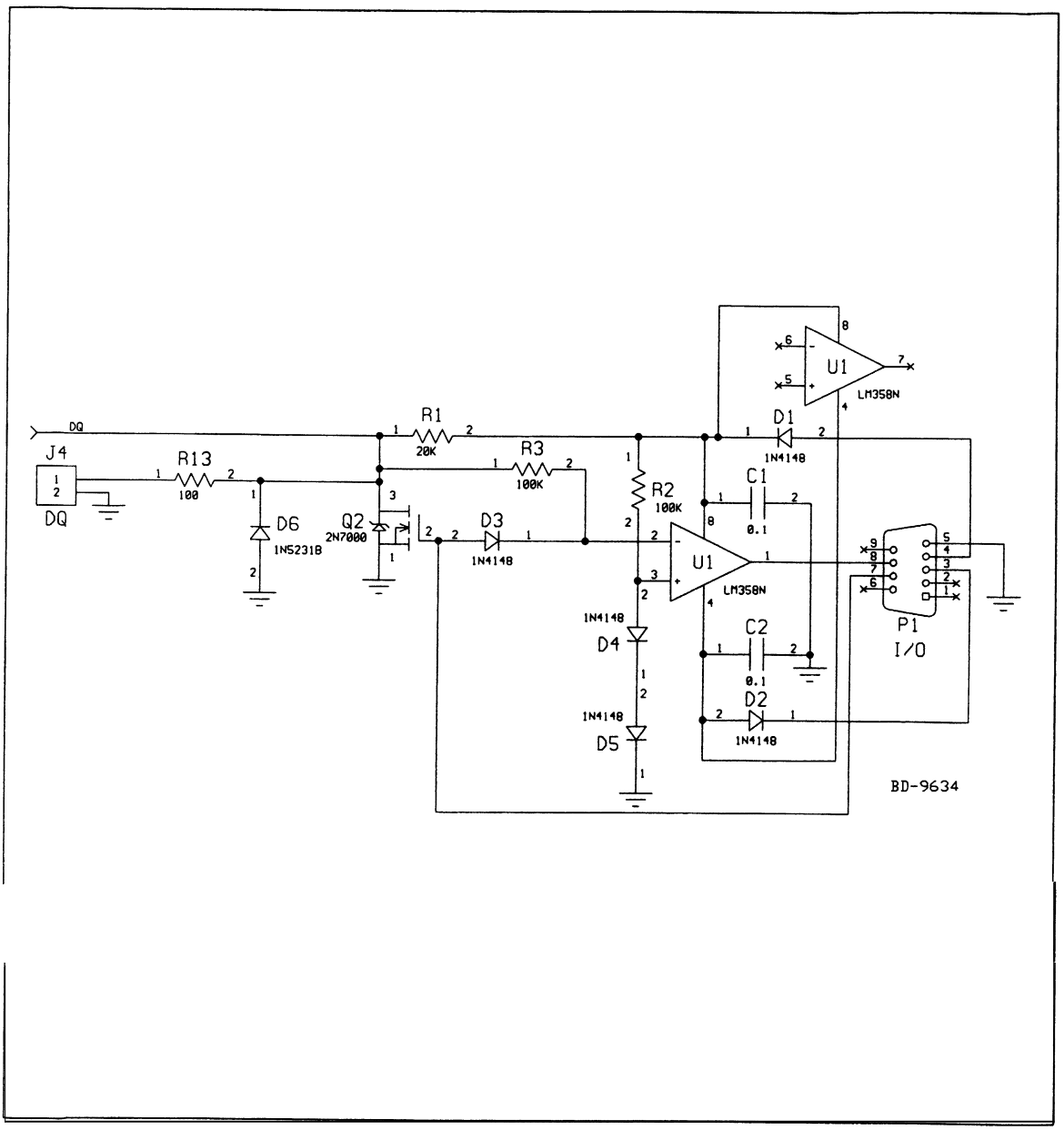
The menu-driven software provided with the EV2011 displays charge/discharge activity and allows user interface to the bq2011 from any standard DOS PC.

A full data sheet for this product is available on our web site (http:llwww.benchmarq.com), or you may contact the factory for one.

EV2011 Board Schematic



EV2011 Board Schematic (Continued)



Notes

BENCHMARQ

bq2011J

Gas Gauge IC

Features

- Conservative and repeatable measurement of available charge in rechargeable batteries
- Designed for portable equipment such as power tools with high discharge rates
- Designed for battery pack integration
  - 120µA typical standby current (self-discharge estimation mode)
  - Small size enables implementations in as little as ½ square inch of PCB
- Direct drive of LEDs for capacity display
- Self-discharge compensation using internal temperature sensor
- Simple single-wire serial communications port for subassembly testing
- 16-pin narrow SOIC

General Description

The bq2011J Gas Gauge IC is intended for battery-pack installation to maintain an accurate record of available battery charge. The IC monitors a voltage drop across a sense resistor connected in series between the negative battery terminal and ground to determine charge and discharge activity of the battery. The bq2011J is designed for systems such as power tools with very high discharge rates.

Battery self-discharge is estimated based on an internal timer and temperature sensor. Compensations for battery temperature and rate of charge or discharge are applied to the charge, discharge, and self-discharge calculations to provide available charge information across a wide range of operating conditions. Initial battery capacity is set using the PROG1-4 and SPFC pins. Actual battery capacity is automatically 'learned' in the course of a discharge cycle from full to empty and may be displayed depending on the display mode.

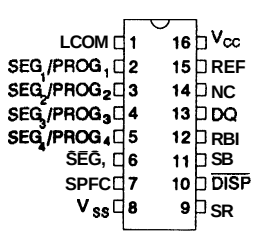
Nominal available charge may be directly indicated using a five-segment LED display. These segments are used to graphically indicate nominal available charge.

The bq2011J supports a simple single-line bidirectional serial link to an external processor (common ground). The bq2011J outputs battery information in response to external commands over the serial link. To support subassembly testing, the outputs may also be controlled by command. The external processor may also overwrite some of the bq2011J gas gauge data registers.

The bq2011J may operate directly from four cells. With the REF output and an external transistor, a simple, inexpensive regulator can be built to provide Vcc from a greater number of cells.

Internal registers include available charge, temperature, capacity, battery ID, and battery status.

Pin Connections



16-Pin Narrow SOIC

PN-W

Pin Names

LCOM	LED common output
$SEG_1/PROG_1$	LED segment 1/ Program 1 input
$SEG_2/PROG_2$	LED segment 2 / Program 2 input
$SEG_3/PROG_3$	LED segment 3/ Program 3 input
$SEG_4/PROG_4$	LED segment 4/ Program 4 input
SEG_5	LED segment 5
SPFC	Programmed full count selection input
REF	Voltage reference output
NC	No connect
DQ	Serial communications input/output
RBI	Register backup input
SB	Battery sense input
$\overline{DISP}$	Display control input
SR	Sense resistor input
Vcc	3.0-6.5V
Vss	Negative battery terminal

Pin Descriptions

LCOM **LED common**

Open-drain output switches Vcc to source current for the LEDs. The switch is off during initialization to allow reading of $PROG_{1-4}$ pull-up or pull-down program resistors. LCOM is high impedance when the display is off.

SEG_1-SEG_5 LED display segment outputs

Each output may activate an LED to sink the current sourced from MODE, the battery, or Vcc.

$PROG_1$-$PROG_4$ Programmed full count selection inputs (dual function with SEG_1 - SEG_4)

These three-level input pins define the programmed full count (PFC) in conjunction with SPFC pin, define the display mode and enable or disable self-discharge.

SPFC **Programmed** full count selection input

This three-level input pin along with $PROG_{1-3}$ define the programmed full count (PFC) thresholds and scale selections described in Table 1 and Table 2. The state of the SPFC pin is only read immediately after a reset condition.

SR **Sense** resistor input

The voltage drop (V_{SR}) across the sense resistor R_S is monitored and integrated over time to interpret charge and discharge activity. The SR input is tied to the low side of the sense resistor and battery pack ground (see Figure 1. $V_{SR} > V_{SS}$ indicates discharge, and $V_{SR} < V_{SS}$ indicates charge. The effective voltage drop, V_{SRO}, as seen by the bq2011J is $V_{SR} + V_{OS}$ (see Table 4).

NC **No connect**

$\overline{DISP}$ Display control input

$\overline{DISP}$ floating allows the LED display to be active during charge and discharge if $V_{SRO} < -1mV$ (charge) or $V_{SRO} > 2mV$ (discharge). Transitioning $\overline{DISP}$ low activates the display for 4 ± 0.5 seconds.

SB **Secondary battery** input

This input monitors the single-cell voltage potential through a high-impedance resistive divider network for the end-of-discharge voltage (EDV) threshold and maximum cell voltage (MCV).

RBI Register backup input

This input is used to provide backup potential to the bq2011J registers during periods when $V_{CC} \leq 3V$. A storage capacitor should be connected to RBI.

DQ **Serial I/O pin**

This is an open-drain bidirectional pin.

REF Voltage reference output for regulator

REF provides a voltage reference output for an optional micro-regulator.

Vcc Supply voltage input

Vss Ground

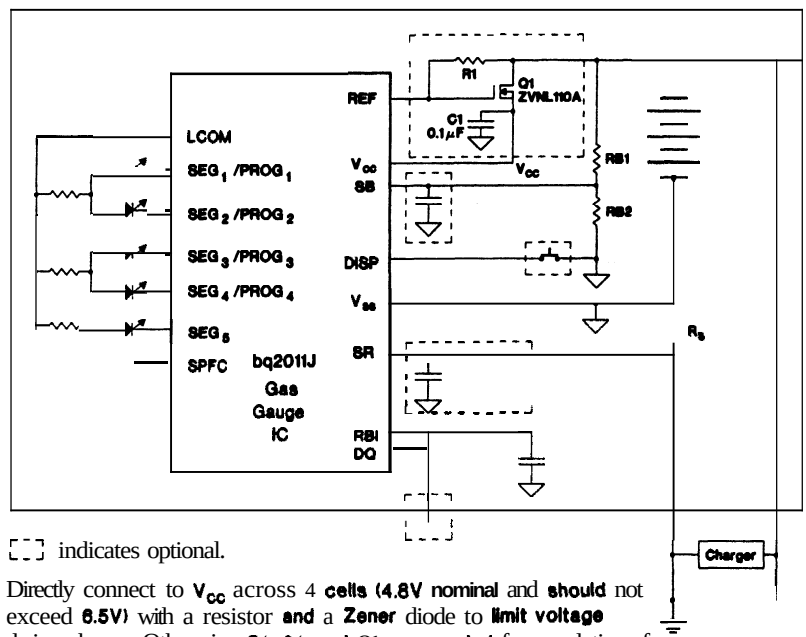
Functional Description

General Operation

The bq2011J determines battery capacity by monitoring the amount of charge input to or removed from a rechargeable battery. The bq2011J measures discharge and charge currents, estimates self-discharge, monitors the battery for low-battery voltage thresholds, and compensates for temperature and charge/discharge rates. The charge measurement is made by monitoring the voltage across a small-value series sense resistor between the negative battery terminal and ground. The available battery *charge* is determined by monitoring this voltage over time and correcting the measurement for the environmental and operating conditions.

Figure 1 shows a typical battery pack application of the bq2011J using the LED display with absolute mode as a charge-state indicator. The bq2011J can be configured to display capacity in either a relative or an absolute display mode. The relative display mode uses the last measured discharge capacity of the battery as the battery "full" reference. The absolute display mode uses the programmed full count (PFC) as the full reference, forcing each segment of the display to represent a fixed amount of charge. A push-button display feature is available for momentarily enabling the LED display.

The bq2011J monitors the charge and discharge currents as a voltage across a sense resistor (see R_S in Figure 1). A filter between the negative battery terminal and the SR pin may be required if the rate of change of the battery current is too great.



[ ] indicates optional.

Directly connect to V_{CC} across 4 cells (4.8V nominal and should not exceed 6.5V) with a resistor and a Zener diode to limit voltage during charge. Otherwise, R1, C1, and Q1 are needed for regulation of > 4 cells.

Programming resistor and ESD-protection diodes are not shown.

R-C on SR may be required (application specific), where the maximum R should not exceed 20K.

SD-006

Figure 1. Battery Pack Application Diagram—LED Display, Absolute Mode

Register Backup

The bq2011J RBI input pin is intended to be used with a storage capacitor to provide backup potential to the internal bq2011J registers when V_{CC} momentarily drops below 3.0V. V_{CC} is output on RBI when V_{CC} is above 3.0V.

After V_{CC} rises above 3.0V, the bq2011J checks the internal registers for data loss or corruption. If data has changed, then the NAC and FULCNT registers are cleared, and the LMD register is loaded with the initial PFC.

Voltage Thresholds

In conjunction with monitoring V_{SR} for charge/discharge currents, the bq2011J monitors the single-cell battery potential through the SB pin. The single-cell voltage potential is determined through a resistor-divider network per the following equation:

$$\frac{RB_1}{RB_2} = N - 1$$

where N is the number of cells, RB_1 is connected to the positive battery terminal, and RB_2 is connected to the negative battery terminal. The single-cell battery voltage is monitored for the end-of-discharge voltage (EDV) and for maximum cell voltage (MCV). The EDV threshold level is used to determine when the battery has reached an 'empty" state, and the MCV threshold is used for fault detection during charging. The EDV and MCV thresholds for the bq2011J are fixed at:

$$V_{EDV} = 0.90V$$
$$V_{MCV} = 2.00V$$

EDV detection is disabled if the discharge is at a rate equivalent to or greater than 6C (OVLD flag = 1) EDV detection is re-enabled approximately one second after the discharge falls below a rate equivalent to less than 6C (OVLD flag = 0).

Reset

The bq2011J recognizes a valid battery whenever V_{SB} is greater than 0.1V typical. V_{SB} rising from below 0.25V resets the device. Reset can also be accomplished with a command over the serial port as described in the Reset Register section.

Temperature

The bq2011J internally determines the temperature in 10°C steps centered from -35°C to +85°C. The temperature steps are used to adapt charge and discharge rate compensations, self-discharge counting, and available charge display translation. The temperature range is available over the serial port in 10°C increments as shown in the following chart:

TMPGG (hex)	Temperature Range
0x	< -30°C
1x	-30°C to -20°C
2x	-20°C to -10°C
3x	-10°C to 0°C
4x	0°C to 10°C
5x	10°C to 20°C
6x	20°C to 30°C
7x	30°C to 40°C
8x	40°C to 50°C
9x	50°C to 60°C
Ax	60°C to 70°C
Bx	70°C to 80°C
Cx	> 80°C

Layout Considerations

The bq2011J measures the voltage differential between the SR and V_{SS} pins. V_{OS} (the offset voltage at the SR pin) is greatly affected by PC board layout. For optimal results, the PC board layout should follow the strict rule of a Single-point ground return. Sharing high-current ground with small signal ground causes undesirable noise on the small signal nodes. Additionally:

- The capacitors (SB and V_{CC}) should be placed as close as possible to the SB and V_{CC} pins, respectively, and their paths to V_{SS} should be as short as possible. A high-quality ceramic capacitor of 0.1µf is recommended for V_{CC}.
- The sense resistor (R_S) should be as close as possible to the bq2011J.
- The R-C on the SR pin should be located as close as possible to the SR pin. The maximum R should not exceed 20K.

Gas Gauge Operation

The operational overview diagram in Figure 2 illustrates the operation of the bq2011J. The bq2011J accumulates a measure of charge and discharge currents, as well as an estimation of self-discharge. Charge and discharge currents are temperature and rate compensated, whereas self-discharge is only temperature compensated.

The main counter, Nominal Available Charge (NAC), represents the available battery capacity at any given time. Battery charging increments the NAC register, while battery-&&&ging and self-discharge decrement

the NAC register and increment the DCR (Discharge Count Register).

The Discharge Count Register (DCR) is used to update the Last Measured Discharge (LMD) register only if a complete battery discharge from full to empty occurs without any partial battery charges. Therefore, the bq2011J adapts its capacity determination based on the actual conditions of discharge.

The battery's initial capacity is equal to the Programmed Full Count (PFC) shown in Table 1. Until LMD is updated, NAC counts up to but not beyond this threshold during subsequent charges. This approach allows the gas gauge to be charger-independent and compatiile with any type of charge regime.

1. Last Measured Discharge (LMD) or learned battery capacity:

   LMD is the last measured discharge capacity of the battery. On initialization (application of Vcc or battery replacement), LMD = PFC. During subsequent discharges, the LMD is updated with the latest measured capacity in the Discharge Count Register (DCR) representing a discharge from full to below EDV. A qualified discharge ie necessary for a capacity transfer from the DCR to the LMD register. The LMD also serves as the 100% reference threshold used by the relative display mode.

2. Programmed Full Count (PFC) or initial battery capacity:

   The initial LMD and gas gauge rate values are programmed by using PFC. The PFC also provides the 100% reference for the absolute display mode. The bq2011J is configured for a given application by selecting a PFC value from Table 1. The correct PFC may be determined by multiplying the rated battery capacity in mAh by the sense resistor value:

   Battery capacity (mAh) • sense resistor (Ω) =

   PFC (mVh)

   Selecting a PFC slightly less than the rated capacity for absolute mode provides capacity above the full reference for much of the battery's life.

Example: Selecting a PFC Value

Given:

Sense resistor = 0.002Ω
Number of cells = 6
Capacity = 1800mAh, NiCd cells
Current range = 1A to 80A
Relative display mode
self-discharge = 0.2%/80
Voltage drop across sense resistor = 2mV to 160mV

Therefore:

1800mAh • 0.002Ω = 3.6mVh

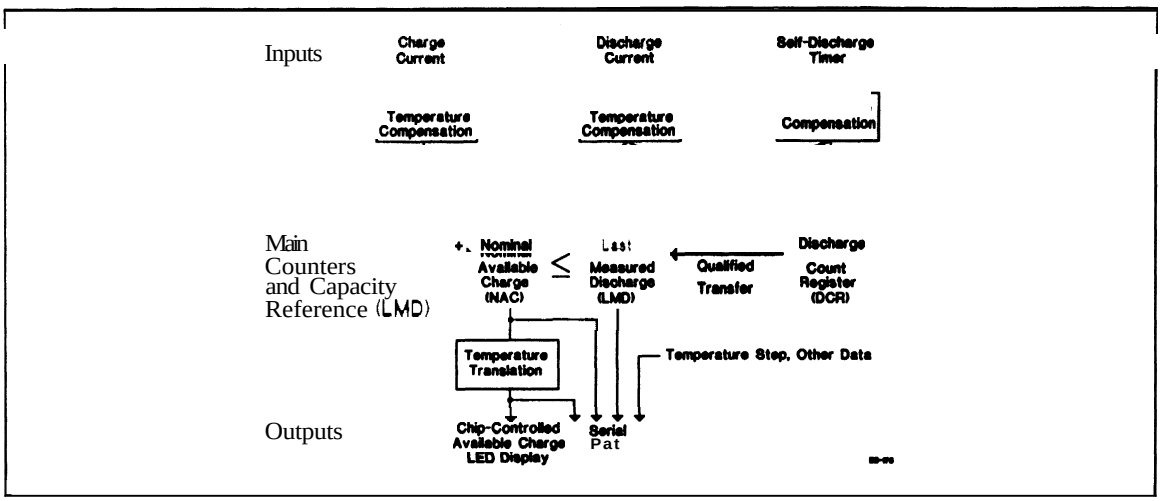


Figure 2. Operational Overview

Select:

PFC = 35840 counts or 3.39mVh
SPFC = Z (float)
PROG1, PROG2 = H or Z
PROG3 = L
PROG4 = H or Z

The initial full battery capacity ie 3.39mVh (1695mAh) until the bq2011J "learns" a new capacity with a qualified discharge from full to EDV.

3. **Nominal Available Charge (NAC):**

NAC counts up during charge to a maximum value of LMD and down during discharge and self discharge to 0. NAC is reset to 0 on initialization and on the first valid charge following discharge to EDV. To prevent overstatement of charge during periods of overcharge, NAC stops incrementing when NAC = LMD.

Note: NAC is set to the value in LMD when $PROG_4$ is pulled low during a reset.

Table 1. bq2011J Programmed Full Count mVh Selections

Programmed Full Count (PFC)	mVh	Scale	Display Mode	SPFC	$PROG_1$	$PROG_2$	$PROG_3$
40192	3.81	1/10560	Absolute	H	H or Z	H or Z	H or Z
32256	3.05	1/10560		Z	H or Z	H or Z	H or Z
28928	2.74	1/10560		L	H or Z	H or Z	H or Z
25856	2.45	1/10560		H	L	H or Z	H or Z
35840	3.39	1/10560		Z	L	H or Z	H or Z
23296	2.21	1/10560		L	L	H or Z	H or Z
40192	3.81	1/10560	Relative	H	H or Z	L	H or Z
32256	3.05	1/10560		Z	H or Z	L	H or Z
28928	2.74	1/10560		L	H or Z	L	H or Z
25856	2.45	1/10560		H	H or Z	H or Z	L
35840	3.39	1/10560		Z	H or Z	H or Z	L
23296	2.21	1/10560		L	H or Z	H or Z	L

Table 2. Programmed Self-Discharge

$PROG_4$	NAC Reset Value	Self-Discharge
H or Z	NAC = 0	Enabled
L	NAC = PFC	Disabled

4. Discharge Count Register (DCR):

The DCR counts up during discharge independent of NAC and could continue increasing after NAC has decremented to 0. Prior to NAC = 0 (empty battery), both discharge and self-discharge increment the DCR. After NAC = 0, only discharge increments the DCR. The DCR resets to 0 when NAC = LMD. The DCR does not roll over but stops counting when it reaches FFFFh.

The DCR value becomes the new LMD value on the first charge after a valid discharge to VEDV if:

No valid charge initiations (charges greater than 256 NAC counts; or 0.006 – 0.01C) occurred during the period between NAC = LMD and EDV detected.

The self-discharge count is not more than 4096 counts (8% to 18% of PFC, specific percentage threshold determined by PFC).

The temperature is ≥ 0°C when the EDV level is reached during discharge.

The valid discharge flag (VDQ) indicates whether the present discharge is valid for LMD update.

Charge Counting

Charge activity is detected based on a negative voltage on the V_{SR} input. If charge activity is detected, the bq2011J increments NAC at a rate proportional to V_{SRO} (V_{SR} + Vos) and, if enabled, activates an LED display if V_{SRO} < -1mV. Charge actions increment the NAC after compensation for charge rate and temperature.

The bq2011J determines a valid charge activity sustained at a continuous rate equivalent to V_{SRO} < -400µV. A valid charge equates to a sustained charge activity greater than 256 NAC counts. Once a valid charge is detected, charge counting continues until V_{SRO} rises above -400µV.

Discharge Counting

All discharge counts where V_{SRO} > 500µV cause the NAC register to decrement and the DCR to increment. Exceeding the fast discharge threshold (FDQ) if the rate is equivalent to V_{SRO} > 2mV activates the display, if enabled. The display becomes inactive after V_{SRO} falls below 2mV.

Self-Discharge Estimation

The bq2011J continuously decrements NAC and increments DCR for self-discharge based on time and temperature. The self-discharge count rate is programmed to be a nominal 1/80 • NAC rate per day or disabled per Table 2. This is the rate for a battery whose temperature is between 20°–30°C. The NAC register cannot not be decremented below 0.

Count Compensations

The bq2011J determines fast charge when the NAC updates at a rate of ≥2 counts/sec. Charge and discharge activity is compeneated for temperature and charge/discharge rate before updating the NAC and/or DCR. Self-discharge estimation ie compensated for temperature before updating the NAC or DCR.

Charge Compensation

Two charge efficiency factors are used for trickle charge and fast charge. Fast charge is defined as a rate of charge resulting in ≥ 2 NAC counts/sec (≥ 0.15C to 0.32C depending on PFC selections; see Table 1). The compensation defaults to the fast charge factor until the actual charge rate is determined.

Temperature adapts the charge rate compensation factors over three ranges between nominal, warm, and hot temperatures. The compensation factors are shown below.

Charge Temperature	Trickle Charge Compensation	Fast Charge Compensation
<30°C	0.80	0.95
30–40°C	0.75	0.90
> 40°C	0.65	0.80

Discharge Compensation

Corrections for the rate of discharge are made by adjusting an internal compensation factor. This factor is based upon the number of NAC counts per second. The actual "C" rate may be calculated by using the following formula:

$$C_{RATE} = \frac{K}{N * LMD}$$

where:

K = 66,000

N = Number of samples

LMD = Contents of address 05h

The compensation factors during discharge are:

Samples	Discharge Compensation Factor	Effective CRATE LMD = 9Dh
N > 70	1.00	CRATE < 6.0C
70 ≥ N > 35	1.05	6 . N ≤ CRATE < 12.0C
35 ≥ N > 23	1.15	12.0C ≤ CRATE < 18.0C
N ≤ 23	1.25	CRATE ≥ 18.0C

Temperature compensation during discharge also takes place. At lower temperatures, the compensation factor increases by 0.05 for each 10°C temperature step below 10°C.

$$\text{Comp. factor} = 1.00 + (0.05 \cdot N)$$

Where N = number of 10°C steps below 10°C and CRATE < 6.0C.

For example:

T > 10°C: Nominal compensation, N = 0

0°C < T < 10°C: N = 1 (i.e., 1.00 becomes 1.05)

-10°C < T < 0°C: N = 2 (i.e., 1.00 becomes 1.10)

-20°C < T < -10°C: N = 3 (i.e., 1.00 becomes 1.15)

-20°C < T < -30°C: N = 4 (i.e., 1.00 becomes 1.20)

Self-Discharge Compensation

The self-discharge compensation is programmed for a nominal rate of 1/80 • NAC per day or disabled. This is the rate for a battery within the 20–30°C temperature range (TMPGG = 6x). This rate varies across 8 ranges from <10°C to >70°C, doubling with each higher temperature step (10°C). See Table 3.

Table 3. Self-Discharge Compensation

Temperature Range	Self-Discharge Compensation Typical Rate/Day
< 10°C	NAC/320
10–20°C	NAC/160
20–30°C	NAC/80
30–40°C	NAC/40
40–50°C	NAC/20
50–60°C	NAC/10
60–70°C	NAC/5
> 70°C	NAC/2.5

Error Summary

Capacity Inaccurate

The LMD is susceptible to error on initialization or if no updates occur. On initialization, the LMD value includes the error between the programmed full capacity and the actual capacity. This error is present until a valid discharge occurs and LMD is updated (see "4. Discharge Count Register" on the previous page). The other cause of LMD error is battery wear-out. As the battery ages, the measured capacity must be adjusted to account for changes in actual battery capacity.

A Capacity Inaccurate counter (CPI) is maintained and incremented each time a valid charge occurs and is reset whenever LMD is updated from the DCR. The counter does not wrap around but stops counting at 255. The capacity inaccurate flag (CI) is set if LMD has not been updated following 64 valid charges.

Current-Sensing Error

Table 3 illustrates the current-sensing error as a function of V_{SR}. A digital filter eliminates charge and discharge counts to the NAC register when V_{SRO} (V_{SR} + V_{OS}) is between -400µV and 500µV.

Table 4. bq2011J Current-Sensing Errors

Symbol	Parameter	Typical	Maximum	Units	Notes
V_{OS}	Offset referred to V_{SR}	± 50	± 150	µV	$\overline{DISP}$ = V_{CC}.
INL	Integrated non-linearity error	± 2	± 4	%	Add 0.1% per °C above or below 25°C and 1% per volt above or below 4.25V.
INR	Integrated non-repeatability error	± 1	± 2	%	Measurement repeatability given similar operating conditions.

Communicating With the bq2011J

The bq2011J includes a simple single-pin (DQ plue return) serial data interface. A hoet processor uses the interface to access various bq2011J registers. Battery characteristics may be easily monitored by adding a single contact to the battery pack. The open-drain DQ pin on the bq2011J should be pulled up by the host system, or may be left floating if the interface is not used.

The interface uses a command-baaed protocol, where the host processor sends a command byte to the bq2011J. The command directs the bq2011J to either store the next eight bits of data received to a register specified by the command byte or output the eight bits of data specified by the command byte.

The communication protocol is asynchronous return-to-one. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 333 bits/sec. The least-significant bit of a command or data byte is transmitted first. The protocol is simple enough that it can be implemented by most host processors using either polled or interrupt processing. Data input from the bq2011J may be sampled using the pulse-width capture timers available on some microcontrollers.

Communication is normally initiated by the host processor sending a BREAK command to the bq2011J. A BREAK is detected when the DQ pin is driven to a logic-law state for a time, t_B or greater. The DQ pin should then be returned to ita normal ready-high logic state for a time, t_{BR}. The bq2011J is now ready to receive a command from the host processor.

The return-to-one data bit frame consists of three distinct sections. The first section is used to start the transmission by either the host or the bq2011J taking the DQ pin to a logic low state for a period, $t_{STRH,B}$. The next section is the actual data transmission, where the data shculd be valid by a period, t_{DSU}, after the negative edge used to start communication. The data should be held for a period, t_{DV}, to allow the host or bq2011J to sample the data bit.

The final section is used to stop the transmission by returning the DQ pin to a logic-high state by at least a period, t_{SSU}, after the negative edge used to start communication. The final logic-high state should be held until a period, t_{SV}, to allow time to ensure that the bit transmission was stopped properly. The timings for data and break communication are given in the serial communication timing specification and illustration sections.

Communication with the bq2011J is always performed with the least-si cant bit being transmitted first. Figure 3 shows an example of a communication sequence to read the bq2011J NAC register.

bq2011J Registers

The bq2011J command and status registers are listed in Table 5 and described below.

Command Register (CMDR)

The write-only CMDR register is accessed when eight valid command bits have been received by the bq2011J. The CMDR register contains two fields:

- W/$\overline{R}$ bit
- Command address

The W/$\overline{R}$ bit of the command register is used to select whether the received command is for a read or a write function.

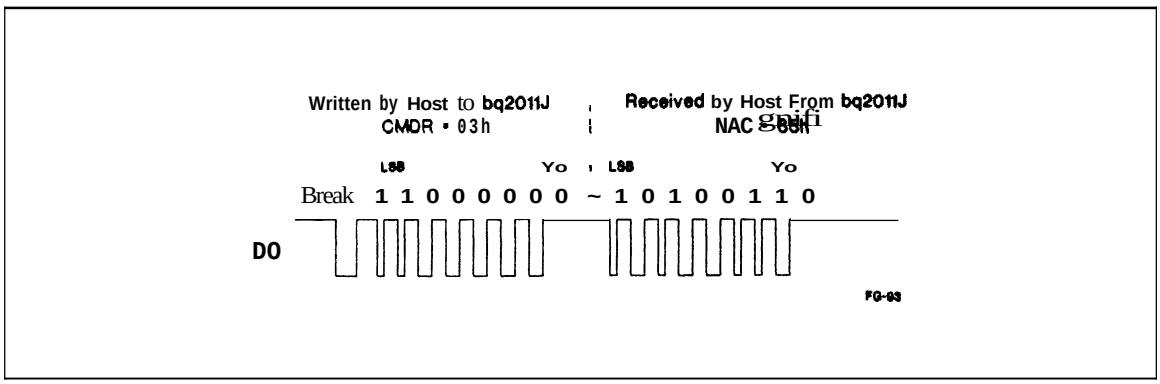


Figure 3. Typical Communication With the bq2011J

Table 5. bq2011J Command and Status Registers

Symbol	Register Name	Loc. (hex)	Read/ Write	Control Field							
				7(MSB)	6	5	4	3	2	1	0(LSB)
CMDR	Command register	00h	Write	W/$\overline{R}$	AD6	AD5	AD4	AD3	AD2	AD1	AD0
FLGS1	Primary status flags register	Olh	Read	CHGS	BRP	MCV	CI	VDQ	n/u	EDV	n/u
TMPGG	Temperature and gas gauge register	02h	Read	TMP3	TMP2	TMP1	TMP0	GG3	GG2	GG1	GG0
NACH	Nominal available charge high byte register	03h	R/W	NACH7	NACH6	NACH5	NACH4	NACH3	NACH2	NACH1	NACHO
NACL	Nominal available charge low byte register	17h	Read	NACL7	NACL6	NACL5	NACL4	NACL3	NACL2	NACL1	NACL0
BATID	Battery identification register	04h	R/W	BATID7	BATID6	BATID5	BATID4	BATID3	BATID2	BATID1	BATID0
LMD	Last measured discharge register	05h	R/W	LMD7	LMD6	LMD5	LMD4	LMD3	LMD2	LMD1	LMD0
FLGS2	Secondary status flags register	06h	Read	CR	DR2	DR1	DR0	n/u	n/u	n/u	OVLD
CPI	Capacity inaccurate count register	09h	Read	CPI7	CPI6	CPI5	CP14	CPI3	CPI2	CPI1	CPIO
OCTL	Output control register	Oah	Write	1	OC5	OC4	0C3	OC2	OC1	n/u	OCE
FULCNT	Full count register	Obh	Read	FUL7	FUL6	FUL5	FUL4	FUL3	FUL2	FUL1	FUL0
RST	Reset register	39h	Write	RST	0	0	0	0	0	0	0

Note: n/u = not used

The W/$\overline{R}$ values are:

CMDR Bits							
7	6	5	4	3	2	1	0
W/$\overline{R}$	-	-	-	-	-	-	-

Where W/$\overline{R}$ is:

0 The bq2011J outputs the requested register contents specified by the address portion of CMDR

1 The following eight bits should be written to the register specified by the address portion of CMDR.

The lower seven-bit field of CMDR contains the address portion of the register to be accessed. Attempts to write to invalid addresses are ignored.

CMDR Bits							
7	6	5	4	3	2	1	0
-	AD6	AD5	AD4	AD3	AD2	AD1	AD0 (LSB)

Primary Status Flags Register (FLGS1)

The read-only FLGS1 register (address=01h) contains the primary bq2011J flags.

The *charge status* flag (CHGS) is asserted when a valid charge rate is detected. Charge rate is deemed valid when V_{SRO} < -400µV. A V_{SRO} of greater than- 400µV or discharge activity clears CHGS.

The CHGS values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
CHGS	-	-	-	-	-	-	-

Where CHGS is:

0 Either discharge activity detected or V_{SRO} > -400µV

1 V_{SRO} < -400µV

The *battery replaced* flag (BRP) is asserted whenever the potential on the SB pin (relative to V_{SS}), V_{SB}, rises above 0.1V and determines the internal registers have been corrupted. The BRP flag is also set when the bq2011J is reset (see the RST register description). BRP is cleared if either the bq2011J is charged until NAC = LMD or discharged until EDV is reached. BRP = 1 signifies that the device has been reset.

The BRP values are:

FLGSI Bib							
7	6	5	4	3	2	1	0
-	BRP	-	-	-	-	-	-

Where BRP is:

0 bq2011J is charged until NAC = LMD or discharged until the EDV flag is asserted

1 SB rising from below 0.1V, or a serial port initiated reset has occurred

The *maximum* cell voltage flag (MCV) in asserted whenever the potential on the SB pin (relative to V_{SS}) is above 2.0V. The MCV flag is asserted until the condition causing MCV is removed.

The MCV values are:

FLGSI Bits							
7	6	5	4	3	2	1	0
-	-	MCV	-	-	-	-	-

Where MCV is:

0 V_{SB} < 2.0V

1 V_{SB} > 2.0V

The *capacity inaccurate* flag (CI) is used to warn the user that the battery has been *charged* a substantial number of times since LMD has been updated. The CI flag is asserted on the 64th charge after the last LMD update or when the bq2011J is reset. The flag is cleared after an LMD update.

The CI values are:

FLGSI Bits							
7	6	5	4	3	2	1	0
-	-	-	CI	-	-	-	-

Where CI is:

0 When LMD is updated with a valid full discharge

1 After the 64th valid charge action with no LMD updates or the bq2011J is reset

The ***valid discharge*** flag (VDQ) is asserted when the bq2011J is discharged from NAC=LMD. The flag remains set until either LMD is updated or one of three actions that can clear VDQ occurs:

- The self-discharge count register (SDCR) has exceeded the maximum acceptable value (4096 counts) for an LMD update.
- A valid charge action equal to 256 NAC counts with $V_{SRO} < -400\mu V$.
- The EDV flag was set at a temperature below 0°C

The VDQ values are:

FLGSI Bits							
7	6	5	4	3	2	1	0
-	-	-	-	VDQ	-	-	-

Where VDQ is:

0 SDCR ≥ 4096, subsequent valid charge action detected, or EDV is asserted with the temperature less than 0°C

1 On first discharge after NAC = LMD

The ***end-of-discharge warning*** flag (EDV) warns the user that the battery is empty. SEG1 blinks at a 4Hz rate. EDV detection is disabled if OVLD = 1. The EDV flag is latched until a valid charge has been detected.

The EDV values are:

FLGSI Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	EDV	-

Where EDV is:

0 Valid charge action detected and $V_{SB} \geq 0.90V$

1 $V_{SB} < 0.90V$ providing that OVLD = 0

Temperature and Gas Gauge Register (TMPGG)

The read-only TMPGG register (address=02h) contains two data fields. The first field contains the battery temperature, The second field contains the available charge from the battery.

TMPGG Temperature Bits							
					2	1	0
TMP3	TMP2	TMP1	TMP0	-	-	-	

The bq2011J contains an internal temperature sensor. The temperature is wed to set charge and discharge efficiency factors as well as to adjust the self-discharge codficient. The temperature register contents may be translated as shown below.

TMP3	TMP2	TMP1	TMP0	Temperature
0	0	0	0	T < -30°C
0	0	0	1	-30°C < T < -20°C
0	0	1	0	-20°C < T < -10°C
0	0	1	1	-10°C < T < 0°C
0	1	0	0	0°C < T < 10°C
0	1	0	1	10°C < T < 20°C
0	1	1	0	20°C < T < 30°C
0	1	1	1	30°C < T < 40°C
1	0	0	0	40°C < T < 50°C
1	0	0	1	50°C < T < 60°C
1	0	1	0	60°C < T < 70°C
1	0	1	1	70°C < T < 80°C
1	1	0	0	T > 80°C

The bq2011J calculates the available charge as a function of NAC, temperature, and a full reference, either LMD or PFC. The results of the calculation are available via the diiplay port or the gas gauge field of the TMPGG register. The register is used to give available capacity in 1/16 increments from 0 to 15/16.

TMPGG Gas Gauge Bits							
7	6	5	4	3	2	1	0
-	-	-	-	GG3	GG2	GG1	GG0

The gas gauge display and the gas gauge portion of the TMPGG register are adjusted for cold temperature dependencies. A piece-wise correction is performed as follows:

Temperature	Available Capacity Calculation
> 0°C	NAC / "Full Reference"
-20°C < T < 0°C	0.75 • NAC / "Full Reference"
< -20°C	0.5 • NAC / "Full Reference"

The adjustment between > 0°C and -20°C < T < 0°C has a 4°C hysteresis.

Nominal Available Charge Register (NAC)

The read/write NACH register (address=03h) and the read-only NACL register (address=17h) are the main gas gauging registers for the bq2011J. The NAC registers are incremented during charge actions and decremented during discharge and self-discharge actions. The correction factors for charge/discharge efficiency are applied automatically to NAC.

If SEG6 = 0 on reset, then NACH = PFC and NACL = 0. If SEG6 = Z or H, the NACH and NACL registers are cleared to zero, NACL stops counting when NACL reaches zero. When the bq2011J detects a valid charge, NACL resets to zero; *writing to the* NAC *register affects the available charge counts and,* therefore, *affects the bq2011J gas gauge operation.*

Battery Identification Register (BATID)

The read/write BATID regieter (address=04h) is available for use by the system to determine the type of battery pack. The BATID contents are retained as long as V_{CC} is greater than 2V. The contents of BATID have no effect on the operation of the bq2011J. There is no default setting for this register.

Last Measured Discharge Register (LMD)

LMD is a read/write register (address=05h) that the bq2011J uses as a measured full reference. The bq2011J adjusts LMD based on the measured discharge capacity of the battery from full to empty. In this way the bq2011J updates the capacity of the battery. LMD is set to PFC during a bq2011J reset.

Secondary Status Flags Register (FLGS2)

The read-only FLGS2 register (address=06h) contains the secondary bq2011J flags.

The charge *rate* flag (CR) is used to denote the fast charge regime. Fast charge is assumed whenever a charge action is initiated. The CR flag remains asserted if the charge rate does not fall below 2 counts/sec.

The CR values are:

FLGS2 Bits							
7	6	5	4	3	2	1	0
CR	-	-	-	-	-	-	-

Where CR is:

0 When charge rate falls below 2 counts/sec

1 When charge rate is above 2 counts/sec

The fast charge regime efficiency factors are wed when CR = 1. When CR = 0, the trickle charge efficiency factors are used. The time to change CR varies due to the user-selectable count rates.

The *discharge rate* flags, DR2–0, are bits 6–4.

FLGS2 Bib							
7	6	5	4	3	2	1	0
-	DR2	DR1	DR0	-			

They are used to determine the present discharge regime as follows:

DR2	DR1	DRO	C_{RATE} @LMD = 90h
0	0	0	C_{RATE} < 6C
0	0	1	6C ≤ C_{RATE} < 12C
0	1	0	12C ≤ C_{RATE} < 18C
0	1	1	C_{RATE} ≥ 18C

The *overload* flag (OVLD) is asserted when a discharge overload is detected, C_{RATE} ≥ 6.0C for LMD = 90h (see Discharge Compensation, page 8). OVLD remains asserted as long as the condition is valid.

FLGS2 Bib							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	OVLD

Full Count Register (FULCNT)

The read-only FULCNT register (address=0bh) provides the system with a diagnostic of the number of times the battery has been fully charged (NAC = LMD). The number of full occurrences can be determined by multiplying the value in the FULCNT register by 16. Any discharge action

other than self-discharge allows detection of another full occurrence during the next valid charge action.

Capacity Inaccurate Count Register (CPI)

The read-only CPI register (address=09h) is used to indicate the number of times a battery has been charged without an LMD update. Because the capacity of a rechargeable battery varies with age and operating conditions, the bq2011J adapts to the changing capacity over time. A complete discharge from full (NAC=LMD) to empty (EDV=1) is required to perform an LMD update assuming there have been no intervening valid charges, the temperature is greater than or equal to 0°C, and the self-discharge counter is less than 4096 counts.

The CPI register is incremented every time a valid charge is detected. The register increments to 255 without rolling over. When the contents of CPI are incremented to 64, the capacity inaccurate flag, CI, is asserted in the FLGS1 register. CPI is reset whenever an update of the LMD register is performed, and the CI flag is also cleared.

Output Control Register (OCTL)

The write-only OCTL register (address=0ah) provides the system with a means to check the display connections for the bq2011J. The segment drivers may be overwritten by data from OCTL when the least-significant bit of OCTL, OCE, is set. The data in bite OC_{5-1} of the OCTL register (see Table 5 on page 10 for details) is output onto the segment pine, SEG_{5-1}, respectively if OCE=1. *Whenever OCE is written to 1, the MSB of OCTL should be set to a 1.* The OCE register location must be cleared to return the bq2011J to normal operation. OCE may be cleared by either writing the bit to a logic zero via the aerial port or by resetting the bq2011J as explained below. Note Whenever the OCTL register is written, the MSB of OCTL should be written to a logic one.

Reset Register (RST)

The reset regieter (address=39h) provides the means to perform a software-controlled reset of the device. A full device reset may be accomplished by first writing LMD (address = 05h) to 00h and then writing the RST register contents from 00h to 80h. *Setting any bit other than the most-significant bit of the RST register is not allowed, and results in improper operation of the bq2011J.*

Resetting the bq2011J sets the following:

- LMD = PFC
- CPI, VDQ, OCE, and NAC = 0
  (NAC = PFC when $PROG_4$ = L)
- CI and BRP = 1

Display

The bq2011J can directly display capacity information using low-power LEDs. If LEDs are used, the segment pins should be tied to Vcc, the battery, or the MODE pin for programming the bq2011J.

The bq2011J displays the battery charge state in either absolute or relative mode. In relative mode, the battery charge is represented as a percentage of the LMD. Each LED segment represents 20% of the LMD.

In absolute mode, each segment represents a fixed amount of charge, based on the initial PFC. In absolute mode, each segment represents 20% of the PFC. As the battery wears out over time, it is possible for the LMD to be below the initial PFC. In this case, all of the LEDs may not turn on, representing the reduction in the actual battery capacity.

The capacity display is also adjusted for the present battery temperature. The temperature adjustment reflects the available capacity at a given temperature but does not affect the NAC register. The temperature adjustments are detailed in the TMPGG register description on page 12

When $\overline{DISP}$ is tied to V_{CC}, the SEG_{1-5} outputs are inactive. When $\overline{DISP}$ is left floating, the display becomes active during charge if the NAC registers are counting at a rate equivalent to V_{SRO} < -1mV or fast discharge if the NAC registers are counting at a rate equivalent to V_{SRO} > 2mV. When pulled low, the segment output becomes active for 4 seconds, M.5 seconds.

The segment outputs are modulated as two banks, with segments 1, 3, and 5 alternating with segments 2 and 4. The segment outputs are modulated at approximately 320Hz, with each bank active for 30%of the period.

SEG_1 blinks at a 4Hz rate whenever V_{SB} has been detected to be below V_{EDV} to indicate a low-battery condition or NAC is leas than 10% of the LMD or PFC, depending on the display mode.

Microregulator

The bq2011J can operate directly from 4 cells. To facilitate the power supply requirements of the bq2011J, an REF output is provided to regulate an external low-threshold n-FET. A micropower source for the bq2011J can be inexpensively built using the FET and an external resistor.

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to V_{SS}	-0.3	+7.0	V	
All other pins	Relative to Vss	-0.3	+7.0	V	
V_{SR}	Relative to Vss	-0.3	+7.0	V	Minimum 100Ω series resistor should be used to protect SR in case of a shorted battery (see the bq2011J application note for details).
T_{OFU}	Operating temperature	0	+70	°C	Commercial
		-40	+85	°C	Industrial

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this datasheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage Thresholds ($T_A = T_{OPR}$; V = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDV}	End-of-discharge warning	0.87	0.90	0.93	V	SB
V_{SRQ}	Valid charge			-400	µV	$V_{SR} + V_{OS}$
V_{SRD}	Valid discharge	500			µV	$V_{SR} + V_{OS}$
V_{MCV}	Maximum singlecell voltage	1.95	2.0	2.05	V	SB
V_{BR}	Battery removed/replaced		0.1	0.25	V	SB

Note: For proper operation of the threshold detection circuit, V_{CC} must be at least 1.5V greater than the voltage being measured.

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	3.0	4.25	6.5	V	V_{CC} excursion from < 2.0V to ≥ 3.0V initializes the unit.
V_{REF}	Reference at 25°C	5.7	6.0	6.3	V	I_{REF} = 5µA
	Reference at -40°C to +85°C	4.5	-	7.5	V	I_{REF} = 5µA
R_{REF}	Reference input impedance	2.0	5.0	-	MΩ	V_{REF} = 3V
I_{CC}	Normal operation	-	90	135	µA	V_{CC} = 3.0V, DQ = 0
		-	120	180	µA	V_{CC} = 4.25V, DQ = 0
		-	170	250	µA	V_{CC} = 6.5V, DQ = 0
V_{SB}	Battery input	0	-	V_{CC}	V	
R_{SBmax}	SB input impedance	10	-	-	MΩ	0 < V_{SB} < V_{CC}
I_{DISP}	$\overline{DISP}$ input leakage	-	-	5	µA	V_{DISP} = V_{SS}
I_{LCOM}	LCOM input leakage	-0.2	-	0.2	µA	$\overline{DISP}$ = V_{CC}
I_{RBI}	RBI data-retention current	-	-	100	nA	V_{RBI} > V_{CC} < 3V
R_{DQ}	Internal pulldown	500	-	-	KΩ	
V_{SR}	Sense resistor input	-0.3	-	2.0	V	V_{SR} > V_{SS} = discharge; V_{SR} < V_{SS} = charge
R_{SR}	SR input impedance	10	-	-	MΩ	-200mV < V_{SR} < V_{CC}
V_{IHPFC}	PROG/SPFC logic input high	V_{CC} - 0.2	-	-	V	SPFC, $PROG_{1-4}$
V_{ILPFC}	PROG/SPFC logic input low	-	-	V_{SS} + 0.2	V	SPFC, $PROG_{1-4}$
V_{IZPFC}	PROG/SPFC logic input Z	float	-	float	V	SPFC, $PROG_{1-4}$
I_{IHPFC}	PROG/SPFC input high current	-	1.2	-	µA	V_{PFC} = V_{CC}/2
I_{ILPFC}	PROG/SPFC input low current	-	1.2	-	µA	V_{PFC} = V_{CC}/2
V_{OLSL}	SEG_X output low, low V_{CC}	-	0.1	-	V	V_{CC} = 3V, I_{OLS} ≤ 1.75mA SEG_1–SEG_5
V_{OLSH}	SEG_X output low, high V_{CC}	-	0.4	-	V	V_{CC} = 6.5V, I_{OLS} ≤ 11.0mA SEG_1–SEG_5
V_{OHML}	LCOM output high, low V_{CC}	V_{CC} - 0.3	-	-	V	V_{CC} = 3V, I_{OHLCOM} = -5.25mA
V_{OHMH}	LCOM output high, high V_{CC}	V_{CC} - 0.6	-	-	V	V_{CC} = 6.5V, I_{OHLCOM} = -33.0mA
I_{OHLCOM}	LCOM source current	-33	-	-	mA	At V_{OHLCOM} = V_{CC} - 0.6V
I_{OLS}	SEG_X sink current	11.0	-	-	mA	At V_{OLSH} = 0.4V, V_{CC} = 6.5V
I_{OL}	Open-drain sink current	5.0	-	-	mA	At V_{OL} = V_{SS} + 0.3V, DQ
V_{OL}	Open-drain output low	-	-	0.5	V	I_{OL} ≤ 5mA, DQ
V_{IHDQ}	DQ input high	2.5	-	-	V	DQ
V_{ILDQ}	DQ input low	-	-	0.8	V	DQ
R_{FLOAT}	Float state external impedance	-	5	-	MΩ	SPFC, $PROG_{1-4}$

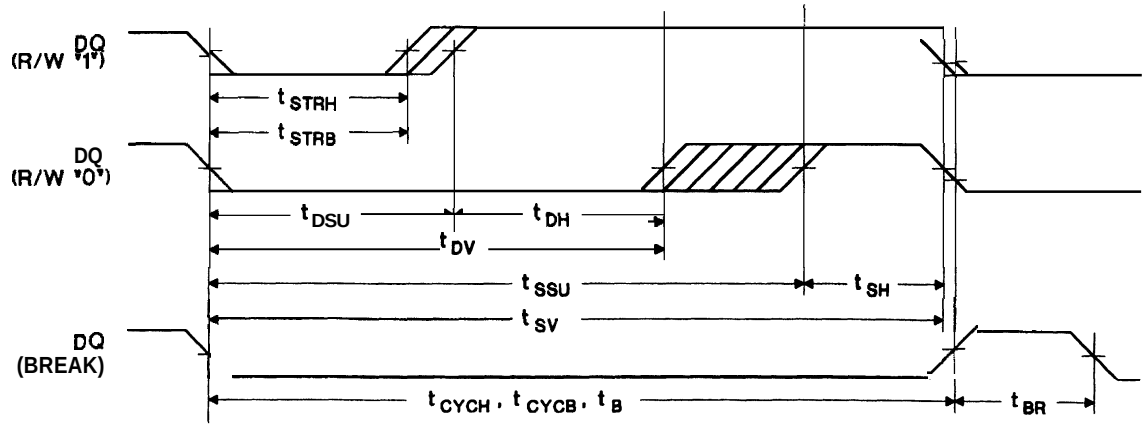
Note: All voltages relative to V_{SS}.

Serial Communication Timing Specification ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYCH}	Cycle time, host to bq2011J	3			me	See note
t_{CYCB}	Cycle time, bq2011J to host	3		6	me	
t_{STRH}	Start hold, host to bq2011J	5	-	-	ns	
t_{STRB}	Start hold, bq2011J to host	500			µs	
t_{DSU}	Data setup			750	µs	
t_{DH}	Data hold	750			µs	
t_{DV}	Data valid	1.50	-	-	ms	
t_{SSU}	Stop setup			2.25	me	
t_{SH}	Stop hold	700			µs	
t_{SV}	Stop valid	2.95	-	-	me	
t_B	Break	3	-	-	ms	
t_{BR}	Break recovery	1			me	

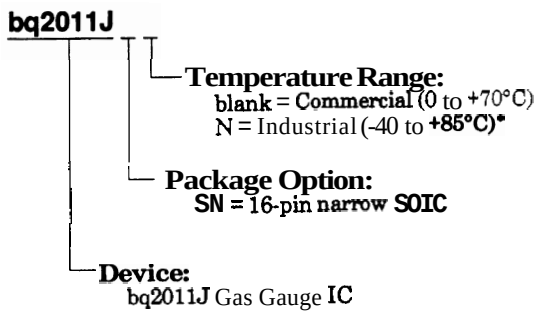
Note: The open-drain DQ pin should be pulled to at least V_{CC} by the host system for proper DQ operation. DQ may be left floating if the serial interface is not used.

Serial Communication Timing Illustration



RC-34

Ordering Information



* Contact factory for availability.

bq2011K

Gas Gauge IC

2

Features

- Conservative and repeatable measurement of available charge in rechargeable batteries
- Designed for portable equipment such as power tools with high discharge rates
- Designed for battery pack integration
  - 120µA typical standby current (self-discharge estimation mode)
  - Small size enables implementations in as little as ½ square inch of PCB
- Direct drive of LEDs for capacity display
- Self-discharge compensation using internal temperature sensor
- Simple single-wire serial communications port for subassembly testing
- 16-pin narrow SOIC

General Description

The bq2011K Gas Gauge IC is intended for battery-pack installation to maintain an accurate record of a battery's available charge. The IC monitore a voltage drop across a sense resistor connected in series between the negative battery terminal and ground to determine charge and discharge activity of the battery. The bq2011K is designed for systems such as power tools with very high discharge rates.

Battery self-discharge is estimated based on an internal timer and temperature sensor. Compensations for battery temperature and rate of charge or discharge are applied to the charge, discharge, and self-discharge calculations to provide available charge information across a wide range of operating conditions. Initial battery capacity is set using the $PROG_{1-4}$ and SPFC pins. Actual battery capacity is automatically 'learned' in the course of a discharge cycle from full to empty and may be displayed depending on the display mode.

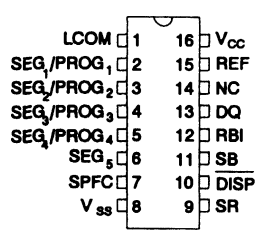
Nominal available charge may be directly indicated using a five-segment LED dirplay. These segments are used to graphically indicate nominal available charge.

The bq2011K supports a simple single-line bidirectional serial link to an external processor (common ground). The bq2011K outputs battery information in response to external commands over the serial link. To support subassembly testing, the outputs may also be controlled by command. The external processor may also overwrite some of the bq2011K gas gauge data registers.

The bq2011K may operate directly from four cells. With the REF output and an external transistor, a simple, inexpensive regulator can be built to provide Vcc from a greater number of cells.

Internal registers include available charge, tempera —, capacity, battery ID, and battery status.

Pin Connections



18-Pin Narrow SOIC

PN-90

Pin Names

LCOM	LED common output	REF	Voltage reference output
$SEG_1/PROG_1$	LED segment 1/ Program 1 input	NC	No connect
$SEG_2/PROG_2$	LED segment 2 / Program 2 input	DQ	Serial communications input/output
$SEG_3/PROG_3$	LED segment 3/ Program 3 input	RBI	Register backup input
$SEG_4/PROG_4$	LED segment 4/ Program 4 input	SB	Battery sense input
SEG_5	LED segment 5	$\overline{DISP}$	Display control input
SPFC	Programmed full count selection input	SR	Sense resistor input
		Vcc	3.0-6.5V
		Vss	Negative battery terminal

Pin Descriptions

LCOM **LED common**

Open-drain output switches Vcc to source current for the LEDs. The switch ia off during initialization to allow reading of $PROG_{1-4}$ pull-up or pull-down program resistors. LCOM is high impedance when the display is off.

SEG_1-SEG_5 LED display segment outputs

Each output may activate an LED to sink the current sourced from LCOM, the battery, or VCC.

$PROG_1$-$PROG_4$ Programmed full count selection inputs (dual function with SEG_1 - SEG_4)

These three-level input pins define the programmed full count (PFC) in conjunction with SPFC pin, define the display mode and enable or disable self-discharge.

SPFC Programmed full count selection input

This three-level input pin along with $PROG_{1-3}$ define the programmed full count (PFC) thresholds described in Table 1. The state of the SPFC pin is only read immediately after a reset condition.

SR Sense resistor input

The voltage drop (V_{SR}) across the sense resistor R_S is monitored and integrated over time to interpret charge and discharge activity. The SR input is tied to the low side of the sense resistor and battery pack ground (see Figure 1. $V_{SR} > V_{SS}$ indicates discharge, and $V_{SR} < V_{SS}$ indicates charge. The effective voltage drop, V_{SRO}, as seen by the bq2011K is $V_{SR} + V_{OS}$ (see Table 4).

NC No connect

$\overline{DISP}$ Display control input

$\overline{DISP}$ floating allows the LED display to be active during certain charge and discharge conditions. Transitioning $\overline{DISP}$ low activates the display for 4 ± 0.5 seconds.

SB Secondary battery input

This input monitors the single-cell voltage potential through a high-impedance resistive divider network for the end-of-discharge voltage (EDV) threshold and maximum cell voltage (MCV).

RBI Register backup input

This input is used to provide backup potential to the bq2011K registers during periods when V_{CC} < 3V. A storage capacitor should be connected to RBI.

DQ serial I/O pin

This is an open-drain bidirectional pin.

REF Voltage reference output for regulator

REF provides a voltage reference output for an optional micro-regulator.

V_{CC} Supply voltage input

V_{SS} Ground

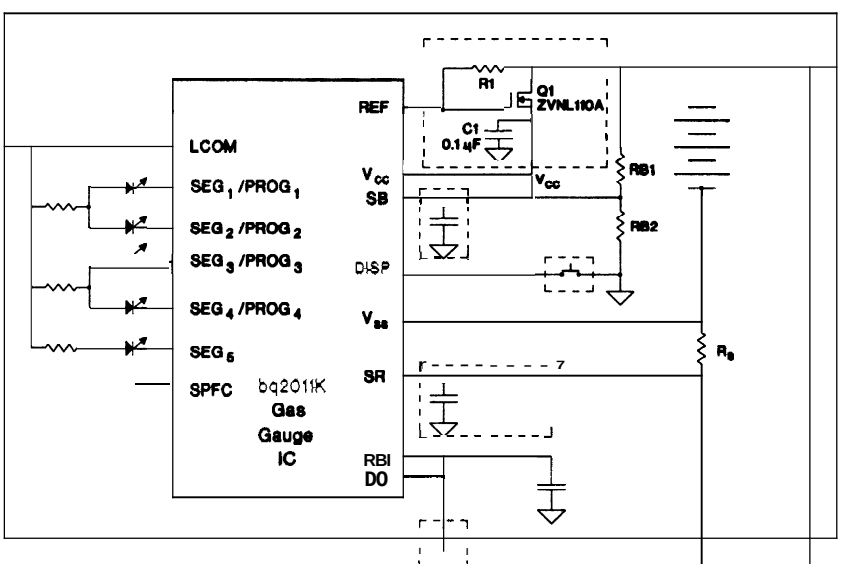
Functional Description

General Operation

The bq2011K determines battery capacity by monitoring the amount of charge input to or removed from a rechargeable battery. The bq2011K measures discharge and charge currents, estimates self-discharge, monitors the battery for low-battery voltage thresholds, and compensates for temperature and charge/discharge rates. The charge measurement ia made by monitoring the voltage across a small-value series sense resistor between the battery's negative terminal and ground. The available battery charge is determined by monitoring this voltage over time and correcting the measurement for the environmental and operating conditions.

Figure 1 shows a typical battery pack application of the bq2011K wing the LED display with abeolute mode as a charge-state indicator. The bq2011K can be configured to display capacity in either a relative or an absolute display mode. The relative display mode uses the last measured discharge capacity of the battery as the battery 'full' reference. The abeolute display mode uses the programmed full count (PFC) as the full reference, forcing each segment of the display to represent a fixed amount of charge. A push-button diaplay feature is available for momentarily enabling the LED display.

The bq2011K monitors the charge and discharge currents as a voltage across a sense resistor (see Rs in Figure 1). A filter between the negative battery terminal and the SR pin may be required if the rate of change of the battery current ia too great.



[ ] indicates optional.

Directly connect to V_{CC} across 4 cells (4.8V nominal and should not exceed 6.5V) with a resistor and a Zener diode to limit voltage during charge. Otherwise, R1, C1, and Q1 are needed for regulation of > 4 cells.

Programming resistor and ESD-protection diodes are not shown.

R-C on SR may be required (application specific), where the maximum R should not exceed 20K.

Figure 1. Application Diagram—LED Display, Absolute Mode

Register Backup

The bq2011K RBI input pin is intended to be used with a storage capacitor to provide backup potential to the internal bq2011K registers when V_{CC} momentarily drops below 3.0V. V_{CC} is output on RBI when V_{CC} is above 3.0V.

After V_{CC} rises above 3.0V, the bq2011K checks the internal registers for data loss or corruption. If data has changed, then the NAC register is cleared, and the LMD register is loaded with the initial PFC.

Voltage Thresholds

In conjunction with monitoring V_{SR} for charge/discharge currents, the bq2011K monitors the single-cell battery potential through the SB pin. The single-cell voltage potential is determined through a resistor-divider network per the following equation:

$$\frac{RB_1}{RB_2} = N - 1$$

where N is the number of cells, RB_1 is connected to the positive battery terminal, and RB_2 is connected to the negative battery terminal. The single-cell battery voltage is monitored for the end-of-discharge voltage (EDV) and for maximum cell voltage (MCV). The EDV threshold level is used to determine when the battery has reached an 'empty" state, and the MCV threshold is used for fault detection during charging. The MCV threshold for the bq2011K is fixed at:

$$V_{MCV} = 2.00V$$

The EDV threshold varies as a function of discharge current as follows:

V_{SRO} (mV)	V_{EDV} (V)
$0 < V_{SRO} \le 10$	1.160
$10 < V_{SRO} \le 20$	1.124
$20 < V_{SRO} \le 40$	1.060
$40 < V_{SRO} \le 60$	0.960
$V_{SRO} > 60$	0 (OVLD)

Reset

Reset can be accomplished with a command over the serial port as described on page 13.

Temperature

The bq2011K internally determines the temperature in 10°C steps centered from -35°C to +85°C. The temperature steps are used to adapt charge and discharge rate compensations, self-discharge counting, and available charge display translation. The temperature range is available over the serial port in 10°C increments as shown below:

TMPGG (hex)	Temperature Range
0x	< -30°C
1x	-30°C to -20°C
2x	-20°C to -10°C
3x	-10°C to 0°C
4x	0°C to 10°C
5x	10°C to 20°C
6x	20°C to 30°C
7x	30°C to 40°C
8x	40°C to 50°C
9x	50°C to 60°C
Ax	60°C to 70°C
Bx	70°C to 80°C
Cx	> 80°C

Layout Considerations

The bq2011K measures the voltage differential between the SR and V_{SS} pine. V_{OS} (the offset voltage at the SR pin) is greatly affected by PC board layout. For optimal results, the PC board layout should follow the strict rule of a single-point ground return. Sharing high-current ground with small signal ground causes undesirable noise on the small signal nadea. Additionally:

- The capacitors (SB and V_{CC}) should be placed as close as possible to the SB and V_{CC} pins, respectively, and their paths to V_{SS} should be as short as possible. A high-quality ceramic capacitor of 0.1µf is recommended for V_{CC}.
- The sense resistor (R_S) should be as close as possible to the bq2011K.
- The R-C on the SR pin should be located as close as possible to the SR pin. The maximum R should not exceed 20K.

Gas Gauge Operation

The operational overview diagram in F i e 2 illustrates the operation of the bq2011K. The bq2011K accumulates a measure of charge and discharge currents, as well as an estimation of self-discharge. Charge currents are temperature and rate compensated, whereas self-discharge is only temperature compensated.

The main counter, Nominal Available Charge (NAC), represents the available battery capacity at any given

time. Battery charging increments the NAC register, while battery discharging and self-discharge decrement the NAC register and increment the DCR (Discharge Count Register).

The Discharge Count Register (DCR) is used to update the Last Measured Discharge (LMD) register only if a complete battery discharge from full to empty occurs without any partial battery charges. Therefore, the bq2011K adapts its capacity determination based on the actual conditions of discharge.

The battery's initial capacity is equal to the Programmed Full Count (PFC) shown in Table 1. Until LMD is updated, NAC counts up to but not beyond this threshold during subsequent charges. This approach allows the gas gauge to be charger-independent and compatible with any type of charge regime.

1. Last Measured Discharge (LMD) or learned battery capacity:

   LMD is the last measured discharge capacity of the battery. On initialization (application of Vcc or battery replacement), LMD = PFC. During subsequent discharges, the LMD is updated with the latest measured capacity in the Discharge Count Register (DCR) representing a discharge from full to below EDV. A qualified discharge is necessary for a capacity transfer from the DCR to the LMD register. The LMD also serves as the 100% reference threshold used by the relative display mode.

2. Programmed Full Count (PFC) or initial battery capacity:

   The initial LMD and gas gauge rate values are programmed by using PFC. The PFC also provides the 100% reference for the absolute display mode. The bq2011K is configured for a given application by selecting a PFC value from Table 1. The correct PFC may be determined by multiplying the rated battery capacity in mAh by the sense resistor value:

   Battery capacity (mAh) • sense resistor (R) =

   PFC (mVh)

   Selecting a PFC slightly less than the rated capacity for absolute mode provides capacity above the full reference for much of the battery's life.

Example: Selecting a PFC Value

Given:

Sense resistor = 0.002Ω
Number of cells = 6
Capacity = 1800mAh, NiCd cells
Current range = 1A to 80A
Relative display mode
Self-discharge = C/80
Voltage drop across sense resistor = 2mV to 160mV

Therefore:

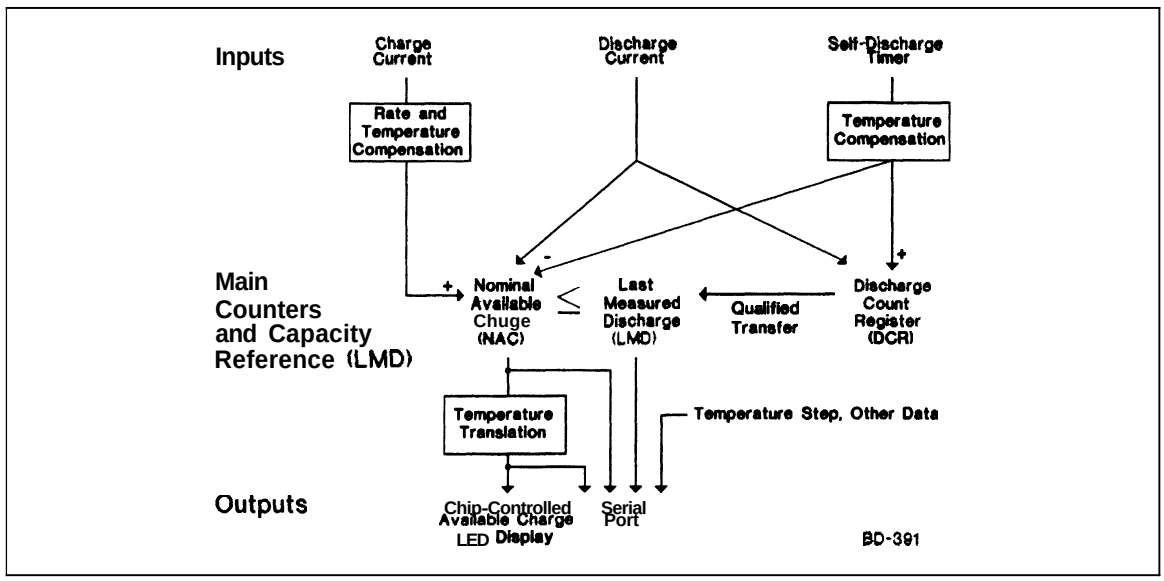


Figure 2. Operational Overview

1800mAh • 0.002Ω = 3.6mVh

Select:

PFC = 35840 counts or 3.39mVh
SPFC = Z (float)
PROG1, PROG2 = H or Z
PROG3 = L
PROG4 = H or Z

The initial full battery capacity is 3.39mVh (1695mAh) until the bq2011K "learns" a new capacity with a qualified discharge from full to EDV.

3. **Nominal** Available Charge (NAC):

NAC counts up during charge to a **maximum** value of LMD and down during **discharge** and **self** discharge to 0. NAC is reset to 0 on initialization and on the first valid charge following discharge to EDV. To prevent **overstatement** of charge during periods of overcharge, NAC stops **incrementing** when NAC = LMD.

Note: NAC is **set** to the value in LMD when $PROG_4$ is pulled low during a reset.

Table 1. bq2011K Programmed Full Count mVh Selections

Programmed Full Count (PFC)	mVh	Scale	Display Mode	SPFC	$PROG_1$	$PROG_2$	$PROG_3$
40192	3.81	1/10560	Absolute	H	H or Z	H or Z	H or Z
32256	3.05	1/10560		Z	H or Z	H or Z	H or Z
28928	2.74	1/10560		L	H or Z	H or Z	H or Z
25856	2.45	1/10560		H	L	H or Z	H or Z
35840	3.39	1/10560		Z	L	H or Z	H or Z
23296	2.21	1/10560		L	L	H or Z	H or Z
40192	3.81	1/10560	Relative	H	H or Z	L	H or Z
32256	3.05	1/10560		Z	H or Z	L	H or Z
28928	2.74	1/10560		L	H or Z	L	H or Z
25856	2.45	1/10560		H	H or Z	H or Z	L
35840	3.39	1/10560		Z	H or Z	H or Z	L
23296	2.21	1/10560		L	H or Z	H or Z	L

Table 2. Programmed Self-Discharge

$PROG_4$	NAC Reset Value	Self-Discharge
H or Z	NAC = 0	Enabled
L	NAC = PFC	Disabled

4. Discharge Count Register (DCR):

The DCR counts up during discharge independent of NAC and could continue increasing after NAC has decremented to 0. Prior to NAC = 0 (empty battery), both discharge and self-discharge increment the DCR. After NAC = 0, only discharge increments the DCR. The DCR resets to 0 when NAC = LMD. The DCR does not roll over but stops counting when it reaches FFFFh.

The DCR value becomes the new LMD value on the first charge after a valid discharge to VEDV if:

No valid charge initiations (charges greater than 256 NAC counts; or 0.006 – 0.01C) occurred during the period between NAC = LMD and EDV detected.

The self-discharge count is not more than 4096 counts (8% to 18% of PFC, specific percentage threshold determined by PFC).

The temperature is ≥ 0°C when the EDV level is reached during discharge.

The valid discharge flag (VDQ) indicates whether the present diiharge is valid for LMD update.

Charge Counting

Charge activity is detected based on a negative voltage on the V_{SR} input. If charge activity is detected, the bq2011K increments NAC at a rate proportional to V_{SR} (V_{SR} + Vos) and, if enabled, activates an LED display if $V_{SR} < -2mV$. Charge actions increment the NAC after compensation for charge rate and temperature.

The bq2011K determines a valid charge activity sustained at a continuous rate equivalent to $V_{SR} < -400\mu V$. A valid charge equates to a sustained charge activity greater than 256 NAC counts. Once a valid charge is detected, charge counting continues until V_{SR} rises above $-400\mu V$.

Discharge Counting

All discharge counts where $V_{SR} > 500\mu V$ cause the NAC register to decrement and the DCR to increment. Exceeding the fast discharge threshold (FDQ) if the rate is equivalent to $V_{SR} > 2mV$ activates the display, if enabled. The display remains active for 10 seconds after V_{SR} falls below 2mV.

Self-Discharge Estimation

The bq2011K continuously decrements NAC and increments DCR for self-discharge based on time and temperature. The self-discharge count rate is programmed to be a nominal 1/80 • NAC rate per day or disabled per Table 2. This is the rate for a battery temperature between 20–30°C. The NAC register cannot not be decremented below 0.

Count Compensations

The bq2011K determines fast charge when the NAC updates at a rate of ≥2 counts/sec. Charge activity is compensated for temperature and rate before updating the NAC and/or DCR. Self-discharge estimation is compensated for temperature before updating the NAC or DCR.

Charge Compensation

Two charge efficiency factors are used for trickle charge and feet charge. Fast charge is defined as a rate of charge resulting in ≥ 2 NAC counts/sec (≥ 0.15C to 0.32C depending on PFC selections; see Table 1). The compensation defaults to the fast charge factor until the actual charge rate is determined.

Temperature adapts the charge rate compensation factors over three rangea between nominal, warm, and hot temperatures. The wmpensationfactors are shown below.

Charge Temperature	Trickle Charge Compensation	Fast Charge Compensation
<30°C	0.80	0.95
30–50°C	0.75	0.90
> 50°C	0.70	0.85

Discharge Compensation

Corrections for the rate of discharge are made by adjusting EDV thresholds. The compensation factor used during discharge is set to 1.00 for all rates and temperatures. The recoverable charge at colder temperatures is adjusted for display purposes only. See page 13.

Self-Discharge Compensation

The self-discharge compensation is programmed for a nominal rate of 1/80 • NAC per day or disabled. This is the rate for a battery within the 20–30°C temperature range (TMPGG = 6x). This rate varies across 8 ranges from <10°C to >70°C, doubling with each higher temperature step (10°C). See Table 3.

Table 3. Self-Discharge Compensation

Temperature Range	Self-Discharge Compensation Typical Rate/Day
< 10°C	NAC/320
10–20°C	NAC/160
20–30°C	NAC/80
30–40°C	NAC/40
40–50°C	NAC/20
50–60°C	NAC/10
60–70°C	NAC/5
> 70°C	NAC/2.5

Error Summary

The LMD is susceptible to error on initialization or if no updates occur. On initialization, the LMD value includes the error between the programmed full capacity and the actual capacity. This error is present until a valid discharge occurs and LMD is updated (see the DCR description in the 'Layout Considerations" section). The other cause of LMD error is battery wear-out. As the battery ages, the measured capacity must be adjusted to account for changes in actual battery capacity.

Current-Sensing Error

Table 4 illustrates the current-sensing error as a function of V_{SR}. A digital filter eliminates charge and discharge counts to the NAC register when V_{SRO} (V_{SR} + V_{OS}) is between -400µV and 500µV.

Communicating With the bq2011K

The bq2011K includes a simple single-pin (DQ plus return) serial data interface. A host processor uses the interface to access various bq2011K registers. Battery characteristics may be easily monitored by adding a single contact to the battery pack. The open-drain DQ pin on the bq2011K should be pulled up by the host system, or may be left floating if the aerial interface is not used.

The interface uses a command-based protocol, where the host processor sends a command byte to the bq2011K. The command directs the bq2011K to either store the nest eight bits of data received to a register specified by the command byte or output the eight bits of data specified by the command byte.

The communication protocol is asynchronous return-to-one. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 333 bits/sec. The least-significant bit of a command or data byte is transmitted first. The protocol is simple enough that it can be implemented by most host processors using either polled or interrupt processing. Data input from the bq2011K may be sampled using the pulse-width capture timers available on some microcontrollers.

Communication is normally initiated by the host processor sending a BREAK command to the bq2011K. A BREAK is detected when the DQ pin is driven to a logic-low state for a time, t_B or greater. The DQ pin should then be returned to its normal ready-high logic state for a time, t_{BR}. The bq2011K is now ready to receive a command from the host processor.

The return-to-one data bit frame consists of three distinct sections. The first section is used to start the transmission

Table 4. bq2011K Current-Sensing Errors

Symbol	Parameter	Typical	Maximum	Units	Notes
V_{OS}	Offset referred to V_{SR}	± 50	± 150	µV	$\overline{DISP}$ = Vcc.
INL	Integrated non-linearity error	± 2	± 4	%	Add 0.1% per °C above or below 25°C and 1% per volt above or below 4.25V.
INR	Integrated non-repeatability error	± 1	± 2	%	Measurement repeatability given similar operating conditions.

by either the host or the bq2011K taking the DQ pin to a logic-low state for a period, $t_{STRH,B}$. The next section is the actual data transmission, where the data should be valid by a period, t_{DSU}, after the negative edge used to start communication. The data should be held for a period, t_{DV}, to allow the host or bq2011K to sample the data bit.

The final section is used to stop the transmission by returning the DQ pin to a logic-high state by at least a period, t_W, after the negative edge used to start communication. The final logic-high state should be held until a period, t_{SV}, to allow time to ensure that the bit transmission was stopped properly. The timings for data and break communication are given in the serial communication timing specification and illustration sections.

Communication with the bq2011K is always performed with the least-significant bit being transmitted first. Figure 3 shows an example of a communication sequence to read the bq2011K NAC register.

bq2011K Registers

The bq2011K command and status registers are listed in Table 5 and described below.

Command Register (CMDR)

The write-only CMDR register is accessed when eight valid command bite have been received by the bq2011K. The CMDR register contains two fields:

- a W/$\overline{R}$ bit
- a Command address

The W/$\overline{R}$ bit of the command register is used to select whether the received command is for a read or a write function.

The W/$\overline{R}$ values are:

CMDR Bits							
7	6	5	4	3	2	1	0
W/$\overline{R}$	-	-	-		-	-	-

Where W/$\overline{R}$ is:

0 The bq2011K outputs the requested register contents specified by the address portion of CMDR

1 The following eight bite should be written to the register specified by the a d k portion of CMDR.

The lower seven-bit field of CMDR contains the address portion of the register to be accessed. Attempts to write to invalid addresses are ignored.

CMDR Bits							
7	6	5	4	3	2	1	0
-	AD6	AD5	AD4	AD3	AD2	AD1	AD0 (LSB)

Primary Status Flags Register (FLGS1)

The read-only FLGS1 register (address=01h) contains the primary bq2011K flags.

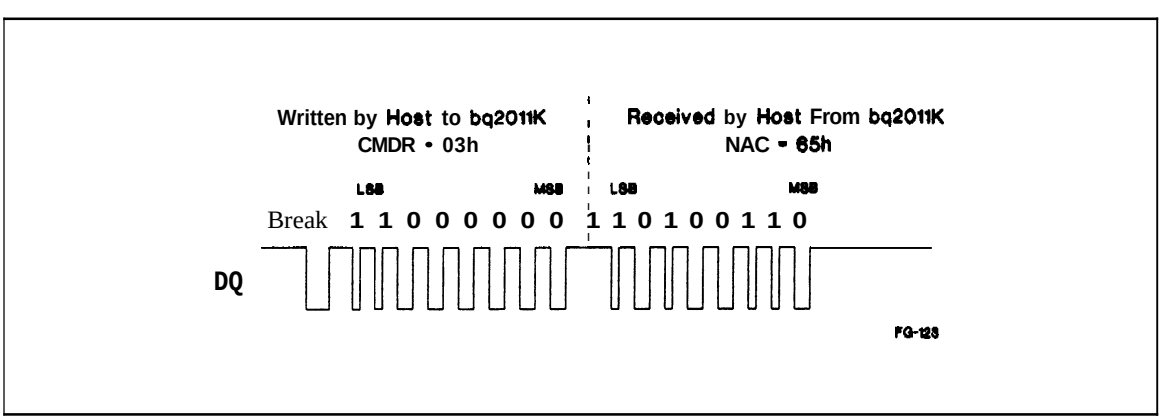


Figure 3. Typical Communication With the bq2011K

Table 5. bq2011K Command and Status Registers

Symbol	Register Name	Loc. (hex)	Read/ Write	Control Field							
				7(MSB)	6	5	4	3	2	1	0(LSB)
CMDR	Command register	00h	Write	W/$\overline{R}$	AD6	AD5	AD4	AD3	AD2	AD1	AD0
FLGS1	Primary status flags register	Olh	Read	CHGS	BRP	MCV	n/u	VDQ	n/u	EDV	n/u
TMPGG	Temperature and gas gauge register	02h	Read	TMP3	TMP2	TMP1	TMP0	GG3	GG2	GG1	GG0
NACH	Nominal available charge high byte register	03h	R/W	NACH7	NACH6	NACH5	NACH4	NACH3	NACH2	NACH1	NACHO
NACL	Nominal available charge low byte register	17h	Read	NACL7	NACL6	NACL5	NACL4	NACL3	NACL2	NACL1	NACL0
BATID	Battery identification register	04h	R/W	BATID7	BATID6	BATID5	BATID4	BATID3	BATID2	BATID1	BATID0
LMD	Last measured discharge register	05h	R/W	LMD7	LMD6	LMD5	LMD4	LMD3	LMD2	LMD1	LMD0
FLGS2	Secondary status flags register	06h	Read	CR	DR2	DR1	DR0		n/u	n/u	OVLD
OCTL	Output control register	Oah	Write	1	0C5	0C4	0C3	OC2	OC1	n/u	OCE
RST	Reset register	39h	Write	RST	0	0	0	0	0	0	0

Note: n/u = not used

The *charge status* flag (CHGS) is asserted when a valid charge rate is detected. Charge rate is deemed valid when $V_{SRO} < -400\mu V$. A V_{SRO} of greater than- 400µV or discharge activity clears CHGS.

The CHGS values are:

FLGSI Bib							
7	6	5	4	3	2	1	0
CHGS	-	-	-	-	-	-	-

Where CHGS is:

0 Either discharge activity detected *or* $V_{SRO} > -400\mu V$

1 $V_{SRO} < -400\mu V$

The battery replaced flag (BRP) is asserted whenever the potential on the SB pin (relative to V_{SS}), V_{SB}, rises above 0.1V and determines the internal registers have been corrupted. The BRP flag is also set when the bq2011K is reset (see the RST register description). BRP is cleared if either the bq2011K is charged until NAC = LMD or discharged until EDV is reached. BRP = 1 signifies that the device has been reset.

The BRP values are:

FLGSI Bits							
7	6	5	4	3	2	1	0
-	BRP	-					

Where BRP is:

0 bq2011K is charged until NAC = LMD or discharged until the EDV flag is asserted

1 Initial *or* full V_{CC} reset, or a serial port initiated reset has occurred

The maximum *cell voltage* flag (MCV) is asserted whenever the potential on the SB pin (relative to V_{SS}) is above 2.0V. The MCV flag is asserted until the condition causing MCV is removed.

The MCV values are:

FLGSI Bits							
7	6	5	4	3	2	1	0
	-	MCV	-	-			

Where MCV is:

0 $V_{SB} < 2.0V$

1 $V_{SB} > 2.0V$

The *valid discharge* flag *(VDQ) is* asserted when the bq2011K is discharged from NAC=LMD. The flag remains set until either LMD is updated or one of three actions that can clear VDQ occurs:

- The self-discharge count register (SDCR) has exceeded the maximum acceptable value (4096 counts) for an LMD update.
- A valid charge action equal to 266 NAC counts with $V_{SRO} < -400\mu V$.
- The EDV flag was set at a temperature below 0°C

The VDQ values are:

FLGSI Bib							
7	6	5	4	3	2	1	0
			-	VDQ	-		

Where VDQ is:

0 SDCR ≥ 4096, subsequent valid charge action detected, *or* EDV is asserted with the temperature less than 0°C

1 On first discharge after NAC = LMD

The *end-of-discharge warning* flag (EDV) warns the user that the battery is empty. SEG1 blinks at a 4Hz rate. EDV detection is disabled if OVLD = 1. The EDV flag is latched until a valid charge has been detected.

The EDV values are:

FLGSI Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	EDV	-

Where EDV is:

0 Valid charge action detected

1 $V_{SB} < V_{EDV}$

Temperature and Gas Gauge Register (TMPGG)

The read-only TMPGG register (address=02h) contains two data fields. The first field contains the battery temperature. The second field contains the available charge from the battery.

TMPGG Temperature Bib							
7	6	5	4	3	2	1	0
TMP3	TMP2	TMP1	TMP0	-	-	-	

The bq2011K contains an internal temperature sensor. The temperature is used to set charge efficiency factors as well as to adjust the self-discharge coefficient. The

temperature register contents may be translated as shown in Table 6.

Table 6. Temperature Register Contents

TMP3	TMP2	TMP1	TMP0	Temperature
0	0	0	0	T < -30°C
0	0	0	1	-30°C < T < -20°C
0	0	1	0	-20°C < T < -10°C
0	0	1	1	-10°C < T < 0°C
0	1	0	0	0°C < T < 10°C
0	1	0	1	10°C < T < 20°C
0	1	1	0	20°C < T < 30°C
0	1	1	1	30°C < T < 40°C
1	0	0	0	40°C < T < 50°C
1	0	0	1	50°C < T < 60°C
1	0	1	0	60°C < T < 70°C
1	0	1	1	70°C < T < 80°C
1	1	0	0	T > 80°C

The bq2011K calculates the available charge as a function of NAC, temperature, and a full reference, either LMD or PFC. The results of the calculation are available via the display port or the gas gauge field of the TMPGG register. The register is used to give available capacity in 1/16 increments from 0 to 15/16.

TMPGG Gas Gauge Bits							
7	6	5	4	3	2	1	0
			-	GG3	GG2	GG1	GG0

The gas gauge display and the gas gauge portion of the TMPGG register are adjusted for cold temperature dependencies. A piece-wise correction is performed as follows:

Temperature	Available Capacity Calculation
> 0°C	NAC / 'Full Reference'
-20°C < T < 0°C	0.75 • NAC / 'Full Reference'
< -20°C	0.5 • NAC / 'Full Reference'

The adjustment between > 0°C and -20°C < T < 0°C has a 4°C hysteresis.

Nominal Available Charge Register (NAC)

The read/write NACH register (address=03h) and the read-only NACL register (address=17h) are the main gas gauging registers for the bq2011K. The NAC registers are incremented during charge actions and decremented during discharge and self-discharge actions. The correction factors for charge/discharge efficiency are applied automatically to NAC.

If SEG_5 = 0 on reset, then NACH = PFC and NACL = 0. If SEG_5 = Z or H, the NACH and NACL registers are cleared to zero, NACL stops counting when NACH reaches zero. When the bq2011K detects a valid charge, NACL resets to zero; *writing* to the NAC register *affects* the *available charge* counts *and, therefore, affects* the *bq2011K* gas gauge *operation.*

Battery Identification Register (BATID)

The read/write BATID register (address=04h) is available for use by the system to determine the type of battery pack. The BATID contents are retained as long as V_{CC} is greater than 2V. The contents of BATID have no effect on the operation of the bq2011K. There is no default setting for this register.

Last Measured Discharge Register (LMD)

LMD is a read/write register (address=05h) that the bq2011K uses as a measured full reference. The bq2011K adjusts LMD based on the measured discharge capacity of the battery from full to empty. In this way the bq2011K updates the capacity of the battery. LMD is set to PFC during a bq2011K reset.

Secondary Status Flags Register (FLGS2)

The read-only FLGS2 register (address=06h) contains the secondary bq2011K flags.

The charge *rate* flag (CR) is used to denote the fast charge regime. Fast charge is assumed whenever a charge action is initiated. The CR flag remains asserted if the charge rate does not fall below 2 counts/sec.

The CR values are:

FLGS2 Bits							
7	6	5	4	3	2	1	0
CR	-						

Where CR is:

0 When charge rate falls below 2 counts/sec

1 When charge rate is above 2 counts/sec

The fast charge regime efficiency factors are used when CR = 1. When CR = 0, the trickle charge efficiency factors are used. The time to change CR varies due to the user-selectablecount rates.

The discharge rate flags, DR2–0, are bits 6–4.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	DR2	DR1	DR0	-	-	-	

They are used to determine the present discharge regime as follows:

DR2	DR1	DRO	V_{SRO}(mV)
0	0	0	$0 < V_{SRO} \le 10$
0	0	1	$10 < V_{SRO} \le 20$
0	1	0	$20 < V_{SRO} \le 40$
0	1	1	$40 < V_{SRO} \le 60$
1	0	0	$V_{SRO} > 60$

The overload flag (OVLD) is asserted when a discharge overload is detected, V_{SRO} > 60mV. OVLD remains asserted as long as the condition is valid.

FLGS2 Bits							
7	6	5	4	3	2	1	0
						-	OVLD

Output Control Register (OCTL)

The write-only OCTL register (address=0ah) provides the system with a means to check the display connections for the bq2011K. The segment drivers may be overwritten by data from OCTL when the least-signiscant bit of OCTL, WE, is set. The data in bits OC_{5-1} of the OCTL register (see Table 6 for details) is output onto the segment pins, SEG_{5-1}, respectively if OCE=1. *Whenever OCE is written to 1, the MSB of OCTL should be set* to a 1. The W E register location must be cleared to return the bq2011K to normal operation. OCE may be cleared by either writing the bit to a logic zero via the serial port or by resetting the bq2011K as explained below. Note: Whenever the OCTL register is written, the MSB of OCTL should be written to a logic one.

Reset Register (RST)

The reset register (address=39h) provides the means to perform a software-controlled reset of the device. A full device reset may be accomplished by first writing LMD (address = 05h) to 00h and then writing the RST register contents from 00h to 80h. *Setting m y* bit other than the *most-significant* bit of the *RST register is not allowed,* a d *results* in *improper operation of* the *bq2011K.*

Resetting the bq2011K sets the following:

- LMD = PFC
- VDQ, OCE, and NAC = 0 (NAC = PFC when $PROG_4$ = L)
- BRP = 1

Display

The bq2011K can directly display capacity information using low-power LEDs. If LEDs are used, the segment pins should be tied to Vcc, the battery, or the LCOM pin through resistors for programmingthe bq2011K.

The bq2011K displays the battery charge state in either absolute or relative mode. In relative mode, the battery charge is represented as a percentage of the LMD. Each LED segment represents 20% of the LMD.

In absolute mode, each segment representa a fixed amount of charge, based on the initial PFC. In absolute mode, each segment represents 20% of the PFC. As the battery wears out over time, it is possible for the LMD to be below the initial PFC. In this case, all of the LEDs may not turn on, representing the reduction in the actual battery capacity.

The capacity display is also adjusted for the present battery temperature. The temperature adjustment reflects the available capacity at a given temperature but does not affect the NAC register. The temperature adjustments are detailed in the TMPGG register description.

When $\overline{DISP}$ is tied to Vcc, the SEG_{1-5} outputs are inactive. When $\overline{DISP}$ is left floating, the display becomes active during charge if the NAC registers are counting at a rate equivalent to V_{SRO} < -2mV or fast discharge if the NAC registers are counting at a rate equivalent to V_{SRO} > 2mV. When $\overline{DISP}$ is left floating, the display also becomes active after the detection of a discharge signal with a minimum amplitude of V_{SR} > 20mV (10 amps for R_S = .002Ω) and a minimum pulse width of 25msec. When $\overline{DISP}$ is pulled low, the segment outputs become active for 4 seconds, ±0.5 seconds.

The segment outputs are modulated as two banks, with segments 1, 3, and 5 alternating with segments 2 and 4. The segment outputs are modulated at approximately 320Hz, with each bank active for 30% of the period.

SEG_1 blinks at a 4Hz rate whenever V_{SB} has been detected to be below V_{EDV} to indicate a low-battery condition or NAC is lees than 10% of the LMD or PFC, depending on the display mode.

Microregulator

The bq2011K can operate directly from 4 cells. To facilitate the power supply requirements of the bq2011K, an REF output is provided to regulate an external low-threshold n-FET. A micropower source for the bq2011K can be inexpensively built using the FET and an external resistor.

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to V_{SS}	-0.3	+7.0	V	
All other pins	Relative to V_{SS}	-0.3	+7.0	V	
V_{SR}	Relative to V_{SS}	-0.3	+7.0	V	Minimum 100Ω series resistor should be used to protect SR in case of a shorted battery (see the bq2011K application note for details).
T_{OPR}	Operating temperature	0	+70	°C	Commercial
		-40	+85	°C	Industrial

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage Thresholds ($T_A = T_{OPR}$; V = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDV}	End-of-discharge warning	0.96 * V_{EDV}	V_{EDV}	1.04 * V_{EDV}	V	SB
V_{SRQ}	Valid charge	-	-	-400	µV	$V_{SR} + V_{OS}$
V_{SRD}	Valid discharge	500	-	-	µV	$V_{SR} + V_{OS}$
V_{MCV}	Maximum single-cell voltage	1.95	2.0	2.05	V	SB

Note: For proper operation of the threshold detection circuit, V_{CC} must be at least 1.5V greater than the voltage being measured.

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	3.0	4.25	6.5		V_{CC} excursion from < 2.0V to ≥ 3.0V initializes the unit.
	Reference at 25°C	5.7	6.0	6.3	V	I_{REF} = 5µA
	Reference at -40°C to +85°C	4.5		7.5	V	I_{REF} = 5µA
R_{REF}	Reference input impedance	2.0	5.0		MΩ	V_{REF} = 3V
I_{CC}	Normal operation	-	90	135	µA	V_{CC} = 3.0V, DQ = 0
		-	120	180	µA	V_{CC} = 4.25V, DQ = 0
		-	170	250	µA	V_{CC} = 6.5V, DQ = 0
V_{SB}	Battery input	0	-	V_{CC}	V	
R_{SBmax}	SB input impedance	10	-	-	MΩ	0 < V_{SB} < V_{CC}
I_{DISP}	$\overline{DISP}$ input leakage	-	-	5	µA	V_{DISP} = V_{SS}
I_{LCOM}	LCOM input leakage	-0.2	-	0.2	µA	$\overline{DISP}$ = V_{CC}
I_{RBI}	RBI data-retention current	-	-	100	nA	V_{RBI} > V_{CC} < 3V
R_{DQ}	Internal pulldown	500	-	-	KΩ	
V_{SR}	Sense resistor input	-0.3		2.0		V_{SR} > V_{SS} = discharge; V_{SR} < V_{SS} = charge
R_{SR}	SR input impedance	10			MΩ	-200mV < V_{SR} < V_{CC}
V_{IHPFC}	PROG/SPFC logic input high	Vcc - 0.2	-		V	SPFC, $PROG_{1-4}$
V_{ILPFC}	PROG/SPFC logic input low		-	V_{SS} + 0.2	V	SPFC, $PROG_{1-4}$
V_{IZPFC}	PROG/SPFC logic input Z	float		float	V	SPFC, $PROG_{1-4}$
I_{IHPFC}	PROG/SPFC input high current		1.2		µA	V_{PFC} = V_{CC}/2
I_{ILPFC}	PROG/SPFC input low current	-	1.2		µA	V_{PFC} = V_{CC}/2
V_{OLSL}	SEG_X output low, low Vcc	-	0.1			V_{CC} = 3V, I_{OLS} ≤ 1.75mA SEG_1–SEG_5
V_{OLSH}	SEG_X output low, high Vcc		0.4			V_{CC} = 6.5V, I_{OLS} ≤ 11.0mA SEG_1–SEG_5
V_{OHML}	LCOM output high, low Vcc	Vcc - 0.3	-		V	V_{CC} = 3V, I_{OHLCOM} = -5.25mA
V_{OHMH}	LCOM output high, high Vcc	Vcc - 0.6	-		V	V_{CC} = 6.5V, I_{OHLCOM} = -33.0mA
I_{OHLCOM}	LCOM source current	-33			mA	At V_{OHLCOM} = Vcc - 0.6V
I_{OLS}	SEG_X sink current	11.0			mA	At V_{OLSH} = 0.4V, V_{CC} = 6.5V
I_{OL}	Open-drain sink current	5.0			mA	At V_{OL} = V_{SS} + 0.3V, DQ
V_{OL}	Open-drain output low			0.5	V	I_{OL} ≤ 5mA, DQ
V_{IHDQ}	DQ input high	2.5			V	DQ
V_{ILDQ}	DQ input low			0.8	V	DQ
R_{FLOAT}	Float state external impedance		5		MR	SPFC, $PROG_{1-4}$

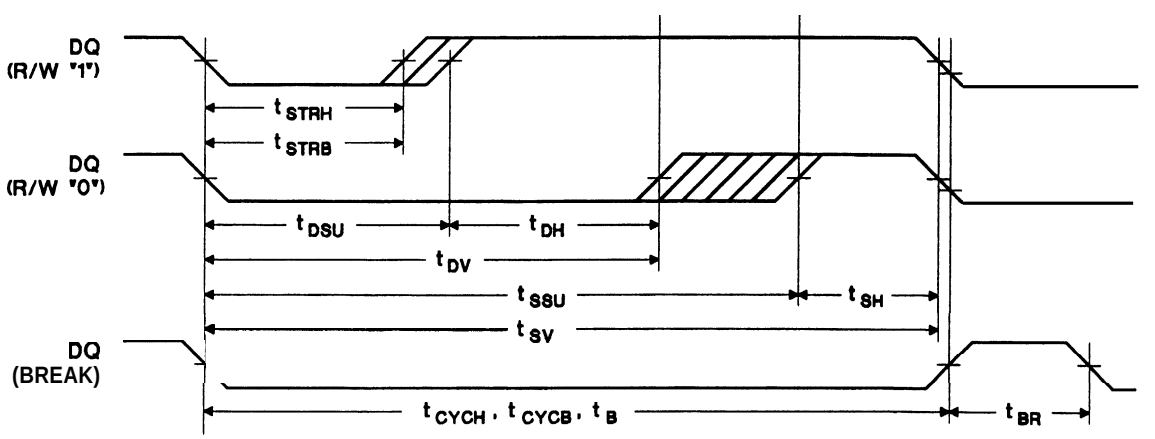
Note: All voltages relative to Vss.

Serial Communication Timing Specification ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYCH}	Cycle time, host to bq2011K	3	-	-	ms	See note
t_{CYCB}	Cycle time, bq2011K to host	3	-	6	ms	
t_{STRH}	Start hold, host to bq2011K	5	-	-	ns	
t_{STRB}	Start hold, bq2011K to host	500	-	-	µs	
t_{DSU}	Data setup	-	-	750	µs	
t_{DH}	Data hold	750	-	-	µs	
t_{DV}	Data valid	1.50	-	-	ms	
t_{SSU}	Stop setup	-	-	2.25	ms	
t_{SH}	Stop hold	700	-	-	µs	
t_{SV}	Stop valid	2.95	-	-	ms	
t_B	Break	3	-	-	ms	
t_{BR}	Break recovery	1	-	-	ms	

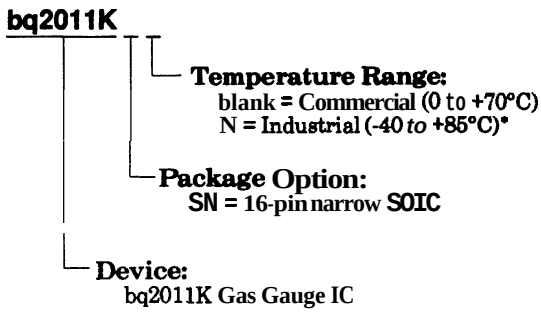
Note: The open-drain DQ pin should be pulled to at least V_{CC} by the host system for proper DQ operation. DQ may be left floating if the serial interface is not used.

Serial Communication Timing Illustration



RC-34

Ordering Information



* Contact factory for availability.

BENCHMARQ

Product Brief **EV2011J/K**

Gas Gauge Evaluation Board

Features

bq2011J/K Gas Gauge IC evaluation and development system

- RS-232 interface hardware for easy access to state-of-charge information via the serial port
- Battery capacity monitoring functions
- LED display of available charge
- DQ serial I/O port comunications functions

General Description

The EV2011J/K provides functional evaluation of the bq2011 IC on a PCB. The actual implementation of a bq2011-based design will be significantly smaller in size. See the bq2011 data sheet (July 1994 C or later) for bq2011 specifications.

A full data sheet for this product is available on our web site (http://www.benchmarq.com), or you may contact the factory for one.

Notes

BENCHMARQ

bq2012

Gas Gauge IC

2

Features

- Conservative and repeatable measurement of available charge in rechargeable batteries
- Charge control output
- Designed for battery pack integration
  - 120µA typical standby current (self-discharge estimation mode)
  - Small size enables implementations in as little as ½ square inch of PCB
- Integrate within a system or as a stand-alone device
  - Display capacity via single-wire serial communication port or direct drive of LEDs
- Measurements compensated for current and temperature
- Self-discharge compensation using internal temperature sensor
- 16-pin narrow SOIC

General Description

The bq2012 Gas Gauge IC is intended for battery-pack or in-system installation to maintain an accurate record of available battery charge. The IC monitors a voltage drop across a sense resistor connected in series between the negative battery terminal and ground to determine charge and discharge activity of the battery.

Self-discharge of NiMH and NiCd batteries is estimated based on an internal timer and temperature sensor. Compensations for battery temperature and rate of charge or discharge are applied to the charge, discharge, and self-discbarge calculations to provide available charge information across a wide range of operating conditions. Battery capacity is automatically recalibrated, or 'learned,' in the course of a discharge cycle from full to empty.

The bq2012 includes a charge control output that, when used with other full-charge safety termination methods, can provide a cost-effective means of controlling charge based on the battery's charge state.

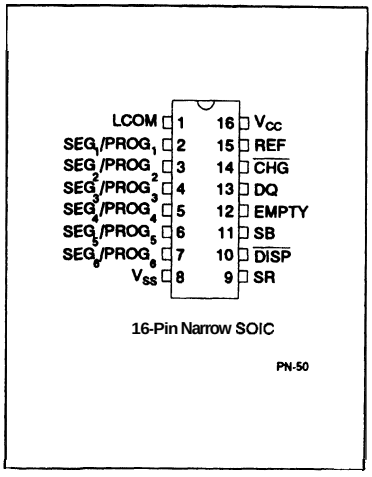
Nominal available charge may be directly indicated using a five- or six-segment LED display. These segments are used to graphically indicate nominal available charge.

The bq2012 supports a simple single-line bidirectional serial link to an external processor (common ground). The bq2012 outputs battery information in response to external commands over the serial link.

Internal registers include available charge, temperature, capacity, battery ID, battery status, and programming pin settings. To support subassembly testing, the outputs may also be controlled. The external processor may also overwrite some of the bq2012 gas gauge data registers.

The bq2012 may operate directly from three or four cells. With the REF output and an external transistor, a simple, inexpensive regulator can be built to provide V_{CC} across a greater number of cells.

Pin Connections



16-Pin Narrow SOIC

PN-50

Pin Names

LCOM	LED common output
$SEG_1/PROG_1$	LED segment 1/ program 1 input
$SEG_2/PROG_2$	LED segment 2/ program 2 input
$SEG_3/PROG_3$	LED segment 3/ program 3 input
$SEG_4/PROG_4$	LED segment 4/ program 4 input
$SEG_5/PROG_5$	LED segment 5/ program 5 input
$SEG_6/PROG_6$	LED segment 6/ program 6 input
REF	Voltage reference output
$\overline{CHG}$	Charge control output
DQ	Serial communications input/output
EMPTY	Empty battery indicator output
SB	Battery sense input
$\overline{DISP}$	Display control input
SR	Sense resistor input
V_{CC}	3.0–6.5V
V_{SS}	System ground

Pin Descriptions

LCOM LED common output

Open-drain output switches V_{CC} to source current for the LEDs. The switch is off during initialization to allow reading of the soft pull-up or pull-down program resistors. LCOM is also high impedance when the display is off.

SEG_1–SEG_6 LED display segment outputs (dual function with $PROG_1$–$PROG_6$)

Each output may activate an LED to sink the current sourced from LCOM.

$PROG_1$–$PROG_2$ Programmed full wunt selection inputs (dual function with SEG_1–SEG_2)

These three-level input pins define the programmed full count (PFC) thresholds described in Table 2.

$PROG_3$–$PROG_4$ Gas gauge rate selection inputs (dual function with SEG_3–SEG_4)

These three-level input pins define the scale factor described in Table 2.

$PROG_5$ Self-discharge rate selection (dual function with SEG_5)

This three-level input pin defines the *self-discharge* compensation rate shown in Table 1.

$PROG_6$ Display mode selection (dual function with SEG_6)

This three-level pin defines the display operation shown in Table 1.

$\overline{CHG}$ Charge control output

This open-drain output becomes active low when charging is allowed. Valid charging conditions are described in the Charge Control section.

SR Sense resistor input

The voltage drop (V_{SR}) across the sense resistor R_S is monitored and integrated over time to interpret charge and discharge activity. The SR input is tied to the high side of the sense resistor. $V_{SR} < V_{SS}$ indicates discharge, and $V_{SR} > V_{SS}$ indicates charge. The effective voltage drop (V_{SRO}) as seen by the bq2012 is $V_{SR} + V_{OS}$ (see Table 5).

$\overline{DISP}$ Display control input

$\overline{DISP}$ high disables the LED display. $\overline{DISP}$ tied to V_{CC} allows $PROG_x$ to connect directly to V_{CC} or V_{SS} instead of through a pull-up or pull-down resistor. $\overline{DISP}$ floating allows the LED display to be active during a valid charge or during discharge if the NAC register is updated at a rate equivalent to $V_{SRO} \leq -4mV$. $\overline{DISP}$ low activates the display. See Table 1.

SB Secondary battery input

This input monitors the single-cell voltage potential through a high-impedance resistive divider network for end-of-discharge voltage (EDV) thresholds, maximum charge voltage (MCV), and battery removed.

EMPTY Battery empty output

This open-drain output becomes high-impedance on detection of a valid end-&-discharge voltage (V_{EDVF}) and is low following the next application of a valid charge.

DQ Serial I/O pin

This is an open-drain bidirectional pin.

REF Voltage reference output for regulator

REF provides a voltage reference output for an optional micro-regulator.

V_{CC} Supply voltage input

V_{SS} Ground

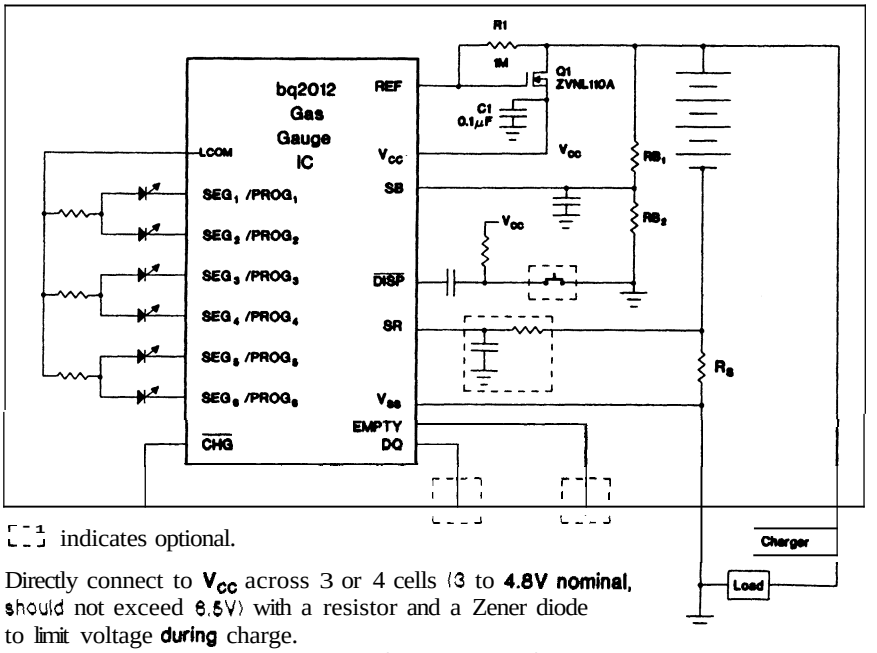
Functional Description

General Operation

The bq2012 determines battery capacity by monitoring the amount of charge input to or removed from a rechargeable battery. The bq2012 measures discharge and charge currents, estimates self-discharge, monitors the battery for low-battery voltage thresholds, and compensates for temperature and charge/discharge rates. The charge measurement is made by monitoring the voltage across a emall-value series sense resistor between the negative battery terminal and ground. The available battery charge is determined by monitoring this voltage over time and correcting the measurement for the environmental and operating conditions.

Figure 1 shows a typical battery pack application of the bq2012 using the LED display capability as a charge-state indicator. The bq2012 can be configured to display capacity in either a relative or an absolute display mode. The relative display mode uses the last measured discharge capacity of the battery as the battery "full" reference. The absolute display mode uses the programmed full count (PFC) as the full reference, forcing each segment of the display to represent a fixed amount of charge. A push-button display feature is available for momentarily enabling the LED display.

The bq2012 monitors the charge and discharge currents as a voltage across a sense resistor (see R_S in Figure 1). A filter between the negative battery terminal and the SR pin may be required if the rate of change of the battery current is too great.



[ ] indicates optional.

Directly connect to V_{CC} across 3 or 4 cells (3 to 4.8V nominal, should not exceed 6.5V) with a resistor and a Zener diode to limit voltage during charge.
Otherwise, R1, C1, and Q1 are needed for regulation of > 4 cells.

Programming resistors (6 max.) and ESD-protection diides are not shown.

R-C on SR may be required (application specific). where the R should not exceed 100K.

Figure 1. Battery Pack Application Diagram-LED Display

Voltage Thresholds

In conjunction with monitoring V_{SR} for charge/discharge currents, the bq2012 monitors the single-cell battery potential through the SB pin. The single-cell voltage potential is determined through a resistor/divider network per the following equation:

$$\frac{RB_1}{RB_2} = N - 1$$

where N is the number of cells, RB_1 is connected to the positive battery terminal, and RB_2 is connected to the negative battery terminal. The single-cell battery voltage is monitored for the end-of-discharge voltage (EDV) and for maximum cell voltage (MCV). EDV threshold levels are used to determine when the battery has reached an 'empty' state, and the MCV threshold is used for fault detection during charging.

Two EDV thresholds for the bq2012 are fixed at:

EDV1 (early warning) = 1.05V

EDVF (empty) = 0.95V

If V_{SB} is below either of the two EDV thresholds, the associated flag is latched and remains latched, independent of V_{SB}, until the next valid charge.

During discharge and charge, the bq2012 monitors V_{SR} for various thresholds. These thresholds are used to compensate the charge and discharge rates. Refer to the count compensation section for details. EDV monitoring is disabled if $V_{SR} \leq -250mV$ typical and resumes ½ second after $V_{SR} > -250mV$.

EMPTY Output

The EMPTY output switches to high impedance when $V_{SB} < V_{EDF}$ and remains latched until a valid charge occurs. The bq2012 also monitors V_{SB} relative to V_{MCV}, 2.25V. V_{SB} falling from above V_{MCV} resets the device.

Reset

The bq2012 recognizes a valid battery whenever V_{SB} is greater than 0.1V typical. V_{SB} rising from below 0.25V or falling from above 2.25V resets the device. Reset can also be accomplished with a command over the serial port as described in the Register Reset section.

Temperature

The bq2012 internally determines the temperature in 10°C steps centered from -35°C to +85°C. The temperature steps are used to adapt charge and discharge rate compensations, self-discharge counting, and available charge display translation. The temperature range is available over the serial port in 10°C increments as shown below:

TMPGG (hex)	Temperature Range
0x	< -30°C
1x	-30°C to -20°C
2x	-20°C to -10°C
3x	-10°C to 0°C
4x	0°C to 10°C
5x	10°C to 20°C
6x	20°C to 30°C
7x	30°C to 40°C
8x	40°C to 50°C
9x	50°C to 60°C
Ax	60°C to 70°C
Bx	70°C to 80°C
Cx	> 80°C

Layout Considerations

The bq2012 measures the voltage differential between the SR and V_{SS} pins. V_{OS} (the offset voltage at the SR pin) is greatly affected by PC board layout. For optimal results, the PC board layout should follow the strict rule of a single-point ground return. Sharing high-current ground with small signal ground causes undesirable noise on the small signal nodes. Additionally:

- The capacitors (SB and V_{CC}) should be placed as close as possible to the SB and V_{CC} pins, respectively, and their paths to V_{SS} should be as short as possible. A high-quality ceramic capacitor of 0.1µf is recommended for V_{CC}.
- The sense resistor (Rs) should be as close as possible to the bq2012.
- The R-C on the SR pin should be located as close as possible to the SR pin. The maximum R should not exceed 100K.

Gas Gauge Operation

The operational overview diagram in Figure 2 illustrates the operation of the bq2012. The bq2012 accumulates a measure of charge and discharge currents, as well as an estimation of self-discharge. Charge and discharge currents are temperature and rate compensated, whereas self-discharge ie only temperature compensated.

The main counter, Nominal Available Charge (NAC), represents the available battery capacity at any given time. Battery charging increments the NAC register, while battery discharging and self-discharge decrement the NAC register and increment the DCR (Discharge Count Register).

The Discharge Count Register (DCR) is used to update the Last Measured Discharge (LMD) register only if a complete battery discharge from full to empty occurs without any partial battery charges. Therefore, the bq2012 adapts its capacity determination baaed on the actual conditions of discharge.

The battery's initial capacity is equal to the programmed full count (PFC) shown in Table 2. Until LMD is updated, NAC counts up to but not beyond this threshold during subsequent charges. This approach allows the gas gauge to be charger-independent and compatible with any type of charge regime.

1. **Last Measured Discharge (LMD) or learned battery capacity:**

   LMD is the last measured discharge capacity of the battery. On initialization (application of Vcc or battery replacement), LMD = PFC. During subsequent discharges, the LMD is updated with the latest measured capacity in the Discharge Count Register (DCR) representing a discharge from full to below EDV1. A qualified discharge is necessary for a capacity transfer from the DCR to the LMD register. The LMD also serves as the 100% reference threshold used by the relative display mode.

2. **Programmed Full Count (PFC) or initial battery capacity:**

   The initial LMD and gas gauge rate values are programmed by using PROG1–PROG4. The PFC also provides the 100% reference for the absolute display mode. The bq2012 is configured for a given application by selecting a PFC value from Table 2. The correct PFC may be determined by multiplying the rated battery capacity in mAh by the sense resistor value:

   Battery capacity (mAh) • sense resistor (Ω) =

   PFC (mVh)

   Selecting a PFC slightly lees than the rated capacity for absolute mode provides capacity above the full reference for much of the battery's life.

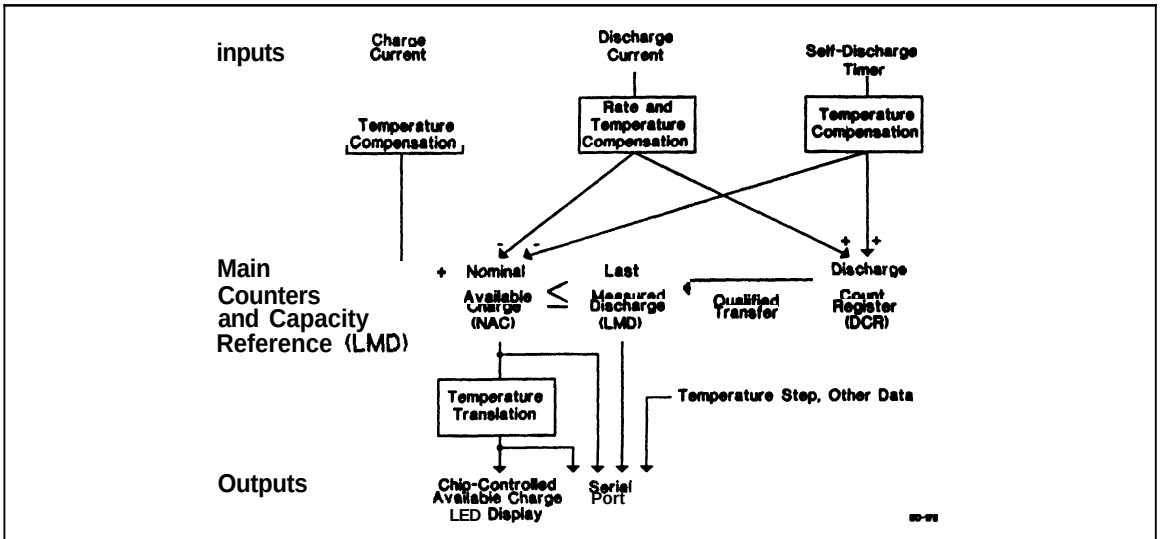


Figure 2. Operational Overview

Example: Selecting a PFC Value

Given:

Sense resistor = 0.1Ω
Number of cells = 6
Capacity = 2200mAh, NiCd battery
Current range = 50mA to 2A
Absolute display mode
Serial port only
Self-discharge = C/64
Voltage drop over sense resistor = 5mV to 200mV

Therefore:

2200mAh * 0.1Ω = 220mVh

Select.

PFC = 33792 counts or 211mVh
$PROG_1$ = float
$PROG_2$ = float
$PROG_3$ = float
$PROG_4$ = low
$PROG_5$ = float
$PROG_6$ = float

The initial full battery capacity is 211mVh (2110mAh) until the bq2012 "learns" a new capacity with a qualified discharge from full to EDV1.

Table 1. bq2012 Programming

Pin Connection	$PROG_5$ Self-Discharge Rate	$PROG_6$ Dbplay Mode	$\overline{DISP}$ Display State
H	Self-diecharge disabled	NAC = PFC on reset	LED disabled
Z	$NAC/64$	Absolute	LED enabled on discharge when V_{SRO} < -4mV or during a valid charge
L	$NAC/47$	Relative	LED on

Note: $PROG_5$ and $PROG_6$ states are independent.

Table 2. bq2012 Programmed Full Count mVh Selections

$PROG_x$		Programmed Full Count (PFC)	$PROG_4$ = L			$PROG_4$ = Z			Units
1	2		$PROG_3$ = H	$PROG_3$ = Z	$PROG_3$ = L	$PROG_3$ = H	$PROG_3$ = Z	$PROG_3$ = L	
-	-	-	Scale = 1/80	Scale = 1/160	Scale = 1/320	Scale = 1/640	Scale = 1/1280	Scale = 1/2560	mVh/ count
H	H	49152	614	307	154	76.8	38.4	19.2	mVh
H	Z	45056	563	282	141	70.4	35.2	17.6	mVh
H	L	40960	512	256	128	64.0	32.0	16.0	mVh
Z	H	36864	461	230	115	57.6	28.8	14.4	mVh
Z	Z	33792	422	211	106	53.0	26.4	13.2	mVh
Z	L	30720	384	192	96.0	48.0	24.0	12.0	mVh
L	H	27648	346	173	86.4	43.2	21.6	10.8	mVh
L	Z	25600	320	160	80.0	40.0	20.0	10.0	mVh
L	L	22528	282	141	70.4	35.2	17.6	8.8	mVh
V_{SR} is equivalent to 2 counts/sec. (nom.)			90	45	22.5	11.25	5.56	2.8	mV

3. Nominal Available Charge **(NAC):**

   NAC count. up during charge to a **maximum** value of LMD and down during discharge and **self-discharge** to **0.** NAC is reset to **0** on initialization **(PROG6 = Z** or low) and **on** reaching EDV1. NAC is set to PFC **on initialization** if PROG6 **=** high. To prevent overstatement of charge during periods of overcharge, NAC stops incrementing when NAC = **LMD.**

4. **Discharge** Count Register (DCR):

   The DCR counts up during discharge independent of NAC and could continue increasing after NAC has decremented to **0. DCR stops** counting when EDV1 is **reached.** Prior to NAC = **0** (empty battery), both discharge and self-discharge increment the DCR **After** NAC **= 0,** only discharge increments the DCR The DCR resets to **0** when NAC = LMD. **The** DCR **does** not **roll** over but stops counting when it **reaches FFFFh.**

   The DCR value becomes the new LMD value on the first charge after a valid discharge to V_{EDV1} if:

   No valid charge initiations **(charges** greater than 256 NAC counts; where $V_{SRO} > V_{SRQ}$) occurred during the period between NAC = LMD and EDV1 detected.

   The self-discharge count is not more than 4096 counts (8% to 18% of PFC, specific percentage threshold determined by PFC).

   The temperature is 2 **0°C** when the EDV1 level **is** reached during discharge.

   The valid discharge flag (VDQ) indicates whether the present discharge is valid for LMD update.

Charge Counting

Charge activity is detected **based** on a **positive** voltage on the V_{SR} input. If charge activity **is** detected, the **bq2012** increments NAC at a rate proportional to V_{SRO} **(V_{SR} + V_{OS})** and, if enabled, activates the LED display if the rate is equivalent to V_{SRO} > 4mV. Charge actions increment the NAC after compensation for charge rate and temperature.

The **bq2012** determines charge activity sustained at a continuous rate equivalent to $V_{SRO} > V_{SRQ}$. A valid charge equates to sustained charge activity greater than 256 NAC **counts. Once** a valid charge is detected, charge counting continues until V_{SRO} **falls** below V_{SRQ}. V_{SRQ} is a programmable threshold as **described** in the Digital Magnitude **Filter** section. The default value for V_{SRQ} **is** 375µV.

Charge Control

Charge **control** is provided by the $\overline{CHG}$ output. This output is **asserted continuously when:**

NAC < 0.94 • LMD and
0.95V < V_{SB} < 2.25V and
0°C < Temp < 50°C and
BRM = 0

This output is **asserted** at a **1/16** duty cycle (low for 0.5 **sec** and **high** for 7.6 **sec)** when the above conditions are not met and:

NAC < LMD and
0.95V < V_{SB} < 2.25V and
Temp < 50°C and
BRM = 0

This output is also asserted at a 1/16 duty cycle (low for 0.5 sec and high for 7.5 sec) for a 2-hour top-off period after:

NAC = LMD and
Temp **< 50°C and**
0.95V < V_{SB} < 2.25V and
BRM = 0

This output is inactive **when:**

NAC = LMD (after a 2-hour **top-off period) or**
Temp **> 50°C** *or*
V_{SB} < 0.95V or
V_{SB} > 2.25V or
BRM = 1

The top-off timer (2 **hours)** is **reset** to allow another top-off after the battery **is** discharged to 0.8 • **LMD (PROG6 = L) or 0.8 • PFC (PROG6 = Z or H).**

Caution: **The** charge control output ($\overline{CHG}$) **should** be used with other forms **of charge** termination such **as** $\Delta T/\Delta t$ **and -ΔV.**

If charge terminates due to maximum temperature, the battery temperature must fall **typically 10°C** below **50°C** before the charge output becomes active again.

Discharge Counting

All discharge counts where $V_{SRO} < V_{SRD}$ **cause** the NAC register to decrement and the DCR to increment. **Exceeding** the fast diecharge **threshold** (FDQ) if the rate is equivalent to V_{SRO} < -4mV **activates** the display, if enabled. The **display** becomes inactive after V_{SRO} rises above -4mV. V_{SRD} is a programmable threshold as described in the Digital Magnitude Filter section. The default value for V_{SRD} is **-300µV.**

Self-Discharge Estimation

The bq2012 continuously decrements NAC and increments [illegible] based on time and temperature. The self-discharge count rate is programmed to be a nominal 1/64 • NAC or 1/47 • NAC per day or disabled as selected by PROG5. This is the rate for a battery whose temperature is between 20°–30°C. The NAC register cannot be decremented below 0.

Count Compensations

The bq2012 determines fast charge when the NAC updates at a rate of ≥2 counts/sec. Charge and discharge are compensated for temperature and charge/discharge rate before updating the NAC and/or DCR. Self-discharge estimation is compensated for temperature before updating the NAC or DCR.

Charge Compensation

Two charge efficiency compensation factors are used for trickle charge and fast charge. Fast charge is defined as a rate of charge resulting in ≥ 2 NAC counts/sec (2 0.15C to 0.32C depending on PFC selections; see Table 2). The compensation defaults to the fast charge factor until the actual charge rate is determined.

Temperature adapts the *charge* rate compensation factor6 over three range8 between nominal, warm, and hot tempera[illegible] The compensation factors are shown below.

Charge Temperature	Trickle Charge Compensation	Fast Charge Compensation
<30°C	0.80	0.95
30–40°C	0.75	0.90
> 40°C	0.65	0.80

Discharge Compensation

Corrections for the rate of discharge are made by adjusting an internal *discharge* compeneation factor. The discharge factor is based on the dynamically measured V_{SR}. The compeneation factors during discharge are:

Approximate V_{SR} Threshold	Discharge Compensation Factor	Efficiencv
V_{SR} > -160 mV	1.00	100%
V_{SR} < -150 mV	1.05	95%

Temperature compensation during discharge also takes place. At lower temperatures, the compensation factor increases by 0.05 for each 10°C temperature range below 10°C.

Compensation factor = 1.0 + (0.05 • N)

Where N = Number of 10°C steps below 10°C and -150mV < V_{SR} < 0.

For example:

T > 10°C : Nominal compensation, N = 0

0°C < T < 10°C: N = 1 (i.e., 1.0 becomes 1.05)

-10°C < T < OOC: N = 2 (i.e., 1.0 become81.10)

-20°C < T < -10°C: N = 3 (i.e., 1.0 becomes 1.15)

-20°C < T < -30°C: N = 4 (i.e., 1.0 becomes 1.20)

Self-Discharge Compensation

The self-discharge compensation is programmed for a nominal rate of 1/64 • NAC or 1/47 • NAC per day. This is the rate for a battery within the 20–30°C temperature range (TMPGG = 6x). This rate varies across 8 ranges from <10°C to >70°C, doubling with each higher temperature step (10°C). See Table 3.

Table 3. Self-Discharge Compensation

Temperature Step	Typical Rate	
	PROG5 = Z or H	PROG5 = L
< 10°C	NAC/256	NAC/188
10–20°C	NAC/128	NAC/94
20–30°C	NAC/64	NAC/47
30–40°C	NAC/32	NAC/23.5
40–50°C	NAC/16	NAC/11.8
50–60°C	NAC/8	NAC/5.88
60–70°C	NAC/4	NAC/2.94
> 70°C	NAC/2	NAC/1.47

Digital Magnitude Filter

The bq2012 has a programmable digital filter to eliminate charge and discharge counting below a set threshold. The default setting is -0.30mV fa- V_{SRD} and +0.38mV fa- V_{SRQ}. The proper digital filter setting can be calculated using the following equation. Table 4 shows typical digital filter settings.

$$V_{SRD}\ (mV) = -45 / DMF$$

$$V_{SRQ}\ (mV) = -1.25 \cdot V_{SRD}$$

Table 4. Typical Digital Filter Settings

DMF	DMF Hex.	V_{SRD} (mV)	V_{SRQ} (mV)
75	4B	-0.60	0.75
100	64	-0.45	0.56
150 (default)	96	-0.30	0.38
175	AF	-0.26	0.32
200	C8	-0.23	0.28

Error Summary

Capacity Inaccurate

The LMD ia susceptible to error on initialization or if no updates occur. On initialization, the LMD value includes the error between the programmed full capacity and the actual capacity. This error is present until a valid discharge occurs and LMD is updated (see DCR description). The other cause of LMD error is battery wear-out. As the battery ages, the measured capacity must be adjusted to account for changes in actual battery capacity.

A Capacity Inaccurate counter (CPI) is maintained and incremented each time a valid charge occurs (qualified by NAC; see the CPI register description) and is reset whenever LMD is updated from the DCR. The counter does not wrap around but stops counting at 255. The capacity inaccurate flag (CI) is set if LMD has not been updated following 64 valid charges.

Current-Sensing Error

Table 5 illustrates the current-sensing error as a function of V_{SR}. A digital filter eliminates charge and discharge counts to the NAC register when V_{SRO} (V_{SR} + V_{OS}) is between V_{SRQ} and V_{SRD}.

Communicating With the bq2012

The bq2012 includes a simple single-pin (DQ plus return) serial data interface. A host processor uses the interface to access various bq2012 registers. Battery characteristics may be easily monitored by adding a single contact to the battery pack. The open-drain DQ pin on the bq2012 should be pulled up by the host system, or may be left floating if the serial interface is not used.

The interface uses a command-based protocol, where the host processor sends a command byte to the bq2012. The command dicta the bq2012 to either store the next eight bits of data received to a register specified by the command byte or output the eight bits of data specified by the command byte.

The communication protocol is asynchronous return-tu one. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 333 bits/sec. The least-significant bit of a command or data byte is transmitted first. The protocol is simple enough that it can be implemented by most host processors *wing* either polled or interrupt processing. Data input from the bq2012 may be sampled using the pulse-width capture *timers* available *on some* microcontrollers.

Communication is normally initiated by the host processor sending a BREAK command to the bq2012. A BREAK is detected when the DQ pin is driven to a logic-low state for a time, t_B or greater. The DQ pin should then be returned to its normal ready-high logic state for a time, t_{BR}. The bq2012 is now ready to receive a command from the hoet processor.

The return-to-one data bit kame consists of three distinct sections. The first section is used to start the transmission by either the host or the bq2012 taking the DQ pin to a logic-low state for a period, $t_{STRH,B}$. The next section is the actual data transmission, where the data should be valid by a period, t_{DSU}, after the negative edge used to start communication. The data should be held for a period, t_{DV}, to allow the host or bq2012 to sample the data bit.

The final section is used to stop the transmission by returning the DQ pin to a logic-high state by at least a period, t_{SSU}, after the negative edge used to start communication. The final logic-high state should be held until a period, t_{SV}, to allow time to ensure that the bit transmission was stopped properly. The timings for data and *break* communication are given in the aerial communication timing specification and illustration sections.

Communication with the bq2012 is always performed with the least-significant bit being transmitted first. Figure 3 shows an example of a communication sequence to read the bq2012 NAC register.

bq2012 Registers

The bq2012 command and status registers are listed in Table 6 and described in the following sections.

Table 5. Current-Sensing Error as a Function of V_{SR}

Symbol	Parameter	Typical	Maximum	Units	Notes
V_{OS}	Offset referred to V_{SR}	± 50	± 150	µV	$\overline{DISP}$ = V_{CC}.
INL	Integrated non-linearity error	± 2	± 4	%	Add 0.1% per °C above or below 25°C and 1% per volt above or below 4.25V.
INR	Integrated non-repeatability error	± 1	± 2	%	Measurement repeatability given similar operating conditions.

Table 6. bq2012 Command and Status Registers

symbol	Register Name	Loc. (hex)	Read/ Write	Control Field							
				7(MSB)	6	5	4	3	2	1	0(LSB)
CMDR	Command register	00h	Write	W/$\overline{R}$	AD6	AD5	AD4	AD3	AD2	AD1	AD0
FLGS1	Primary status flags register	01h	Read	CHGS	BRP	B	CI	VDQ		EDV1	EDVF
TMPGG	Temperature and gas gauge register	02h	Read	TMP3	TMP2	TMP1	TMP0	GG3	GG2	GG1	GG0
NACH	Nominal available charge high byte register	03h	R/W	NACH7	NACH6	NACH5	NACH4	NACH3	NACH2	NACH1	NACH0
NACL	Nominal available charge low byte register	17h	Read	NACL7	NACL6	NACL5	NACL4	NACL3	NACL2	NACL1	NACL0
BATID	Battery identification register	04h	R/W	BATID7	BATID6	BATID5	BATID4	BATID3	BATID2	BATID1	BATID0
LMD	Last measured discharge register	05h	R/W	LMD7	LMD6	LMD5	LMD4	LMD3	LMD2	LMD1	LMD0
FLGS2	Secondary status flags register	06h	Read	CR	DR2	DR1	DR0	n/u	n/u	n/u	OVLD
PPD	Program pin pull-down register	07h	Read	n/u	n/u	PPD6	PPD5	PPD4	PPD3	PPD2	PPD1
PPU	Program pin pull-up register	08h	Read	n/u	n/u	PPU6	PPU5	PPU4	PPU3	PPU2	PPU1
CPI	Capacity inaccurate count register	09h	Read	CPI7	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	CPI0
DMF	Digital magnitude filter register	0ah	R/W	DMF7	DMF6	DMF5	DMF4	DMF3	DMF2	DMF1	DMF0
RST	Reset register	39h	Write	RST	0	0	0	0	0	0	0

Note: n/u = not used

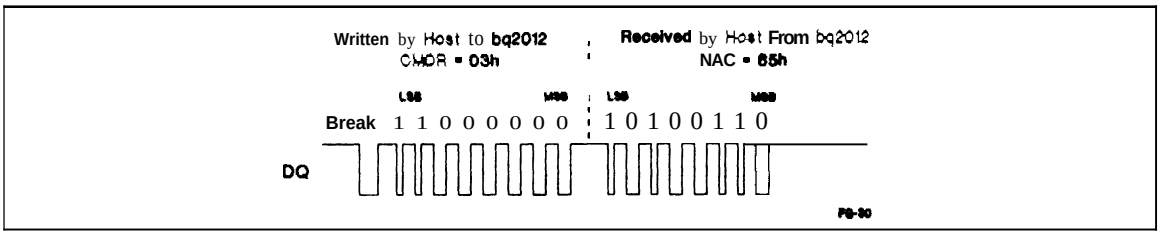


Figure 3. Typical Communication With the bq2012

Command Register (CMDR)

The write-only CMDR register is accessed when eight valid command bits have been received by the bq2012. The CMDR register contains two fields:

- W/$\overline{R}$ bit
- Command address

The W/$\overline{R}$ bit of the command register is used to select whether the received command is for a read or a write function.

The W/$\overline{R}$ values are:

CMDR Bits							
7	6	5	4	3	2	1	0
W/$\overline{R}$	-	-	-	-	-	-	-

Where W/$\overline{R}$ is:

0 The bq2012 outputs the requested register contents specified by the address portion of CMDR

1 The following eight bits should be written to the register specified by the address portion of CMDR

The lower seven-bit field of CMDR contains the address portion of the register to be accessed. Attempts to write to invalid addresses are ignored.

CMDR Bits							
7	6	5	4	3	2	1	0
-	AD6	AD5	AD4	AD3	AD2	AD1	AD0 (LSB)

Primary Status Flags Register (FLGS1)

The read-only FLGSl register (address=01h) contains the primary bq2012 flags.

The *charge status* flag (CHGS) is asserted when a valid charge rate is detected. Charge rate is deemed valid when $V_{SRO} > V_{SRQ}$. A V_{SRO} of less than V_{SRQ} or discharge activity clears CHGS.

The CHGS values are:

FLGSl Bits							
7	6	5	4	3	2	1	0
CHGS	-						

Where CHGS is:

0 Either discharge activity detected or $V_{SRO} < V_{SRQ}$

1 $V_{SRO} > V_{SRQ}$

The *battery* replaced flag (BRP) is asserted whenever the potential on the SB pin (relative to V_{SS}), V_{SB}, falls from above the maximum cell voltage. MCV (2.25V), or rises above 0.1V. The BRP flag is also set when the bq2012 is reset (see the RST register description). BRP is reset when either a valid charge action increments NAC to be equal to LMD, or a valid charge action is detected after the EDVl flag is asserted. BRP = 1 signifies that the device has been reset.

The BRP values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	BRP	-	-	-	-	-	-

Where BRP is:

0 Battery is charged until NAC = LMD or discharged until the EDVl flag is asserted

1 V_{SB} dropping from above MCV, V_{SB} rising from below 0.1V, or a serial port initiated reset has occurred

The ***battery removed*** flag (BRM) is asserted whenever the potential on the SB pin (relative to Vss) rises above MCV or falls below 0.1V. The BRM flag is asserted until the condition causing BRM is removed.

The BRM values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	BRM	-	-	-	-	-

Where BRM is:

0 $0.1V < V_{SB} < 2.25V$

1 $0.1\ V > V_{SB}$ or $V_{SB} > 2.25V$

The ***capacity*** inaccurate flag (CI) is used to warn the user that the battery has been charged a substantial number of times since LMD has been updated. The CI flag is asserted on the 64th charge after the last LMD update or when the bq2012 is reset. The flag is cleared after an LMD update.

The CI values *are:*

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	CI	-	-	-	-

Where CI is:

0 When LMD is updated with a valid full discharge

1 After the 64th valid charge action with no LMD updates

The ***valid discharge*** flag (VDQ) is asserted when the bq2012 is discharged from NAC = LMD. The flag remains set until either LMD is updated or one of three actions that can clear VDQ occurs:

- The self-discharge count register (SDCR) has exceeded the maximum acceptable value (4096 counts) for an LMD update.
- A valid charge action sustained at $V_{SRO} > V_{SRQ}$ for at least 256 NAC *counts.*
- The EDV1 flag was set at a temperature below 0°C

The VDQ values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
			-	VDQ	-		

Where VDQ is:

0 SDCR ≥ 4096, subsequent valid charge action detected, or EDV1 is asserted with the temperature less than 0°C

1 On first discharge after NAC = LMD

The ***charge control*** flag, $\overline{CHG}$, is *asserted* whenever the $\overline{CHG}$ pin is asserted (see the charge control section on page 7 for a description of the CHG pin function).

The $\overline{CHG}$ values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
				-	$\overline{CHG}$	-	-

Where $\overline{CHG}$ is:

0 When the $\overline{CHG}$ pin is asserted active low, signifying that the bq2012 is in a state to allow charge activity.

1 When the $\overline{CHG}$ pin is high-impedance, signifying that no charge activity should take place.

The ***first end-of-discharge warning*** flag (EDV1) warns the user that the battery is almost empty. The first segment pin, SEG_1, is modulated at a 4 Hz rate if the display is enabled once EDV1 is asserted, which should warn the user that loss of battery power is imminent. The EDV1 flag is latched until a valid charge has been detected.

The EDV1 values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
					-	EDV1	-

Where EDV1 is:

0 Valid charge action detected, $V_{SB} \geq 1.05V$

1 $V_{SB} < 1.05V$ providing that OVLD=0 (see FLGS2 register description)

The ***final end-of-discharge warning*** flag (EDVF) flag is used to warn that battery power is at a failure condition. All segment drivers are turned off. The EDVF flag is latched until a valid charge has been detected. The EMPTY pin is also forced to a high-impedance state on assertion of EDV1. The host system may pull EMPTY high, which may be used to disable circuitry to prevent deep-discharge of the battery.

The EDVF values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
						-	EDVF

Where EDVF is:

0 Valid charge action detected, $V_{SB} \geq 0.95V$

1 $V_{SB} < 0.95V$ providing that OVLD=0 (see FLGS2 register description)

Temperature and Gas Gauge Register (TMPGG)

The read-only TMPGG register (address=02h) contains two data fields. The first field contains the battery temperature. The second field contains the available charge from the battery.

TMPGG Temperature Bits							
7	6	5	4	3	2	1	0
TMP3	TMP2	TMP1	TMP0	-			

The bq2012 contains an internal temperature sensor. The temperature is used to set charge and discharge efficiency factors as well as to adjust the self-discharge coefficient.

The temperature register contents may be translated as shown in Table 7.

The bq2012 calculates the available charge as a function of NAC, temperature, and a full reference, either LMD or PFC. The results of the calculation are available via the display port or the gas gauge field of the TMPGG register. The register is used to give available capacity in 1/16 increments from 0 to 15/16.

TMPGG Gas Gauge Bits							
7	6	5	4	3	2	1	0
			-	GG3	GG2	GG1	GG0

The gas gauge display and the gas gauge portion of the TMPGG register are adjusted for cold temperature dependencies. A piece-wise correction is performed as follows:

Temperature	Available Capacity Calculation
> 0°C	NAC / "Full Reference"
-20°C < T < 0°C	0.75 • NAC / 'Full Reference'
< -20°C	0.5 • NAC / "Full Reference'

Table 7. Temperature Register Translation

TMP3	TMP2	TMP1	TMP0	Temperature
0	0	0	0	T < -30°C
0	0	0	1	-30°C < T < -20°C
0	0	1	0	-20°C < T < -10°C
0	0	1	1	-10°C < T < 0°C
0	1	0	0	0°C < T < 10°C
0	1	0	1	10°C < T < 20°C
0	1	1	0	20°C < T < 30°C
0	1	1	1	30°C < T < 40°C
1	0	0	0	40°C < T < 50°C
1	0	0	1	50°C < T < 60°C
1	0	1	0	60°C < T < 70°C
1	0	1	1	70°C < T < 80°C
1	1	0	0	T > 80°C

The adjustment between > 0°C and -20°C < T < 0°C has a 10°C hysteresis.

Nominal Available Charge Registers (NACH/NACL)

The read/write NACH high-byte register (address=03h) and the read-only NACL low-byte register (address=17h) are the main gas gauging register for the bq2012. The NAC registers are incremented during charge actions and decremented during discharge and self-discharge actions. The correction factors for charge/discharge efficiency are applied automatically to NAC.

On reset, if $PROG_6$ = Z or low, NACH and NACL are cleared to 0; if $PROG_6$ = high, NACH = PFC and NACL = 0. When the bq2012 detects a valid EDVI, NACH and NACL are reset to 0. Writing *to the NAC registers affects the avaibbk charge counts and, therefore, affects the bq2012 gas gauge operation. Do not write the NAC registers to a value greater than LMD.*

Battery Identification Register (BATID)

The read/write BATID register (address=04h) is available for use by the system to determine the type of battery pack. The BATID contents are retained as long as Vcc is greater than 2V. The contents of BATID have no effect on the operation of the bq2012. There is no default setting for this register.

Last Measured Discharge Register (LMD)

LMD is a read/write register (address=05h) that the bq2012 uses as a measured full reference. The bq2012

adjusts LMD based on the measured discharge capacity of the battery from full to empty. In this way the bq2012 updates the capacity of the battery. WID is set to PFC during a bq2012 reset.

Secondary Status Flags Register (FLGS2)

The read-only FLGS2 register (address=06h) contains the secondary bq2012 flags.

The charge *rate* flag (CR) is used to denote the fast charge regime. Fast charge is assumed whenever a charge action is initiated. The CR flag remains asserted if the charge rate does not fall below 2 counts/sec.

The CR values are:

FLGS2 Bits							
7	6	5	4	3	2	1	0
CR	-	-	-	-	-	-	-

Where CR is:

0 When charge rate falls below 2 counts/sec

1 When charge rate is above 2 counts/sec

The fast charge regime efficiency factors are used when CR = 1. When CR = 0, the trickle charge efficiency factors are used. The time to change CR varies due to the user-selectable count rates.

The ***discharge*** rate flags, DR2–0, are bits 6-4.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	DR2	DR1	DR0	-	-	-	

They are used to determine the current discharge regime as follows:

DR2	DR1	DRO	V_{SR} (V)
0	0	0	$V_{SR} > -150mV$
0	0	1	$V_{SR} < -150mV$

The ***overload*** flag (OVLD) is asserted when a discharge overload is detected, $V_{SR} < -250mV$. OVLD remains asserted as long as the condition persists and is cleared when $V_{SR} > -250mV$. The overload condition is used to stop sampling of the battery terminal characteristics for end-of-discharge determination. Sampling is re-enabled 0.5 secs after the overload condition is removed.

FLGS2 Bits							
7	6	5	4	3	2	1	0
						-	OVLD

DR2–0 and OVLD are set based on the measurement of the voltage at the SR pin relative to Vss. The rate at which this measurement is made varies with device activity.

Program Pin Pull-Down Register (PPD)

The read-only PPD register (address=07h) contains some of the programming pin information for the bq2012. The segment drivers, SEG_{1-6}, have a corresponding PPD register location, PPD_{1-6}. A given location is set if a pull-down resistor has been detected on its corresponding segment driver. For example, if SEG_1 and SEG_4 have pull-down resistors, the contents of PPD are xx001001.

Program Pin Pull-Up Register (PPU)

The read-only PPU register (address=08h) contains the rest of the programming pin information for the bq2012. The segment drivers, SEG_{1-6}, have a corresponding PPU register location, PPU_{1-6}. A given location is set if a pull-up resistor has been detected on its corresponding segment driver. For example, if SEG_3 and SEG_6 have pull-up resistors, the contents of PPU are xx100100.

PPD/PPU Bits							
8	7	6	5	4	3	2	1
-	-	PPU_6	PPU_5	PPU_4	PPU_3	PPU_2	PPU_1
-	-	PPD_6	PPD_5	PPD_4	PPD_3	PPD_2	PPD_1

Capacity Inaccurate Count Register (CPI)

The read-only CPI register (address=09h) is used to indicate the number of times a battery has been charged without an LMD update. Because the capacity of a rechargeable battery varies with age and operating conditions, the bq2012 adapts to the changing capacity over time. A complete discharge from full (NAC=LMD) to empty (EDV1=1) is required to perform an LMD update assuming there have been no intervening valid charges, the temperature is greater than or equal to 0°C, and the self-discharge counter is lees than 4096 counts.

The CPI register is incremented every time a valid charge is detected if NAC < 0.94 • LMD. When NAC ≥ 0.94 • LMD, the CPI register increments on the first valid charge; CPI does not increment again for a valid charge until NAC is discharged below 0.94 • LMD. This prevents continuous trickle charging from incrementing CPI if self-discharge decrements NAC. The CPI register increments to 255 without rolling over. When the contents of CPI are incremented to 64, the capacity inaccurate flag, CI, is asserted in the FLGS1 register. The CPI register is reset whenever an update of the LMD register is performed, and the CI flag is also cleared.

Digital Magnitude Filter (DMF)

The read-write **DMF register (address** = Oah) provides the **system** with a means to change the default **settings** of the digital magnitude filter. By writing different values **into** this register, the **limits** of V_{SRD} and V_{SRQ} can be adjusted.

Note: Care should be taken when writing to this register. A V_{SRD} and V_{SRQ} below the specified Vos may adversely affect the accuracy of the **bq2012.** Refer to Table 4 for recommended **settings** for the **DMF register.**

Reset Register (RST)

The reset register **(address=39h)** provides the **means** to perform a software-controlled **reset** of the device. By writing the RST register **contents from 00h** to 80h, a **bq2012 reset** is **performed.** ***Setting*** any ***bit*** other ***than the most-significant bit of the RST*** register ***is not allowed, and results*** in ***improper operation of the bq2012.***

Resetting the **bq2012 sets** the following:

- LMD = **PFC**
- **CPI, VDQ,** NACH, and **NACL = 0**
- **CI and BRP = 1**

Note: NACH = **PFC** when $PROG_6$ = H.

Display

The **bq2012** can directly display capacity information using low-power LEDs. If **LEDs** are **used,** the program pine should be resietively tied to V_{CC} or **Vss** for a program high or program low, respectively.

The bq2012 displays the battery charge **state** in either absolute or relative mode. In relative mode, the battery charge is represented as a percentage of the LMD. Each **LED** segment **represents 20%** of the LMD. The sixth segment is not used.

In absolute mode, each segment represente a fixed amount of charge, **based** on the initial PFC. In absolute mode, each segment represents **20%** of the PFC, with the sixth segment **representing** *overfull' (charge above the **PFC). As the** battery **wears** out over time, it is **possible** for the LMD to be below the initial PFC. In this case, all of **the** LEDs ***may*** not turn on, **representing** the reduction in the actual **battery** capacity.

The capacity display **is also** adjusted for **the** present battery temperature. The temperature adjustment reflects the available **capacity** at a given temperature but does not **affect the** NAC register. The temperature **adjustmenta** ***are*** detailed in the TMPGG register **description.**

When $\overline{DISP}$ **is tied** to V_{CC}, the SEG_{1-6} **outputs are** inactive. **When** $\overline{DISP}$ **is left** floating, the **display** becomes active **whenever** the NAC **registers** ***are*** counting at a rate equivalent to $V_{SRO} < -4mV$ or $V_{SRO} > V_{SRQ}$. When pulled low, **the segment outputs** became active immediately. A capacitor tied to $\overline{DISP}$ allows the **display** to remain active for a short period of time after **activation** by a push-button switch.

The segment outputa are modulated as two banks of three, **with segments** 1, 3, and 5 alternating with **segmenta** 2, 4, and 6. The **segment outputs are** modulated at approximately **100Hz** with **each** segment bank active for 30% of the period.

SEG_1 **blinks** at a 4Hz **rate** whenever V_{SB} has been detected to be below V_{EDV1} **(EDV1 = 1),** indicating a low-**battery** condition. V_{SB} below V_{EDVF} **(EDVF = 1)** disables the display output.

Microregulator

The **bq2012** can operate directly from three or four **cells.** To facilitate the power supply requirements of the **bq2012,** an REF output is provided to regulate an external low-*hold **n-FET.** A **micropower source** for the **bq2012** can be inexpensively **built** using the FET and an external resistor; eee Figure 1.

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to Vss	-0.3	+7.0	V	
All other pine	Relative to Vss	-0.3	+7.0	V	
REF	Relative to Vss	-0.3	+8.5	V	Current limited by R1 (see Figure 1)
V_{SR}	Relative to Vss	-0.3	+7.0	V	Minimum 100Ω series resistor should be used to protect SR in case of a shorted battery (see the bq2012 applicationnote for details).
T_{OPR}	Operating temperature	0	+70	°C	Commercial
		-40	+85	°C	Industrial

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage Thresholds ($T_A = T_{OPR}$; V = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDVF}	Final empty warning	0.93	0.95	0.97	V	SB
V_{EDV1}	First empty warning	1.03	1.05	1.07	V	SB
V_{SR1}	Discharge compensation threshold	-120	-150	-180	mV	SR, V_{SR} + V_{OS} (see note 2)
V_{ORD}	Overload threshold	-230	-250	-280	mV	SR, V_{SR} + V_{OS}
V_{SRO}	SR sense range	-300	-	+2000	mV	SR, V_{SR} + V_{OS}
V_{SRQ}	Valid charge	375	-	-	µV	V_{SR} + V_{OS} (see note 1)
V_{SRD}	Valid discharge	-	-	-300	µV	V_{SR} + V_{OS} (see note 1)
V_{MCV}	Maximum single-cell voltage	2.20	2.25	2.30	V	SB
V_{BR}	Battery removed/replaced	-	0.1	0.25	V	SB pulled low
		2.20	2.25	2.30	V	SB pulled high

Notes:
1. Default value; value set in DMF register. V_{OS} is affected by PC board layout. Proper layout guidelines should be followed for optimal performance. See "LayoutConsiderations."
2. Proper threshold measurements require V_{CC} to be more than 1.5V greater than the desired signal value.

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	3.0	4.25	6.5	V	V_{CC} excursion from < 2.0V to ≥ 3.0V initializes the unit.
V_{REF}	Reference at 25°C	5.7	6.0	6.3	V	I_{REF} = 5µA
	Reference at -40°C to +85°C	4.5	-	7.5	V	I_{REF} = 5µA
R_{REF}	Reference input impedance	2.0	5.0	-	MΩ	V_{REF} = 3V
I_{CC}	Normal operation	-	90	135	µA	V_{CC} = 3.0V
		-	120	180	µA	V_{CC} = 4.25V
		-	170	250	µA	V_{CC} = 6.5V
V_{SB}	Battery input	-	-	2.4	V	
R_{SBmax}	SB input impedance	10	-	-	MΩ	$0 < V_{SB} < V_{CC}$
I_{DISP}	$\overline{DISP}$ input leakage	-	-	5	µA	$V_{DISP} = V_{SS}$
I_{LCOM}	LCOM input leakage	-0.2	-	0.2	µA	$\overline{DISP} = V_{CC}$
R_{DQ}	Internal pulldown	500	-	-	KΩ	
V_{SR}	Sense resistor input	-0.3	-	2.0	V	$V_{SR} < V_{SS}$ = discharge; $V_{SR} > V_{SS}$ = charge
R_{SR}	SR input impedance	10	-	-	MΩ	-200mV < V_{SR} < V_{CC}
V_{IH}	Logic input high	V_{CC} - 0.2	-	-	V	$PROG_1$–$PROG_6$
V_{IL}	Logic input low	-	-	V_{SS} + 0.2	V	$PROG_1$–$PROG_6$
V_{IZ}	Logic input Z	float	-	float	V	$PROG_1$–$PROG_6$
V_{OLSL}	SEG_X output low, low V_{CC}	-	0.1	-	V	V_{CC} = 3V, I_{OLS} ≤ 1.75mA SEG_1–SEG_6
V_{OLSH}	SEG_X output low, high V_{CC}	-	0.4	-	V	V_{CC} = 6.5V, I_{OLS} ≤ 11.0mA SEG_1–SEG_6
V_{OHLCL}	LCOM output high, low V_{CC}	V_{CC} - 0.3	-	-	V	V_{CC} = 3V, I_{OHLCOM} = -5.25mA
V_{OHLCH}	LCOM output high, high V_{CC}	V_{CC} - 0.6	-	-	V	V_{CC} = 6.5V, I_{OHLCOM} = -33.0mA
I_{IH}	$PROG_{1-6}$ input high current	-	1.2	-	µA	$V_{PROG} = V_{CC}/2$
I_{IL}	$PROG_{1-6}$ input low current	-	1.2	-	µA	$V_{PROG} = V_{CC}/2$
I_{OHLCOM}	LCOM source current	-33	-	-	mA	At $V_{OHLCH} = V_{CC}$ - 0.6V
I_{OLS}	SEG_X sink current	-	-	11.0	mA	At V_{OLSH} = 0.4V
I_{OL}	Open-drain sink current	-	-	5.0	mA	At $V_{OL} = V_{SS}$ + 0.3V DQ, EMPTY, $\overline{CHG}$
V_{OL}	Open-drain output low	-	-	0.5	V	I_{OL} ≤ 5mA, DQ, EMPTY
V_{IHDQ}	DQ input high	2.5	-	-	V	DQ
V_{ILDQ}	DQ input low	-	-	0.8	V	DQ
R_{PROG}	Soft pull-up or pull-down resistor value (for programming)	-	-	200	KΩ	$PROG_1$–$PROG_6$
R_{FLOAT}	Float state external impedance	-	5	-	MΩ	$PROG_1$–$PROG_6$

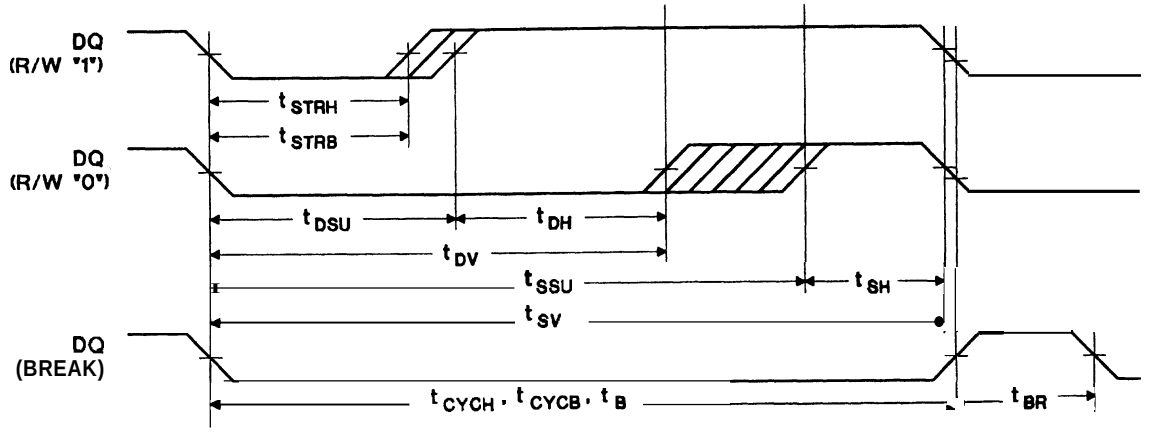
Note: All voltages relative to V_{SS}.

Serial Communication Timing Specification

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYCH}	Cycle time, host to bq2012	3			me	See note
t_{CYCB}	Cycle time, bq2012 to host	3		6	me	
t_{STRH}	Start hold, host to bq2012	5			ns	
t_{STRB}	Start hold, bq2012 to host	500			µs	
t_{DSU}	Data setup			750	µs	
t_{DH}	Data hold	750			µs	
t_{DV}	Data valid	1.50			me	
t_{SSU}	Stop setup			2.26	ms	
t_{SH}	Stop hold	700			µs	
t_{SV}	Stop valid	2.95			me	
t_B	Break	3			ms	
t_{BR}	Break recovery	1			ms	

Note: The open-drain DQ pin should be pulled to at least V_{CC} by the host system for proper DQ operation. DQ may be left floating if the serial interface is not used.

Serial Communication Timing Illustration



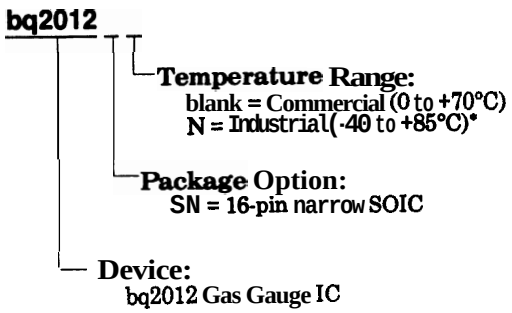
RC-34

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	7	Addition to Table 2	Added bottom row

Note: Change 1 = Sept. 1996 B changes from July 1994.

Ordering Information



* Contact factory for availability.

bq2012 Evaluation System

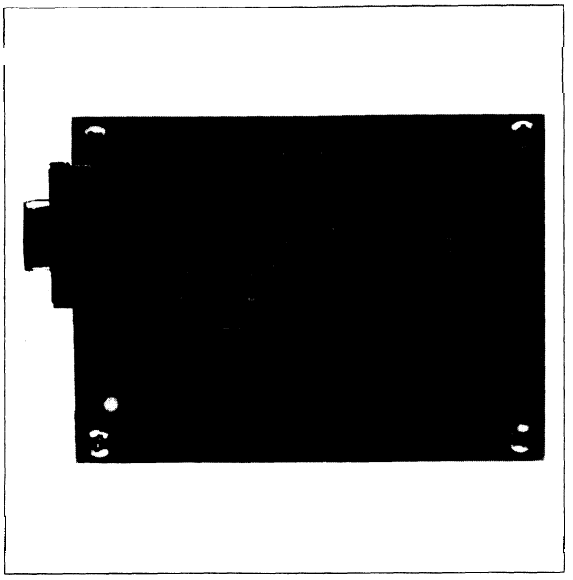
Features

- bq2012 Gas Gauge IC evaluation and development system
- ➤ RS-232 interface hardware for easy access to state-of-charge information via the serial port
- ➤ Alternative terminal block for direct connection to the serial port
- ➤ Battery state-of-charge monitoring for 5- to 10-cell (series) applications (2 user-selectable options for 3, 4, or greater than 10 cells)
- ➤ On-board regulator for greater than 4-cell applications
- ➤ State-of-charge information displayed on bank of 6 LEDs
- Nominal capacity jumper-configurable
- Cell chemistry jumper-configurable
- Display mode jumper-configurable

General Description

The EV2012 Evaluation System provides a development and evaluation environment for the bq2012 Gas Gauge IC. The EV2012 incorporates a bq2012, a sense resistor, and all other hardware necessary to provide a capacity monitoring function for 3 to 12 series NiCd or NiMH cells.

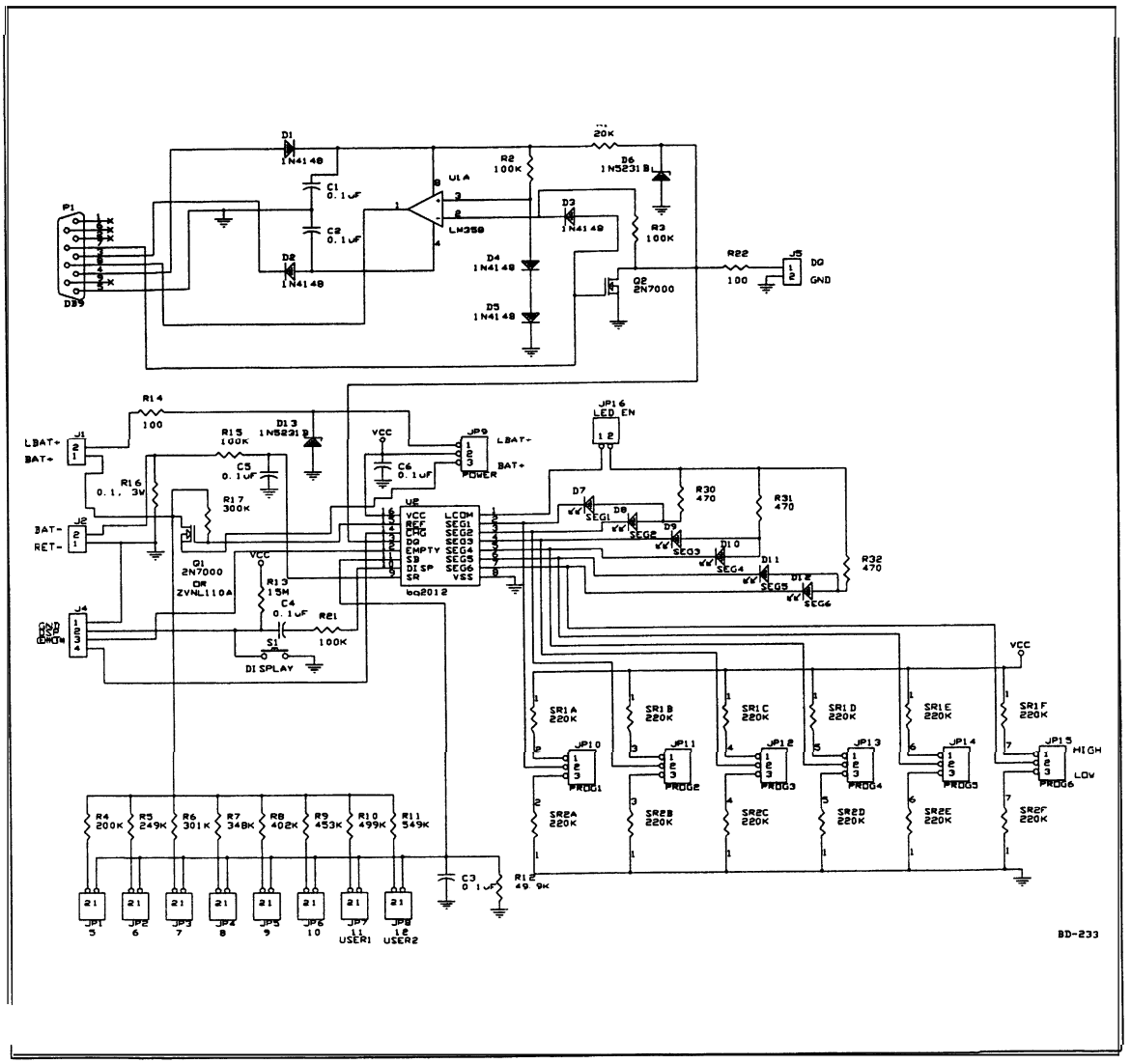
Hardware for an RS-232 interface is included on the EV2012 so that easy access to the state-of-charge information can be achieved via the serial port of the bq2012. Direct connection to the serial port of the bq2012 is also made available for check-out of the final hardware/software implementation.



The menu-driven software provided with the EV2012 displays charge/discharge activity and allows user interface to the bq2012 from any standard DOS PC.

A full data sheet for this product is available on our web site (http://www.benchmarq.com), or you may contact the factory for one.

EV2012 Board Schematic



bq2014

Gas Gauge IC With External Charge Control

Features

- **Conservative** and repeatable **measurement** of available charge in rechargeable batteries
- Charge control output **operates** an **external charge controller such as** the **bq2004** Fast Charge IC
- **Designed** for battery pack integration
  - **120µA typical standby** current
- Integrate within a system or **as** a stand-alone device
  - Display capacity via single-**wire** serial communication port or direct drive of **LEDs**
- **Measurements** compensated for current and temperature
- **Self-discharge compensation** using **internal** temperature **sensor**
- User-selectable end-of-discharge **threshold**
- Battery voltage, nominal available charge, temperature, etc. available wer serial **port**
- 16-pin narrow SOIC

General Description

The **bq2014** Gas Gauge IC is intended for battery-pack or in-eyetem installation to maintain an accurate record of available **battery** charge. The IC **monitors** the voltage drop across a sense resistor connected in series between **the** negative battery terminal and **ground** to determine charge and **discharge** activity of the battery.

Self-discharge **of** NiMH and **NiCd** batteriee is estimated based on an internal **timer** and temperature sensor. Compensations for battery **temperature** and rate of charge or discharge are applied **to** the charge, discharge, and self-discharge calculations to provide available charge information **across** a wide range of operating conditions. Battery capacity is **automatically recalibrated,** or **"learned,"** in the **course of** a discharge **cycle from full** to empty.

The **bq2014** includes a charge control **output** that **controls** an **external Fast** Charge **IC** such **as** the bq2004.

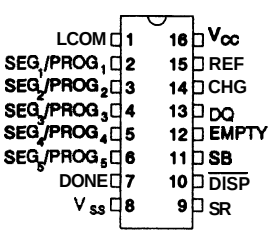
Nominal Available Charge **(NAC)** may be directly indicated using a **five-segment** LED **display.**

The **bq2014 supports** a simple single-line bidirectional serial link to an external **processor** (with a common ground). The **bq2014 outputs** battery information in response to external **commands over the serial link.**

Internal registers include available charge, temperature, capacity, battery voltage, battery ID, battery etatus, and programming pin settings. To support subassembly testing, the outputa may also be controlled. The **external processor** may also overwrite **some** of the **bq2014 gas** gauge data **registers.**

The **bq2014** may operate directly from three or four cells. **With** the **REF** output and an external **transistor,** a simple, inexpensive regulator can be built to provide Vcc **across** a greater number **of** cells.

Pin Connections



16-Pin Narrow SOIC

PN-84

Pin Names

LCOM	LED **common** output	**REF**	Voltage reference output
SEG1/PROG1	LED segment 1/ **program 1 input**	**CHG**	Charge control output
SEG2/PROG2	LED segment 2/ program 2 **input**	**DQ**	Serial communications **input/output**
SEG3/PROG3	LED segment 3/ **program** 3 **input**	EMPTY	Empty battery indicator **output**
SEG4/PROG4	LED segment **4/ program 4 input**	SB	Battery sense input
SEG5/PROG5	LED segment 5/ program 5 *input*	**$\overline{\text{DISP}}$**	Display control input
DONE	**Fast** charge complete	SR	Sense resistor input
		Vcc	**3.0-6.5V**
		Vss	**System** ground

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Pin Descriptions

LCOM **LED** common output

Open-drain output switches Vcc to source current for the LEDs. The switch is off during initialization to allow reading of the soft pull-up or pull-down programming resistore. LCOM is also in a high impedance state when the display is off.

SEG_1–SEG_5 **LED** display segment **outputs (dual function** with **$PROG_1$–$PROG_5$)**

Each output may activate an LED to sink the current sourced from LCOM.

$PROG_1$–$PROG_2$ **Programmed** full **count** selection inputs **(dual** function with **SEG_1–SEG_2)**

These three-level input pins define the programmed full count (PFC) thresholds described in Table 2.

$PROG_3$–$PROG_4$ **Gas** gauge rate selection inputs **(dual** function with **SEG_3–SEG_4)**

These three-level input pins defiie the **scale factor** described in Table 2.

$PROG_5$ **Self-discharge rate** selection **(dual function** with **SEG_5)**

This three-level input pin defines the **selfdis**charge compensation **rate** shown in Table 1.

CHG Charge control output

This open-drain output becomes active high when charging is allowed.

DONE Fast charge complete

This input is used to communicate the status of an external charge controller such as the bq2004 **Fast** Charge IC. Note: This pin must be pulled down to Vss using a 200KΩ resistor.

SR Sense **resistor** input

The voltage drop **(V_{SR}) across** the **sense** resistor Rs is **monitored** and integrated over time to interpret charge and discharge activity. **The** SR input is tied to the high side of the **sense resistor. $V_{SR} < V_{SS}$** indicates **discharge,** and **$V_{SR} > V_{SS}$** indicates charge. The effective voltage drop **(V_{SRO})** as seen by the **bq2014** is **$V_{SR} + V_{OS}$** (see Table **5).**

$\overline{DISP}$ **Display control input**

$\overline{DISP}$ high disables the LED display. **$\overline{DISP}$** tied to Vcc **allows PROGx to** connect directly to Vcc or **Vss instead of through** a pull-up or pull-down **resistor.** $\overline{DISP}$ floating allows the LED display to be active during a valid charge or during **discharge** if the NAC **register** is **update**d at a rate equivalent to **$V_{SRO} \leq -4mV$.** $\overline{DISP}$ low **activates** the display. See Table 1.

SB Secondary **battery** input

This input monitors the single-cell voltage potential through a high-impedance resistive divider network for end-of-discharge voltage (EDV) thresholds, maximum charge voltage (MCV), and battery removed.

EMPTY Battery empty output

This open-drain output becomes **high-impedance** on detection of a valid **final end-of-discharge** voltage **(V_{EDVF})** and is low following the next application of a valid charge.

DQ **Serial I/O pin**

This is an open-drain bidirectional pin.

REF Voltage reference output for **regulator**

REF provides a voltage reference output for an optional micro-regulator.

V_{CC} Supply voltage **input**

V_{SS} Ground

Functional Description

General Operation

The bq2014 determines battery capacity by monitoring the amount of charge input to or removed from a rechargeable battery. The bq2014 measures discharge and charge currents, estimates self-discharge, monitors the battery for low-battery voltage thresholds, and compensates for temperature and charge/discharge rates. The charge measurement is made by monitoring the voltage across a small-value series sense resistor between the battery's negative terminal and ground. The available battery charge is determined by monitoring this voltage over time and correcting the measurement for the environmental and operating conditions.

Figure 1 shows a typical battery pack application of the bq2014 using the LED display capability as a charge-state indicator. The bq2014 is configured to display capacity in a relative display mode. The relative display mode uses the last measured *discharge* capacity of the battery as the battery "full" reference. The LED segments output a percentage of the available charge based on NAC and LMD. A push-button display feature is available for momentarily enabling the LED display.

The bq2014 monitors the *charge* and discharge currents as a voltage across a sense resistor (see R_S in Figure 1). A filter between the negative battery terminal and the SR pin is required.

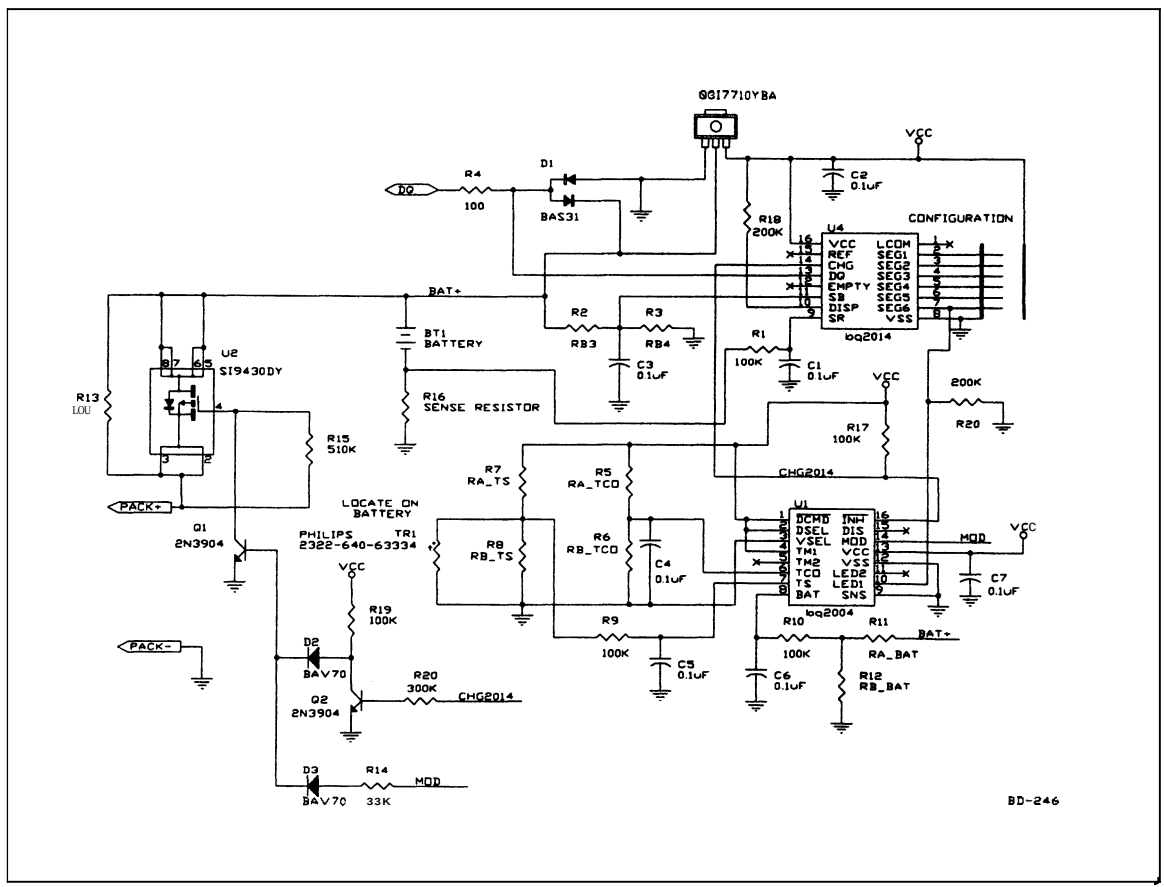


Figure 1. Battery Pack Application Diagram—LED Display

Voltage Thresholds

In conjunction with monitoring V_{SR} for charge/discharge currents, the bq2014 monitors the single-cell battery potential through the SB pin. The single-cell voltage potential is determined through a resistor/divider network per the following equation:

$$\frac{R2}{R3} = N - 1$$

where N is the number of cells, R2 is connected to the positive battery terminal, and R3 is connected to the negative battery terminal. The single-cell battery voltage is monitored for the end-of-discharge voltage (EDV) and for maximum cell voltage (MCV). EDV threshold levels are used to determine when the battery has reached an "empty" state, and the MCV threshold is used for fault detection during charging.

Two EDV thresholds for the bq2014 are programmable with the default values fixed at:

EDV1 (early warning) = 1.05V

EDVF (empty) = 0.95V

If V_{SB} is below either of the two EDV thresholds, the associated flag is latched and remains latched, independent of V_{SB}, until the next valid charge (as defined in the section entitled 'Gas Gauge Operation"). The V_{SB} value is also available over the serial port.

Duriig discharge and charge, the bq2014 monitors V_{SR} for various thresholds. These thresholds are used to compensate the charge and discharge rates. Refer to the count compensation section for details. EDV monitoring is disabled if $V_{SR} \leq -250mV$ typical and resumes ½ second after $V_{SR} > -250mV$.

EMPTY Output

The EMPTY output switches to high impedance when $V_{SB} < V_{EDF}$ and remains latched until a valid charge occurs.

Reset

The bq2014 recognizes a valid battery whenever V_{SB} is greater than 0.1V typical. V_{SB} rising from below 0.25V or falling from above 2.25V (V_{MCV}) resets the device. Reset can also be accomplished with a command over the serial port as described in the Reset Register section.

Temperature

The bq2014 internally determines the temperature in 10°C steps centered from -35°C to +85°C. The temperature steps are used to adapt charge and discharge rate wmpensations, self-discharge counting, and available charge display translation. The temperature range is available over the serial port in 10°C increments as shown below:

TMPGG (hex)	Temperature Range
0x	< -30°C
1x	-30°C to -20°C
2x	-20°C to -10°C
3x	-10°C to 0°C
4x	0°C to 10°C
5x	10°C to 20°C
6x	20°C to 30°C
7x	30°C to 40°C
8x	40°C to 50°C
9x	50°C to 60°C
Ax	60°C to 70°C
Bx	70°C to 80°C
Cx	> 80°C

Layout Considerations

The bq2014 measures the voltage differential between the SR and V_{SS} pins. V_{OS} (the offset voltage at the SR pin) is greatly affected by PC board layout. For optimal results, the PC board layout should follow the strict rule of a single-point ground return. Sharing high-current ground with small signal ground causes undesirable noise on the small signal nodes. Additionally:

- The capacitors (C2 and C3) should be placed as close as possible to the SB and V_{CC} pine, respectively, and their paths to V_{SS} should be as short as possible. A high-quality ceramic capacitor of 0.1µf is recommended for V_{CC}.
- The sense resistor filter (R1, C1) should be placed as cloee as possible to the SR pin.
- The sense resistor (R16) should be as close as possible to the bq2014.

Gas Gauge Operation

The operational overview diagram in Figure 2 illustrates the operation of the bq2014. The bq2014 accumulates a measure of charge and discharge currents, as well as an estimation of self-discharge. Charge and discharge currents are temperature and rate compensated, whereas eelf-discharge is only temperature compensated.

The main counter, Nominal Available Charge (NAC), represents the available battery capacity at any given time. Battery charging increments the NAC register, while battery discharging and self-discharge decrement the NAC register and increment the DCR (Discharge Count Register).

The Discharge Count Register (DCR) is used to update the Last Measured Discharge (LMD) register only if a complete battery discharge from full to empty occurs without *any* partial battery charges. Therefore, the bq2014 adapts its capacity determination based on the actual conditions of discharge.

The battery's initial capacity is equal to the programmed full count (PFC) shown in Table 2. Until LMD is updated, NAC counta up to but not beyond this threshold during subsequent charges. This approach allows the gas gauge to be charger-independent and compatible with any type of charge regime.

Many actions in the bq2014 are triggered by detection of a "valid charge." NAC is stored in an asynchronous, 2-byte counter; the lower byte is NACL and the upper byte is NACH. A valid charge hae occurred anytime the charge lasts long enough to cause an increment in NACH. Small increments of charging are not considered 'valid' if they result in counts in NACL but do not generate a roll-wer (carry) that increments NACH. NACL is reset anytime the counter direction changes from down to up, so the number of counta required to cause a roll-over and a valid charge is always 256. The counter may be incrementing by 2, 4, 8, or more counts per increment, however, depending on the scaling factors selected. Therefore, a valid charge may be constituted by a smaller number of counter increments.

1. **Last Measured Discharge (LMD) or learned battery** capacity:

   LMD is the lest measured discharge capacity of the battery. On initialization (application of Vcc or battery replacement), LMD = PFC. During subsequent discharges, the LMD is updated with the latest measured capacity in the Discharge Count Register (DCR) representing a discharge from full to below EDV1. A qualified discharge is necessary for a capacity transfer from the DCR to the LMD register. The LMD also serves as the 100% reference threshold used by the relative display mode.

2. **Programmed Full Count (PFC) or initial battery capacity:**

   The initial LMD and gas gauge rate values are programmed by using $PROG_1$–$PROG_4$. The bq2014 is configured for a given application by selecting a PFC value from Table 2. The correct PFC may be

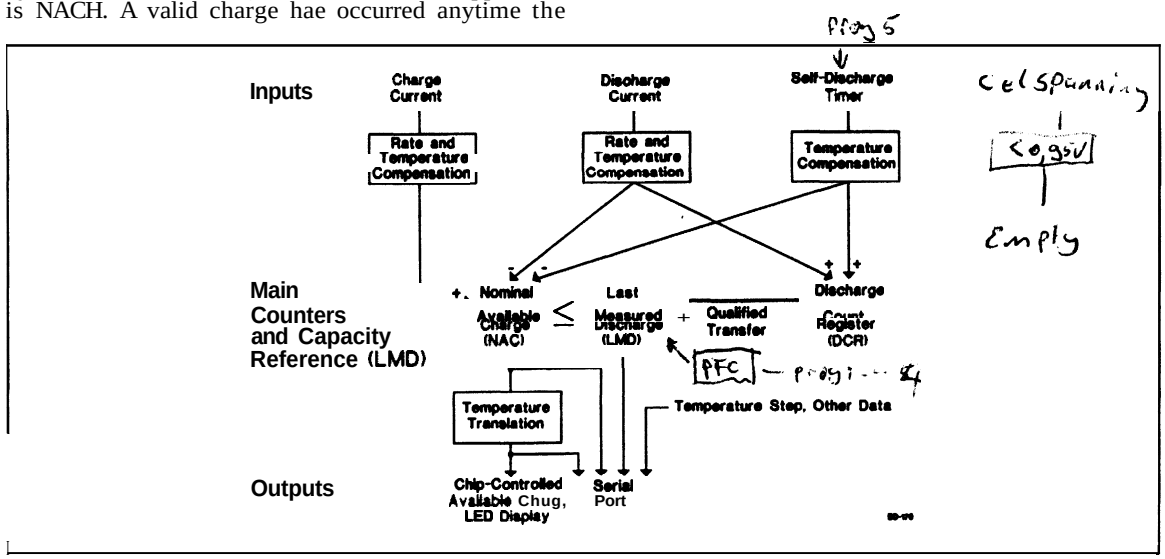


Figure 2. Operational Overview

determined by multiplying the rated battery capacity in mAh by the sense resistor value:

Battery capacity (mAh) • sense resistor (R) =

PFC (mVh)

Selecting a PFC slightly less than the rated capacity for absolute mode provides capacity above the full reference for much of the battery's life.

Example: Selecting a PFC Value

Given:

Sense resistor = 0.1Ω
Number of cells = 6
Capacity = 2200mAh, NiCd battery
Current range = 50mA to 2A
Relative display mode
Serial port only
Self-discharge = $C/_{64}$
Voltage drop over sense resistor = 5mV to 200mV

Therefore:

2200mAh • 0.1Ω = 220mVh

Select:

PFC = 33792 counts or 211mVh
$PROG_1$ = float
$PROG_2$ = float
$PROG_3$ = float
$PROG_4$ = low
$PROG_5$ = float
DONE = low

Table 1. bq2014 Programming

Pin Connection	$PROG_5$ Self-Discharge Rate	$\overline{DISP}$ Display State
H	Disabled	LED disabled
Z	$NAC/_{64}$	LED enabled on discharge when V_{SRO} < -4mV or during a valid charge
L	$NAC/_{47}$	LED on

Table 2. bq2014 Programmed Full Count mVh Selections

$PROG_x$		Programmed Full Count (PFC)	$PROG_4$ = L			$PROG_4$ = Z			Units
1	2		PROG3 = H	PROG3 = Z	PROG3 = L	PROG3 = H	PROG3 = Z	PROG3 = L	
-	-	-	Scale = 1/80	Scale = 1/160	Scale = 1/320	Scale = 1/640	Scale = 1/1280	Scale = 1/2560	mVh/ count
H	H	49152	614	307	154	76.8	38.4	19.2	mVh
H	Z	45056	563	282	141	70.4	35.2	17.6	mVh
H	L	40960	512	256	128	64.0	32.0	16.0	mVh
Z	H	36864	461	230	115	57.6	28.8	14.4	mVh
Z	Z	33792	422	211	106	53.0	26.4	13.2	mVh
Z	L	30720	384	192	96.0	48.0	24.0	12.0	mVh
L	H	27648	346	173	86.4	43.2	21.6	10.8	mVh
L	Z	25600	320	160	80.0	40.0	20.0	10.0	mVh
L	L	22528	282	141	70.4	35.2	17.6	8.8	mVh
VSR equivalent to 2 counts/s (nom.)			90	45	22.5	11.25	5.6	2.8	mV

The initial full battery capacity is 2110mVh (2110mAh) until the bq2014 "learns" a new capacity with a qualified discharge from full to EDV1.

3. Nominal Available Charge (NAC):

NAC counts up during charge to a maximum value of LMD and down during discharge and self-discharge to 0. NAC is reset to 0 on initialization and on the first valid charge after EDV = 1. To prevent overstatement of charge during periods of overcharge, NAC stops incrementing when NAC = LMD.

4. Discharge Count Register (DCR):

The DCR counts up during discharge independent of NAC and could continue increasing after NAC has decremented to 0 until V_{SB} < EDV1. Prior to NAC = 0 (empty battery), both discharge and self-discharge increment the DCR. After NAC = 0, only discharge increments the DCR. The DCR resets to 0 when NAC = LMD. The DCR does not roll over but stops counting when it reaches FFFFh.

The DCR value becomes the new LMD value on the first charge after a valid discharge to V_{EDV1} if:

- No valid charges have occurred during the period between NAC = LMD and EDV1 detected.
- The self-discharge count is not more than 4096 counts (8% to 18% of PFC, specific percentage threshold determined by PFC).
- The temperature is ≥ 0°C when the EDV1 level is reached during discharge.

The valid discharge flag (VDQ) indicates whether the present discharge is valid for LMD update.

Charge Counting

Charge activity is detected baaed on a positive voltage on the V_{SR} input. The bq2014 determines charge activity sustained at a continuous rate equivalent to V_{SRO} (V_{SR} + V_{OS}) > V_{SRQ}. Once a valid charge in detected, charge counting continues until V_{SRO} falls below V_{SRQ}. V_{SRQ} is a programmable threshold (as described in the Digital Magnitude Filter section) and has a default value of 375µV. If charge activity is detected, the bq2014 increments NAC at a rate proportional to V_{SRO}. If enabled, the bq2014 then activates an LED display. Charge actions increment the NAC after compensation for charge rate and temperature.

Charge Control

Charge control is provided by the CHG output. This output is asserted continuously when NAC > 0.94 * LMD. CHG is also asserted when a valid charge is detected (CHGS in the FLGS1 register is also set). CHG is low when NAC < 0.94 • LMD and there is no valid charge activity.

DONE Input

When the bq2014 detects a valid charge complete with an active-high signal on the DONE input, NAC is set to LMD for NAC/64 (NiCd) self-discharge setting. NAC is set to 94% of LMD (if NAC is below 94%) for NAC/47 (NiMH) self-diecharge setting. VDQ is set along with DONE.

Discharge Counting

All discharge counts where V_{SRO} < V_{SRD} cause the NAC register to decrement and the DCR to increment if EDV1 =0. Exceeding the fast discharge threshold (FDQ) if the rate is equivalent to V_{SRO} < -4mV activates the display, if enabled. The display becomes inactive after V_{SRO} rises above -4mV. V_{SRD} is a programmable threshold as described in the Digital Magnitude Filter section. The default value for V_{SRD} is -300µV.

Self-Discharge Estimation

The bq2014 continuously decrements NAC and increments DCR for self-discharge based on time and temperature. The self-discharge count rate is programmed to be a nominal 1/64 • NAC or 1/47 • NAC per day or disabled as selected by PROG5. This is the rate for a battery whose temperature is between 20°–30°C. The NAC register cannot be decremented below 0.

Count Compensations

The bq2014 determines fast charge when the NAC updates at a rate of ≥2 counts/sec. Charge and discharge are compensated for temperature and charge/discharge rate before updating the NAC and/or DCR. Self-discharge estimation is compensated for temperature before updating the NAC or DCR.

Charge Compensation

Two charge efficiency compensation factors are used for trickle charge and fast charge. Fast charge is defined as a rate of charge resulting in ≥ 2 NAC counts/sec (≥ 0.15C to 0.32C depending on PFC selections; see Table 2). The compensation defaults to the fast charge factor until the actual charge rate is determined.

Temperature adapts the charge rate compensation factors over three ranges between nominal, warm, and hot temperatures. The compensation factors are shown below.

Charge Temperature	Trickle Charge Compensation	Fast Charge Compensation
<40°C	0.80	0.95
>40°C	0.75	0.90

Discharge Compensation

Corrections for the rate of discharge are made by adjusting an internal discharge compensation factor. The *discharge* factor is based on the dynamically measured V_{SR}.

The compensation factors during discharge are:

Approximate V_{SR} Threshold	Discharge Compensation Factor	Efficiency
V_{SR} > -150 mV	1.00	100%
V_{SR} < -150 mV	1.05	95%

Temperature compensation during discharge also takes place. At lower temperatures, the compensation factor increases by 0.05 for each 10°C temperature range below 10°C.

$$\text{Comp. factor} = 1.0 + (0.05 \cdot N)$$

Where N = Number of 10°C steps below 10°C and $-150\text{mV} < V_{SR} < 0$.

For example:

T > 10°C: Nominal compensation, N = 0

0°C < T < 10°C: N = 1 (i.e., 1.0 becomes 1.05)

-10°C < T < 0°C: N = 2 (i.e., 1.0 becomes 1.10)

-20°C < T < -10°C: N = 3 (i.e., 1.0 becomea 1.15)

-20°C < T < -30°C: N = 4 (i.e., 1.0 becomes 1.20)

Self-Discharge Compensation

The self-discharge compensation is programmed for a nominal rate of 1/64 • NAC per day, 1/47 • NAC per day, or disabled. This is the rate for a battery within the 20–30°C temperature range (TMPGG = 6x). This rate varies across 8 range8 from <10°C to >70°C, doubling with each higher temperature step (10°C). See Table 3.

Table 3. Self-Discharge Compensation

Temperature Step	Typical Rate	
	$PROG_5$ = Z	$PROG_5$ = L
< 10°C	NAC/256	NAC/188
10–20°C	NAC/128	NAC/94
20–30°C	NAC/64	NAC/47
30–40°C	NAC/32	NAC/23.5
40–50°C	NAC/16	NAC/11.8
50–60°C	NAC/8	NAC/5.88
60–70°C	NAC/4	NAC/2.94
> 70°C	NAC/2	NAC/1.47

Digital Magnitude Filter

The bq2014 has a programmable digital filter to eliminate charge and discharge counting below a set threshold. The default setting is -0.30mV for V_{SRD} and +0.38mV for V_{SRQ}. The proper digital filter setting can be calculated using the following equation. Table 4 shows typical digital filter settings.

$$V_{SRD}\,(\text{mV}) = -45 / \text{DMF}$$

$$V_{SRQ}\,(\text{mV}) = -1.25 \cdot V_{SRD}$$

Table 4. Typical Digital Filter Settings

DMF	DMF Hex.	V_{SRD} (mV)	V_{SRQ} (mV)
75	4B	-0.60	0.75
100	64	-0.45	0.56
150 (default)	96	-0.30	0.38
175	AF	-0.26	0.32
200	C8	-0.23	0.28

Error Summary

Capacity Inaccurate

The LMD is susceptible to error on initialization or if no updates *occur*. On initialization, the LMD value includes the error between the programmed full capacity and the actual capacity. This error is present until a valid discharge occurs and LMD is updated (see DCR description, page 7). The other cause of LMD error is battery wear-out. As the battery ages, the measured capacity must be adjusted to account for changes in actual battery capacity.

A Capacity Inaccurate counter (CPI) is maintained and incremented each time a valid charge occurs (qua ed by NAC; see the CPI register description) and is reset when-

Table 5. Current-Sensing Error as a Function of V_{SR}

Symbol	Parameter	Typical	Maximum	Units	Notes
V_{OS}	Offset referred to V_{SR}	±50	±150	µV	$\overline{DISP}$ = V_{CC}.
INL	Integrated non-linearity error	±2	±4	%	Add 0.1% per °C above or below 25°C and 1% per volt above or below 4.25V.
INR	Integrated non-repeatability error	±1	±2	%	Measurement repeatability given similar operating conditions.

ever LMD is updated from the DCR. The counter does not wrap around but stops counting at 255. The capacity inaccurate flag (CI) is set if LMD has not been updated following 64 valid charges.

Current-Sensing Error

Table 5 illustrates the current-sensing error as a function of V_{SR}. A digital filter eliminates charge and discharge counts to the NAC register when V_{SRO} (V_{SR} + V_{OS}) is between V_{SRQ} and V_{SRD}.

Communicating With the bq2014

The bq2014 includes a simple single-pin (DQ plus return) serial data interface. A host processor uses the interface to access various bq2014 registers. Battery characteristics may be easily monitored by adding a single contact to the battery pack. The open-drain DQ pin on the bq2014 should be pulled up by the host system, or may be left floating if the serial interface is not used.

The interface uses a command-based protocol, where the hoet processor sends a command byte to the bq2014. The command directs the bq2014 to either store the next eight bits of data received to a register specified by the command byte or output the eight bits of data specified by the command byte.

The communication protocol is asynchronous return-to-one. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 333 bits/sec. The least-significant bit of a command or data byte is transmitted first. The protocol is simple enough that it can be implemented by most hoet processors using either polled or interrupt processing. Data input from the bq2014 *may* be sampled using the pulse-width capture timers available on some microcontrollers.

Communication is normally initiated by the host processor sending a BREAK command to the bq2014. A BREAK is detected when the DQ pin is driven to a logic-low state for a time, t_B or greater. The DQ pin should then be returned to its normal ready-high logic state for a time, t_{BR}. The bq2014 is now ready to receive a command from the hoet processor.

The return-to-one data bit frame consists of three distinct sections. The first d o n is used to start the t[illegible] ion by either the hoet or the bq2014 taking the DQ pm to a logic-low state for a period, $t_{STRH,B}$. The next section is the actual data t[illegible] ion, where the data should be valid by a period, t_{DSU}, after the negative edge used to start communication. The data should be held for a period, t_{DV}, to allow the host or bq2014 to sample the data bit.

The final section is used to stop the transmission by returning the DQ pin to a logic-high state by at least a period, t_{SSU}, after the negative edge used to start communication. The final logic-high state should be held until a period, t_{SV}, to allow time to ensure that the bit transmission was stopped properly. The timings for data and break communication are given in the serial communication timing specification and illustration sections.

Communication with the bq2014 is always performed with the least-significant bit being transmitted first. Figure 3 shows an example of a communication sequence to read the bq2014 NAC register.

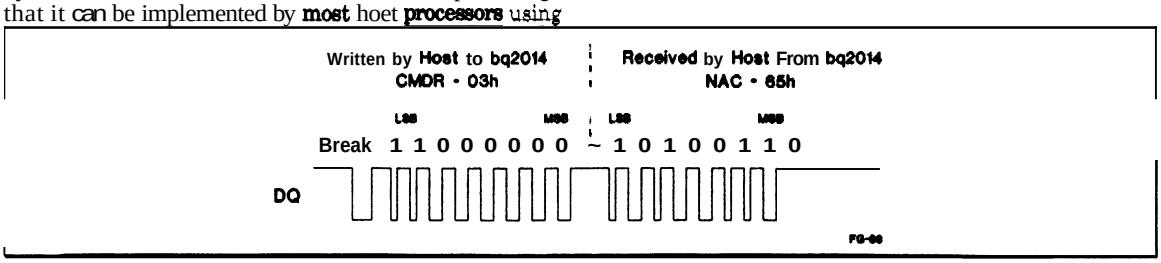


Figure 3. Typical Communication With the bq2014

bq2014 Registers

The bq2014 command and status registers are listed in Table 6 and described below.

Command Register (CMDR)

The write-only CMDR register is accessed when eight valid command bits have been received by the bq2014. The CMDR register contains two fields:

- W/$\overline{R}$ bit
- Command address

The W/$\overline{R}$ bit of the command register is used to select whether the received command is for a read or a write function.

The W/$\overline{R}$ values are:

CMDR Bits							
7	6	5	4	3	2	1	0
W/$\overline{R}$	-	-	-	-	-	-	-

Where W/$\overline{R}$ is:

0 The bq2014 outputs the requested register contents specified by the address portion of CMDR.

1 The following eight bits should be written to the register specified by the address portion of CMDR.

The lower seven-bit field of CMDR contains the address portion of the register to be accessed. Attempts to write to invalid addresses are ignored.

CMDR Bits							
7	6	5	4	3	2	1	0
-	AD6	AD5	AD4	AD3	AD2	AD1	AD0 (LSB)

Primary Status Flags Register (FLGS1)

The read-only FLGSl register (address=01h) contains the primary bq2014 flags.

The charge *status* flag (CHGS) is asserted when a valid charge rate is detected. Charge rate is deemed valid when $V_{SRO} > V_{SRQ}$. A V_{SRO} of less than V_{SRQ} or discharge activity clears CHGS.

The CHGS values are:

FLGSl Bits							
7	6	5	4	3	2	1	0
CHGS	-						

Where CHGS is:

0 Either discharge activity detected or $V_{SRO} < V_{SRQ}$

1 $V_{SRO} > V_{SRQ}$

The battery replaced flag (BRP) is asserted whenever the potential on the SB pin (relative to V_{SS}), V_{SB}, falls from above the maximum cell voltage, MCV (2.25V), *or* rises above 0.1V. The BRP flag is also eat when the bq2014 is reset (see the RST register description). BRP is reset when either a valid charge action increments NAC to be equal to LMD, or a valid charge action is detected after the EDVl flag is asserted. BRP = 1 signifies that the device has been reset.

The BRP values are:

FLGSl Bits							
					2	1	0
-	BRP	-			-	-	-

Where BRP is:

0 Battery is charged until NAC = LMD or discharged until the EDVl flag is asserted

1 V_{SB} dropping from above MCV, V_{SB} rising from below 0.1V, or a serial port initiated reset has occurred

The battery *removed* flag (BRM) is asserted whenever the potential on the SB pin (relative to V_{SS}) rises above MCV or falls below 0.1V. The BRM flag is asserted until the condition causing BRM is removed. Due to signal filtering, 30 seconds may have to transpire for BRM to react to battery insertion or removal.

The BRM values *are:*

FLGSl Bits							
7							
-	-	BRM	-			-	-

Where BRM is:

0 $0.1V < V_{SB} < 2.25V$

1 $0.1 V > V_{SB}$ or $V_{SB} > 2.25V$

The *capacity inaccurate* flag *(CI)* is used to warn the ueer that the battery has been charged a substantial number of times since LMD has been updated. The CI flag is asserted on the 64th charge after the last LMD update or when the bq2014 is reset. The flag is cleared after an LMD update.

Table 6. bq2014 Command and Status Registers

Symbol	Register Name	Loc. (hex)	Read/ Write	Control Field							
				7(MSB)	6	5	4	3	2	1	0(LSB)
CMDR	Command register	00h	Write	W/$\overline{R}$	AD6	AD5	AD4	AD3	AD2	AD1	AD0
FLGS1	Primary status flags register	Olh	Read	CHGS	BRP	BRM	CI	VDQ	n/u	EDV1	EDVF
TMPGG	Temperature and gas gauge register	02h	Read	TMP3	TMP2	TMP1	TMP0	GG3	GG2	GG1	GG0
NACH	Nominal available charge high byte register	03h	R/W	NACH7	NACH6	NACH5	NACH4	NACH3	NACH2	NACH1	NACH0
NACL	Nominal available charge low byte register	17h	Read	NACL7	NACL6	NACL5	NACL4	NACL3	NACL2	NACL1	NACL0
BATID	Battery identification register	04h	R/W	BATID7	BATID6	BATID5	BATID4	BATID3	BATID2	BATID1	BATID0
LMD	Last measured discharge register	05h	R/W	LMD7	LMD6	LMD5	LMD4	LMD3	LMD2	LMD1	LMD0
FLGS2	Secondary status flags register	06h	Read	CR	DR2	DR1	DR0	n/u	n/u	n/u	OVLD
PPD	Program pin pull-down register	07h	Read	n/u	n/u	PPD6	PPD5	PPD4	PPD3	PPD2	PPD1
PPU	Program pin pull-up register	08h	Read	n/u	n/u	PPU6	PPU5	PPU4	PPU3	PPU2	PPU1
CPI	Capacity inaccurate count register	09h	Read	CPI7	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	CPI0
DMF	Digital magnitude filter register	0Ah	R/W	DMF7	DMF6	DMF5	DMF4	DMF3	DMF2	DMF1	DMF0
VSB	Battery voltage	0Bh	Read	VSB7	VSB6	VSB5	VSB4	VSB3	VSB2	VSB1	VSB0
VTS	End-of-discharge threshold select	0Ch	R/W	VTS7	VTS6	VTS5	VTS4	VTS3	VTS2	VTS1	VTS0
RST	Reset register	39h	Write	RST	0	0	0	0	0	0	0

Note: n/u = not used

The CI values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
		-	CI	-			

Where CI is:

0 When LMD is updated with a valid full discharge

1 After the 64th valid charge action with no LMD updates or when the device is reset

The *valid discharge* flag (VDQ) is asserted when the bq2014 is discharged from NAC = LMD or DONE is valid. The flag remains set until either LMD is updated or one of three actions that can clear VDQ occurs:

- The self-discharge count register (SDCR) has exceeded the maximum acceptable value (4096 counts) for an LMD update.
- A valid charge action sustained at $V_{SRO} > V_{SRQ}$ for at least 256 NAC counts.
- The EDV1 flag was set at a temperature below 0°C

The VDQ values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
			-	VDQ	-		

Where VDQ is:

0 SDCR ≥ 4096, subsequent valid charge action detected, or EDV1 is asserted with the temperature less than 0°C

1 On first discharge after NAC = LMD or DONE is valid

The *first end-of-discharge warning* flag (EDV1) warns the user that the battery is almost empty. The first segment pin, SEG_1, is modulated at a 4Hz rate if the display is enabled once EDV1 is asserted, which should warn the user that loss of battery power is imminent. The EDV1 flag is latched until a valid charge has been detected. The EDV1 threshold is externally controlled via the VTS register (see Voltage Threshold Register on this page).

The EDV1 values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
					-	EDV1	-

Where EDV1 is:

0 Valid charge action detected, $V_{SB} \geq V_{TS}$

1 $V_{SB} < V_{TS}$ providing that OVLD=0 (see FLGS2 register description)

The *fiml end-of-discharge warning* flag (EDVF) flag is used to warn that battery power is at a failure condition. All segment drivers are turned off. The EDVF flag is latched until a valid charge haa been detected. The EMPTY pin is also forced to a high-impedance state on assertion of EDVF. The host system may pull EMPTY high, which may be used to disable circuitry to prevent deep-discharge of the battery. The EDVF threshold is set 100mV below the EDV1 threshold.

The EDVF values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
						-	EDVF

Where EDVF is:

0 Valid charge action detected, $V_{SB} \geq V_{TS} - 100mV$

1 $V_{SB} < V_{TS} - 100mV$ providing that OVLD=0 (see FLGS2 register description)

Voltage Threshold Register (VTS)

The end-of-discharge threshold voltages (EDV1 and EDVF) can be set using the VTS register (address = 0Ch). The read/write VTS register sets the EDV1 trip mint. EDVF is set 100mV below EDV1. The default value in the VTS register is 70h, representing EDV1 = 1.05V and EDVF = 0.95V. EDV1 = 2.4V • (VTS/256).

VTS Register Bits							
7	6	5	4	3	2	1	0
VTS7	VTS6	VTS5	VTS4	VTS3	VTS2	VTS1	VTS0

Battery Voltage Register (VSB)

The read-only battery voltage register is used to read the single-cell battery voltage on the SB pin. The VSB register is updated approximately once per second with the present value of the battery voltage. V_{SB} = 2.4V • (VSB/256).

VSB Register Bits							
7	6	5	4	3	2	1	0
VSB7	VSB6	VSB5	VSB4	VSB3	VSB2	VSB1	VSB0

Temperature and Gas Gauge Register (TMPGG)

The read-only TMPGG register (address=02h) contains two data fields. The first field contains the battery temperature. The second field containe the available charge from the battery.

TMPGG Temperature Bits							
7	6	5	4	3	2	1	0
TMP3	TMP2	TMP1	TMP0	-			

The bq2014 contains an internal temperature sensor. The temperature is used to set charge and discharge efficiency factors as well as to adjust the self-discharge coefficient. The temperature register contents may be translated as shown in Table 7.

The bq2014 calculates the available charge as a function of NAC, temperature, and LMD. The results of the calculation are available via the display port or the gaa gauge field of the TMPGG register. The register is used to give available capacity in 1/16 increments from 0 to 15/16.

TMPGG Gas Gauge Bits							
7	6	5	4	3	2	1	0
			-	GG3	GG2	GG1	GG0

The gae gauge display and the gas gauge portion of the TMPGG register are adjusted for cold temperature dependencies. A piece-wise correction is performed as follows:

Temperature	Available Capacity Calculation
> 0°C	NAC / "Full Reference'
-20°C < T < 0°C	0.75 • NAC / "Full Reference"
< -20°C	0.6 • NAC / "Full Reference"

The adjustment between > 0°C and -20°C < T < 0°C has a 10°C hysteresis.

Nominal Available Charge Registers (NACH/NACL)

The read/write NACH high-byte register (address=03h) and the read-only NACL low-byte register (address=17h) are the main gas gauging registers for the bq2014. The NAC registers are incremented during charge actions and decremented during discharge and self-discharge actions. The correction factors for charge/discharge efficiency are applied automatically to NAC.

Table 7. Temperature Register Translation

TMP3	TMP2	TMP1	TMP0	Temperature
0	0	0	0	T < -30°C
0	0	0	1	-30°C < T < -20°C
0	0	1	0	-20°C < T < -10°C
0	0	1	1	-10°C < T < 0°C
0	1	0	0	0°C < T < 10°C
0	1	0	1	10°C < T < 20°C
0	1	1	0	20°C < T < 30°C
0	1	1	1	30°C < T < 40°C
1	0	0	0	40°C < T < 50°C
1	0	0	1	50°C < T < 60°C
1	0	1	0	60°C < T < 70°C
1	0	1	1	70°C < T < 80°C
1	1	0	0	T > 80°C

On reset, NACH and NACL are cleared to 0. When the bq2014 detects a charge, NACL resets to 0. NACH and NACL are reset to 0 on the first valid charge after V_{SB} = EDV1. Writing to the *NAC registers affects the available charge counts and, therefore, affects the bq2014 gas gauge operation. Do not write the NAC registers to a value greater than LMD.*

Battery Identification Register (BATID)

The read/write BATID register (address=04h) is available for use by the system to determine the type of battery pack. The BATID contents are retained as long as Vcc is greater than 2V. The contents of BATID have no effect on the operation of the bq2014. There is no default setting for this register.

Last Measured Discharge Register (LMD)

LMD is a read/write register (address=05h) that the bq2014 uses as a measured full reference. The bq2014 adjusts LMD based on the measured discharge capacity of the battery from full to empty. In this way the bq2014 updates the capacity of the battery. LMD is set to PFC during a bq2014 reset.

Secondary Status Flags Register (FLGS2)

The read-only FLGS2 register (address=06h) contains the secondary bq2014 flags.

The *charge rate* flag (CR) is used to denote the fast charge regime. Fast charge is assumed whenever a charge action is initiated. The CR flag remains asserted if the charge rate does not fall below 2 counts/sec.

The CR values are:

FLGS2 Bits							
7	6	5	4	3	2	1	0
CR	-	-	-	-	-	-	-

Where CR is:

0 When charge rate falls below 2 counts/sec

1 When charge rate is above 2 counts/sec

The fast charge regime efficiency factors are used when CR = 1. When CR = 0, the trickle charge efficiency factors are used. The time to change CR varies due to the user-selectable count rates.

The *discharge rate* flags, DR2–0, are bits 6–4.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	DR2	DR1	DR0	-	-		

They are used to determine the current discharge regime as follows:

DR2	DR1	DRO	V_{SR} (V)
0	0	0	$V_{SR} > -150mV$
0	0	1	$V_{SR} < -150mV$

The *overload* flag (OVLD) is asserted when a discharge overload is detected, $V_{SR} < -250mV$. OVLD remains asserted as long as the condition persists and is cleared after $V_{SR} > -150mV$. The overload condition ie used to atop sampling of the battery terminal characteristics for end-of-discharge determination when excessive discharges occur.

FLGS2 Bits							
7	6	5	4	3	2	1	0
						-	OVLD

DR2–0 and OVLD are set based on the measurement of the voltage at the SR pin relative to Vss. The rate at which this measurement is made varies with device activity.

Program Pin Pull-Down Register (PPD)

The read-only PPD register (address=07h) contains some of the programming pin information for the bq2014. The segment drivers, SEG_{1-5} and DONE, have corresponding PPD register locations, PPD_{1-6}. A given location is set if a pull-down resistor has been detected on its corresponding segment driver. For example, if SEG_1 and SEG_4 have pull-down resistors, the contents of PPD are xx101001. (Note: DONE must be pulled down for proper operation.)

Program Pin Pull-Up Register (PPU)

The read-only PPU register (address=08h) contains the rest of the programming pin information for the bq2014. The segment drivers, SEG_{1-5} and DONE, have corresponding PPU register locations, PPU_{1-6}. A given location is set if a pull-up resistor has been detected on its corresponding segment driver. For example, if SEG_3 and DONE have pull-up resistors, the contents of PPU are xx100100.

PPD/PPU Bits							
8	7	6	5	4	3	2	1
	-	PPU_6	PPU_5	PPU_4	PPU_3	PPU_2	PPU_1
	-	PPD_6	PPD_5	PPD4	PPD_3	PPD_2	PPD_1

Capacity Inaccurate Count Register (CPI)

The read-only CPI register (address=09h) is used to indicate the number of times a battery has been charged without an LMD update. Because the capacity of a rechargeable battery varies with age and operating conditions, the bq2014 adapts to the changing capacity over time. A complete discharge from full (NAC=LMD) to empty (EDV1=1) is required to perform an LMD update assuming there have been no intervening valid charges, the temperature is greater than or equal to 0°C, and the self-dischargecounter is leas than 4096 counts.

The CPI register is incremented every time a valid charge is detected. When NAC > 0.94 • LMD, however, the CPI register increments on the first valid charge; CPI does not increment again for a valid charge until NAC < 0.94 • LMD. This prevents continuous trickle charging from incrementing CPI if self-discharge decrements NAC. The CPI register increments to 255 without rolling over. When the contents of CPI are incremented to 64, the capacity inaccurate flag, CI, is asserted in the FLGS1 register. The CPI register is reset whenever an update of the LMD register is performed, and the CI flag is also cleared.

Digital Magnitude Filter (DMF)

The read-write DMF register (address = 0Ah) provides the system with a means to change the default settings of the digital magnitude filter. By writing different values into this register, the limits of Vsm and V_{SRQ} can be adjusted.

Note: Care should be taken when writing to this register. A V_{SRD} and V_{SRQ} below the specified Vos may adversely affect the accuracy of the bq2014. Refer to Table 4 for recommended settings for the DMF register.

Reset Register (RST)

The reset register (address=39h) provides the means to perform a software-controlled reset of the device. By writing the RST register contents from 00h to 80h, a bq2014 reset is performed. *Setting* any *bit other than the most-significant bit of the RST register is not allowed, and results in improper operation of the bq2014.*

Resetting the bq2014 sets the following:

- LMD = PFC

  CPI, VDQ, NACH, and NACL = 0

- CI and BRP = 1

Note: Self-discharge is disabled when $PROG_5$ = H.

Display

The bq2014 can directly display capacity infurmation using low-power LEDs. If LEDs are used, the program pine should be resistively tied to V_{CC} or V_{SS} for a program high or program low, respectively.

The bq2014 displays the battery charge state in relative mode. In relative mode, the battery charge is represented as a percentage of the LMD. Each LED segment represents 20% of the LMD.

The capacity display is also adjusted for the battery temperature. The temperature adjustment reflects the available capacity at a given temperature but does not *affect* the NAC register. The temperature adjustments are detailed in the TMPGG register description.

When $\overline{DISP}$ is tied to V_{CC}, the SEG_{1-5} outputs are inactive. **Note: DISP** must be tied to V_{CC} if the LEDs are not used. When $\overline{DISP}$ is left floating, the display becomes active whenever the NAC registers are counting at a rate equivalent to $V_{SRO} < -4mV$ or charge current is detected, $V_{SRO} > V_{SRQ}$. When pulled low, the segment outputs become active immediately. A capacitor tied to $\overline{DISP}$ allows the display to remain active for a short period of time after activation by a paah-button switch.

The segment outputs are modulated as two banks of three, with segments 1, 3, and 6 alternating with segments 2 and 4. The segment outputs are modulated at approximately 100Hz with each segment bank active for 30% of the period.

SEG_1 blinks at a 4Hz rate whenever V_{SB} has been detected to be below V_{EDV1} (EDV1 = 1), indicating a low-battery condition. V_{SB} below V_{EDVF} (EDVF = 1) disables the display output.

Microregulator

The bq2014 can operate directly from 3 or 4 cells. To facilitate the power supply requirements of the bq2014, an REF output is provided to regulate an external low-threshold n-FET. A micropower source for the bq2014 can be inexpensively built using the FET and an external resistor; see Figure 1.

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to Vss	-0.3	+7.0	V	
All other pins	Relative to Vss	-0.3	+7.0	V	
REF	Relative to Vss	-0.3	+8.5	V	Current limited by R1 (see Figure 1)
V_{SR}	Relative to Vss	-0.3	+7.0	V	Minimum 100Ω series resistor should be used to protect SR in case of a shorted battery (see the bq2014 application note for details).
T_{OPR}	Operating temperature	0	+70	°C	Commercial
		-40	+85	°C	Industrial

Note: Permanent device damage may occur if **Absolute Maximum Ratings are exceeded.** Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage Thresholds (TA = TOPR; V = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDVF}	Final empty warning, default	0.92	0.95	0.98	V	SB
V_{EDV1}	First empty warning, default	1.02	1.05	1.08	V	SB
V_{SR1}	Discharge compensation threshold	-120	-150	-180	mV	SR
V_{SRO}	SR sense range	-300		+2000	mV	SR
V_{OVLD}	Overload threshold	-220	-250	-280	mV	SR
V_{SRQ}	Valid charge	375			µV	V_{SR} + Vos (see note 1)
V_{SRD}	Valid discharge			-300	µV	V_{SR} + Vos (see note 1)
V_{MCV}	Maximum single-cell voltage	2.20	2.25	2.30	V	SB
V_{BR}	Battery removed/replaced		0.1	0.25	V	SB pulled low
		2.20	2.26	2.30	V	SB pulled high

Notes:

1. Default value; value set in DMF register. Vos is affected by PC board layout. Proper layout guidelines should be followed for optimal performance.
2. To ensure correct threshold determination and proper operation, $V_{CC} > V_{SB} + 1.5V$

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	3.0	4.25	6.5	V	V_{CC} excursion from < 2.0V to ≥ 3.0V initializes the unit.
V_{REF}	Reference at 25°C	5.7	6.0	6.3	V	I_{REF} = 5µA
	Reference at -40°C to +85°C	4.5	-	7.5	V	I_{REF} = 5µA
R_{REF}	Reference input impedance	2.0	5.0	-	MΩ	V_{REF} = 3V
I_{CC}	Normal operation	-	90	135	µA	V_{CC} = 3.0V
		-	120	180	µA	V_{CC} = 4.25V
		-	170	250	µA	V_{CC} = 6.5V
V_{SB}	Battery input	-	-	2.4	V	
R_{SBmax}	SB input impedance	10	-	-	MΩ	0 < V_{SB} < V_{CC}
I_{DISP}	$\overline{DISP}$ input leakage	-	-	5	µA	V_{DISP} = V_{SS}
I_{LCOM}	LCOM input leakage	-0.2	-	0.2	µA	$\overline{DISP}$ = V_{CC}
R_{DQ}	Internal pulldown	500	-	-	KΩ	
V_{SR}	Sense resistor input	-0.3	-	2.0	V	V_{SR} < V_{SS} = discharge; V_{SR} > V_{SS} = charge
R_{SR}	SR input impedance	10	-	-	MΩ	-200mV < V_{SR} < V_{CC}
V_{IH}	Logic input high	V_{CC} - 0.2	-	-	V	$PROG_1$–$PROG_5$
V_{IL}	Logic input low	-	-	V_{SS} + 0.2	V	$PROG_1$–$PROG_5$; note 1
V_{IZ}	Logic input Z	float	-	float	V	$PROG_1$–$PROG_5$
V_{OLSL}	SEG_X output low, low V_{CC}	-	0.1	-	V	V_{CC} = 3V, I_{OLS} ≤ 1.75mA SEG_1–SEG_5
V_{OLSH}	SEG_X output low, high V_{CC}	-	0.4	-	V	V_{CC} = 6.5V, I_{OLS} ≤ 11.0mA SEG_1–SEG_5
V_{OHLCL}	LCOM output high, low V_{CC}	V_{CC} - 0.3	-	-	V	V_{CC} = 3V, I_{OHLCOM} = -5.25mA
V_{OHLCH}	LCOM output high, high V_{CC}	V_{CC} - 0.6	-	-	V	V_{CC} = 6.5V, I_{OHLCOM} = -33.0mA
I_{IH}	$PROG_{1-5}$ input high current	-	1.2	-	µA	V_{PROG} = V_{CC}/2
I_{IL}	$PROG_{1-5}$ input low current	-	1.2	-	µA	V_{PROG} = V_{CC}/2
I_{OHLCOM}	LCOM source current	-33	-	-	mA	At V_{OHLCH} = V_{CC} - 0.6V
I_{OLS}	SEG_X sink current	-	-	11.0	mA	At V_{OLSH} = 0.4V
I_{OL}	Open-drain sink current	-	-	5.0	mA	At V_{OL} = V_{SS} + 0.3V DQ, EMPTY, CHG
V_{OL}	Open-drain output low	-	-	0.5	V	I_{OL} ≤ 5mA, DQ, EMPTY
V_{IHDQ}	DQ input high	2.5	-	-	V	DQ
V_{ILDQ}	DQ input low	-	-	0.8	V	DQ
R_{PROG}	Soft pull-up or pull-down resistor value (for programming)	-	-	200	KΩ	$PROG_1$–$PROG_5$
R_{FLOAT}	Float state external impedance	-	5	-	MΩ	$PROG_1$–$PROG_5$

Notes: All voltages relative to V_{SS}.

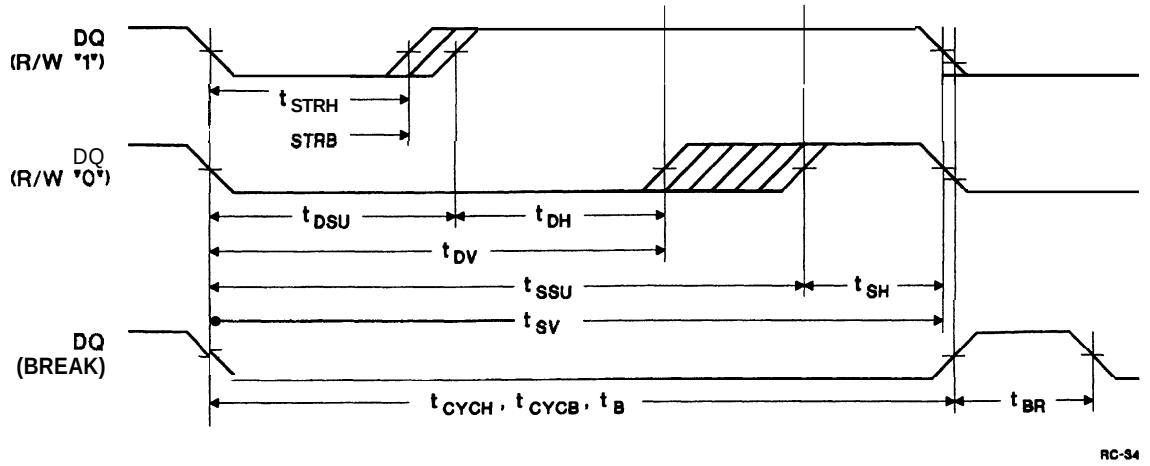
1. **DONE** must be pulled low for proper operation.

Serial Communication Timing Specification

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYCH}	Cycle time, host to bq2014	3			ms	See note
t_{CYCB}	Cycle time, bq2014 to host	3		6	ms	
t_{STRH}	Start hold, host to bq2014	5			ns	
t_{STRB}	Start hold, bq2014 to host	500			µs	
t_{DSU}	Data setup			750	µs	
t_{DH}	Data hold	750			µs	
t_{DV}	Data valid	1.50			ms	
t_{SSU}	Stop setup			2.25	ms	
t_{SH}	Stop hold	700			µs	
t_{SV}	Stop valid	2.95			ms	
t_B	Break	3			ms	
t_{BR}	Break recovery	1			ms	

Note: The open-drain DQ pin should be pulled to at least V_{CC} by the host system for proper DQ operation. DQ may be left floating if the serial interface is not used.

Serial Communication Timing Illustration

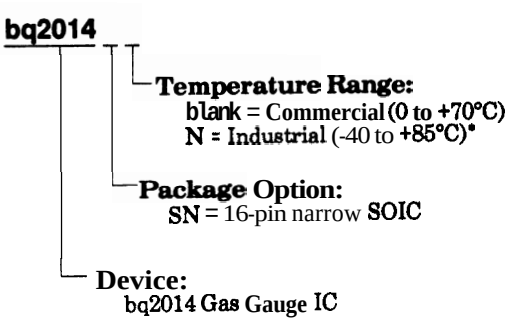


Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	1, 3, 5, 6, 7, 13, 15	Changed display mode	Relative display mode only
1	1, 17	**DONE** pin	Removed **PROG6**
1	2, 17	**DONE** pin	Added: DONE pin **must be** pulled to **Vss with** a 200KΩ **resistor**
1	6	Table 1	Removed PROG6
1	7	**DONE** input	Was: NAC is set to 90%... Is: NAC **is set to 94%...**
1	8, Table 3	$PROG_5$ = Z	**Was: $PROG_5$ = Z or H** Is: **$PROG_5$** = Z
2	8	Temperature Compensation table	**Replaced**
2	6	Table 2	Added **V_{SR} definition**
2	6	Valid charge **definition**	Added **definition**
2	14	Overload flag	Was: 0.5sec. after **V_{SR}** > -250mV Is: after **V_{SR} = -150mV**

Note: Change 1 = Dec. 1994 B "Final" changes from Aug. 1994 A "Preliminary."
Change 2 = Dec. 1995 C from Dec. 1994 B.

Ordering Information



* Contact factory for availability.

BENCHMARQ

Advance Information **bq2014H**

Gas Gauge IC With External Charge Control

Features

- Conservative and repeatable measurement of available charge in rechargeable batteries
- Charge control output operates an external charge controller *such* as the bq2004 Fast Charge IC
- 16-pin narrow SOIC
- Designed for battery pack integration
  - 120µA typical standby current
- Integrate within a system or as a stand-alone device
  - Display capacity via single-wire serial communication port or direct drive of LEDs
- Measurements compensated for current and temperature
- Self-discharge compensation using internal temperature sensor
- User-selectable end-of-diecharge threshold
- Battery voltage, nominal available charge, temperature, etc. available over serial port
- High-speed (5Kbits/sec.) DQ bus interface

General Description

The bq2014H Gae Gauge IC is intended for battery-pack or in-eyetem installation to maintain an accurate record of available battery charge. The IC monitors the voltage drop across a senee resistor connected in series between the negative battery terminal and ground to determine charge and discharge activity of the battery.

Self ——— of NiMH and NiCd batteries is estimated based on an internal timer and temperature sensor. Compensations for battery temperature and rate of charge or discharge are applied to the charge, discharge, and self-discharge calculations to provide available charge information across a wide range of operating conditions. Battery capacity is automatically recalibrated, or "learned," in the course of a discharge cycle from full to emptv.

The bq2014H includes a charge control output that controls an external Fast Charge IC such as the bq2004.

Nominal Available Charge (NAC) may be directly indicated ueing a five-segment LED display.

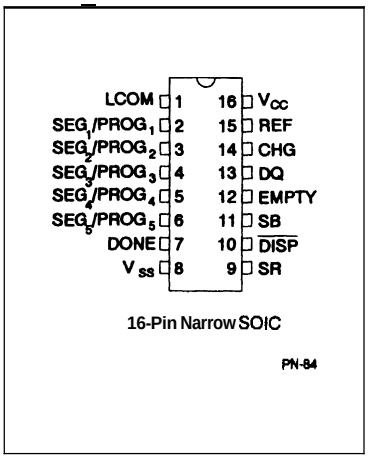
The bq2014H supports a simple eingle-line bidirectional serial link to an external processor (with a common ground). The bq2014H outputs bat*tery* information in response to external commands over the aerial lirk.

Internal registers include available charge, temperature, capacity, battery voltage, battery ID, battery status, and programming pin settings. To support subassembly testing, the outputa may also be controlled. The external processor may also overwrite some of the bq2014H gas gauge data registers.

The bq2014H may operate directly from three or four cells. With the REF output and an external transistor, a simple, inexpensive regulator can be built to provide Vcc across a greater number of cells.

The 5Kbits/sec. DQ bus interface is 16-times faster than the bq2014, reducing communications overhead in the monitoring microcontroller.

Pin Connections



16-Pin Narrow SOIC

PN-84

Pin Names

LCOM	LED common output
SEG1/PROG1	LED segment 1/ program 1 input
SEG2/PROG2	LED segment 2/ program 2 input
SEG3/PROG3	LED segment 3/ program 3 input
SEG4/PROG4	LED segment 4/ program 4 input
SEG5/PROG5	LED segment 5/ program 5 input
DONE	Fast charge complete
REF	Voltage reference output
CHG	Charge control output
DQ	Serial communications input/output
EMPTY	Empty battery indicator output
SB	Battery *sense* input
$\overline{\text{DISP}}$	Display control input
SR	Sense resistor input
Vcc	3.0-6.5V
vss	System ground

Sept. 1996

Notes

bq2014 Evaluation Board

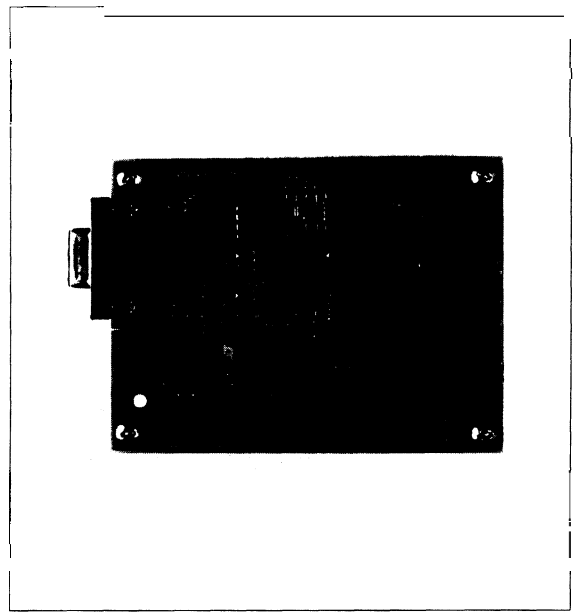
Features

- bq2014 Gas Gauge IC evaluation and development system
- ➤ RS-232 interface hardware for easy access to state-of-charge information via the serial port
- ➤ Alternative terminal block for direct connection to the serial port
- ➤ Battery state-of-charge monitoring for 5- to 10-cell (series) applications (2 user-selectable options for 3, 4, or greater than 10 cells)
- ➤ On-board regulator for greater than 4-cell applications
- ➤ State-of-charge information displayed on bank of 5 LEDs
- Nominal capacity jumper-configurable
- Cell chemistry jumper-configurable

General Description

The EV2014 evaluation system provides a development and evaluation environment for the bq2014 Gas Gauge IC. The EV2014 incorporates a bq2014, a sense resistor, and all other hardware necessary to provide a capacity monitoring functiion for 3 to 12 series NiCd or NiMH cells.

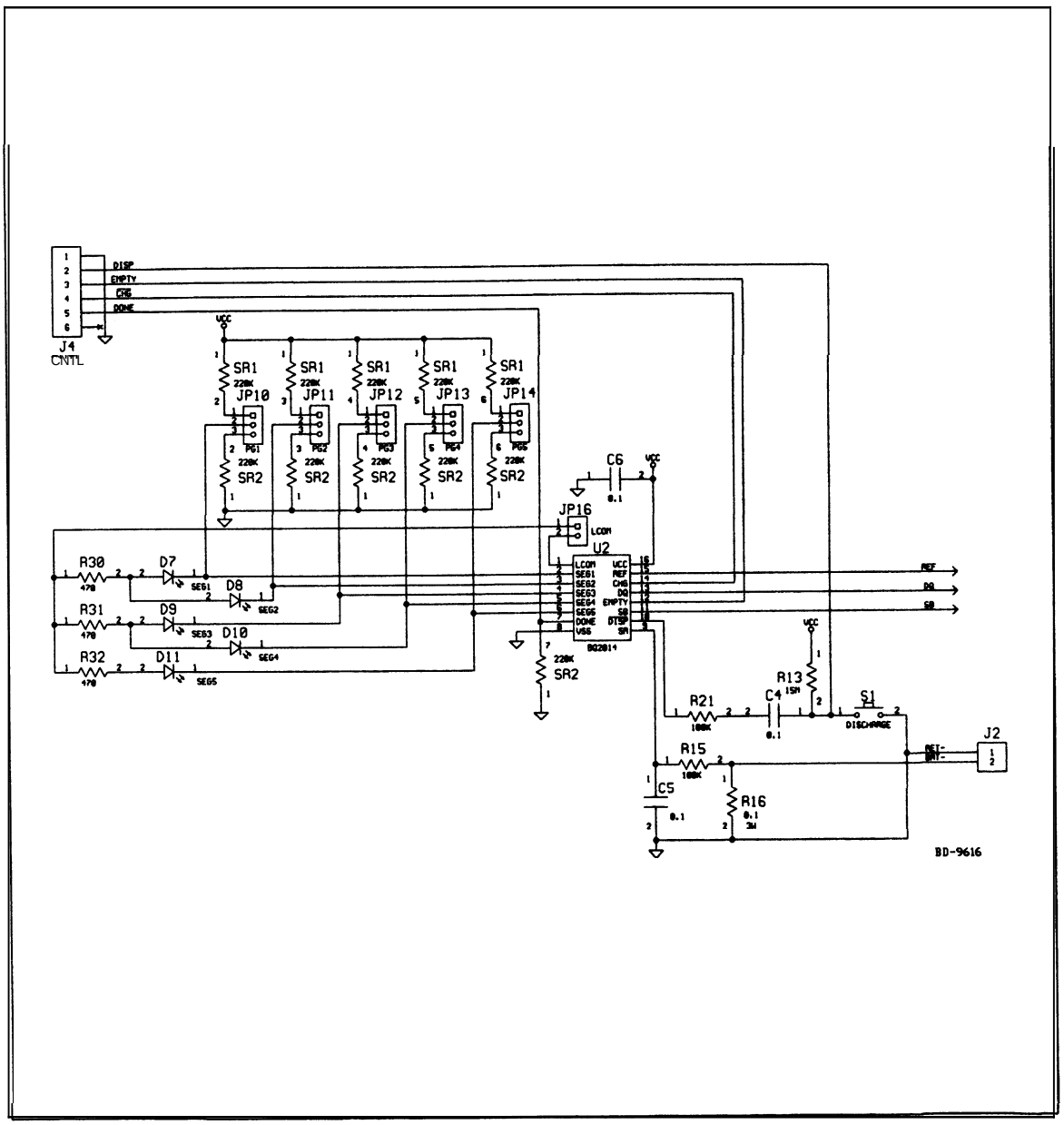
Hardware for an RS-232 interface is included on the EV2014 so that easy access to the battery state-of-charge information can be achieved via the serial port of the bq2014. Direct connection to the serial port of the bq2014 is also made available for check-out of the final hardware/software implementation.



The menu-driven software provided with the EV2014 displays charge/discharge activity and allows user interface to the bq2014 from any standard DOS PC.

A full data sheet for this product is available on our web site (http:Nwww.benchmarq.com), or you may contact the factory for one.

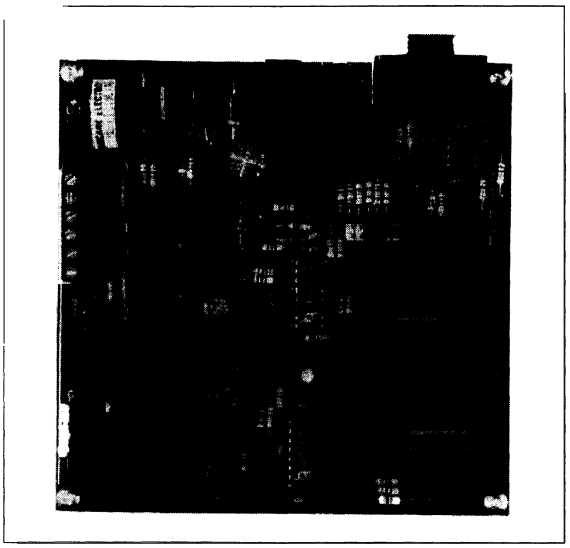
EV2014 Board Schematic



Gas Gauge and Fast Charge Evaluation System

Features

- bq2014 Gas Gauge and bq2004 Fast Charge evaluation and development system
- ➤ Battery state-of-charge monitoring and fast charge control of four to ten NiCd or NiMH cells
- ➤ Charge current sourced from an on-board switch-mode regulator (up to 3.0A)
- ➤ Fast charge termination by $\Delta T/\Delta t$, $-\Delta V$, PVD, maximum temperature, maximum time, and maximum voltage
- ➤ RS-232 interface hardware for easy access to state-of-charge information
- ➤ Nominal capacity and cell chemistry are jumper configurable



General Description

The EV2014x evaluation system provides a development and evaluation environment for the bq2014 Gas Gauge IC and the bq2004 Fast Charge IC. The EV2014x incorporates a bq2014, a bq2004, and all the external components required to reliably fast charge and accurately monitor the capacity of four to ten NiCd or NiMH cells.

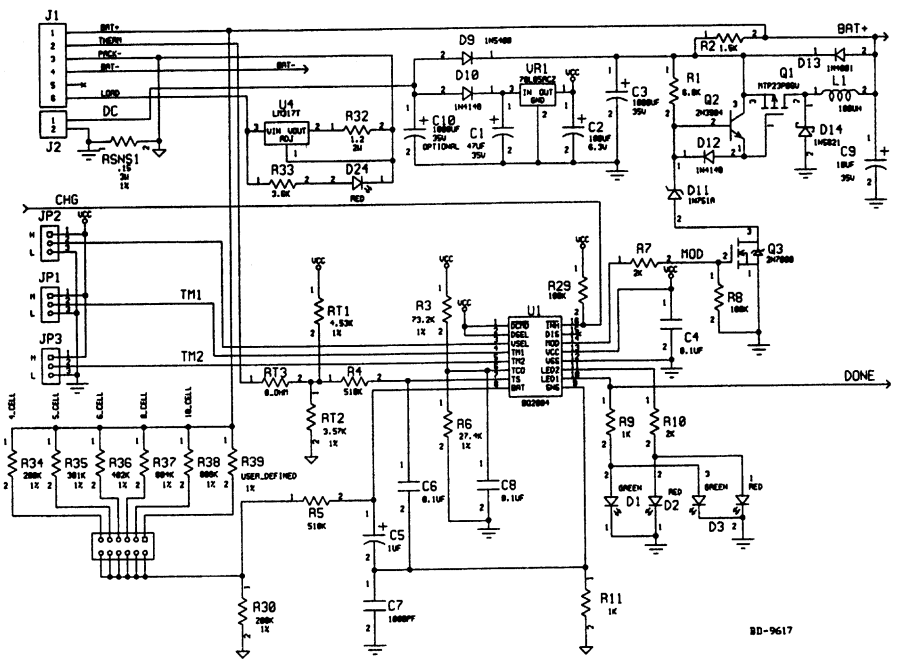
The bq2004 regulates the fast charge current. Fast charge is terminated by any of the following: $\Delta T/\Delta t$ (the rate of change in temperature versus time), $-\Delta V$ (negative voltage change) or PVD (peak voltage detect), maximum temperature, maximum time, and maximum voltage. The board provides a direct connection for an NTC thermistor. Jumper settings select the voltage termination mode, the termination hold-off time, top-off, and maximum charge time limits.

The EV2014x includes an RS-232 interface for easy access to the battery state of charge information via the serial port of the bq2014. The menu-driven gas gauge software provided displays charge/discharge activity and allows user interface to the bq2014 from any standard DOS PC.

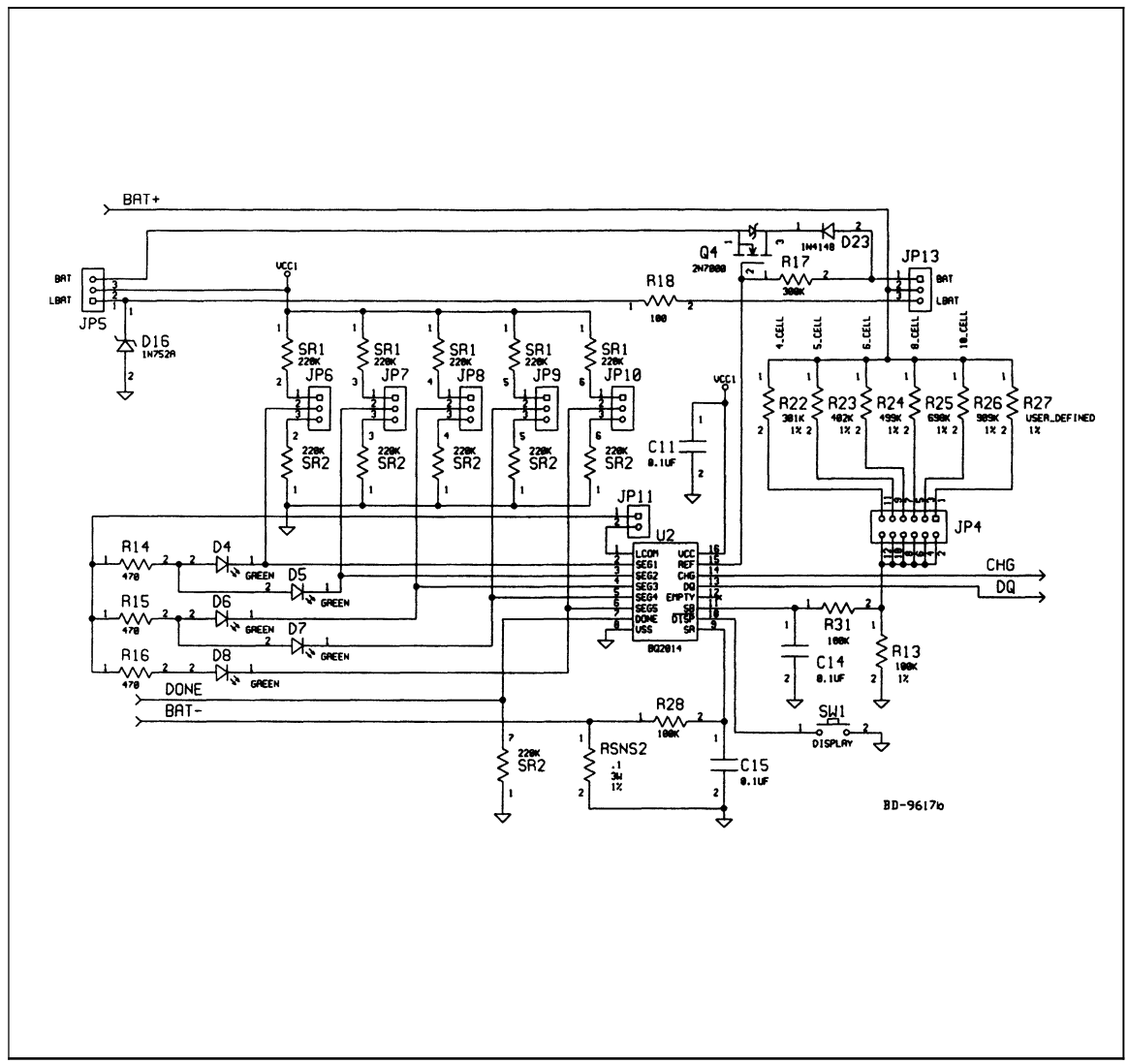
The user supplies the power supply and the batteries. The user configures the EV2014x board for the number of cells, nominal battery capacity, and cell chemistry. On-board LEDs indicate charging status and remaining capacity. The capacity LEDs are activated by the push button switch.

A full data sheet for this product is available on our web site (http://www.benchmarq.com), or you may contact the factory for one.

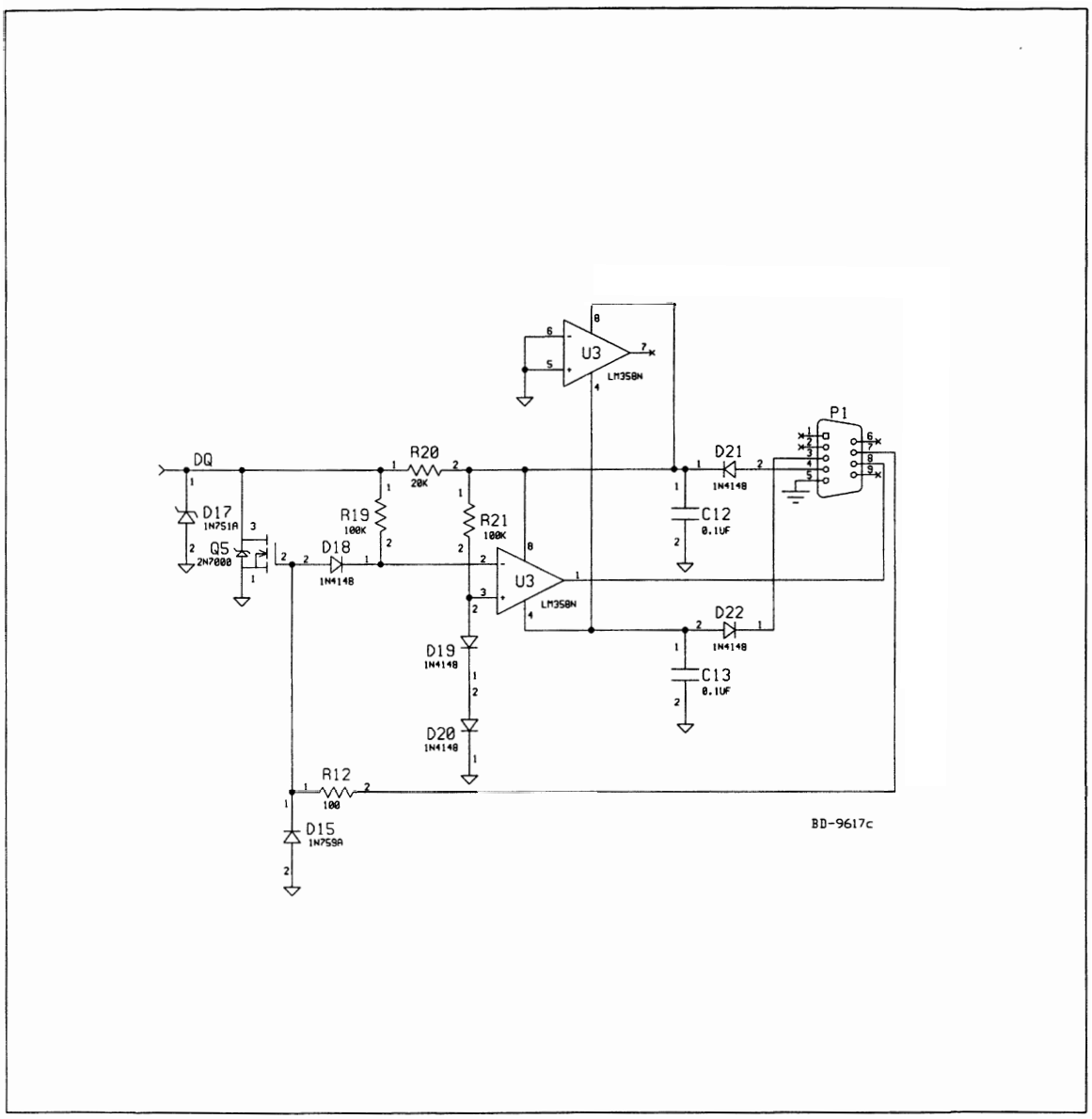
EV2014x Board Schematic



EV2014x Board Schematic (Continued)



EV2014x Board Schematic (Continued)



BENCHMARQ

Using NiMH and Li-Ion Batteries in Portable Applications

Introduction

Lithium Ion (Li-Ion) batteries are becoming more available in the marketplace, allowing system designers to use both nickel metal-hydride (NiMH) and Li-Ion battery types to power their portable equipment. The batteries, however, require different charge schemes. NiMH batteries are usually fast-charged at a constant current and terminated by either peak voltage detection, PVD, or the increasing rise in temperature at the end of full charge, $\Delta T/\Delta t$. Li-Ion batteries are usually charged at a constant voltage with a 1C current limit. Charge is usually terminated by time or when the charging current drops to a very low rate, typically less than C/30, indicating that the battery is full.

In addition to battery charging, the designer has the task of battery monitoring and capacity reporting. NiMH batteries are typically monitored for end-of-discharge voltage, battery temperature, and charge and discharge current. With a fairly flat discharge voltage over about Woof its capacity, capacity gauging for NiMH is done by determining the Amp-hour capacity removed during discharge and replaced during charge. NiMH batteries loose capacity due to self-discharge, which is determined by the temperature of the battery and is about 1.5 to 2 percent at 25°C.

Li-Ion batteries also require monitoring for capacity and state of charge. Li-Ion batteries using coke electrodes have a sloping discharge as shown in Figure 1. In some cases, the voltage during discharge can be used as an indicator of state of charge, but the voltage must be corrected for charge/discharge rate and ambient temperature. Voltage is acceptable for full or empty indication, but the better approach would be to monitor the capacity removed and the capacity replaced to determine the battery state of charge. This method would be more applicable to the other type of Li-Ion battery, which uses graphite electrodes. The graphite Li-Ion battery has a much flatter discharge profiie making voltage-based gauging much less accurate than the coke Li-Ion batteries. The self-dischargefor both types of Li-Ion batteries is about 1/10th of that for NiMH batteries.

Benchmarq Microelectronics is developing charge controllers, battery protectors, and capacity gauging ICs specifically tailored for the Li-Ion battery. Today, however, Li-Ion batteriea can be charged and monitored using existing Benchmarq products. The purpose of this paper is to describe how a subsystem can be developed that will support both NiMH and Li-Ion batteries using existing Benchmarq ICs and easily transition to the new IC developments.

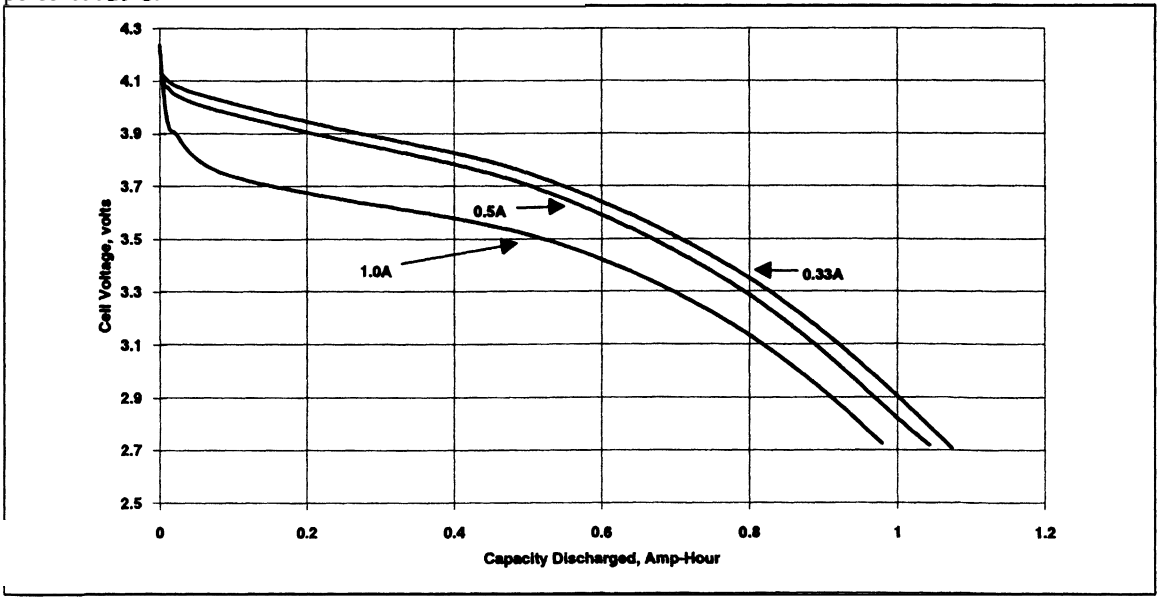


Figure 1. Li-Ion Battery Discharge Curve (Coke Electrodes)

Charger

The charger is based on the bq2004 operating in the switch-mode topology as shown in Figure 2. The charger can be controlled by either a bq2004 or a bq2004E. The charger is operated in a buck configuration where BAT+ is the battery pack positive contact and BAT - is the battery pack negative contact. When the battery is a NiMH pack, the SELC connection is not connected. When the battery is a Li-Ion battery, then the SELC contact is tied to the BAT+ contact within the battery pack. The battery also provides a thermistor contact so that charging can be qualified by the battery temperature and ΔT/Δt can be used for charge termination.

L1 is made using a composite core, MICROMETALS PN ST50-267, in a toroid geometry (see attached data sheet). The toroid is wound with 70 turns of 22 gauge copper magnet wire. The initial inductance is about 3mH. Because the inductance is a function of the current, the greater the current, the lower the inductance. This property allows for a greater range of current with smaller changes in switching frequency. The current range is needed for the lithium battery where the charge current decreases during charging as the battery EMF approaches the maximum allowable charging voltage. The switching frequency is about 30KHz.

When the SELC contact is floated, the charge selection is made for NiMH. In this mode, the bq2004 is configured for 1C charging with top-off and pulse trickle. The charge current is set to 2.25A. In this example, the battery divider is configured for nine cells. The ΔT/Δt sensitivity is configured using R8 and R9, and the maximum charge temperature is set by the resistors R5 and R6. The bqCharge disk provides a program to calculate the proper values for these resistors depending on the application requirements and the thermistor choice. The

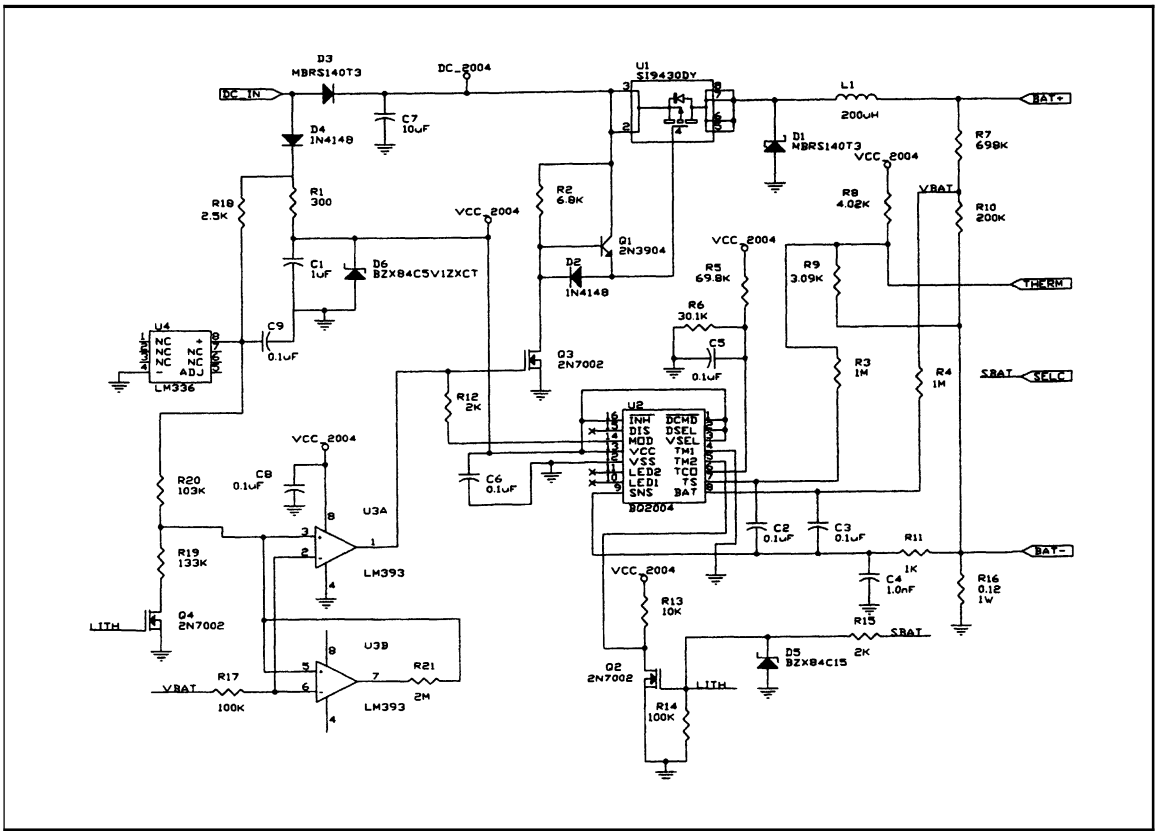


Figure 2. Li-Ion/NiMH bq2004 Switch-Mode Charging System

functional operation of the bq2004 and bq2004E is described in their respective data sheets.

When the SELC contact in at the BAT+ potential, the Li-Ion mode is selected. The battery pack is configured for three-by-three battery configuration, three strings of three cells in series connected in parallel. The TM1 and TM2 pine are set to provide a six-hour time-out with no top-off for trickle. The battery starts charging at the current limit eat to 1.9A and ie voltage-limited to 4.225V. For graphite Li-Ion cells, R19 and R20 are changed to limit charge voltage to 4.125V. *During* charging, the *current* varies as the battery EMF reaches the voltage limit. Full charge in indicated after the time-out *of* six hours.

Capacity Gauging

Capacity gauging is an important user feature for both NiMH and Li-Ion. Capacity gauging is provided by the bq2014 for NiMH batteries and can be co gured using the information in the bq2014 data sheet. The bq2014 can also be used for Li-Ion capacity gauging and is &-cussed in thin paper.

Figure 3 shows the bq2014 monitoring an NiMH battery configured similar to that described in the above charger section. The application *can* identity the battery pack as NiMH by bit 4 *of* the PPU register. This bit in 0 for nickel-based chemistries. The bq2014 provides the proper compensation for charge and discharge rates kith compensation and self-discharge correction. The bq2014 provides software-adjustable end-of-discharge voltage selection. Battery voltage is also available. The capacity of a battery is reported in a 8-bit register pair. The typical application scales this value based on the sense resistor used to get the Amp-hour capacity. The application can also scale the capacity to Watt-hours by using the battery voltage. During discharge, the battery voltage is read from the bq2014 and averaged with the end-of-discharge voltage. This is the average available voltage for the remaining die-

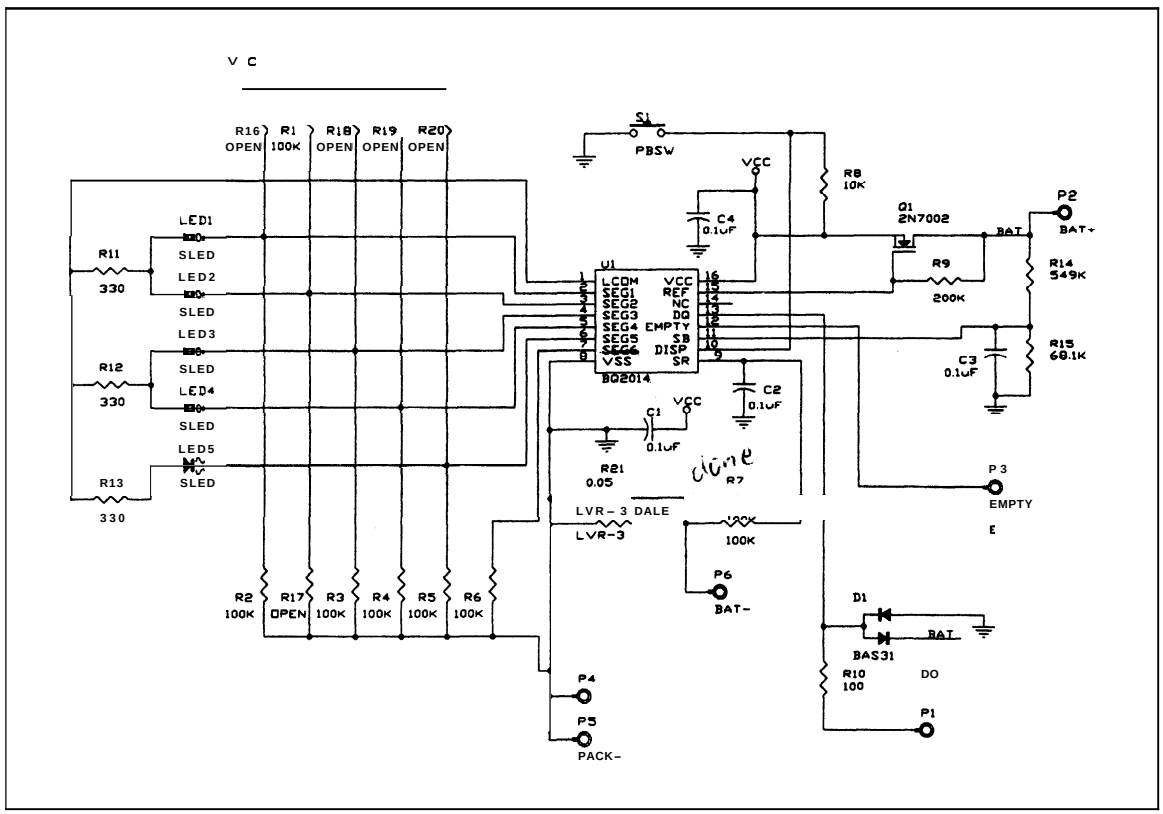


Figure 3. bq2014 NiMH Battery Capacity Monitoring System

charge at the current discharge rate. The average voltage is then multiplied by the remaining capacity to get the remaining Watthours. Although NiMH batteries are usually gauged in Amp-hours due to their relatively flat discharge profile, Watt-hour capacity can also be used for consistency with Li-Ion batteries.

Li-Ion battery capacity can be obtained using the bq2014 as shown in Figure 4. The primary difference is the configuration for the capacity and pulling PROG5 high to disable self-discharge compensation. The self-discharge for Li-Ion batteries is about 1/10th of that for NiMH and can be neglected in most applications. For those applications that choose to compensate for elf-discharge, the BATID register can be written with the week of the year so the time that the battery might have been exposed to self-discharge can be measured; however, in most applications, this correction is small enough to be neglected. Although the capacity for Li-Ion batteries is usually reported in Watt-hours, the capacity can be computed as described above. Figure 5 shows the cycle profile for a Li-Ion battery that has been discharged to 2.7 volts per cell after various levels of partial recharge. The battery capacity is determined properly, and the user can be comfortable with using the battery near the end of capacity.

Summary

Benchmarq is developing a family of compatible Li-Ion chargers, protectors, and capacity gauges. Using existing products, manufacturers can go to market today with chargers from Benchmarq that support both NiMH and Li-Ion batteries. Battery capacity can be determined for both NiMH and Li-Ion batteriee using the bq2014.

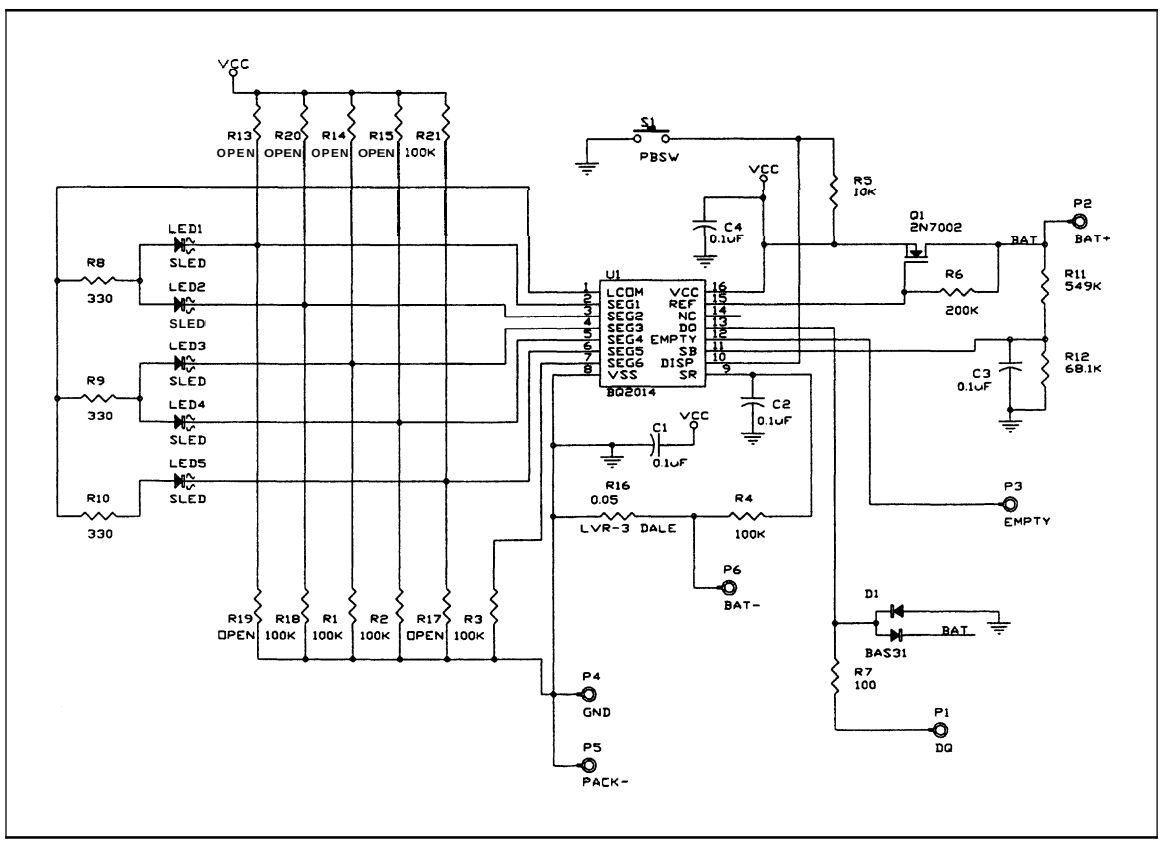


Figure 4. bq2014 Li-Ion Battery Capacity Monitoring System

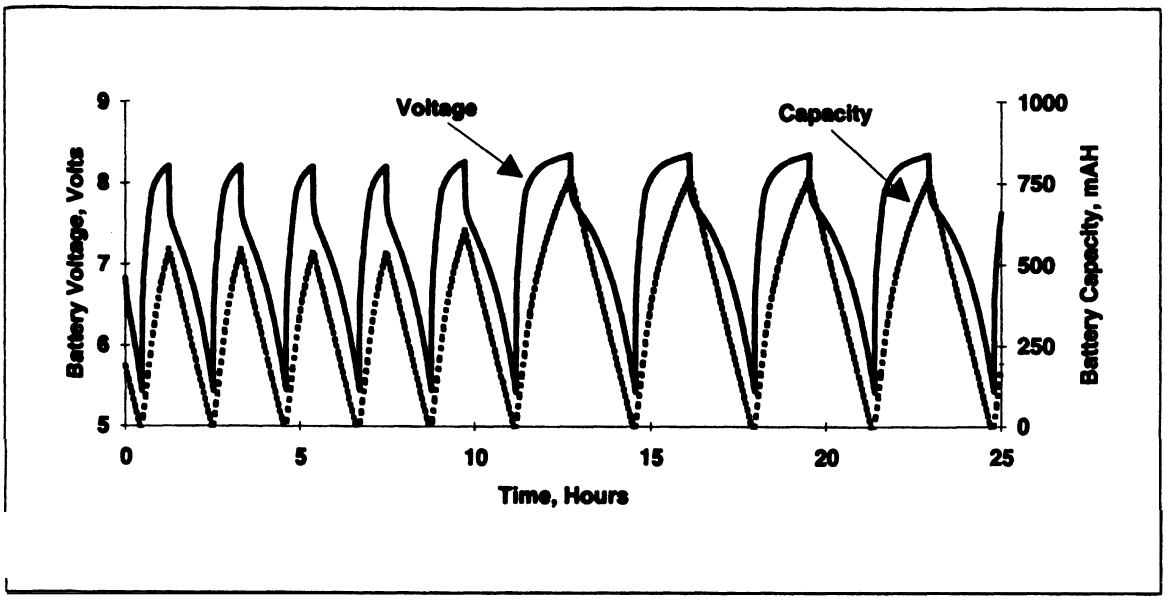


Figure 5. **Li-Ion Battery** Discharge and Capacity Profile

Notes

BENCHMARQ

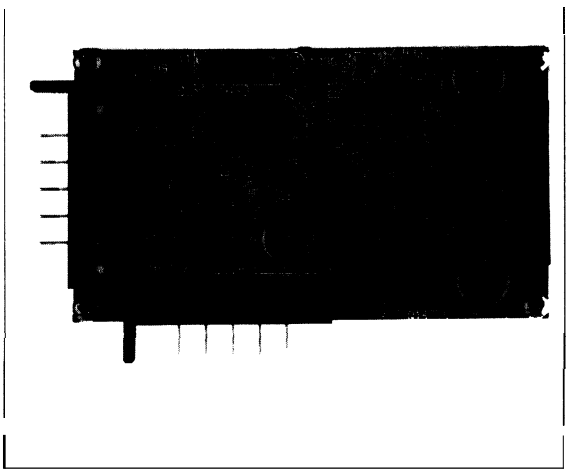
Product Brief **DV2043S7**

Level 2 Smart Charger With Dual Battery Selector

2

Features

- Level 2 Smart Charger evaluation and development board with Dual Battery Selector
- ➤ Supports System Management Bus specification and Level 2 Smart Charger specifications rev. 1.0
- ➤ Supports the Smart Battery Selector specification and handles switching between external DC and one or two battery packs
- ➤ Supports stand-alone or in-system charging
- ➤ Charge voltage regulation range from 10 to 17.4V, current regulation range from 0 to 2.4A
- DC input range from 18 to 24V
- High-efficiency, low-ripple switch-mode design with high-side current sensing
- For safety, charging is suspended on charging command timeout or maximum temperature
- Interrupts host on change in selector status (battery or DC removed or replaced)



General Description

The DV2043S7 Smart Charger Development System with Smart Battery Selector provides a development environment for Smart Charger devices compliant to the System Management Bus, Smart Charger, and Smart Battery Selector specifications. The unit supports single- or dual-battery configurations. The two-chip design provides stand-alone or in-system charging of SMBus-compliant batteries or dumb batteries under host control. Using a high-efficiency switch-mode regulator, the DV2043S7 will charge from 0 to 2.4A and voltage compliance of 10 to 17.4V. The bq2054 plus microcontroller high-side current sensing design can be modified to support other voltage and current requirements.

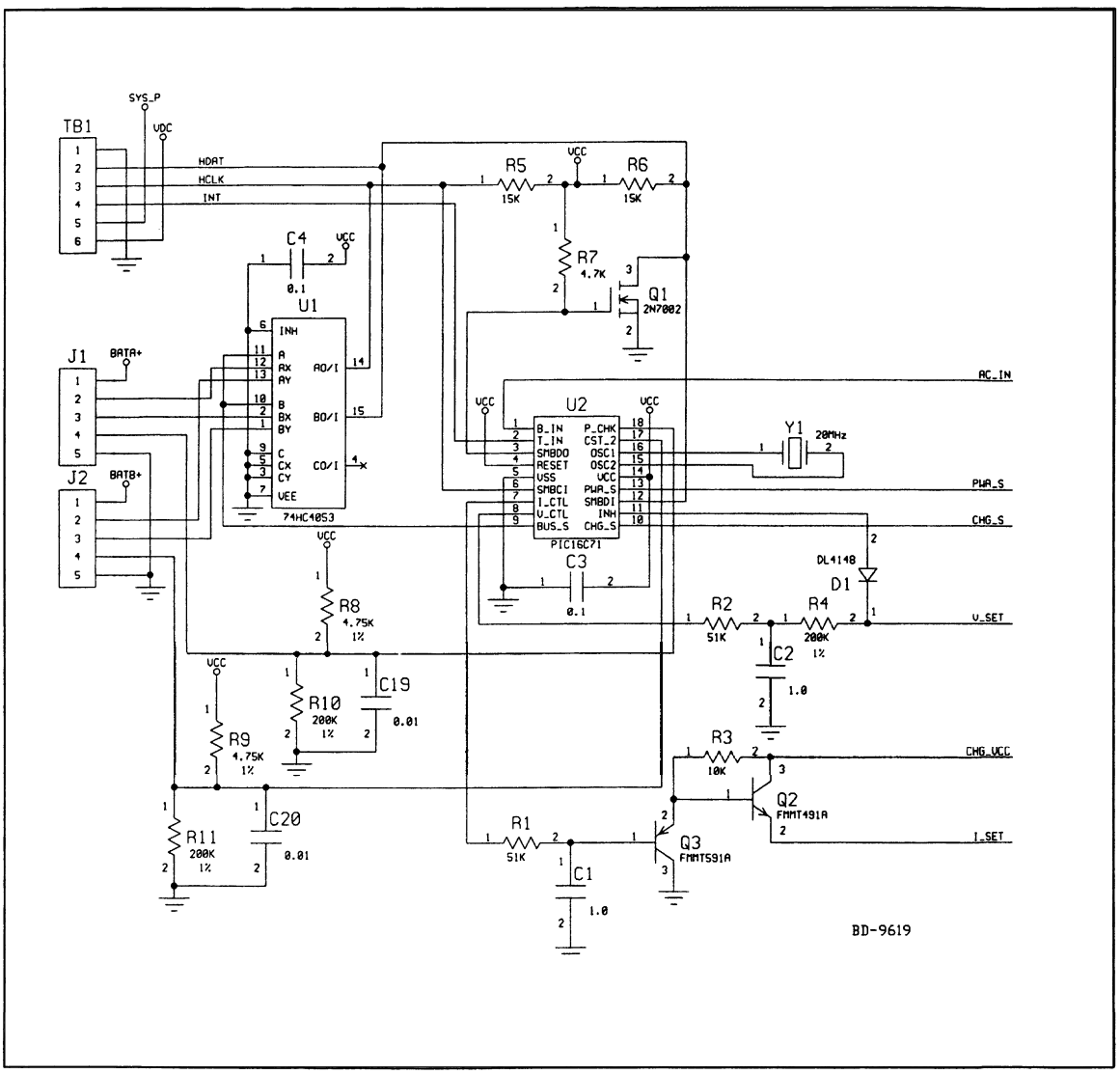
Charging begins with a pre-charge qualification phase. The bq2054 performs a low-current qualification test to detect batteries that have failed. The bq2054 pre-charges under-voltage batteries for as long as 34 minutes to try to bring the pack up to minimum voltage (8V). If this time expires and the pack voltage is still under 8V, then the DV2043S7 indicates a battery fault. The DV2043S7, responding to Smart Charger commands, adjusts the current and voltage to the appropriate levels. Charging terminates when the battery signifies a full charge condition. If maximum charging temperature is exceeded or if communication with the battery is lost, the DV2043S7 suspends charging until it receives new charging commands or until temperature returns to allowable levels.

The microcontroller communicates with the SMBus and provides the voltage and current scaling to the bq2054. The bq2054 is designed to regulate both current and voltage using an internal PWM and reference circuit. Efficiencies greater than 85% are possible using the DV2043S7 design, allowing for low-power dissipation. The DV2043S7 is ideal for in-system charging where a high-efficiency design is ideal.

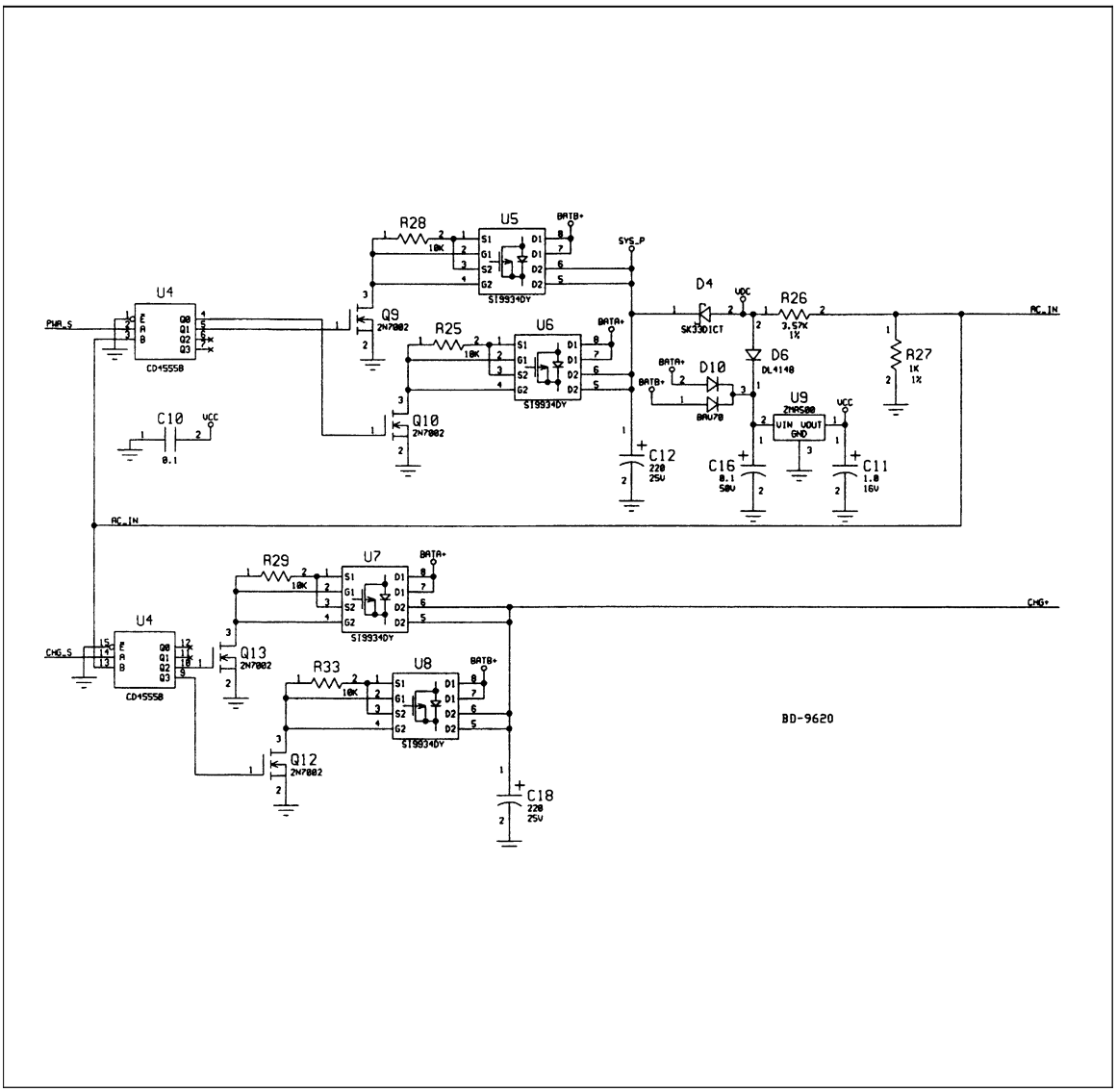
A full data sheet for this product is available on our web site (http://www.benchmarq.com), or you may contact the factory for one.

Aug. 1996

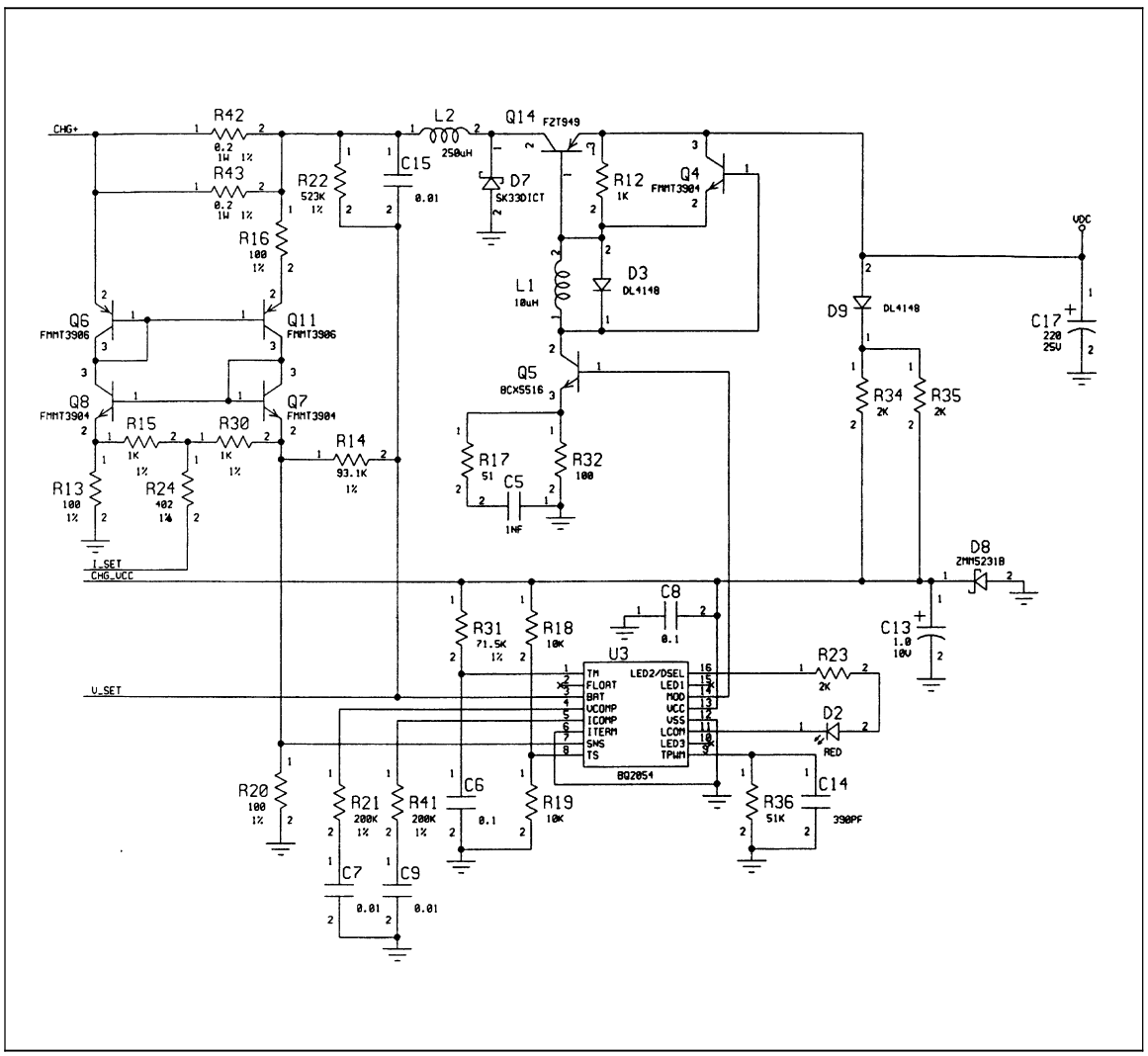
DV2043S7 Board Schematic



DV2043S7 Board Schematic (Continued)



DV2043S7 Board Schematic (Continued)



Gas Gauge IC With SMBus Interface

Features

- Provides conservative and repeatable measurement of **available** charge in NiCd, **NiMH,** and Lithium Ion rechargeable batteries
- ➤ Designed for battery pack integration
  - **120µA** typical standby current
  - Small size enables implementations in as little **as** ¾ square inch of PCB
- ➤ **Supports** Rev. 1.0 System Management Bus interface and Smart Battery Data **specifications**
- **Measurements** compensated for current and temperature
- Programmable self-discharge and charge compensation
- ➤ **Supports** SBData charge control commands for Li-Ion, NiMH, and NiCd chemistries
- ➤ 16-pin narrow SOIC

General Description

The **bq2040 Gas** Gauge **IC** With **SMBus** Interface is intended for battery-pack or in-system **installation** to maintain an accurate **record** of available battery charge. **The** bq2040 directly **supports** NiCd, NiMH, and Lithium Ion battery **chemistries.**

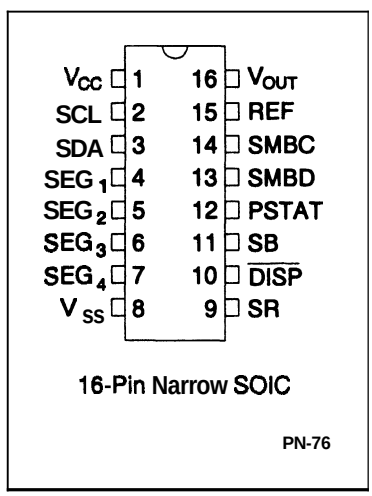
The **bq2040** supports the **System** Management Bus **(SMBus) protocol** and the Smart Battery Data (SBData) specifications (Rev. 1.0). Battery voltage, temperature, **state-**of-charge, capacity, charge-cycle count, etc. are available over the **SMBus** serial link. Battery-charge **state** can be **directly** indicated using a four-segment LED display to graphically depict battery full-to-empty in 25% **increments.**

The bq2040 estimates battery self-discharge based on an internal timer, temperature **sensor,** and **user-**programmable rate information stored in external **E²PROM.** The **bq2040** applies **compensations** for battery temperature and rate of charge or discharge to the charge, discharge, and **self-discharge** calcu**lations,** providing available charge information **across** a wide range of operating conditions. The **bq2040** automatically recalibrates, or 'learns' battery **capacity** in **the** full **course** of a discharge cycle **from** full to **empty.**

The **bq2040** may operate directly **from** three **or** four nickel chemistry cells. With the REF output and an external **transistor,** a simple, inexpensive regulator **can** be built to provide **Vcc** for other battery cell **configurations.**

An external **E²PROM** is **used** to program initial values into the **bq2040.** Valuer **such as** design capacity, **chemistry,** and aerial number, can be **customized** for individual battery pack configurations.

Pin Connections



16-Pin Narrow SOIC

PN-76

Pin Names

VOUT	**Supply output**	**SB**	**Battery** sense input
SEG1	LED segment 1	$\overline{\text{DISP}}$	Display control input
SEG2	LED segment 2	SR	Sense resistor input
SEG3	LED segment 3	SMBC	Serial communication clock
SEG4	LED segment 4	**SMBD**	Serial communication data **input/output**
SCL	**Serial** memory clock	**Vcc**	**3.0-6.5V**
SDA	Serial memory data	**Vss**	**System** ground
REF	Voltage reference **output**		
PSTAT	Protector status		

Pin Descriptions

SEG_1–SEG_4 **LED** display segment outputs

Each output may activate an external LED to sink the current sourced from V_{CC}.

SMBC System management bus clock

This open-drain bi-directional pin is used to clock the data transfer to and from the bq2040.

SMBD System management bus data

This open-drain bi-directional pin is used to transfer address and data to and from the bq2040.

SCL Serial memory clock

This output is used to clock the data transfer between the bq2040 and the external configuration memory.

SDA Serial memory data

This bi-directional pin is used to transfer address and data to and from the bq2040 and the external configuration memory.

V_{OUT} **Supply output**

This output supplies power to the external E^2PROM configuration memory.

PSTAT Protector status input

This input is used to report the protector status during charge. SBD charge current broadcasts zero current if this input is high. PSTAT should be connected to V_{SS} if Li-Ion batteries are not used.

SR **Sense resistor input**

The voltage drop (V_{SR}) across pins SR and V_{SS} is monitored and integrated over time to interpret charge and discharge activity. The SR input is connected to the sense resistor and the negative terminal of the battery. $V_{SR} < V_{SS}$ indicates discharge, and $V_{SR} > V_{SS}$ indicates charge. The effective voltage drop, V_{SRO}, as seen by the bq2040 is $V_{SR} + V_{OS}$ (see Table 3).

$\overline{DISP}$ Display control input

$\overline{DISP}$ high disables the LED display. DISP floating allows the LED display to be active during charge or during discharge if the rate is greater than a user-programmable threshold. $\overline{DISP}$ low activates the display.

SB **Secondary battery** input

This input monitors the single-cell voltage potential through a high-impedance resistive divider network The pack voltage is reported in the SBD register function Voltage() (0x09) and is compared to end-of-diecharge and charge voltage parameters.

REF Voltage reference output for regulator

REF provides a voltage reference output for an optional micro-regulator.

V_{CC} Supply voltage input

V_{SS} Ground

Functional Description

General Operation

The bq2040 determines battery capacity by monitoring the amount of charge input to or removed from a rechargeable battery. The bq2040 measures discharge and charge currents, estimates self-discharge, monitore the battery for low-battery voltage thresholds, and compensates for temperature and charge rates. The charge measurement is made by monitoring the voltage across a small-value series sense resistor between the negative battery terminal and ground. The available battery charge is determined by monitoring this voltage over time and correcting the measurement for the environmental and operating conditions.

Figure 1 shows a typical battery pack application of the bq2040 using the LED capacity display, the serial port, and an external E^2PROM for battery pack programming information. The bq2040 can be configured for battery chemistry, manufacturer name and serial number, display mode, self-discharge compensation, and various other battery-specific information. Table 1 outlines the externally programmable functions available in the bq2040. Refer to the Programming the bq2040 section for further details.

An internal temperature sensor eliminates the need for an external thermistor—reducing wet and components. An internal, temperature-compensated time-base eliminates the need for an external oscillator, further reducing cost and components. The entire circuit in Figure 1 could occupy less than ¾ square inch of board space.

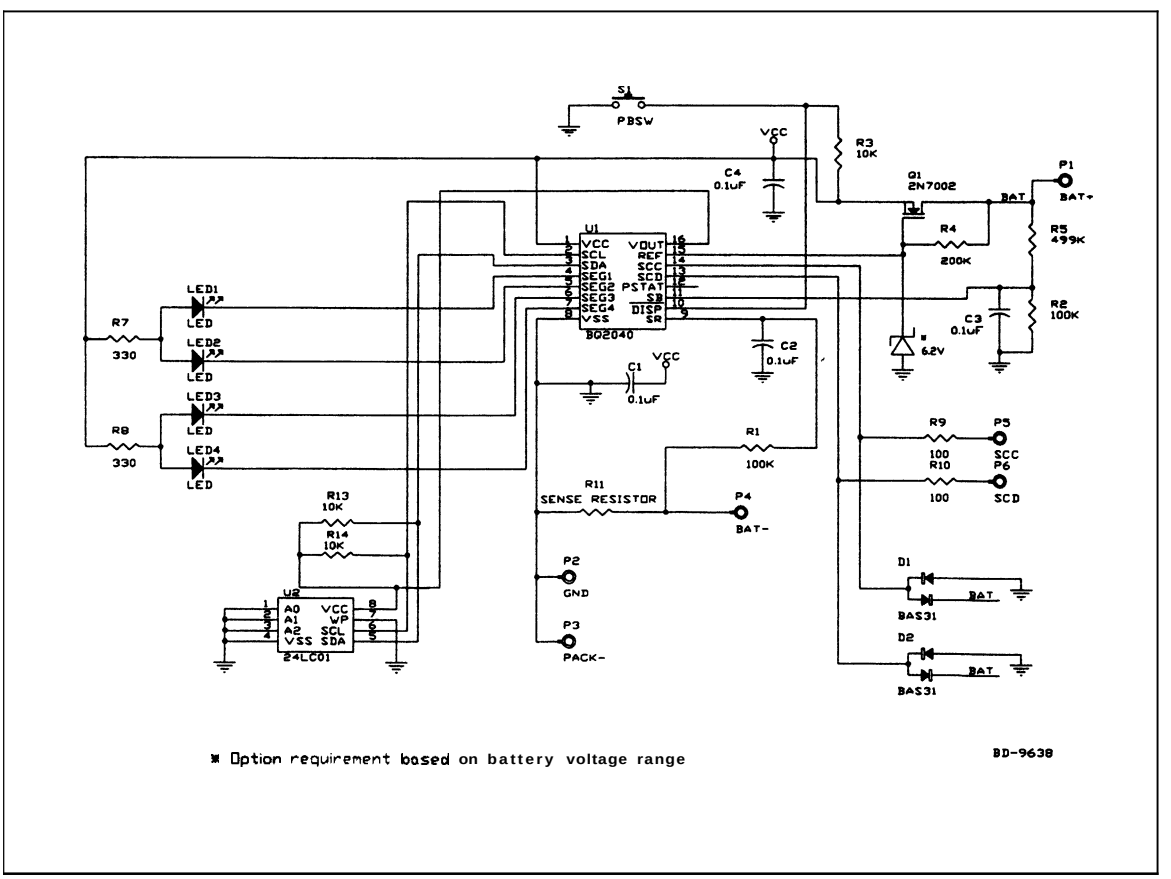


Figure 1. Battery Pack Application Diagram--LED Display

Table 1. Configuration Memory Programming Values

Parameter Name	Address	Length	Units
Design capacity	TBD	16 bits: low byte, high byte	mAh
Initial battery voltage	TBD	8 bite	N/A
Fast charging current	TBD	16 bits: low byte, high byte	mA
Charging voltage	TBD	16 bite: low byte, high byte	mV
Remain capacity alarm	TBD	16 bite: low byte, high byte	N/A
FLAGS1	TBD	8 bite	N/A
FLAGS2	TBD	8 bits	N/A
Current measurement gain	TBD	16 bits: low byte, high byte	N/A
EDV_1	TBD	16 bits: low byte, high byte	mV
EDV_F	TBD	16 bite: low byte, high byte	mV
Temperature offset	TBD	16 bits: low byte, high byte	°K
Self-discharge rate	TBD	16 bits: low byte, high byte	N/A
Digital filter	TBD	8 bits	N/A
Current integration gain	TBD	16 bits: low byte, high byte	N/A
Discharge display threshold	TBD	8 bite	N/A
Battery voltage offset	TBD	8 bits	mV
Battery voltage gain	TBD	8 bits	N/A
Slow charging current	TBD	16 bits: low byte, high byte	mA
Reserved	TBD		
Design voltage	TBD	16 bits: low byte, high byte	mV
Specification info	TBD	16 bite: low byte, high byte	N/A
Manufacturer date	TBD	16 bits: low byte, high byte	N/A
Serial number	TBD	16 bite: low byte, high byte	N/A
Manufacturer name	TBD	8 + 120 bits	N/A
Device name	TBD	8 + 120 bits	N/A
Chemistry	TBD	8 + 120 bits	N/A
Manufacturer data	TBD	8 +120 bits	N/A

Note: N/A = Not applicable; data packed or coded.

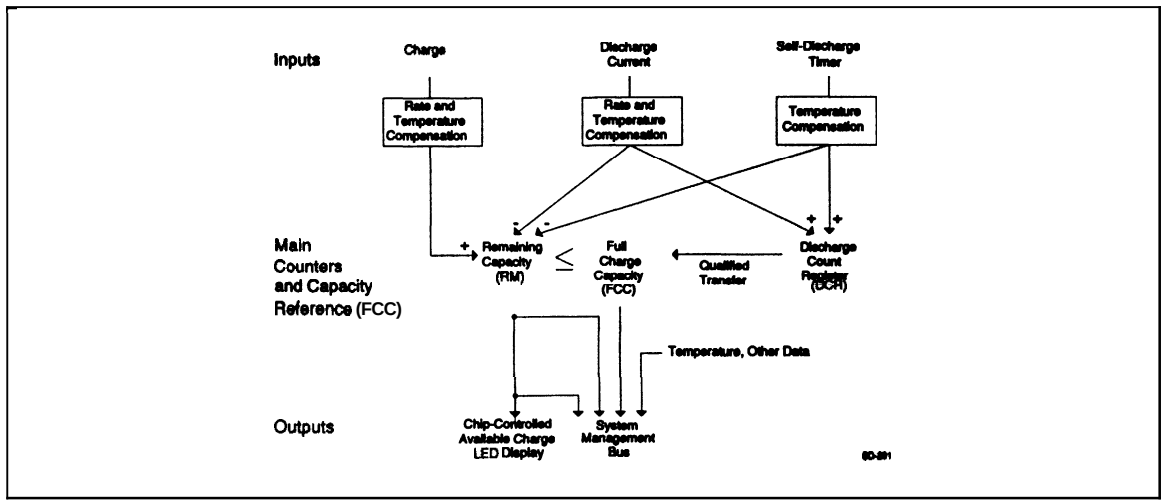


Figure 2. Operational Overview

Voltage Thresholds

In conjunction with monitoring V_{SR} for charge/discharge currents, the bq2040 monitors the battery potential through the SB pin. The voltage potential is determined through a resistor divider network per the following equation:

$$\frac{R_5}{R_2} = \frac{MBV}{2.25} - 1$$

where MBV is the maximum battery voltage, R_5 is connected to the positive battery terminal, and R_2 is connected to the negative battery terminal. should be rounded to the next highest integer. The battery voltage is monitored for the end-of-discharge voltage (EDV) and for maximum cell voltage (MCV) and for alarm warning conditions. EDV threshold levels are used to determine when the battery has reached an 'empty' state, and the MCV threshold is used for fault detection during charging. The battery voltage gain and two EDV thresholds are programmed via E²PROM. See the Programming the bq2040 section for further details.

If V_{SB} is below either of the two EDV thresholds, the associated flag is latched and remains latched, independent of V_{SB}, until the next valid charge.

EDV monitoring may be disabled under certain conditions. If the discharge current is greater than approximately 6A, EDV monitoring is disabled and resumes after the current falls below 6A.

Reset

The bq2040 is reset when first connected to the battery pack. The bq2040 can also be reset with a command over the serial port, as described in the Software Reset section.

Temperature

The bq2040 monitors temperature using an internal sensor. The temperature is used to adapt charge/discharge and self-discharge compensations as well as maximum temperature and $\Delta T/\Delta t$ during bq2040 controlled *charge*. Temperature may also be accessed wer the serial port. See the Prog[redacted]g the bq2040 section for further details.

Layout Considerations

The bq2040 measures the voltage differential between the SR and Vss pins. V_{OS} (the offset voltage at the SR pin) is greatly affected by PC board layout. For optimal results, the PC board layout should follow the strict rule of a single-point ground return. Sharing high–current ground with small signal ground causes undesirable noise on the small signal nodes. Additionally, in reference to Figure 1:

- The capacitors (C1, C3, and C4) should be placed as close as possible to the SB and V_{CC} pins, and their paths to Vss should be as short as possible. A high-quality ceramic capacitor of 0.1µf is recommended for Vcc.
- The sense resistor capacitor (C2) should be placed as close as possible to the SR pin.

- The sense resistor (R_{11}) should be as close as possible to the bq2040.
- The IC should be close to the cells for the best temperature measurement.

An optional zener may be necessary to ensure Vcc is not above the maximum rating during operation.

Gas Gauge Operation

The operational overview diagram in Figure 2 illustrates the operation of the bq2040. The bq2040 accumulates a measure of charge and discharge currents, as well as an estimation of self-discharge. Charge and discharge currents are temperature-compensated, and charge is rate-compensated. Self-discharge is only temperature compensated.

The main counter, Remaining Capacity (RM), represents the available battery capacity at any given time. Battery charging increments the RM register, while battery discharging and self-discharge decrement the RM register and increment the DCR (Discharge Count Register).

The Diecharge-Count Register (DCR) is used to update the Full-Charge Capacity (FCC) register only if a complete battery discharge from full to empty occurs without any partial battery charges. Therefore, the bq2040 adapts its capacity determination based on the actual conditions of discharge.

The battery's initial capacity is equal to the Design Capacity (DC). Until FCC is updated, RM counts up to, but not beyond, this threshold during subsequent charges.

1. Full-Charge Capacity or learned-battery capacity:

   FCC is the last measured discharge capacity of the battery. On initialization (application of V_{CC}), FCC = DC. During subsequent discharges, the FCC is updated with the latest measured capacity in the Discharge Count Register (DCR), representing a discharge from full to below EDV1. A qualified discharge is necessary for a capacity transfer from the DCR to the FCC register. The FCC also serves as the 100% reference threshold used by the relative display mode.

2. Design Capacity (DC):

   The DC is the user specified battery capacity and is programmed by using an external E^2PROM. The DC also provides the 100% reference for the absolute display mode.

3. Remaining Capacity (RM):

   RM counts up during charge to a maximum value of FCC and down during discharge and self-discharge to 0. RM is reset to 0x0A on initialization and when EDV1 = 1 and a valid charge is detected. To prevent overstatement of charge during periods of overcharge, RM stops incrementing when RM = FCC. RM may optionally be written to a user-defined value when fully charged when the battery pack is under bq2040 charge control. See bq2040 Charge Control for further details.

4. Discharge Count Register (DCR):

   The DCR counts up during discharge independent of RM and can continue increasing after RM has decremented to 0. Prior to RM = 0 (empty battery), both discharge and self-discharge increment the DCR. After RM = 0, only discharge increments the DCR. The DCR resets to 0 when RM = FCC. The DCR does not roll over but stops counting when it reachw FFFFh.

   The DCR value becomes the new FCC value on the first charge after a valid discharge to V_{EDV1} if:

   - No valid charge initiations (charges greater than 10mAh, where $V_{SRO} > V_{SRQ}$) occurred during the period between RM = FCC and EDV1 detected.
   - The self-discharge count is not more than 256mAh.
   - The temperature is ≥ 273°K when the EDV1 level is reached during discharge.

   The valid discharge flag (VDQ) indicates whether the present discharge is valid for FCC update. An FCC update cannot be greater than 256mAh.

Charge Counting

Charge activity is detected based on a positive voltage on the V_{SR} input. If charge activity is detected, the bq2040 increments RM at a rate proportional to V_{SRO} and, if enabled, activates an LED display. Charge actions increment the RM after compensation for charge rate and temperature.

The bq2040 determines charge activity sustained at a continuous rate equivalent to $V_{SRO} > V_{SRQ}$. A valid charge equates to sustained charge activity greater than 10 mAh. Once a valid charge is detected, charge counting continues until V_{SRO} falls below V_{SRQ}. V_{SRQ} is a programmable threshold as described in the Digital Magnitude Filter section.

Discharge Counting

All discharge counts where $V_{SRO} < V_{SRD}$ cause the RM register to decrement and the DCR to increment. V_{SRD} is a programmable threshold as described in the Digital Magnitude Filter section.

Self-Discharge Estimation

The bq2040 continuously decrements RM and increments DCR for self-discharge based on time and temperature. The self-discharge rate is dependent on the battery chemistry. The bq2040 self-discharge estimation rate is externally programmed in E^2PROM and can be programmed from 0 to 25% per day at 20°C. This rate doubles every 10°C from 0°C to 70°C.

Charge Control

The bq2040 supports SBD charge control by broadcasting ChargingCurrent() and ChargingVoltage() to the Smart Charger address. Smart-charger broadcasts can be disabled by writing bit 14 of BatteryStatus() to 1. The bq2040-based charge control can be disabled by setting bit 4 in Flags2 (MSB of 0x2f) to 1. See Programming the bq2040 for further details. If RM is below the full charge percentage, then the bq2040 will broadcast the fast charge current and voltage to the Smart Charger, if enabled. The bq2040 will broadcast the maintenance current values (trickle-rate) if Voltage() ie below EDVF.

The bq2040 internal charge control is compatible with Li-Ion and nickel-baaed chemistries. For Li-Ion, the bq2040 will broadcast the required charge current and voltage according to the values programmed in the esternal E^2PROM. During a valid charge (VQ = 1), if Current (0x0a) falls below 50mA while Voltage (0x09) is within 256mV of the charging voltage, the bq2040 will signal a valid charge termination where the Terminate-Charge and My-Charged bit is set in Battery Status.

For nickel-based chemistries, the bq2040 will broadcast the required charge current and voltage according to the programmed values in the external E^2PROM. Maximum Temperature and AT/& are used as valid charge termination methods. Note: Nickel-based chemistries require a charge voltage higher than the maximum cell voltage during charge to ensure constant-current charging. During a valid charge (VQ = 1), if the bq2040 determines a maximum temperature or AT/& rate greater than the programmed value, the Terminate Charge and Fully-Charged bit will be set in Battery Status.

Once the bq2040 determines a valid charge termination condition, charging current is set to 0 until this condition ceases (ΔT/Δt, MaxT, min. current). After a valid charge termination and the terminate condition ceases, maintenance (trickle) charge current and voltage will be broadcast to the Smart Charger. This process continues until RM falls below the full charge percentage. The bq2040 will then request the fast-charge current and voltage to the Smart Charger.

During fast charge, the bq2040 will suspend charge by requesting zero current and setting the Terminate-Charge-Alarm bit in Battery Status. Charge is suspended if the actual charge current is 25% greater than the programmed charged current. If the programmed charge current is less than 1024mA, overcurrent suspend will occur if the actual charge current is 256mA greater than the programmed value. Charge is also suspended if the actual battery voltage is 5% greater than the programmed charge voltage. If PSTAT goes high, then the bq2040 will suspend charge until the PSTAT goes low and Current() is zero. If the battery temperature is greater than the programmed maximum temperature prior to charge, then the bq2040 will suspend charge requests until the temperature falls below 50°C.

After a valid charge termination, RM may optionally be set to a value from 0 to 100% of the Full Charge Capacity. If RM is below the value programmed in Full Charge Percent, RM will be set to Full Charge Percent upon valid charge termination. If RM is above the Full Charge Percent, RM is not modified. This value also is used to determine when the bq2040 braodcasts fast-charge or maintenance-charge information.

Count Compensations

Charge activity is compensated for temperature and rate before updating the RM and/or DCR. RM is compensated for temperature before updating the RM register. Self-discharge estimation is compensated for temperature before updating RM or DCR.

Charge Compensation

Charge efficiency is compensated for rate, temperature, and battery chemistry. For Li-Ion chemistry cells, the charge efficiency is unity for all cases. However, the charge efficiency for nickel chemistry cells is adjusted wing the following equation:

$$RM = RM * (Q_{EFC} - Q_{ET})$$

where RelativeStateofCharge ≤ FullChargePercentage

and Q_{EFC} is the programmed fast charge efficiency varying from .75 to .99.

$$RM = RM * (Q_{ETC} - Q_{ET})$$

where RelativeStateofCharge ≥ FullChargePercentage

and Q_{ETC} is the programmed maintenance (trickle) charge efficiency varying from .50 to .97.

Q_{ET} is used to adjust the charge efficiency as the battery temperature increases according to the following:

$$Q_{ET} = 0 \text{ if } T < 30°C$$

$$Q_{ET} = 0.02 \text{ if } 30°C \le T < 40°C$$

$$Q_{ET} = 0.05 \text{ if } T \ge 40°C$$

Remaining Capacity Compensation

The bq2040 adjusts the RM as a function of temperature. This adjustment accounts for the reduced capacity of the battery at colder temperatures. The following equation is used to adjust RM:

If T ≥ 5°C

RemainingCapacity () = NominalAvailableCapacity()

If T < 5°C

RC() = NAC() (1 + TCC * (T - 5°C))

where T = temperature °C

TCC = 0.016 for Li-Ion cells

TCC = 0.0004 for Ni chemistry cells

Digital Magnitude Filter

The bq2040 has a programmable digital filter to eliminate charge and discharge counting below a set threshold. Table 2 shows typical digital filter settings. The proper digital filter setting can be calculated using the following equation.

$$V_{SRD}\ (mV) = -45 / DMF$$

$$V_{SRQ}\ (mV) = -1.25 \cdot V_{SRD}$$

Table 2. Typical Digital Filter Settings

DMF	DMF Hex.	V_{SRD} (mV)	V_{SRQ} (mV)
75	4B	-0.60	0.75
100	64	-0.45	0.56
150 (default)	96	-0.30	0.38
175	AF	-0.26	0.32
200	C8	-0.23	0.28

Error Summary

Capacity Inaccurate

The FCC is susceptible to error on initialization or if no updates occur. On initialization, the FCC value includes the error between the design capacity and the actual capacity. This error is present until a valid discharge occurs and FCC is updated (see the DCR description). The other cause of FCC error is battery wear-out. As the battery ages, the measured capacity must be adjusted to account for changes in actual battery capacity.

Current-Sensing Error

Table 3 illustrates the current-sensing error as a function of V_{SR}. A digital filter eliminates charge and discharge counts to the RM register when V_{SR} is between V_{SRQ} and V_{SRD}.

Display

The bq2040 can directly display capacity information using low-power LEDs. The bq2040 displays the battery charge state in either absolute or relative mode. In relative mode, the battery charge is represented as a percentage of the FCC. Each LED segment represents 25% of the FCC.

In absolute mode, each segment represents a fixed amount of charge, based on the initial design capacity. In absolute mode, each segment represents 25% of the design capacity. As the battery wears out over time, it is possible for the FCC to be below the initial design capacity. In this case, all of the LEDs may not turn on in absolute mode, representing the reduction in the actual battery capacity.

The displayed capacity is compensated for the present battery temperature. The displayed capacity will vary as temperature varies, indicating the available charge at the present conditions.

Table 3. bq2040 Current-Sensing Errors

Symbol	Parameter	Typical	Maximum	Units	Notes
V_{OS}	Offset referred to V_{SR}	± 50	± 150	µV	$\overline{DISP}$ = V_{CC}.
INL	Integrated non-linearity error	± 2	± 4	%	Add 0.1% per °C above or below 25°C and 1% per volt above or below 4.25V.
INR	Integrated non-repeatability error	± 1	± 2	%	Measurement repeatability given similar operating conditions.

When $\overline{DISP}$ is tied to Vcc, the SEG_{1-4} outputs are inactive. When $\overline{DISP}$ is left floating, the display becomes active whenever the bq2040 recognizes a valid charge or if the discharge rate exceeds the programmed fast discharge display threshold. When pulled low, the segment outputs become active immediately for a period of approximately 4 seconds.

The segment outputs are modulated as two banks of two, with segments 1 and 3 alternating with segments 2 and 4. The segment outputs are modulated at approximately 100Hz with each segment bank active for 30% of the period.

SEG_1 blinks at a 4Hz rate whenever V_{SB} has been detected to be below V_{EDV1} (EDV_1 = 1), indicating a low-battery condition. V_{SB} below V_{EDVF} (EDV_F = 1) disables the display output.

Microregulator

The bq2040 can operate directly from 3 or 4 nickel chemistry cells. To facilitate the power supply requirements of the bq2040, an REF output is provided to regulate an external low-threshold n-FET. A micropower source for the bq2040 can be inexpensively built using the FET and an external resistor; see Figure 1.

Communicating With the bq2040

The bq2040 includes a simple two-pin (SMBC and SMBD) serial data interface. A hoet processor uses the interface to access various bq2040 registers. This allows battery characteristics to be easily monitored, by adding two contacts to the battery pack. The open-drain SMBD and SMBC pine on the bq2040 are pulled up by the host system, or may be connected to Vss, if the serial interface is not used.

The interface uses a command-based protocol, where the host processor sends the smart battery address and an eight-bit command byte to the bq2040. The command directs the bq2040 to either store the next data received to a register specified by the command byte or output the data specified by the command byte.

bq2040 Data Protocols

The SMBus Host, acting in the role of an SMBus master, uses the read word and write word protocols to wmmunicate integer data with the bq2040. The read block protocol is used to access block data, such as ManufacturerName(). When the bq2040 needs to inform the SMBus Host about an alarm condition or to inform the Smart Battery Charger about its desired charging voltage or current, the bq2040, acting as an SMBus master, uses the write word protocol to communicate with the SMBus Host or Smart Battery Charger acting as an SMBus slave.

SMBus Host-to-bq2040 Message Protocol

The SMBus Host communicates with the bq2040 using one of three protocols:

- Read word
- Write word
- Read block

The particular protocol used is a function of the command. The protocols used are shown in Figure 3.

bq2040-to-Smart Battery Charger Message Protocol

The bq2040, acting as an optional SMBus master, sometimes tries to alter the charging characteristics. It also may send critical messages to the Smart Battery Charger, behaving as an SMBus slave wing the SMBus write word protocol. Communication begins with the Smart Battery Charger's address, followed by a command code and a two-byte value. The Smart Battery Charger adjusts its output to correspond with the request. See Figure 4.

bq2040 Critical Message Protocol

The bq2040 to SMBus Host message is sent using the SMBus write word protocol. Communication begins with the SMBus Host's address, followed by the bq2040's address, which also replaces the command code. The SMBus Host or Smart Battery Charger can now determine that the bq2040 was the originator of the message and that the following 16 bits are its statue. See Figure 6.

SMBus Host-to-Smart Battery Messages (see Table 7)

ManufacturerAccess() (0x00)

This read or write word is optional and its meaning is implementation specific.

RemainingCapacityAlarm() (0x01)

This read or write word sets or gets the LowCapacity threshold value. Whenever the RemainingCapacity() falls below the RemainingCapacity alarm value, the Smart Battery sends AlarmWarning() messages to the SMBus Hoet with the REMAINING_CAPACITY_ALARM bit set. A value of 0 disables this alarm. The value is set to 10% of the design capacity at time of manufacture. The value will remain unchanged until altered by the RemainingCapacityAlarm() function.

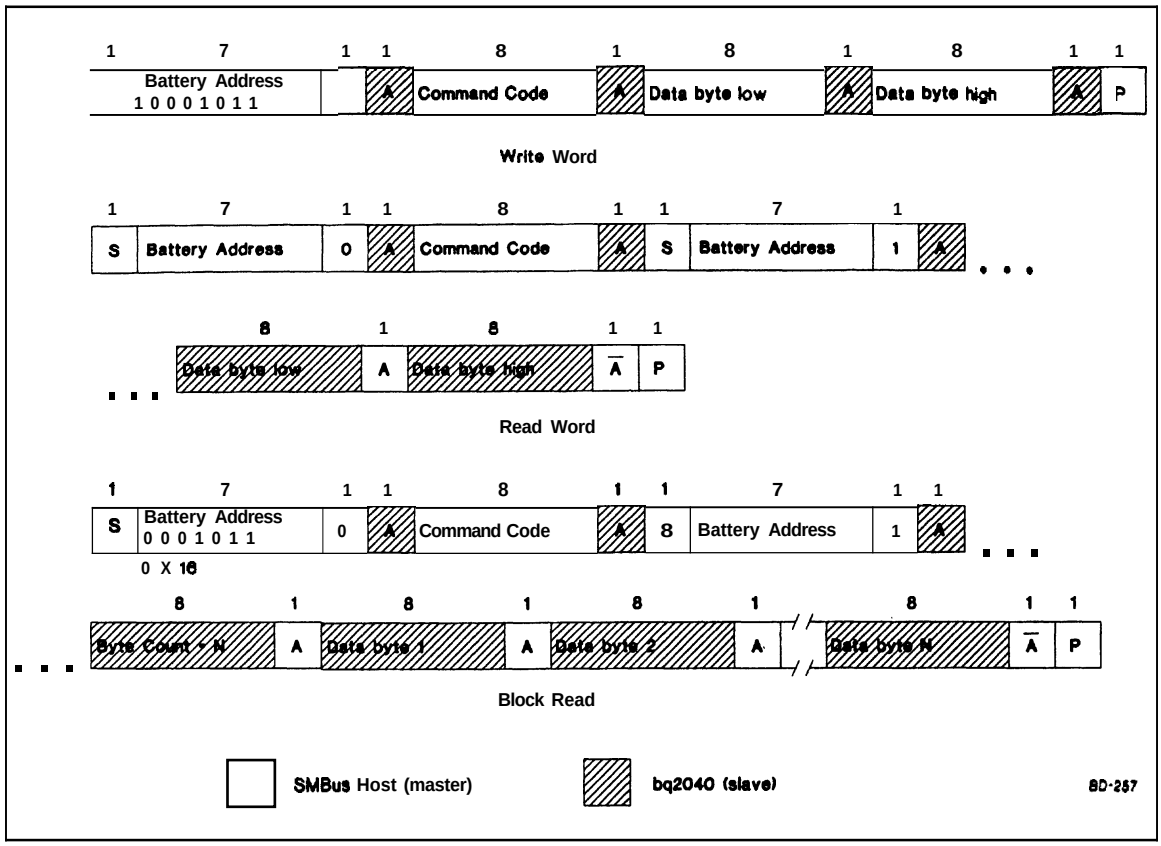


Figure 3. SMBus Host Protocols

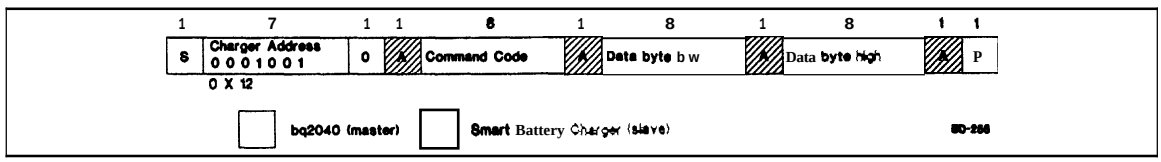


Figure 4. bq2040-to-Smart Battery Charger Message Protocol

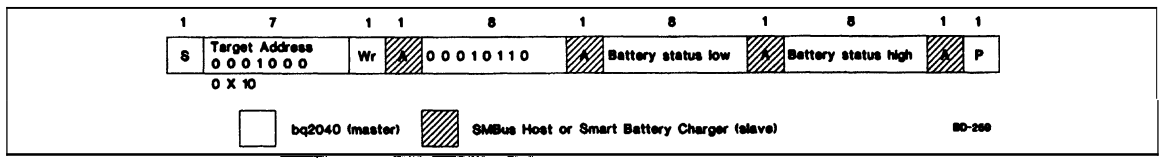


Figure 5. bq2040-to-Bus Host Message Protocol

Units: mAh

Range: 0 to 65,535 mAh

RemainingTimeAlarm() (0x02)

This read/write word sets or gets the RemainingTime alarm value. Whenever the AverageTimeTo Empty0 falls below the RemainingTime value, the Smart Battery sends AlarmWarning() messages to the SMBus Host with the REMAINING–TIME–ALARM bit set. A RemainingTime value of 0 disables this alarm. The RemainingTime alarm is set to 10 minutes at the time of manufacture. The RemainingTime alarm value may be changed until altered by the RemainingTimeAlarm() function.

Units: Minutes

Range: 0 to 65,536 minutes

BatteryMode() (0x03)

This read/write word selects the various battery operational modes. The bq2040 supports the battery's capacity information specified in mAh. This function also determines whether the ChargingCurrent() and ChargingVoltage() values are broadcast to the Smart Battery Charger when the Smart Battery requires charging (CHARGER-MODE bit).

CHARGER–MODE bit enables or disables the Smart Battery's transmission of ChargingCurrent() and ChargingVoltage() messages to the Smart Battery Charger. When set, the Smart Battery will not transmit ChargingCurrent() and ChargingVoltage() values to the Smart Battery Charger. When cleared, the Smart Battery will transmit the ChargingCurrent() and ChargingVoltage() values to the Smart Battery Charger when charging is desired.

CAPACITY_MODE bit indicates that capacity information will be reported in mAh and current is in mA units.

Field	Bits Used	Format	Allowable Values
Reserved	0–6, 8-13		
Condition Flag	7	read only bit flag	0 = Battery OK 1 = Conditioning cycle requested
CHARGER_MODE	14	bit flag	0 = Enable broadcast to charger 1 = Disable broadcast to charger
CAPACITY_MODE	15	bit flag	0 = Report in mA or mAh

AtRate() (0x04)

This read/write word is the first half of a two-function set used to set the AtRate value used in calculations made by the AtRateTimeToFull(), and AtRateTimeTo Empty().

- When the AtRate value is positive, the AtRateTimeToFull() function returns the predicted time to full-charge at the AtRate value of charge.
- When the AtRate value is negative, the AtRateTimeTo Empty0 function returns the predicted operating time at the AtRate value of discharge.

Units: mA

Range: -32,768 mA to 32,767 mA

Note: The AtRate value is set to zero at time of manufacture (default).

AtRateTimeToFull() (0x05)

This read-only word returns the predicted remaining time to fully charge the battery at the AtRate value (mA) and is valid only if read immediately after an AtRate() command.

Unite: minutes

Range: 0 to 66,534 min

Granularity: 2 min or better

Invalid Data Indication: 65,535 indicates the battery is not being charged

AtRateTimeToEmpty() (0x06)

This read-only word returns the predicted remaining operating time if the battery is discharged at the AtRate value and is valid only if read immediately after an AtRate() command.

Units: minutes

Range: 0 to 65,534 min

Granularity: 2 min or better

Invalid Data Indication: 66,535 indicates the battery is not being discharged

AtRateOK() (0x07)

This read-only word returns a Boolean value that indicates whether or not the EDV_1 flag has been set.

Boolean: Indicates if the battery can supply additional energy

Units: Boolean

Range: TRUE • 0 ,FALSE 0

Temperature0 (0x08)

This read-only word returns the cell-pack's internal temperature (°K).

Output: unsigned int—cell temperature in tenths of degrees Kelvin increments

Unite: 0.1°K

Range: 0 to +500.0°K

Granularity: 0.5°K or better

Accuracy: ±3°K

Voltage() (0x09)

This read-only word returns the cell-pack voltage (mV).

Output: unsigned int—battery terminal voltage in mV

Units: mV

Range: 0 to 65,535 mV

Granularity: 0.2% of design voltage

Accuracy: ±0.2% of design voltage

Current() (0x0a)

This read-only word returns the current through the battery's terminals (mA).

Output: signed int—charge/discharge rate in mA —positive for charge, negative for discharge

Units: mA

Range: 0 to 32,767 mA for charge or 0 to -32,768 mA for discharge

Granularity 0.2% of the DesignCapacity() or better

Accuracy: ±0.2% of the Design Capacity

AverageCurrent() (0x0b)

This read-only word returns a rolling average of the current through the battery's terminals. The AverageCurrent() function returns meaningful values after the battery's first minute of operation.

Output: signed int—charge/discharge rate in mA — positive for charge, negative for discharge

units: mA

Range: 0 to 32,767 mA for charge or 0 to -32,768 mA for diecharge

Granularity 0.2% of the DesignCapacity() or better

Accuracy: ±0.2% of the Design Capacity

MaxError() (0x0c)

This read-only word returns the expected margin of error (%).

Output: unsigned int—percent uncertainty

Unite: %

Range: 0 to 100%

Granularity: 1% or better

RelativeStateOfCharge() (0x0d)

This read-only word returns the predicted remaining battery capacity expressed as a percentage of FullChargeCapacity() (%).

Output unsigned int—percent of remaining capacity

Units: %

Range: 0 to 100%

Granularity: 1% or better

AbsoluteStateOfCharge() (0x0e)

This read-only word returns the predicted remaining battery capacity as a percentage of DesignCapacity() (%). Note that AbsoluteStateOfCharge can return values greater than 100%.

Output: unsigned int—percent of remaining capacity

Units: %

Range: 0 to 65,535 %

Granularity: 1% or better

Accuracy: ±MaxError()

RemainingCapacity() (0x0f)

This read-only word returns the predicted remaining battery capacity. The RemainingCapacity() value is expressed in mAh at the nominal discharge rate.

Output: unsigned int--estimated remaining capacity in mAh

Units: mAh

Range: 0 to 65,535 mAh

Granularity: 0.2% of DesignCapacity() or better

FullChargeCapacity() (0x10)

This read-only word returns the predicted pack capacity when it is fully charged. The FullChargeCapacity() value is expressed in mAh at a C/5 discharge rate.

Output: unsigned int—estimated full charge capacity in mAh or 10mWh

Units: mAh

Range: 0 to 65,535 mAh

Granularity: 0.2% of design capacity or better

RunTimeToEmpty() (0x11)

This read-only word returns the predicted remaining battery life at the present rate of discharge (minutes). The RunTimeToEmpty() value is calculated based on Current().

Output: unsigned int—minutes of operation left

Unite: minutes

Range: 0 to 65,534 minutes

Granularity. 2 minutes or better

Invalid data indication: 65.535 indicates battery is being charged

AverageTimeToEmpty() (0x12)

This read-only word returns the predicted remaining battery life at the present average discharge rate (minutes). The AverageTimeToEmpty is calculated based on AverageCurrent().

Output: unsigned int—minutes of operation left

Units: minutes

Range: 0 to 65,534 minutes

Granularity 2 minutes or better

Invalid data indication: 65,535 indicates battery is being charged

AverageTimeToFull() (0x13)

This read-only word returns the predicted time until the Smart Battery reaches full charge at the present average charge rate (minutes).

Output: unsigned int—remaining time in minutes

Unite: minutes

Range: 0 to 65,534 minutes

Granularity: 2 minutes or better

Invalid data indication: 65,635 indicates battery is not being charged

BatteryStatus() (0x16)

This read-only word returns The *Smart* Battery's status word (flags). Some of the BatteryStatus() flags (REMAINING–CAPACITY–ALARM and REMAINING_TIME_ALARM) are calculated based on current. Sea Table 4. for definitions.

unsigned int: Status Register with alarm conditions bit mapped as follows:

Alarm Bits	
0x8000	OVER_CHARGED_ALARM
0x4000	TERMINATE_CHARGE_ALARM
0x2000	reserved
0x1000	OVER_TEMP_ALARM
0x0800	TERMINATE_DISCHARGE_ALARM
0x0400	reserved
0x0200	REMAINING_CAPACITY_ALARM
0x0100	REMAINING_TIME_ALARM
Status Bits	
0x0080	INITIALIZED
0x0040	DISCHARGING
0x0020	FULLY_CHARGED
0x0010	FULLY_DISCHARGED
Error Code	
0x0000–0x000f	reserved for error codes

Some of the BatteryStatus() flags are calculated based on current. See Table 8 for definitions.

CycleCount() (0x17)

This read-only word returns the number of charge/discharge cycles the battery has experienced. A charge/discharge cycle starts from a base value equivalent to the battery's state-of-charge, upon completion of a charge cycle. The bq2040 increments the cycle counter during the current charge cycle, if the battery has been discharged to below 85% of the state-of-charge at the end of the last charge cycle. A discharge > 0.5% prevents false reporting of small charge/discharge cycles.

Output: unsigned int—count of charge/discharge cycles the battery has experienced

Unite: cycles

Range: 0 to 65,535 cycles; 65,535 indicates battery has experienced 65,535 or more cycles

Granularity: 1 cycle

DesignCapacity() (0x18)

This read-only word returns the theoretical capacity of a new pack The DesignCapacity() value is expressed in mAh at the nominal discharge rate.

Output: unsigned int—battery capacity in mAh

Unite: mAh

Range: 0 to 65,535 mAh

DesignVoltage() (0x19)

This read-only word returns the theoretical voltage of a new pack (mV).

Output: unsigned int—the battery's normal terminal voltage in mV

Units: mV

Range: 0 to 65,535 mV

SpecificationInfo() (0x1a)

This read-only word returns the version number of the SmartBattery specification the battery pack supports, as well as voltage and current scaling information in packed integer. The SpecificationInfo is packed as follows: (major version number * 0x10 + minor version number) + (voltage scaling + current scaling • 0x10) • 0x100.

Field	Bits Used	Format	Allowable Value
Revision	0–3	4-bit binary value	0–15
Version	4–7	4-bit binary value	0–15
VScale	8–11	4-bit binary value	0–3 (multiples voltage by 10 ^ VScale)
IPScale	12–15	4-bit binary value	0–3 (multiples current/power by 10 ^ IPScale)

ManufactureDate() (0x1b)

This read-only word returns the date the cell was manufactured in a packed integer word. The date is packed as follows: (year - 1980), month, day.

Field	Bits Used	Format	Allowable Value
Day	0–4	5-bit binary value	1–31 (corresponds to date)
Month	5–8	4-bit binary value	1–12 (corresponds to month number)
Year	9–15	7-bit binary value	0 • 127 (corresponds to year biased by 1980)

SerialNumber() (Oxlc)

This read-only word returns a serial number. This number, when combined with the ManufacturerName(), the DeviceName(), and the ManufactureDate(), uniquely identifies the battery (unsigned int).

Output: unsigned int

ManufacturerName() (0x20)

This read-only string returns a character string where the first byte is the number of characters available. The maximum number of characters is 16. The character string contains the battery manufacturer's name. For example, "BattCorp" identifies the Smart Battery manufacturer as BattCorp.

Output: string--character string

DeviceName() (0x21)

This read-only string returns a character string where the first byte is the number of characters available. The maximum number of characters is 15. The 15-byte character string contains the battery's name. For example, a DeviceName() of "MBC301" indicates that the battery is a model BC301.

Output: string—character string

DeviceChemistry() (0x22)

This read-only string returns a character string where the first byte is the number of characters available. The maximum number of characters is 15. The 15-byte character string contains the battery's chemistry. For example, if the DeviceChemistry() function returns "NiMH," the battery pack contains nickel metal hydride cells.

Output: string--character string

ManufacturerData() (0x23)

This read-only string allows access to an up to 15-byte manufacturer data string where the first five bytes are user-defmable in the external configuration memory and bytes six through fifteen are defined according to the followingtable.

Output: block data-data whose meaning is assigned by the Smart Battery's manufacturer

bq2040 or SMB Host-to-Smart Battery Charger Messages(See Table 6)

Whenever the BatteryMode() CHARGER_MODE bit is set to zero (default) and the bq2040 detects the presence of a Smart Battery Charger (level 2 charger—refer to the Smart Battery Charger Specification), the bq2040 sends the ChargingCurrent() and ChargingVoltage() values to the Smart Battery Charger. The bq2040 continues broadcasting these values at 12-second intervals.

ChargingCurrent() (0x14)

The bq2040 sends the desired charging rate to the Smart Battery Charger (mA).

Output: unsigned int —maximum charger output current in mA

Units: mA

Range: 0 to 65,534 mA

Granularity: 0.2% of the design capacity or better

Accuracy: ± 0.2% of the design capacity

Invalid data indication: 65,535 indicates the Smart Battery Charger should operate as a voltage source outside its maximum regulated current range

ChargingVoltage() (0x15)

The bq2040 sends the desired voltage to the Smart Battery Charger (mV).

Output: unsigned int—charger output current in mV

Units: mV

Range: 0 to 65,534 mV

Granularity: 0.2% of the design voltage or better

Accuracy: ± 0.2% of the design voltage

Invalid data indication: 65,535 indicates the Smart Battery Charger should operate as a current source outside its maximum regulated voltage range

bq2040 Critical Messages

Whenever the bq2040 detects a critical condition, it becomes a bus master and sends AlarmWarning() messages to both the Smart Battery Charger, if enabled, and the SMBus Host, as appropriate, notifying them of the critical condition(s). The message sent by the AlarmWarning() function is similar to the message retuned by the BatteryStatus() function. The bq2040 continues broadcasting the AlarmWarning() at 12-second intervals until the critical condition(s) has been corrected.

AlarmWarning() (0x16)

The bq2040, acting as a bus master device to the SMBus Host and/or the Smart Battery Charger, sends this message to notify them that one or more alarm conditions exist. Alarm indications are encoded as bit fields in the Battery's statue, which is then sent to the SMBus Host and/or Smart Battery Charger by this function. The AlarmWarning() is repeated at 12-second intervals until the condition(s) causing the alarm haa been corrected.

Output: unsigned int—Status Register with alarm conditions bit mapped as follows:

Alarm Bits	
0x8000	OVER_CHARGED_ALARM
0x4000	TERMINATE_CHARGE_ALARM
0x2000	reserved
0x1000	OVER_TEMP_ALARM
0x0800	TERMINATE_DISCHARGE_ALARM
0x0400	reserved
0x0200	REMAINING_CAPACITY_ALARM
0x0100	REMAINING_TIME_ALARM
Status Bits	
0x0080	INITIALIZED
0x0040	DISCHARGING
0x0020	FULLY_CHARGED
0x0010	FULLY–DISCHARGED
Error Code	
0x0000–0x000f	All bits set high prior to AlarmWarning() transmission

Note: Alarm bits 0x0200 and 0x0100 cause the AlarmWarning() to be sent only to the SMBus Host. All other

alarm bite cause the AlarmWarning() to be sent to both the SMBus Host and the Smart Battery Charger, if CHARGER–MODE = 0.

Status Bits and Error Codes

Status bits are listed in Table 4 and error codes are listed in Table 5.

FLAGS1&2() (0x2c)

This read-only register returns an unsigned integer representing the internal status registers of the bq2040. The MSB represents FLAGS2, and the LSB represents FLAGS1. See Table 6 for the bit description for FLAGS1&2.

FLAGS2

The *Display Mode* flag (DMODE), Bit 7, determines whether the bq2040 displays Relative or Absolute capacity.

The DMODE values are:

FLAGS2 Bits							
7	6	5	4	3	2	1	0
DMODE	-	-	-	-	-	-	-

Where DMODE is:

0 Selects Absolute display

1 Selects Relative display

The *Protector Status* flag (PSTAT), bit 6, determines if the overvoltage protector for Li-Ion cells is active. If PSTAT = 1, then the bq2040 broadcasts Terminate_Charge and sets the charging current to zero until the average current is zero and PSTAT = 0.

The PSTAT values are:

FLAGS2 Bits							
7	6	5	4	3	2	1	0
-	PSTAT	-	-	-	-	-	-

Where PSTAT is:

0 Protector status OK

1 Protector status not OK; suspend charge

The *Chemistry* flag (CHM), Bit 5, selects Li-Ion or Nickel compensation factors.

The CHM values are:

FLAGS2 Bits							
7	6	5	4	3	2	1	0
-	-	CHM	-	-	-	-	-

Where CHM is:

0 Selects Nickel

1 Selects Li-Ion

Bit 4, the *Charge Control* flag (CC), determines whether a bq2040-based charge termination will set RM to a user-defined programmable full charge capacity.

The CC values are:

FLAGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	CC	-	-	-	-

Where CC is:

0 RM is not modified on valid bq2040 charge termination

1 RM is set to a programmable percentage of the FCC when a valid bq2040 charge termination occurs

Bit 3 is reserved.

Bit 2, the *Overvoltage* flag (OV), is set when the bq2040 detects a pack voltage 5% greater than the programmed charging voltage. This bit is cleared when the pack voltage falls 5% below the programmed charging voltage.

The OV values are:

FLAGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	OV	-	-

Where OV is:

0 BatteryVoltage() < 1.05 * ChargingVoltage

1 BatteryVoltage() ≥ 1.05 * ChargingVoltage

Table 6. Bit Description for FLAGS1 and FLAGS2

	(MSB) 7	6	5	4	3	2	1	0 (LSB)
FLAGS2	DMODE	PSTAT	CHM	CC		OV	LTF	OC
FLAGS1	ΔT/Δt1	ΔT/Δt0	VQ	WRINH	VDQ	SEDV	EDV1	EDVF

- = Reserved

Bit 1, the Low *Temperature Fault* flag (LTF), is set when temperature<0°C and cleared when temperature>5°C.

The LTF values are:

FLAGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	LTF	-

Where LTF is:

0 Temperature>5°C

1 Temperature<0°C

Bit 0, the *Overcurrent* flag (OC), is set when the average current is 25% greater than the programmed charging current. If the charging current ie programmed less than 1024mA, overcurrent is set if the average current is 256mA greater than the programmed charging current. This flag is cleared when the average current falls below 256mA.

The OC values are:

FLAGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	OC

Where OC is:

0 Average current is less than 1.25 • charging current or less than 256mA if charging current is programmed less than 1024mA

1 Average current exceeds 1.25 • charging current or 256mA if the charging current ie programmed leas than 1024mA. This bit is cleared if average current<256mA

FLAGS1

Bit 7 and bit 6, the *Delta Tempemture* flags, signify whether the bq2040 is sensing a valid ΔT/Δt for charge termination. Both bits must transition to a 1 to signify that the rise in battery temperature exceeds the programmed rate threshold. The bits are clear if the rate of temperature falls below the programmed ΔT/Δt rate.

The $\Delta T/\Delta t_0$, $\Delta T/\Delta t_1$ values are:

FLAGSl Bit8							
7	6	5	4	3	2	1	0
$\Delta T/\Delta t_1$	$\Delta T/\Delta t_0$	-	-	-	-	-	-

Where $\Delta T/\Delta t_0$, $\Delta T/\Delta t_1$ is:

0 Temperature < Programmed ΔT/Δt rate

1 Temperature > Programmed ΔT/Δt rate

The *Valid Charge* flag (VQ), Bit 5, is set when $V_{SRO} \geq V_{SRQ}$ and 10mAh of charge has accumulated. This bit is cleared during a discharge and when $V_{SRO} \leq V_{SRQ}$.

The VQ values are:

FLAGSl Bit8							
7	6	5	4	3	2	1	0
	-	VQ	-	-	-	-	-

Where VQ is:

0 $V_{SRO} \leq V_{SRQ}$

1 VSRO ≥ VSRQ and 10mAh of charge has accumulated

The Write Inhibit flag (WRINH), Bit 4, allows or inhibits writes to all registers.

The WRINH values are:

FLAGSl Bit8							
7	6	5	4	3	2	1	0
		-	WRINH	-	-	-	-

Where WRINH is:

0 Allows writes to all registers

1 Inhibits all writes and secures the bq2040 from invalid/undesired writes.

WRINH should be set at the time of pack assembly and tested to prevent normally read-write registers from accidental over-writing.

The *Valid Discharge* flag (VDQ), Bit 3, is set when a valid discharge is occurring (discharge cycle valid for learning new full charge capacity) and cleared if a partial charge is detected, EDV1 is asserted when T<0°C, or self-discharge accounts for more than 256mAh of the discharge.

The VDQ values are:

FLAGSl Bits							
7	6	5	4	3	2	1	0
				VDQ	-	-	

Where VDQ is:

0 Self-discharge is greater than 256mAh, EDVl = 1 when T<0°C or VQ = 1

1 On first discharge after RM=FCC

The Stop *EDV* flag (SEDV), Bit 2, is set when the discharge current>6.15A and cleared when the discharge current falls below 6.15A.

The SEDV values are:

FLAGS1 Bits							
7	6	5	4	3	2	1	0
				-	SEDV	-	-

Where SEDV is:

0 Current<6.15A

1 Current>6.15A

The First *End-of-DischargeVoltage* flag (EDV1), Bit 1, is set when Voltage()<EDV1=1 if SEDV=0 and cleared when VQ=1 and Voltage()>EDV1.

The EDVl values are:

FLAGS1 Bits							
7	6	5	4	3	2	1	0
					-	EDVl	-

Where EDVl is:

0 VQ = 1 and Voltage ()> EDVl

1 Voltage() < EDVl and SEDV = 0

The *Final* End-of-Discharge*Voltage* flag (EDVF), Bit 0, is set when Voltage()<EDVF=1 if SEDV=0 and cleared when VQ=1 and Voltage()>EDVF.

The EDVF values are:

FLAGS1 Bits							
7	6	5	4	3	2	1	0
						-	EDVF

Where EDVF is:

0 VQ = 1 and Voltage > EDVF

1 Voltage < EDVF and SEDV = 0

Software Reset

The bq2040 can be reset over the serial port by confirming that the WRINH bit is set to zero in FLAGS1, writing MaxError() (0x0c) to any value other than 2, and writing the reset register (0x44) to 8009, causing the bq2040 to reinitialize and read the default values from the external E^2PROM.

Programming the bq2040

The bq2040 requires the proper programming of an external E^2PROM for proper device operation. Each module can be calibrated for the greatest accuracy, or general "default" values can be used. A programming kit (interface board, software, and cable) for an IBM-compatible PC is available from Benchmarq. Please contact Benchmarq for further detail

The bq2040 uses a 24C01 or equivalent serial E^2PROM for storing the various initial values, calibration data, and string information. Table 1 outlines the parameters and addresses for this information. Tables 9 and 10 detail the various register contents and show an example program value for an 1800mAh NiMH battery pack, using a 50mΩ sense resistor.

Table 7. Error Codes (BatteryStatus() (0x16))

Error	Code	Access	Description
OK	0x0000	read/write	bq2040 processed the function code without detecting any errors
Busy	0x0001	read/write	bq2040 is unable to process the function code at this time
NotReady	0x0002	read/write	bq2040 cannot read or write the data at this time – try again later
UnsupportedCommand	0x0003	read/write	bq2040 does not support the requested function code
AccessDenied	0x0004	write	bq2040 detected an attempt to write to a read-only function code
Overflow/Underflow	0x0005	read/write	bq2040 detected a data overflow or underflow
BadSize	0x0006	write	bq2040 detected an attempt to write to a function code with an incorrect size data block
UnknownError	0x0007	read/write	bq2040 detected an unidentifiable error

Note: Reading the bq2040 after an error clears the *error* code.

Table 8. Status Bits

Alarm Bit8		
Bit Name	**Set When:**	**Reset When:**
OVER-CHARGE- ———	bq2040 detects over-temperature, ΔT/Δt, or minimum charge current conditions exist (Note: valid charge termination).	A discharge occurs or when ΔT/Δt, over-temperature, or minimum current ceases during charge.
TERMINATE_CHARGE_ALARM	bq2040 detects over-current, over-voltage, over-temperature, or ΔT/Δt conditions exist during charge. Charging current is set to zero, indicating a charge suspend.	A discharge occurs or when all conditions causing the event cease.
OVER_TEMP_ALARM	bq2040 detects that its internal temperature is greater than the programmed value (valid termination).	Internal temperature falls below 50°C.
TERMINATE_DISCHARGE_ALARM	bq2040 determines that it has supplied all the charge that it can without being damaged (EDVF).	Battery reaches a state of charge sufficient for it to once again safely supply power.
REMAINING_CAPACITY_ALARM	bq2040 detects that the RemainingCapacity() is less than that set by the RemainingCapacity() function.	Either the value set by the RemainingCapacityAlarm() function is lower than the Remaining Capacity() or the RemainingCapacity() is increased by charging.
REMAINING-TIME-ALARM	bq2040 detects that the estimated remaining time at the present discharge rate is less than that set by the RemainingTimeAlarm() function.	Either the value set by the RemainingTimeAlarm() function lower than the AverageTimeToEmpty() or the AverageTimeToEmpty() increased by charging.
Status Bits		
Bit Name	**Set When:**	**Reset When:**
INITIALIZED	bq2040 is aet when the bq2040 has reached a full or empty state.	Battery detects that power-on or user-initiated reset has occurred.
DISCHARGING	bq2040 determines that it is not being charged.	Battery detects that it is being charged.
FULLY_CHARGED	bq2040 determines a valid charge termination. RM will then be set to full charge percentage if necessary.	RM discharges below the full charge percentage
FULLY_DISCHARGED	bq2040 determines that it has supplied all the charge that it can without being damaged (that is, continued uae will result in permanent capacity lose to the battery)	RelativeStateOfCharge() is greater than or equal to 10%

Table 9. Example Register Contents (Preliminary)

Description	E²PROM Address		E²PROM Hex Content8		Example Values	Notes
	Low Byte	High Byte	Low Byte	High Byte		
Design Capacity			08	07	1800mAh	This sets the initial full charge battery capacity stored in FCC. FCC is updated with the actual full to empty discharge capacity after a valid discharge from RM = FCC to Voltage() = EDV1.
Initial Battery Voltage			30	2a	10800mV	This register is used to adjust the battery voltage. Comparing the values read from the bq2040 to two known input voltages allows the bq2040 to calibrate the battery voltage to within 1%. This action adjusts for errors in the resistor-dividers used for the SB input and bq2040 offset errors.
Fast charging current			08	07	1800mA	This register is wed to set the fast charge current for the smart Charger.
Fast charging voltage			c4	3b	15300mV	This register is wed to set the fast charge voltage for the Smart Charger.
Remaining Capacity Alarm			b4	00	180mAh	This value represents the low capacity alarm value.
FLAGS1			10			This enables writes to all registers and should be set to 10h prior to pack ehipment to inhibit undesirable writes to the bq2040.
FLAGS2			b0		Li-Ion = a0h NiMH = 80h	See FLAGS2 register for the bit description and the proper value for programming FLAGS2. Selects relative display mode, Lithium Ion compensation factors, and enables bq2040 Smart Charger control.
Current Measurement Gain[1]			ee	02	37.5/.05	The current gain measurement and current integration gain are related and defined for the bq2040 current measurement. 0x0c = 37.5/sense resistor value in ohms.
EDV1			16	db	9450mV (1.05V/cell)	The value programmed is the two's complement of the threshold voltage in mV.
EDVF			d8	dc	9000mV (1.0V/cell)	The value programmed is the two's complement of the threshold voltage in mV.

Note: 1. Can be adjusted to calibrate the battery pack.

Table 9. Example Register Contents (Continued)

Description	E²PROM Address		E²PROM Hex Contents		Example Values	Notes
	Low Byte	High Byte	Low Byte	High Byte		
Temperature Offset[1]			32		5.0°C	The default value is 0x80 (12.8° + nominal value). Actual temp (20°C) = Nominal temp. (15°C) - temp. offset (5°C) where temperature determined by the bq2040 can be adjusted from 0° to 25.5° (Temperature offset (0-255) * .1) + nominal value temp.
Maximum Charge Temperature, ΔT/Δt			87		61.2°C (74 - (8 * 1.6)) ΔT/Δt = 7	Maximum charge temperature is 74 - (mt * 1.6)°C (upper nibble). ΔT/Δt rate is in the lower nibble and varies from 0 to 15, where 0 is more sensitive than 15. Typical value is 7.
Self-Discharge Rate			f0		.15C	This packed field is the 2s complement of ((RM/4)/(RM/x)) where RM/x is the desired self-discharge rate per day at room temperature.
Digital Filter			fa		.18mV	This field is used to set the digital magnitude filter as described in Table 2.
Current Integration Gain[1]			40	00	3.2/.05	This field represents the following: 3.2/sense resistor in ohms. It is used by the bq2040 to scale the measured voltage values on the SR pi. in mA and mAh. This register also compensates for variations in the reported sense resistor value.
Full Charge Percentage			a0		96% = 60 2.3 (60) = a0	This packed field is the 2s complement of the desired value in RM when the bq2040 determines a full charge termination. If RM is below this value, RM is set to this value. If RM is above this value, then RM is not adjusted.
Charge Compensation			bd		85% = maintenance comp. 95% = fast charge comp.	This packed value is used to set the fast charge and maintenance charge efficiency for nickel-based batteries. The upper nibble adjusts the maintenance charge compensation; the lower nibble adjusts the fast charge compeneation. Maintenance, upper nibble = (eff% * 256 - 128)/8 Fast charge, lower nibble = (eff% * 256 - 192)/4
Battery Voltage Offset[1]			00		0mV	This value is used to adjust the battery voltage offset according to the following: Voltage offset (mV) = V_{SB} * 1000 + V_{OFF}) * no. of cells
Voltage Gain[1]			09	05	9.02	Voltage gain is packed as two units. For example, R5/R2 = 9.09 would be stored as: whole number stored in 0x1a (=09h) and the decimal component stored in Oxlb as 256 * 0.02 = 05.
Serial Number			12	27	10002	This contains the optional pack serial number.

Note: 1. Can be adjusted to calibrate the battery pack.

Table 9. Example Register Contents (Continued)

Description	E²PROM Address		E²PROM Hex Contents		Example Values	Notes
	Low Byte	High Byte	Low Byte	High Byte		
Charge Cycle Count			00	00	0	This field contains the charge cycle count and should be set to zero for a new battery.
Reserved						
Maintenance Charge Current			64	00	100mA	This field contains the desired maintenance current after fast charge termination by the bq2040.
Reserved						
Design Voltage			30	2a	10800mV	This is nominal battery pack voltage.
Specification Information			00	00		This is the default value for this register.
Manufacturer Date			a1	20	May 1,1996 = 8353	Packed per the ManufactureDate() description, which represents May 1.1996 in this example.

Table 10. Example Register Contents (String Data)

String Description	Address	0x ?0	0x ?1	0x ?2	0x ?3	0x ?4	0x ?5	0x ?6	0x ?7	0x ?8	0x ?9-?f
Reserved		00	00	00	00	00	00	00	00	00	00
Manufacturer's Name		09	42 B	45 E	4e N	43 C	48 H	4d M	41 A	52 R	51 Q
Device Name		08	42 B	51 Q	32 2	30 0	39 9	31 1	41 A	34 4	00-00
Chemistry		04	4e N	69 I	4d M	48 H	00	00	00	00	00-00
Manufacturer's Data		04	44 D	52 R	31 1	35 5	00	00	00	00	00-00

Table 11. bq2040 Master Functions

Function	Code	Access	Data
ChargingCurrent (to Smart Battery Charger)	0x14	write	mA
ChargingVoltage (to Smart Battery Charger)	0x15	write	mV
AlarmWarning (to SMBus Host)	0x16	write	word
AlarmWarning (to Smart Battery Charger)	0x16	write	word

Table 12. Smart Battery Slave Functions (Preliminary)

Function	Code	Access	Units	Defaults
ManufacturerAccess	0x00	read/write	word	
RemainingCapacityAlarm	0 1	read/write	mAh	0.1* DC
RemainingTimeAlarm	0x02	read/write	minutes	000Ah
BatteryMode	0 3	read/write	bit flags	0000h
AtRate	0x04	read/write	mA	0000h
AtRateTimeToFull	0x05	read	minutes	FFFFh
AtRateTimeToEmpty	0x06	read	minutes	FFFFh
AtRateOK	0 7	read	Boolean	0000h
Temperature	0x08	read	0.1°K	
Voltage	0x09	read	mV	
Current	0x0a	read	mA	0000h
AverageCurrent	0x0b	read	mA	0000h
MaxError	0x0c	read	percent	2%
RelativeStateOfCharge	0x0d	read	percent	0000h
AbsoluteStateOfCharge	0x0e	read	percent	0000h
RemainingCapacity	0x0f	read	mA .	0000h
FullChargeCapacity	0x10	read	mAh	E^2
RunTimeToEmpty	0x11	read	minutes	
AverageTimeToEmpty	0x12	read	minutes	
AverageTimeToFull	0x13	read	minutes	
ChargingCurrent	Ox14	read	mA	E^2
ChargingVoltage	Ox15	read	mV	E^2
BatteryStatus	Ox16	read	bit flags	0050h
CycleCount	0x17	read	count	0000h
DesignCapacity	0x18	read	mAh	E^2
DesignVoltage	0x19	read	mV	E^2
SpecificationInfo	0x1a	read	unsigned int	E^2
ManufactureDate	Oxlb	read	unsigned int	E^2
SerialNumber	Oxlc	read	number	E^2
Reserved	0x1d - 0x1f			
ManufacturerName	0x20	read	string	E^2
DeviceName	0x21	read	string	E^2
DeviceChemistry	0x22	read	string	E^2
ManufacturerData	*0x23*	read	string	E^2

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to V_{SS}	-0.3	+7.0	V	
All other pins	Relative to V_{SS}	-0.3	+7.0	V	
REF	Relative to V_{SS}	-0.3	+8.5	V	Current limited by R1 (see Figure 1)
V_{SR}	Relative to V_{SS}	-0.3	+7.0	V	Minimum 100Ω series resistor should be used to protect SR in case of a shorted battery (see the bq2040 application note for details).
T_{OPR}	Operating temperature	0	+70	°C	Commercial
		-40	+85	°C	Industrial

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage Thresholds ($T_A = T_{OPR}$; V = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
E_{VSB}	Battery voltage error relative to SB	-30mV		30mV	V	See note

Note: The accuracy of the voltage measurement may be improved by adjusting the battery voltage offset, stored in external E^2PROM. For proper operation, V_{CC} should be 1.5V greater than V_{SB}.

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Note8
Vcc	Supply voltage	3.0	4.25	6.5	V	Vcc excursion from < 2.0V to ≥ 3.0V initializes the unit.
V_{REF}	Reference at 25°C	5.7	6.0	6.3	V	I_{REF} = 5µA
	Reference at -40°C to +85°C	4.5		7.5	V	I_{REF} = 5µA
R_{REF}	Reference input impedance	2.0	5.0		MΩ	V_{REF} = 3V
I_{CC}	Normal operation		90	135	µA	V_{CC} = 3.0V
			120	180	µA	V_{CC} = 4.25V
			170	250	µA	V_{CC} = 6.5V
V_{SB}	Batteryinput	0		Vcc	V	
R_{SBmax}	SB input impedance	10			MΩ	0 < V_{SB} < Vcc
I_{DISP}	$\overline{DISP}$ input leakage			5	µA	V_{DISP} = Vss
I_{LVOUT}	Vom output leakage	-0.2		0.2	µA	E^2PROM off
V_{SR}	Sense resistor input	-0.3		2.0	V	V_{SR} < V_{SS} = discharge; V_{SR} > V_{SS} =charge
R_{SR}	SR input impedance	10			MΩ	-200mV < V_{SR} < Vcc
V_{IH}	Logicinput high	1.4		5.5	V	SCL, SDA, SMBC, SMBD
V_{IL}	Logic input low	-0.5		0.6V	V	SCL, SDA, SMBC, SMBD
V_{OL}	Data, clock output low			0.4	V	I_{OL}=350µA, SDA, SMBD
I_{OL}	Sink current	100		350	µA	V_{OL}≤0.4V, SDA, SMBD
V_{OLSL}	SEG_X output low, low Vcc		0.1		V	Vcc = 3V, I_{OLS} ≤ 1.75mA SEG_1–SEG_6
V_{OLSH}	SEG_X output low, high Vcc		0.4		V	Vcc = 6.5V, I_{OLS} ≤ 11.0mA SEG_1–SEG_6
V_{OHVL}	V_{OUT} output, low Vcc	Vcc - 0.3	-		V	Vcc = 3V, I_{VOUT} = -5.25mA
V_{OHVH}	V_{OUT} output, high Vcc	Vcc - 0.6	-		V	Vcc = 6.5V, I_{VOUT} = -33.0mA
I_{VOUT}	Vom *source* current	-33			mA	At V_{OHVH} = Vcc - 0.6V
I_{OLS}	SEG_X sink current			11.0	mA	At V_{OLSH} = 0.4V

Note: All voltages relative to Vss.

AC Specifications

Symbol	Parameter	Min	Max	Units	Notes
F_{SMB}	SMBus operating frequency	10	100	KHz	
T_{BUF}	Bus free time between stop and start condition	4.7		µs	
$T_{HD:STA}$	Hold time after (repeated) start condition	4.0		µs	
$T_{SU:STA}$	Repeated start condition setup time	4.7		µs	
$T_{SU:STO}$	Stop condition setup time	4.0		µs	
$T_{HD:DAT}$	Data hold time	0		ns	
$T_{SU:DAT}$	Data setup time	250		ns	
$T_{TIMEOUT}$	Message timeout	25	35	ms	See note 1.
T_{PD}	Data output delay time	300	3500	ns	External memory only. See note 5.
T_{LOW}	Clock low period	4.7		µs	
T_{HIGH}	Clock high period	4.0	50	µs	See note 2.
$T_{LOW:SEXT}$	Cumulative clock low extend time (slave device)		25	ms	See note 3.
$T_{LOW:MEXT}$	Cumulative clock low extend time (master device)		10	ms	See note 4.
T_F	Clock/Data fall time		300	ns	
T_R	Clock/data rise time		1000	ns	

Notes:

1. A device times out when any clock low exceeds this value.
2. T_{HIGH} Max provides a simple guaranteed method for devices to detect bus idle conditions.
3. $T_{LOW:SEXT}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from the initial start to the stop. If a slave device exceeds this time, it is expected to release both its clock and data lines and reset itself.
4. $T_{LOW:MEXT}$ is the cumulative time a master device is allowed to extend its clock cycles within each byte of a message as defined from start-to-ack, ack-to-ack, or ack-to-stop.
5. The external memory must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

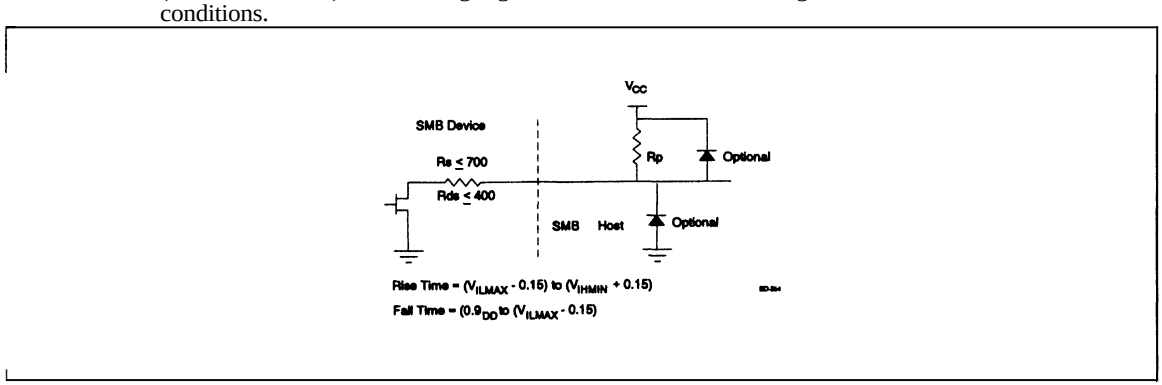
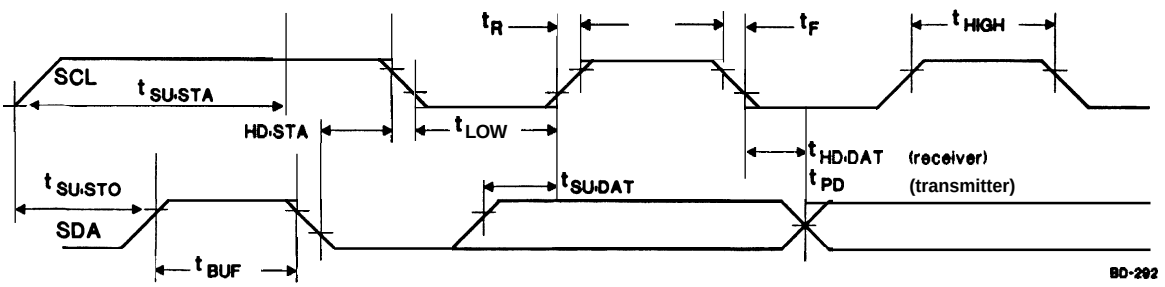
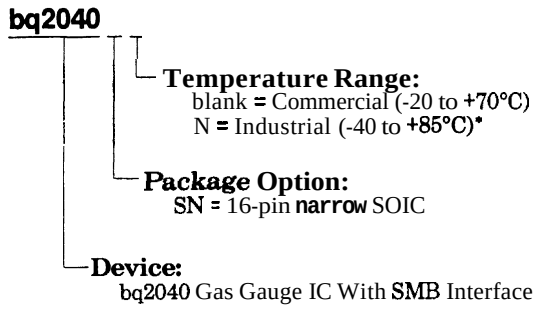


Figure 6. AC Test Conditions

Bus Timing Data



Ordering Information



* Contact factory for availability.

BENCHMARQ

bq2050

Lithium Ion Power Gauge™ IC

2

Features

- Conservative and repeatable measurement of available capacity in Lithium Ion rechargeable batteries
- Designed for battery pack integration
  - 120µA typical operating current
  - Small size enables implementations in as little as ½ square inch of PCB

  Integrate within a system or as a stand-alone device
  - Display capacity via single-wire serial communication port or direct drive of LEDs
- Measurements compensated for current and temperature
- Self-dischargecompensation using internal temperature sensor
- 16-pin narrow SOIC

General Description

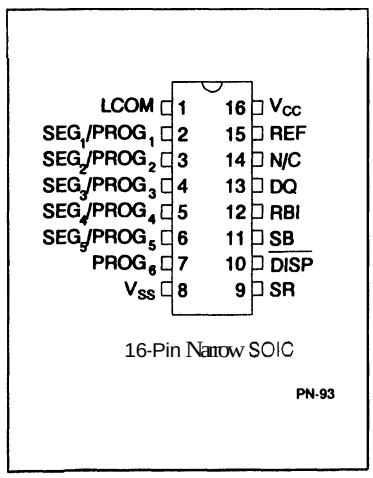
The bq2050 Lithium Ion Power Gauge™ IC is intended for battery-pack or in-system installation to maintain an accurate record of available battery capacity. The IC monitors a voltage drop across a sense resistor connected in series between the negative battery terminal and ground to determine charge and discharge activity of the battery. Compensations for battery temperature and rate of charge or discharge are applied to the charge, discharge, and self-discharge calculations to provide available capacity information across a wide range of operating conditions. Battery capacity is automatically recalibrated, or 'learned," in the course of a discharge cycle from full to empty.

Nominal available capacity may be directly indicated using a five-segment LED display. These segments are used to graphically indicate available capacity. The bq2050 supports a simple single-line bidirectional serial link to an external processor (common ground). The bq2050 outputs battery information in response to external commands over the serial link.

The bq2050 may operate directly from one cell (V_{BAT} > 3V). With the REF output and an external transistor, a simple, inexpensive regulator can be built for systems with more than one series cell.

Internal registers include available capacity, temperature, scaled available energy, battery ID, battery status, and programming pin settings. To support subassembly teating, the outputs may also be controlled. The external processor may also overwrite some of the bq2050 power gauge data registers.

Pin Connections



16-Pin Narrow SOIC

PN-93

Pin Names

LCOM	LED common output	REF	Voltage reference output
$SEG_1/PROG_1$	LED segment 1/ program 1 input	N/C	No connect
$SEG_2/PROG_2$	LED segment 2/ program 2 input	DQ	Serial communications input/output
$SEG_3/PROG_3$	LED segment 3/ program 3 input	RBI	Register backup input
$SEG_4/PROG_4$	LED segment 4/ program 4 input	SB	Battery sense input
$SEG_5/PROG_5$	LED segment 5/ program 5 input	$\overline{DISP}$	Display control input
$PROG_6$	Program 6 input	SR	Sense resistor input
		V_{CC}	3.0-6.5V
		V_{SS}	System ground

Pin Descriptions

LCOM **LED** common output

Open-drain output switches V_{CC} to source current for the LEDs. The switch is off during initialization to allow reading of the soft pull-up or pull-down program resistors. LCOM is also high impedance when the display is off.

SEG_1–SEG_5 **LED** display segment outputs **(dual function** with **$PROG_1$–$PROG_6$)**

Each output may activate an LED to sink the current sourced from **LCOM.**

$PROG_1$–$PROG_2$ Programmed full count selection inputs **(dual** function with **SEG_1–SEG_2)**

These three-level input pins define the programmed full count **(PFC)** thresholds described in Table 2.

$PROG_3$– **Power** gauge rate **selection** inputs **(dual** $PROG_4$ function with **SEG_3–SEG_4)**

These three-level input pins define the scale factor described in Table 2.

$PROG_5$ Self-discharge rate selection **(dual function** with **SEG_5)**

This three-level input pin defines the selfdischarge and battery compensation factors as shown in Table 1.

$PROG_6$ Capacity initialization selection

This three-level pin defines the battery state of charge at reset as shown in Table 1.

N/C **No connect**

SR **Sense** resistor input

The voltage drop (V_{SR}) across the sense resistor R_S is monitored and integrated over time to interpret charge and discharge activity. The SR input is tied between the negative terminal of the battery and the sense resistor. $V_{SR} < V_{SS}$ indicates discharge, and $V_{SR} > V_{SS}$ indicates charge. The effective voltage drop, V_{SRO}, as seen by the bq2050 is $V_{SR} + V_{OS}$.

$\overline{DISP}$ **Display** control input

$\overline{DISP}$ high disables the LED display. $\overline{DISP}$ tied to V_{CC} allows $PROG_X$ to connect directly to V_{CC} or V_{SS} instead of through a pull-up or pull-down resistor. $\overline{DISP}$ floating allows the LED display to be active during charge. $\overline{DISP}$ low activates the display. See Table 1.

SB Secondary battery input

This input monitors the battery cell voltage potential through a high-impedance resistive divider network for end-of-discharge voltage (EDV) thresholds, and battery removed.

RBI Register backup input

This pin is used to provide backup potential to the bq2050 registers during periods when $V_{CC} \leq 3V$. A storage capacitor or a battery can be connected to RBI.

DQ Serial I/O pin

This is an open-drain bidirectional pin.

REF Voltage reference output for regulator

REF provides a voltage reference output for an optional micro-regulator.

V_{CC} Supply voltage input

V_{SS} **Ground**

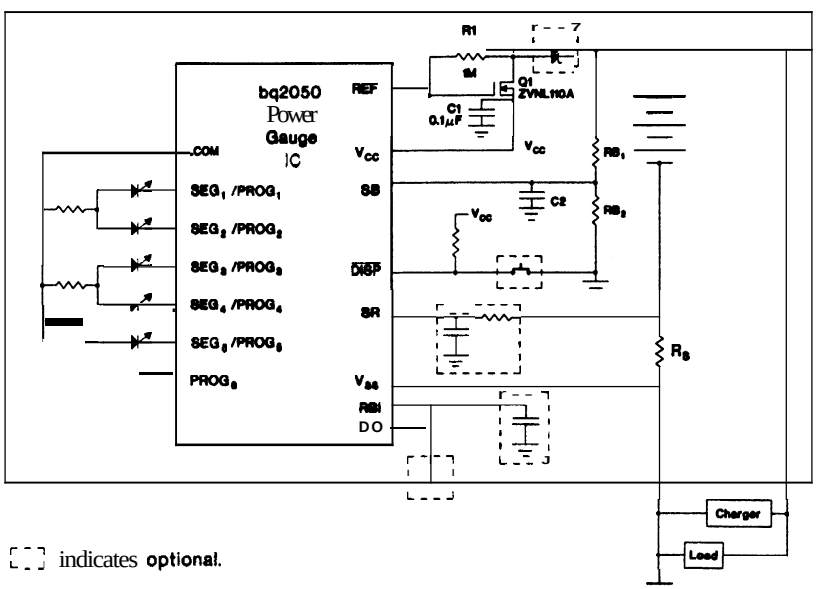
Functional Description

General Operation

The bq2050 determines battery capacity by monitoring the amount of current input to or removed from a rechargeable battery. The bq2050 measures discharge and charge currents, measures battery voltage, estimates self-discharge, monitors the battery for low battery voltage thresholds, and compensates for temperature and charge/discharge rates. The current measurement in made by monitoring the voltage across a mall-value series sense resistor between the negative battery terminal and ground. The estimate of scaled available energy is made using the remaining average battery voltage during the discharge cycle and the remaining nominal available charge. The scaled available energy meaeurement is corrected for the environmental and operating conditions.

Figure 1 shows a typical battery pack application of the bq2050 using the LED display capability as a charge-state indicator. The bq2050 in configured to display capacity in relative display mode. The relative display mode uses the last measured discharge capacity of the battery as the battery 'full' reference. A push-button display feature in available for momentarily enabling the LED display.

The bq2050 monitors the charge and discharge currents as a voltage across a sense resistor (see R_S in Figure 1). A filter between the negative battery terminal and the SR pin may be required if the rate of change of the battery current is too great.



[ ] indicates optional.

Directly connect to V_{CC} across 1 cell (V_{BAT} > 3V).

Otherwise, RI, C1, and 01 u e needed for regulation of > 1 cell.

Programming resistors (6 max.) and ESD-protection diodes are not shown.

R-C on SR may be required. application-specific.

A series Zener may be used to limit discharge current at low voltages in designs using 3 or more cells.

BD-316

Figure 1. Battery Pack Application Diagram—LED Display

Voltage Thresholds

In conjunction with monitoring V_{SR} for charge/discharge currents, the bq2050 monitors the battery potential through the SB pin. The voltage is determined through a resistor-divider network per the following equation:

$$\frac{RB1}{RB2} = 2N - 1$$

where N is the number of cells, RB1 is connected to the positive battery terminal, and RB2 is connected to the negative battery terminal. The single-cell battery voltage is monitored for the end-of-discharge voltage (EDV). EDV threshold levels are used to determine when the battery has reached an 'empty' state.

Two EDV thresholds for the bq2050 are programmable with the default values fixed at:

EDV1 (early warning) = 1.52V

EDVF (empty) = 1.47V

If V_{SB} is below either of the two EDV thresholds, the associated flag is latched and remains latched, independent of V_{SB}, until the next valid charge. The V_{SB} value is also available over the serial port.

During discharge and charge, the bq2050 monitors V_{SR} for various thresholds used to compensate the charge and discharge rates. Refer to the count compensation section for details. EDV monitoring is disabled if the discharge rate is greater than 2C (typical) and resumes ½ second after the rate falls below 2C.

RBI Input

The RBI input pin is intended to be used with a storage capacitor or external supply to provide backup potential to the internal bq2050 registers when V_{CC} drops below 3.0V. V_{CC} is output on RBI when V_{CC} is above 3.0V. A diode is required to isolate the external supply.

Reset

The bq2050 can be reset either by removing Vcc and grounding the RBI pin for 15 seconds or by writing 0x80 to register 0x39.

Temperature

The bq2050 internally determines the temperature in 10°C steps centered from approximately -35°C to +85°C. The temperature steps are used to adapt charge and discharge rate compensations, self-discharge counting, and available charge display translation. The temperature range is available over the serial port in 10°C increments as shown in the following table:

TMP (hex)	Temperature Range
0x	< -30°C
1x	-30°C to -20°C
2x	-20°C to -10°C
3x	-10°C to 0°C
4x	0°C to 10°C
5x	10°C to 20°C
6x	20°C to 30°C
7x	30°C to 40°C
8x	40°C to 50°C
9x	50°C to 60°C
Ax	60°C to 70°C
Bx	70°C to 80°C
Cx	> 80°C

Layout Considerations

The bq2050 measures the voltage differential between the SR and V_{SS} pins. V_{OS} (the offset voltage at the SR pin) is greatly affected by PC board layout. For optimal results, the PC board layout should follow the strict rule of a single-point ground return. Sharing high-current ground with small signal ground causes undesirable noise on the small signal nodes. Additionally:

- The capacitors (C1 and C2) should be placed as close as possible to the V_{CC} and SB pins, respectively, and their paths to Vss should be as short as possible. A high-quality ceramic capacitor of 0.1µf is recommended for V_{CC}.
- The sense resistor capacitor should be placed as close as possible to the SR pin.
- The sense resistor (R_S) should be as close as possible to the bq2050.

Gas Gauge Operation

The operational overview diagram in Figure 2 illustrates the operation of the bq2050. The bq2050 accumulates a measure of charge and discharge currents, as well as an estimation of self-discharge. Charge and discharge currents are temperature and rate compensated, whereas self-discharge is only temperature compensated.

The main counter, Nominal Available Capacity (NAC), represents the available battery capacity at any given time. Battery charging increments the NAC register, while battery discharging and self-discharge decrement the NAC register and increment the DCR (Discharge Count Register).

The Discharge Count Register (DCR) is used to update the Last Measured Discharge (LMD) register only if a complete battery discharge from full to empty occurs without any partial battery charges. Therefore, the bq2050 adapts its capacity determination based on the actual conditions of discharge.

The battery's initial capacity is equal to the Programmed Full Count (PFC) shown in Table 2. Until LMD is updated, NAC counts up to but not beyond this threshold during subsequent charges. This approach allows the gas gauge to be charger-independent and compatible with any type of charge regime.

1. **Last Measured Discharge (LMD) or learned battery capacity:**

   LMD is the last measured discharge capacity of the battery. On initialization (application of V_{CC} or battery replacement), LMD = *. During subsequent discharges, the LMD is updated with the latest measured capacity in the Discharge Count Register (DCR) representing a discharge from full to below EDV1. A qualified discharge is necessary for a capacity transfer from the DCR to the LMD register. The LMD also serves as the 100% reference threshold used by the relative display mode.

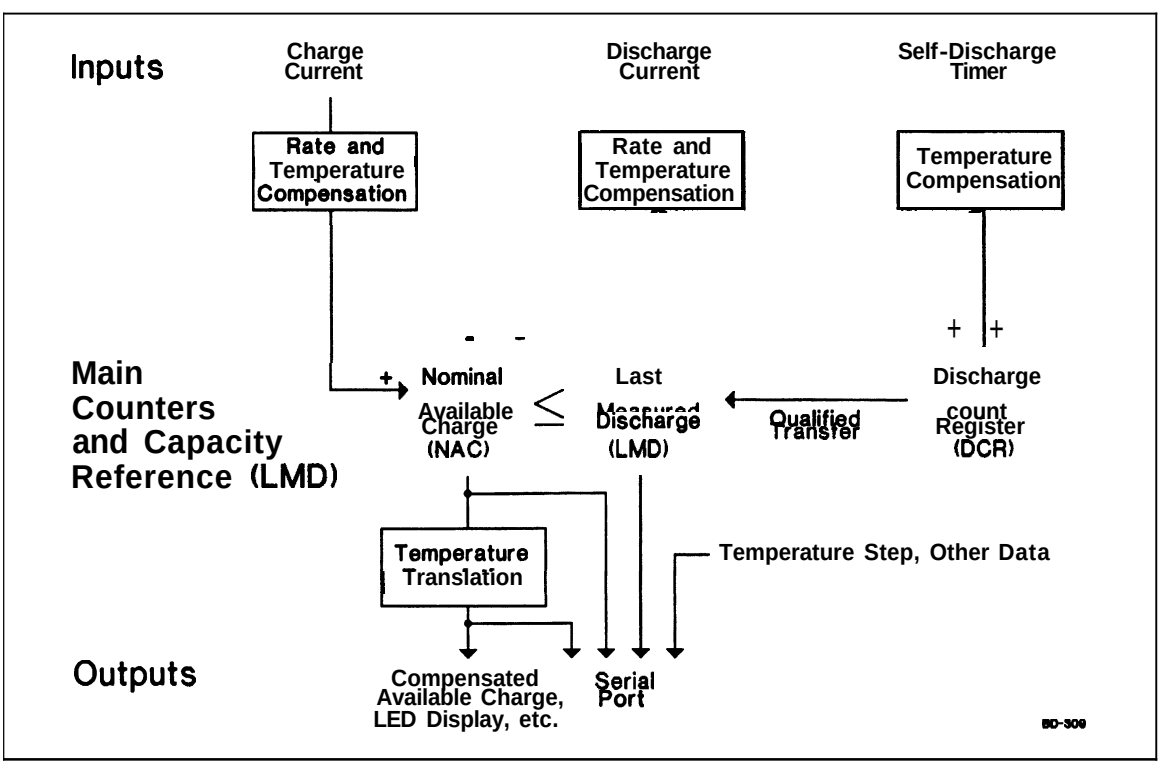


Figure 2. Operational Overview

2 **Programmed Full Count (PFC) or initial battery capacity:**

The initial LMD and gas gauge rate values are programmed by using $PROG_1$–$PROG_4$. The bq2050 is configured for a given application by selecting a PFC value from Table 2. The correct PFC may be determined by multiplying the rated battery capacity in mAh by the sense resistor value:

Battery capacity (mAh) • sense resistor (Ω) =

PFC (mVh)

Selecting a PFC slightly leas than the rated capacity provides a conservative capacity reference until the bq2050 "learns" a new capacity reference.

Example:* *Selecting a PFC Value

Given:

Sense resistor = 0.05Ω
Number of cells = 2
Capacity = 1000mAh, Li-Ion battery, coke-anode
Current range = 50mA to 1A
Relative display mode
Serial port only
Self-discharge = $^{NAC}/_{512}$ per day @ 25°C
Voltage drop over sense resistor = 2.5mV to 50mV
Nominal discharge voltage = 3.6V

Therefore:

1000mAh • 0.05Ω = 50mVh

Table 1. bq2050 Programming

Pin Connection	$PROG_5$ Compensation/ Self-Discharge	$PROG_6$ NAC on Reset	$\overline{DISP}$ Display State
H	Table 4/Disabled	PFC	LEDs disabled
Z	Table 4/$^{NAC}/_{512}$	0	LEDs on when charging
L	Table 3/$^{NAC}/_{512}$	0	LEDs on for 4 sec.

Note: $PROG_5$ and $PROG_6$ states are independent.

Table 2. bq2050 Programmed Full Count mVh Selections

$PROG_x$		Programmed Full Count (PFC)	$PROG_4$ = L			$PROG_4$ = Z			Units
1	2		PROG3 = H	PROG3 = Z	PROG3 = L	PROG3 = H	PROG3 = Z	PROG3 = L	
-	-	-	SCALE = 1/80	SCALE = 1/160	SCALE = 1/320	SCALE = 1/640	SCALE = 1/1280	SCALE = 1/2560	mVh/ count
H	H	49152	614	307	154	76.8	38.4	19.2	mVh
H	Z	45056	563	282	141	70.4	35.2	17.6	mVh
H	L	40960	512	256	128	64.0	32.0	16.0	mVh
Z	H	36864	461	230	115	57.6	28.8	14.4	mVh
Z	Z	33792	422	211	106	53.0	26.4	13.2	mVh
Z	L	30720	384	192	96.0	48.0	24.0	12.0	mVh
L	H	27648	346	173	86.4	43.2	21.6	10.8	mVh
L	Z	25600	320	160	80.0	40.0	20.0	10.0	mVh
L	L	22528	282	141	70.4	35.2	17.6	8.8	mVh
VSR equivalent to 2 counts/sec. (nom.)			90	45	22.5	11.25	5.6	2.8	mV

Select:

PFC = 30720 counts or **48mVh**
$PROG_1$ = float
$PROG_2$ = low
$PROG_3$ = high
$PROG_4$ = float
$PROG_5$ = float
$PROG_6$ = float

The initial full battery capacity is **48mVh** (960mAh) until the bq2050 'learns" a new capacity with a **qualified** discharge from full to EDV1.

3. Nominal Available Capacity (NAC):

NAC counts up during charge to a maximum value of LMD and **down** during **discharge** and **self-discharge to 0. NAC is reset to 0 on initialization and on the first** valid *charge* **following** discharge to **EDV1.** To prevent **overstatement** of charge during **periods** of overcharge, NAC **stops incrementing** when NAC = LMD.

4. **Discharge** Count Register (DCR):

The DCR counts up **during** discharge independent of NAC and **could** continue **increasing** after NAC **has decremented** to **0.** Prior to NAC = **0 (empty** battery), both discharge and self-discharge increment the **DCR.** After NAC **= 0,** only discharge increments the **DCR.** The DCR resets to 0 when NAC = LMD. The DCR does not **roll** over but **stops counting when** it reaches FFFFh.

The **DCR** value becomes the new LMD value on the first charge after a valid discharge to **V_{EDV1} if:**

No valid charge initiations (charges greater than 256 NAC counts, where **$V_{SRO} > V_{SRQ}$)** occurred during the period between NAC = LMD and EDV1 detected.

The self-discharge count is not more than 4096 counts (8% to 18% of PFC, specific percentage threshold determined by PFC).

The temperature is **≥ 0°C** when the EDV1 level is reached during discharge.

The valid diecharge flag (VDQ) **indicates** whether the present diecharge is valid for LMD update.

5. **Scaled** Available Energy **(SAE):**

SAE is **useful** in determining the available energy within the battery, and may provide a more useful capacity reference in battery chemistries with sloped voltage **profiles** during diecharge. SAE may be converted to a **mWh** value using the following formula:

$$E(mWh) = (SAEH * 256 + SAEL) * \frac{2.4 * SCALE * (R_{B1} + R_{B2})}{R_S * R_{B2}}$$

where **R_{B1}, R_{B2}** and **R_S are resistor** values in ohms. SCALE is the selected scale **from** Table 2. **SAEH** and SAEL **are** digital **values** mad **via** DQ.

6. **Compensated** Available Capacity **(CAC)**

CAC counts similar to NAC, but contains the available capacity compensated for discharge rate and temperature.

Charge Counting

Charge activity is **detected based** on a **positive** voltage on the V_{SR} input. If charge activity is **detected, the bq2050 increments** NAC at a rate **proportional** to **V_{SR}** and, if enabled, activates an LED display. Charge **actions** increment the NAC after **compensation** for temperature.

The **bq2050 determines** charge activity sustained at a continuous rate equivalent to **$V_{SRO} > V_{SRQ}$**. A valid charge equates to **sustained** charge activity greater than **256** NAC **counts.** Once a valid **charge** is detected, charge **counting continues** until **V_{SRO}** (V_{SR} + **V_{OS}) falls** below **V_{SRQ}. V_{SRQ}** is **210µV,** and is **described** in the Digital Magnitude Filter **section.**

Discharge Counting

Discharge activity is **detected** based on a **negative** voltage on the **V_{SR}** input. **All discharge counts where $V_{SRO} < V_{SRD}$** cause the NAC **register** to decrement and **the** DCR to increment. **V_{SRD}** is **-200µV,** and is described in the Digital Magnitude **Filter section.**

Self-Discharge Estimation

The bq2050 continuously **decrements** NAC and **increments DCR for self-discharge based on time and temperature. The self-discharge count rate is programmed to be a nominal 1/512** • NAC per day or disabled. **This** is the rate for a **battery whose** temperature is between 20°–30°C. The NAC **register** cannot be decremented below **0.**

Count Compensations

Discharge Compensation

Corrections for the rate of discharge, temperature, and anode type are made by adjusting an internal compensation factor. This factor is based on the measured rate of discharge of the battery. Tables 3A and 3B outline the [redacted] factor typically used for graphite anode **Li-Ion batteries,** and **Tables** 4A and 4B outline the **factors** typically used **for coke anode** Li-Ion batteries. **The** compensation factor is applied to CAC and is **based** on discharge rate and temperature.

Table 3A. Graphite Anode

Approximate Discharge Rate	Discharge Compensation Factor	Efficiency
< 0.5C	1.00	100%
≥ 0.5C	1.05	95%

Table 3B.

Temperature	Temperature Compensation Factor	Efficiency
≥ 10°C	1.00	100%
0°C to 10°C	1.10	90%
-10°C to 0°C	1.35	74%
≤ -10°C	2.50	40%

Table 4A. Coke Anode

Approximate Discharge Rate	Discharge Compensation Factor	Efficiency
<0.5C	1.00	100%
≥ 0.5C	1.15	86%

Table 4B.

Temperature	Temperature Compensation Factor	Efficiency
≥ 10°C	1.00	100%
0°C to 10°C	1.25	80%
-10°C to 0°C	2.00	50%
≤ -10°C	8.00	12%

Charge Compensation

The bq2050 applies the following temperature compensation to NAC during charge:

Temperature	Temperature Compensation Factor	Efficiency
< 10°C	0.95	95%
≥ 10°C	1.00	100%

This compensation applies to both types of Li-Ion cells.

Self-Discharge Compensation

The self-discharge compensation is programmed for a nominal rate of 1/512 • NAC per day. This is the rate for a battery within the 20–30°C temperature range. This rate varies across 8 ranges from <10°C to >70°C, changing with each higher temperature (approximately 10°C). See Table 5 below:

Table 5. Self-Discharge Compensation

Temperature Range	Typical Rate PROG5 = Z or L
< 10°C	NAC/2048
10–20°C	NAC/1024
20–30°C	NAC/512
30–40°C	NAC/256
40–50°C	NAC/128
50–60°C	NAC/64
60–70°C	NAC/32
> 70°C	NAC/16

Self-discharge may be disabled by connecting PROG5 = H.

Digital Magnitude Filter

The bq2050 has a digital filter to eliminate charge and discharge counting below a set threshold. The bq2050 setting is 200µV for V_{SRD} and 210µV for V_{SRQ}.

Table 6. bq2050 Current-Sensing Errors

Symbol	Parameter	Typical	Maximum	Units	Notes
V_{OS}	Offset referred to V_{SR}	± 50	± 180	µV	$\overline{DISP}$ = V_{CC}.
INL	Integrated non-linearity error	± 2	± 4	%	Add 0.1% per °C above or below 25°C and 1% per volt above or below 4.25V.
INR	Integrated non-repeatability error	± 1	± 2	%	Measurement repeatability given similar operating conditions.

Error Summary

Capacity Inaccurate

The LMD is susceptible to error on initialization or if no updates occur. On initialization, the LMD value includes the error between the programmed full capacity and the actual capacity. This error is present until a valid discharge occurs and LMD is updated (see the DCR description on page 7). The other cause of LMD error is battery wear-out. As the battery ages, the measured capacity must be adjusted to account for changes in actual battery capacity.

A Capacity Inaccurate counter (CPI) is maintained and incremented each time a valid charge occurs (qualified by NAC; see the CPI register description) and is reset whenever LMD is updated from the DCR. The counter does not wrap around but stops counting at 255. The capacity inaccurate flag (CI) is set if LMD has not been updated following 64 valid charges.

Current-Sensing Error

Table 5 illustrates the current-sensing error as a function of V_{SRO}. A digital filter eliminates charge and discharge counts to the NAC register when V_{SRO} is between V_{SRQ} and V_{SRD}.

Communicating With the bq2050

The bq2050 includes a simple single-pin (DQ plus return) serial data interface. A host processor uses the interface to access various bq2050 registers. Battery characteristics may be easily monitored by a d d i i a single contact to the battery pack. The open-drain DQ pin on the bq2050 should be pulled up by the host system, or may be left floating if the serial interface is not used.

The interface uses a command-based protocol, where the host processor sends a command byte to the bq2050. The command directs the bq2050 to either store the next eight bits of data received to a register specified by the command byte or output the eight bits of data specified by the command byte.

The communication protocol is asynchronous return-to-one. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 333 bits/sec. The leaat-significant bit of a command or data byte is transmitted first. The protocol is simple enough that it can be implemented by moet hoet processors using either polled or interrupt processing. Data input from the bq2050 may be sampled using the pulse-width capture timers available on some microcontrollers.

If a communication error occurs, e.g. t_{CYCB} > 6ms, the bq2050 should be sent a BREAK to reinitiate the aerial interface. A BREAK is detected when the DQ pin ia driven to a logic-low state for a time, ta or greater. The DQ pin should then be returned to its normal ready-high logic state for a time, t_{BR}. The bq2050 is now ready to receive a command from the host processor.

The return-to-one data bit frame consists of three distinct sections. The first section is used to start the transmission by either the host or the bq2050 taking the DQ pin to a logic-low state for a period, $t_{STRH,B}$. The next section is the actual data transmission, where the data should be valid by a period, t_{DSU}, after the negative edge used to start communication. The data should be held for a period, t_{DV}, to allow the host or bq2050 to sample the data bit.

The final section is used to stop the transmission by returning the DQ pin to a logic-high state by at least a period, t_{SSU}, after the negative edge used to start communication. The final logic-high state should be held until a period, t_{SV}, to allow time to ensure that the bit transmission waa stopped properly. The timings for data and break communication are given in the aerial communication timing specification and illustration sections.

Communication with the bq2050 is always performed with the least-significant bit being transmitted first. Figure 3 shows an example of a communication sequence to read the bq2050 NAC register.

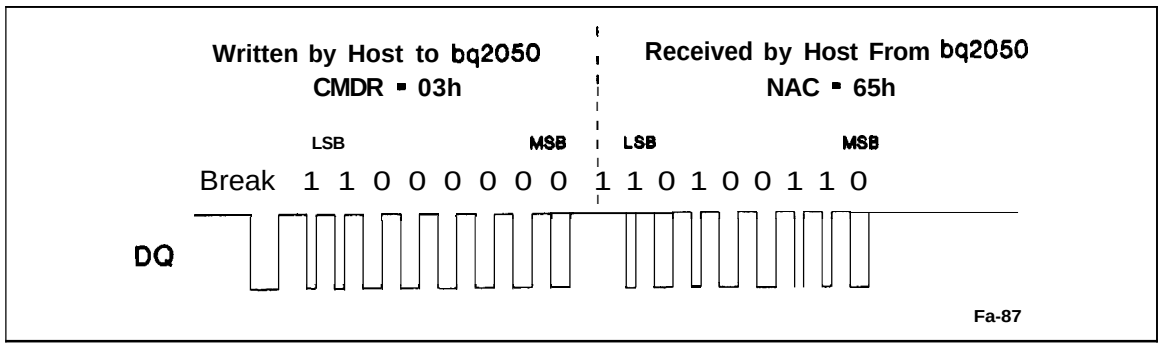


Figure 3. Typical Communication With the bq2050

bq2050 Registers

The bq2050 command and status registers are listed in Table 7 and described below.

Command Register (CMDR)

The write-only CMDR register is accessed when eight valid command bits have been received by the bq2050. The CMDR register contains two fields:

- W/$\overline{R}$ bit
- Command address

The W/$\overline{R}$ bit of the command register is used to select whether the received command is for a read or a write function.

The W/$\overline{R}$ values are:

CMDR Bits							
7	6	5	4	3	2	1	0
W/$\overline{R}$	-	-	-	-	-	-	-

Where W/$\overline{R}$ is:

0 The bq2050 outputs the requested register contents specified by the address portion of CMDR.

1 The following eight bits should be written to the register specified by the address portion of CMDR

The lower seven-bit field of CMDR contains the address portion of the register to be accessed. Attempts to write to invalid addresses are ignored.

CMDR Bib							
7	6	5	4	3	2	1	0
-	AD6	AD5	AD4	AD3	AD2	AD1	AD0 (LSB)

Primary Status Flags Register (FLGS1)

The read-only FLGSl register (address=01h) contains the primary bq2050 flags.

The charge *status* flag (CHGS) is asserted when a valid charge rate is detected. Charge rate is deemed valid when $V_{SRO} > V_{SRQ}$. A V_{SRO} of less than V_{SRQ} or discharge activity clears CHGS.

The CHGS values are:

FLGSl Bib							
7	6	5	4	3	2	1	0
CHGS	-	-	-	-	-	-	-

Where CHGS is:

0 Either discharge activity detected or $V_{SRO} < V_{SRQ}$

1 $V_{SRO} > V_{SRQ}$

The battery replaced flag (BRP) is asserted whenever the bq2050 is reset either by application of Vcc or by a serial port command. BRP is reset when either a valid charge action increments NAC to be equal to LMD, or a valid charge action is detected after the EDV1 flag is asserted. BRP = 1 signifies that the device has been reset.

The BRP values are:

FLGSl Bits							
7	6	5	4	3	2	1	0
-	BRP	-	-	-	-	-	-

Table 7. bq2050 Command and Status Registers

Symbol	Register Name	Loc. (hex)	Read/ Write	Control Field							
				7(MSB)	6	5	4	3	2	1	0(LSB)
CMDR	Command register	00h	Write	W/$\overline{R}$	AD6	AD5	AD4	AD3	AD2	AD1	AD0
FLGS1	Primary status flags register	01h	Read	CHGS	BRP	n/u	CI	VDQ	n/u	EDV1	EDVF
TMP	Temperature register	02h	Read	TMP3	TMP2	TMP1	TMP0	GG3	GG2	GG1	GG0
NACH	Nominal available capacity high byte register	03h	R/W	NACH7	NACH6	NACH5	NACH4	NACH3	NACH2	NACH1	NACH0
NACL	Nominal available capacity low byte register	17h	Read	NACL7	NACL6	NACL5	NACL4	NACL3	NACL2	NACL1	NACL0
BATID	Battery identification register	04h	R/W	BATID7	BATID6	BATID5	BATID4	BATID3	BATID2	BATID1	BATID0
LMD	Last measured discharge register	05h	R/W	LMD7	LMD6	LMD5	LMD4	LMD3	LMD2	LMD1	LMD0
FLGS2	Secondary status flags register	06h	Read	n/u	DR2	DR1	DR0	n/u	n/u	n/u	OVLD
PPD	Program pin pull-down register	07h	Read	n/u	n/u	PPD6	PPD5	PPD4	PPD3	PPD2	PPD1
PPU	Program pin pull-up register	08h	Read	n/u	n/u	PPU6	PPU5	PPU4	PPU3	PPU2	PPU1
CPI	Capacity inaccurate count register	09h	Read	CPI7	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	CPI0
VSB	Battery voltage register	0Bh	Read	VSB7	VSB6	VSB5	VSB4	VSB3	VSB2	VSB1	VSB0
VTS	End-of-discharge threshold select register	0Ch	R/W	VTS7	VTS6	VTS5	VTS4	VTS3	VTS2	VTS1	VTS0
CACH	Compensated available capacity high byte register	0Dh	Read	CACH7	CACH6	CACH5	CACH4	CACH3	CACH2	CACH1	CACH0
CACL	Compensated available capacity low byte register	0Eh	Read	CACL7	CACL6	CACL5	CACL4	CACL3	CACL2	CACL1	CACL0
SAEH	Scaled available energy high byte register	0Fh	Read	SAEH7	SAEH6	SAEH5	SAEH4	SAEH3	SAEH2	SAEH1	SAEH0
SAEL	Scaled available energy low byte register	10h	Read	SAEL7	SAEL6	SAEL5	SAEL4	SAEL3	SAEL2	SAEL1	SAEL0
RST	Reset register	39h	Write	RST	0	0	0	0	0	0	0

Note: n/u = not used

Where BRP is:

0 Battery is charged until NAC = LMD or discharged until the EDVl flag is asserted

1 bq2050 is reset

The ***capacity inaccurate*** flag (CI) is used to warn the user that the battery has been charged a substantial number of times since LMD has been updated. The CI flag is asserted on the 64th charge after the last LMD update or when the bq2050 is reset. The flag is cleared after an LMD update.

The CI values are:

FLGSI Bits							
7	6	5	4	3	2	1	0
-	-	-	CI	-	-	-	-

Where CI is:

0 When LMD is updated with a valid full discharge

1 After the 64th valid charge action with no LMD updates or the bq2050 is reset

The ***valid discharge*** flag (VDQ) is asserted when the bq2050 is discharged from NAC=LMD. The flag remains set until either LMD is updated or one of three actions that can clear VDQ occurs:

- The self-discharge count register (SDCR) has exceeded the maximum acceptable value (4096 counts) for an LMD update.
- A valid charge action sustained at $V_{SRO} > V_{SRQ}$ for at least 256 NAC counts.
- The EDVl flag was set at a temperature below 0°C

The **VDQ** values are:

FLGSI Bits							
7	6	5	4	3	2	1	0
			-	VDQ	-	-	

Where VDQ is:

0 SDCR ≥ 4096, subsequent valid charge action detected, or EDVl is asserted with the temperature less than 0°C

1 On first discharge after NAC = LMD

The ***first end-of-discharge warning*** flag (EDVl) warns the user that the battery is almost empty. The first segment pin, SEG_1, is modulated at a 4Hz rate if the display is enabled once EDVl is asserted, which should warn the user that loss of battery power is imminent. The EDVl flag is latched until a valid charge has been detected. The EDVl threshold is externally controlled via the VTS register (see Voltage Threshold Register on this page).

The EDVl values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
					-	EDVl	-

Where EDVl is:

0 Valid charge action detected, $V_{SB} \geq V_{TS}$

1 $V_{SB} < V_{TS}$ providing that the discharge rate is < 2C

The ***final end-of-discharge warning*** flag (EDVF) flag is used to warn that battery power is at a failure condition. All segment drivers are turned off. The EDVF flag is latched until a valid charge has been detected. The EMPTY pin is also forced to a high-impedance state on assertion of EDVF. The host system may pull EMPTY high, which may be used to disable circuitry to prevent deep-discharge of the battery. The EDVF threshold is set 50mV below the EDVl threshold.

The EDVF values are:

FLGSI Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	EDVF

Where EDVF is:

0 Valid charge action detected, $V_{SB} \geq (V_{TS} - 50mV)$

1 $V_{SB} < (V_{TS} - 50mV)$ providing the discharge rate is < 2C

Temperature Register (TMP)

The read-only TMP register (address=02h) contains the battery temperature.

TMP Temperature Bits							
7	6	5	4	3	2	1	0
TMP4	TMP3	TMP2	TMP1	-	-	-	-

The bq2050 contains an internal temperature sensor. The temperature is used to set charge and discharge efficiency factors as well as to adjust the self-discharge coefficient. The temperature register contents may be translated as shown in Table 7.

Table 7. Temperature Register

TMP3	TMP2	TMP1	TMP0	Temperature
0	0	0	0	T < -30°C
0	0	0	1	-30°C < T < -20°C
0	0	1	0	-20°C < T < -10°C
0	0	1	1	-10°C < T < 0°C
0	1	0	0	0°C < T < 10°C
0	1	0	1	10°C < T < 20°C
0	1	1	0	20°C < T < 30°C
0	1	1	1	30°C < T < 40°C
1	0	0	0	40°C < T < 50°C
1	0	0	1	50°C < T < 60°C
1	0	1	0	60°C < T < 70°C
1	0	1	1	70°C < T < 80°C
1	1	0	0	T > 80°C

The bq2050 calculates the gas gauge bits, GG3-GG0 as a function of CACH and LMD. The results of the calculation give available capacity in 1/16 increments from 0 to 15/16.

TMPGG Gas Gauge Bits							
7	6						
-	-		-	GG3	GG2	GG1	GG0

Nominal Available Charge Registers (NACH/NACL)

The read/write NACH high-byte register (address=03h) and the read-only NACL low-byte register (address=17h) are the main gas gauging register for the bq2050. The NAC registers are incremented during charge actions and decremented during discharge and self-discharge actions. The correction factors for charge/discharge efficiency are applied automatically to NAC. NACH and NACL are set to 0 during a bq2050 reset.

Writing to the NAC registers affects the available charge counts and, therefore, affects the bq2050 gas gauge operation. Do not write the NAC registers to a value greater than LMD.

Battery Identification Register (BATID)

The read/write BATID register (address=04h) is available for use by the system to determine the type of battery pack. The BATID contents are retained as long as V_{CC} is greater than 2V. The contents of BATID have no effect on the operation of the bq2050. There is no default setting for this register.

Last Measured Discharge Register (LMD)

LMD is a read/write register (address=05h) that the bq2050 uses as a measured full reference. The bq2050 adjusts LMD based on the measured discharge capacity of the battery from full to empty. In this way the bq2050 updates the capacity of the battery. LMD is set to PFC during a bq2050 reset.

Secondary Status Flags Register (FLGS2)

The read-only FLGS2 register (address=06h) contains the secondary bq2050 flags.

The *discharge rate* flags, DR2–0, are bits 6–4.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	DR2	DR1	DR0	-	-	-	

They are used to determine the current discharge regime as follows:

DR2	DR1	DR0	Discharge Rate
0	0	0	DRATE < 0.5C
0	0	1	0.5C ≤ DRATE < 2C

The *overload flag* (OVLD) is asserted when a discharge rate in excess of 2C is detected. OVLD remains asserted as long as the condition persists and is cleared 0.5 seconds after the rate drops below 2C. The overload condition is used to stop sampling of the battery terminal characteristics for end-of-discharge determination.

FLGS2 Bits							
7	6	5	4	3	2	1	0
						.	OVLD

Program Pin Pull-Down Register (PPD)

The read-only PPD register (address=07h) contains some of the programming pin information for the bq2050. The segment drivers, SEG_{1-6}, have a corresponding PPD register location, PPD_{1-6}. A given location is set if a pull-down resistor has been detected on its corresponding segment driver. For example, if SEG_1 and SEG_4 have pull-down resistors, the contents of PPD are xx001001.

Program Pin Pull-Up Register (PPU)

The read-only PPU register (address=08h) contains the rest of the programming pin information for the bq2050. The segment drivers, SEG_{1-6}, have a corresponding PPU register location, PPU_{1-6}. A given location is set if a pull-up resistor has been detected on its corresponding segment

driver. For example, if SEG_3 and SEG_6 have pull-up resistors, the contents of PPU are xx100100.

PPD/PPU Bits							
7	6	5	4	3	2	1	0
	-	PPU_6	PPU_5	PPU_4	PPU_3	PPU_2	PPU_1
	-	PPD_6	PPD_5	PPD_4	PPD_3	PPD_2	PPD_1

Capacity Inaccurate Count Register (CPI)

The read-only CPI register (address=09h) is used to indicate the number of times a battery has been charged without an LMD update. Because the capacity of a rechargeable battery varies with age and operating conditions, the bq2050 adapts to the changing capacity over time. A complete discharge from full (NAC=LMD) to empty (EDV1=1) is *required* to perform an LMD update assuming there have been no intervening valid charges, the temperature is greater than or equal to 0°C, and the self-discharge counter is less than 4096 counts.

The CPI register is incremented every time a valid charge is detected. When NAC > 0.94 • LMD, however, the CPI register increments on the first valid charge; CPI does not increment again for a valid charge until NAC < 0.94 • LMC. This prevents continuous trickle charging from incrementing CPI if self-discharge decrements NAC. The CPI register increments to 255 without rolling over. When the contents of CPI are incremented to 64, the capacity inaccurate flag, CI, is asserted in the FLGS1 register. The CPI register is reset whenever an update of the LMD register is performed, and the CI flag is also cleared.

Battery Voltage Register (VSB)

The read-only battery voltage register is used to read the single-cell battery voltage on the SB pin. The VSB register (address = 0Bh) is updated approximately once per second with the present value of the battery voltage. $V_{SB} = 2.4V \cdot (VSB/256)$.

VSB Register Bits							
7	6	5	4	3	2	1	0
VSB7	VSB6	VSB5	VSB4	VSB3	VSB2	VSB1	VSB0

Voltage Threshold Register (VTS)

The end-of-discharge threshold voltages (EDV1 and EDVF) can be set using the VTS register (address = 0Ch). The read/write VTS register sets the EDV1 trip point. EDVF is set 50mV below EDV1. The default value in the VTS register is A2h, representing EDV1 = 1.52V and EDVF = 1.47V. EDV1 = 2.4V • (VTS/256).

VTS Register Bits							
7	6	5	4	3	2	1	0
VTS7	VTS6	VTS5	VTS4	VTS3	VTS2	VTS1	VTS0

Compensated Available Charge Registers (CACH/CACL)

The read-only CACH high-byte register (address = 0Dh) and the read-only CACL low-byte register (address = 0Eh) represent the available charge compensated for discharge rate and temperature. CACH and CACL use piece-wise corrections as outlined in Tables 3A, 3B, 4A, and 4B, and will vary as conditions change. The NAC and LMD registers are not affected by the discharge rate and temperature.

Scaled Available Energy Registers (SAEH/SAEL)

The read-only SAEH high-byte register (address = 0Fh) and the read only SAEL low-byte register (address = 10h) are used to scale battery voltage and CAC to a value which can be translated to watt-hours remaining under the present conditions. SAEL and SAEH may be converted to mWh using the formula on page 7.

Reset Register (RST)

The reset register (address = 39h) enables a software-controlled reset of the device. By writing the RST register contents from 00h to 80h, a bq2050 reset is performed. Setting any bit other *than* the *most-significant bit* of the *RST* register *is not* allowed *and* results in *improper* opemtwn of the *bq2050*.

Resetting the bq2050 sets the following:

- LMD = PFC
- CPI, VDQ, NACH, and NACL = 0
- CI and BRP = 1

Note: Self-discharge is disabled when $PROG_5$ = H.

Display

The bq2050 can directly display capacity information using low-power LEDs. If LEDs are used, the program pins should be resistively tied to Vcc or Vss for a program high or program low, respectively.

The bq2050 displays the battery *charge* state in relative mode. In dative mode, the battery *charge* is represented as a percentage of the LMD. Each LED segment represents 20% of the LMD.

The capacity display is also adjusted for the present battery temperature. The temperature adjustment reflects

pacity at a given temperature but does
JAC register. The temperature adjust-
iled in the CACH and CACL register

ed to V_{CC}, the SEG_{1-5} outputs are inactive.
left floating, the display becomes active
2050 detects a charge in progress V_{SRO} >
lled low, the segment outputs become ac-
of four seconds, ± 0.5 seconds.

tputs are modulated as two banks, with
nd 5 alternating with segments 2 and 4.
itputs are modulated at approximately
h segment bank active for 30% of the

SEG_1 blinks at a 4Hz rate whenever V_{SB} has been detected to be below V_{EDV1} (EDV1 = 1), indicating a low-battery condition. V_{SB} below V_{EDVF} (EDVF = 1) disables the display output.

Microregulator

The bq2050 can operate directly from one cell. A micropower source for the bq2050 can be inexpensively built using the FET and an external resistor to accommodate a greater number of cells; see Figure 1.

2

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
Vcc	Relative to Vss	-0.3	+7.0	V	
All other pins	Relative to Vss	-0.3	+7.0	V	
REF	Relative to Vss	-0.3	+8.5	V	Current limited by R1
V_{SR}	Relative to Vss	-0.3	+7.0	V	Minimum 100Ω aeries be used to protect SR i shorted battery (see th application note for de
T_{OPR}	Operating temperature	0	+70	°C	Commercial
		-40	+85	°C	Industrial

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functi should be limited to the Recommended DC Operating Conditions detailed in this data sheet. ditions beyond the operational limits for extended periods of time may affect device reliabilit

DC Voltage Thresholds ($T_A = T_{OPR}$; V = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	
V_{EDVF}	Final empty warning	1.44	1.47	1.50	V	SB
V_{EDV1}	First empty warning	1.49	1.52	1.55	V	SB
V_{SRO}	SR sense range	-300	-	+2000	mV	SR, V
V_{SRQ}	Valid charge	210			µV	V_{SR} +
V_{SRD}	Valid discharge			-200	µV	V_{SR} +
V_{MCV}	Maximum single-cell voltage	2.20	2.25	2.30	V	SB

Note: Vos is affected by PC board layout. Proper layout guidelines should be followed for optir See "Layout Considerations."

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	3.0	4.25	6.5	V	V_{CC} excursion from < 2.0V to ≥ 3.0V initializes the unit.
V_{REF}	Reference at 25°C	5.7	6.0	6.3	V	I_{REF} = 5µA
	Reference at -40°C to +85°C	4.5	-	7.5	V	I_{REF} = 5µA
R_{REF}	Reference input impedance	2.0	5.0	-	MΩ	V_{REF} = 3V
I_{CC}	Normal operation	-	90	135	µA	V_{CC} = 3.0V, DQ = 0
		-	120	180	µA	V_{CC} = 4.25V, DQ = 0
		-	170	250	µA	V_{CC} = 6.5V, DQ = 0
V_{SB}	Battery input	0	-	V_{CC}	V	
R_{SBmax}	SB input impedance	10	-	-	MΩ	0 < V_{SB} < V_{CC}
I_{DISP}	$\overline{DISP}$ input leakage	-	-	5	µA	V_{DISP} = V_{SS}
I_{LCOM}	LCOM input leakage	-0.2	-	0.2	µA	$\overline{DISP}$ = V_{CC}
I_{RBI}	RBI data retention current	-	-	100	nA	V_{RBI} > V_{CC} < 3V
R_{DQ}	Internal pulldown	500	-	-	KΩ	
V_{SR}	Sense resistor input	-0.3	-	2.0	V	V_{SR} < V_{SS} = discharge; V_{SR} > V_{SS} = charge
R_{SR}	SR input impedance	10	-	-	MΩ	-200mV < V_{SR} < V_{CC}
V_{IH}	Logic input high	V_{CC} - 0.2	-	-	V	$PROG_1$–$PROG_6$
V_{IL}	Logic input low	-	-	V_{SS} + 0.2	V	$PROG_1$–$PROG_6$
V_{IZ}	Logic input Z	float	-	float	V	$PROG_1$–$PROG_6$
V_{OLSL}	SEG_X output low, low V_{CC}	-	0.1	-	V	V_{CC} = 3V, I_{OLS} ≤ 1.75mA SEG_1–SEG_5
V_{OLSH}	SEG_X output low, high V_{CC}	-	0.4	-	V	V_{CC} = 6.5V, I_{OLS} ≤ 11.0mA SEG_1–SEG_5
V_{OHLCL}	LCOM output high, low V_{CC}	V_{CC} - 0.3	-	-	V	V_{CC} = 3V, I_{OHLCOM} = -5.25mA
V_{OHLCH}	LCOM output high, high V_{CC}	V_{CC} - 0.6	-	-	V	V_{CC} = 6.5V, I_{OHLCOM} = -33.0mA
I_{IH}	$PROG_{1-6}$ input high current	-	1.2	-	µA	V_{PROG} = V_{CC}/2
I_{IL}	$PROG_{1-6}$ input low current	-	1.2	-	µA	V_{PROG} = V_{CC}/2
I_{OHLCOM}	LCOM source current	-33	-	-	mA	At V_{OHLCH} = V_{CC} - 0.6V
I_{OLS}	SEG_{1-5} sink current	-	-	11.0	mA	At V_{OLSH} = 0.4V
I_{OL}	Open-drain sink current	-	-	5.0	mA	At V_{OL} = V_{SS} + 0.3V DQ
V_{OL}	Open-drain output low	-	-	0.5	V	I_{OL} ≤ 5mA, DQ
V_{IHDQ}	DQ input high	2.5	-	-	V	DQ
V_{ILDQ}	DQ input low	-	-	0.8	V	DQ
R_{PROG}	Soft pull-up or pull-down resistor value (for programming)			200	KΩ	$PROG_1$–$PROG_6$
R_{FLOAT}	Float state external impedance	-	5		MΩ	$PROG_1$–$PROG_6$

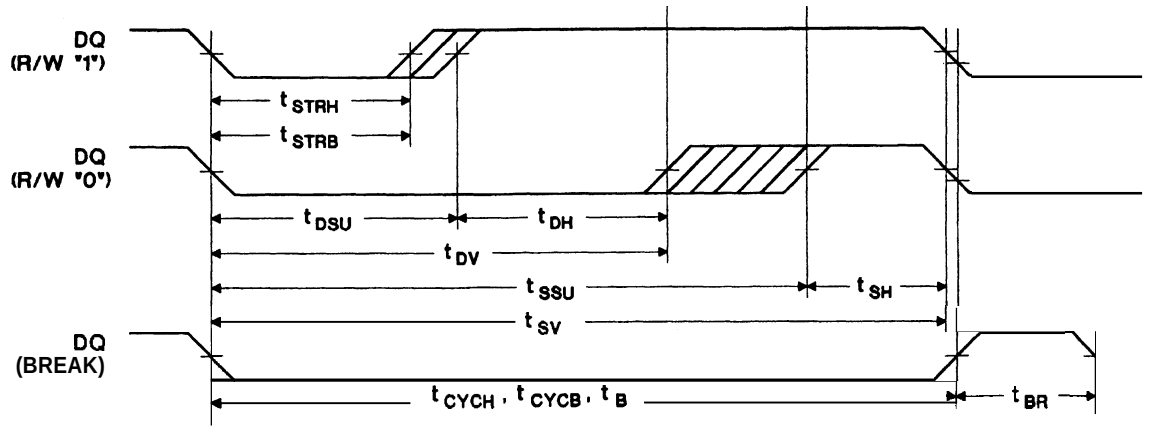
Note: All voltages relative to V_{SS}.

Serial Communication Timing Specification ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYCH}	Cycle time, host to bq2050	3			ma	See note
t_{CYCB}	Cycle time, bq2050 to host	3		6	ms	
t_{STRH}	Start hold, host to bq2050	5		-	ns	
t_{STRB}	Start hold, bq2050 to host	500			µs	
t_{DSU}	Data setup			750	µs	
t_{DH}	Data hold	750			µs	
t_{DV}	Data valid	1.50			ms	
t_{SSU}	Stop setup			2.25	ms	
t_{SH}	Stop hold	700			µs	
t_{SV}	Stop valid	2.95			ms	
t_B	Break	3			ms	
t_{BR}	Break recovery	1		-	ms	

Note: The open-drain DQ pin should be pulled to at least V_{CC} by the host system for proper DQ operation. DQ may be left floating if the serial interface is not used.

Serial Communication Timing Illustration



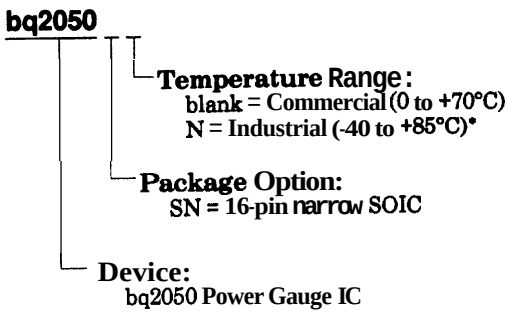
RC-34

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	4	Changed reset procedure	Was: Reset by issuing command over serial port Is: Reset by removing V_{CC} and grounding RBI for 15 s.
1	11, 14	Deleted reset register	
2	16	Changed values	V_{EDVF}: Min. was 1.45; Max. was 1.49 Min. now is 1.44; Max. now is 1.50 V_{EDV1}: Min. was 1.50; Min. now is 1.49
2	17	Changed values	V_{CC}: Min. was 2.5; Min. now is 3.0
2	4, 11, 13, 14	Reinserted reset register	
2	9	Maximum offset	V_{OS}: Max. was 150 Max. now is 180

Note: **Change 1** = June 1995 changes from Dec. 1994.
Change 2 = Sept. 1996 changes from June 1995.

Ordering Information



* Contact factory for availability.

BENCHMARQ

Preliminary **bq2050H**

Lithium Ion Power Gauge™ IC

Features

- Conservative and repeatable measurement of available capacity in Lithium Ion rechargeable batteries
- 16-pin narrow SOIC
- Designed for battery pack integration
  - 120µA typical operating current
  - Small size enables implementations in as little as ½ square inch of PCB
- Integrate within a system or as a stand-alone device
  - Display capacity via single-wire serial communication port or direct drive of LEDs
- Measurements compensated for current and temperature
- ➤ *Self-discharge* compensation using internal temperature sensor
- High-speed (5Kbit/sec.) DQ bus interface

General Description

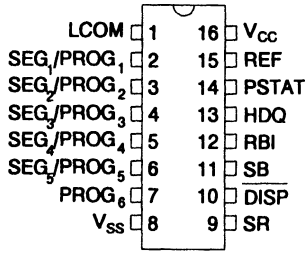
The bq2050H Lithium Ion Power Gauge™ IC is intended for battery-pack or in-system installation to maintain an accurate record of available battery capacity. The IC monitors a voltage drop across a sense resistor connected in series between the negative battery terminal and ground to determine charge and discharge activity of the battery. Compensations for battery temperature and rate of charge or discharge are applied to the charge, discharge, and self-discharge calculatione to provide available capacity information across a wide range of operating conditions. Battery capacity is automatically recalibrated, or "learned," in the course of a discharge cycle from full to empty.

Nominal available capacity may be directly indicated using a five-segment LED display. These segments are used to graphically indicate available capacity. The bq2050H supports a simple standard or high-speed single-line bidirectional serial link to an external processor (common ground). The 5Kbit/sec. DQ bus interface is 16-times faster than the bq2050, reducing communications overhead in the monitoring microcontroller. The bq2050H outputs battery information in response to external commands over the serial link.

The bq2050H may operate directly from one cell (V_{BAT} > 3V). With the REF output and an external transistor, a simple, inexpensive regulator can be built for systems with more than one series cell.

Internal registers include available capacity, temperature, scaled available energy, battery ID, battery status, and programming pin settings. The external processor may also overwrite some of the bq2050H power gauge data registers.

Pin Connections



16-Pin Narrow SOIC

PN-93

Pin Names

LCOM	LED common output	**REP**	Voltage reference output
SEG1/PROG1	LED segment 1/ program 1 input	PSTAT1	Protector status input
SEG2/PROG2	LED segment 2/ program 2 input	**HDQ**	Serial communications input/output
SEG3/PROG3	LED segment 3/ program 3 input	RBI	Register backup input
SEG4/PROG4	LED segment 4/ program 4 input	SB	Battery sense *input*
SEG5/PROG5	LED segment 5/ program 5 input	$\overline{DISP}$	Display control input
PROG6	Program 6 input	SR	Sense resistor input
		Vcc	3.0-5.5V
		Vss	System ground

Pin Descriptions

LCOM — LED common output

Open-drain output switches Vcc to source current for the LEDs. The switch is off during initialization to allow reading of the soft pull-up or pull-down program resistors. LCOM is also high impedance when the display is off.

SEG_1–SEG_5 — LED display segment outputs (dual function with $PROG_1$–$PROG_6$)

Each output may activate an LED to sink the current sourced from LCOM.

$PROG_1$–$PROG_2$ — Programmed full count selection inputs (dual function with SEG_1–SEG_2)

These three-level input pins define the programmed full count (PFC) thresholds described in Table 2.

$PROG_3$–$PROG_4$ — Power gauge rate selection inputs (dual function with SEG_3–SEG_4)

These three-level input pins define the scale factor described in Table 2.

$PROG_5$ — Selfdischarge rate selection (dual function with SEG_5)

This three-level input pin defines the self-discharge and battery compensation factors as well as the serial interface timing speed, shown in Table 1.

$PROG_6$ — Capacity initialization selection

This three-level pin defines the battery state of charge at reset as shown in Table 1.

PSTAT — Protector status input

This input provides overvoltage status from a Li-Ion protector circuit. It should connect to Vss when not used.

SR — Sense resistor input

The voltage drop (V_{SR}) across the sense resistor Rs is monitored and integrated over time to interpret charge and discharge activity. The SR input is tied between the negative terminal of the battery and the sense resistor. $V_{SR} < V_{SS}$ indicates discharge, and $V_{SR} > V_{SS}$ indicates charge. The effective voltage drop, V_{SRO}, as seen by the bq2050H is $V_{SR} + V_{OS}$.

$\overline{DISP}$ — Display control input

$\overline{DISP}$ high disables the LED display. $\overline{DISP}$ tied to Vcc allows PROGx to connect directly to Vcc or Vss instead of through a pull-up or pull-down resistor. $\overline{DISP}$ floating allows the LED display to be active during charge. $\overline{DISP}$ low activates the display. See Table 1.

SB — Secondary battery input

This input monitors the battery cell voltage potential through a high-impedance resistive divider network for end-of-discharge voltage (EDV) thresholds, and battery removed.

RBI — Register backup input

This pin is used to provide backup potential to the bq2050H registers during periods when $V_{CC} \leq 3V$. A storage capacitor or a battery can be connected to RBI.

HDQ — Serial communication input/output

This is an open-drain bidirectional pin operating at standard or high-speed timing.

REF — Voltage reference output for regulator

REF provides a voltage reference output for an optional micro-regulator.

VCC — Supply voltage input

Vss — Ground

Functional Description

General Operation

The **bq2050H** determines battery capacity by monitoring the amount of current input to or removed from a rechargeable battery. The **bq2050H measures** discharge and charge currents, **measures** battery voltage, estimates self-discharge, monitors the battery for low battery voltage thresholds, and compensates for temperature and **charge/discharge rates.** The current measurement **is** made by monitoring the voltage **across** a small-value series sense resistor between the negative battery terminal and ground. The estimate of scaled available energy is made using the remaining average battery voltage during the discharge cycle and the remaining nominal available charge. The **scaled** available **energy measurement** is corrected for the environmental and operating conditions.

Figure 1 shows a typical battery pack application of the bq2050H **using** the **LED display** capability **as** a charge-state indicator. The **bq2050H** is configured to **display** capacity in relative **display** made. **The dative display** mode **uses** the **last measured** discharge **capacity** of the battery **as** the battery 'full' **reference.** A push-button **display** feature is available for momentarily enabling the **LED** display.

The bq2050H monitors the **charge** and discharge **currents as** a voltage **across** a sense **resistor** *(see* **Rs in Fig** ure 1**).** A filter between the negative battery terminal and the SR pin may be **required** if the rate of **change** of the battery current is **too** great.

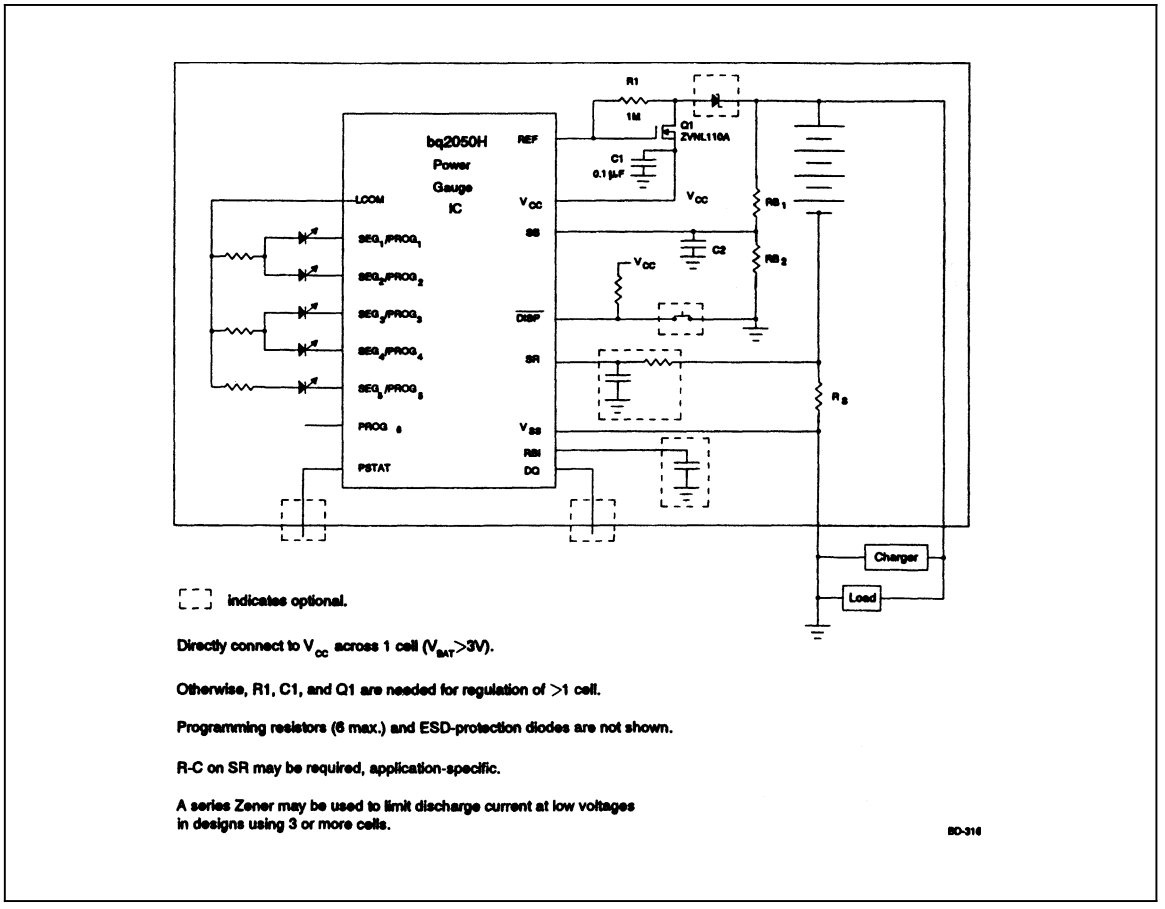


Figure 1. Battery Pack Application Diagram—LED Display

Voltage Thresholds

In conjunction with monitoring V_{SR} for charge/discharge currents, the bq2050H monitors the battery potential through the SB pin. The voltage is determined through a resistor-divider network per the following equation:

$$\frac{RB1}{RB2} = 2N - 1$$

where N is the number of cells, RB1 is connected to the positive battery terminal, and RB2 is connected to the negative battery terminal. The single-cell battery voltage is monitored for the end-of-discharge voltage (EDV). EDV threshold levels are used to determine when the battery has reached an "empty" state.

Two EDV threaholds for the bq2050H are programmable with the default values fixed at:

EDV1 (early warning) = 1.52V

EDVF (empty) = 1.47V

If V_{SB} is below either of the two EDV thresholds, the associated flag is latched and remains latched, independent of V_{SB}, until the next valid charge. The V_{SB} value is also available over the serial port.

During discharge and charge, the bq2050H monitors V_{SR} for various thresholds used to compensate the charge and discharge rates. Refer to the count compensation section for details. EDV monitoring is disabled if the discharge rate is greater than 2C (typical) and resumes ½ second after the rate falls below 2C.

RBI Input

The RBI input pin is intended to be used with a storage capacitor or external supply to provide backup potential to the internal bq2050H registers when V_{CC} drops below 3.0V. V_{CC} is output on RBI when V_{CC} is above 3.0V. A diode is required to isolate the external supply.

Reset

The bq2050H can be reset either by removing V_{CC} and grounding the RBI pin for 15 seconds or by writing 0x80 to register 0x39.

Temperature

The bq2050H internally determines the temperature in 10°C steps centered from approximately -35°C to +85°C. The temperature steps are used to adapt charge and discharge rate compensations, self-discharge counting, and available charge display translation. The temperature range is available over the serial port in 10°C increments as shown in the following table:

TMP (hex)	Temperature Range
0x	< -30°C
1x	-30°C to -20°C
2x	-20°C to -10°C
3x	-10°C to 0°C
4x	0°C to 10°C
5x	10°C to 20°C
6x	20°C to 30°C
7x	30°C to 40°C
8x	40°C to 50°C
9x	50°C to 60°C
Ax	60°C to 70°C
Bx	70°C to 80°C
Cx	> 80°C

Layout Considerations

The bq2050H measures the voltage differential between the SR and V_{SS} pins. V_{OS} (the offset voltage at the SR pin) is greatly affected by PC board layout. For optimal results, the PC board layout should follow the strict rule of a single-point ground return. Sharing high-current ground with small signal ground causes undesirable noise on the small signal nodes. Additionally:

- The capacitors (C1 and C2) should be placed as close as possible to the Vcc and SB pins, respectively, and their paths to V_{SS} should be as short as possible. A high-quality ceramic capacitor of 0.1µf is recommended for Vcc.
- The sense resistor capacitor should be placed as close as possible to the SR pin.
- The sense resistor (Rs) should be as close as possible to the bq2050H.

Gas Gauge Operation

The operational overview diagram in Figure 2 illustrates the operation of the bq2050H. The bq2050H accumulates a measure of charge and discharge currents, as well as an estimation of self-discharge. Charge and discharge currents are temperature and rate compensated, whereas self-discharge is only temperature compensated.

The main counter, Nominal Available Capacity (NAC), represents the available battery capacity at any given time. Battery charging increments the NAC register, while battery discharging and self-discharge decrement the NAC register and increment the DCR (Discharge Count Register).

The Discharge Count Register (DCR) is used to update the Last Measured Discharge (LMD) register only if a complete battery discharge from full to empty occurs without any partial battery charges. Therefore, the bq2050H adapts its capacity determination based on the actual conditions of discharge.

The battery's initial capacity is equal to the Programmed Full Count (PFC) shown in Table 2. Until LMD is updated, NAC counts up to but not beyond thie threshold during subsequent charges. This approach allows the gas gauge to be charger-independent and compatible with any type of charge regime.

1. **Last Measured Discharge (LMD) or learned battery capacity.**

   LMD is the last measured discharge capacity of the battery. On initialization (application of V_{CC} or battery replacement), LMD = PFC. During subsequent discharges, the LMD is updated with the latest measured capacity in the Discharge Count Register (DCR) representing a discharge from full to below EDV1. A qualified discharge is necessary for a capacity transfer from the DCR to the LMD register. The LMD also serves as the 100% reference threshold used by the relative display mode.

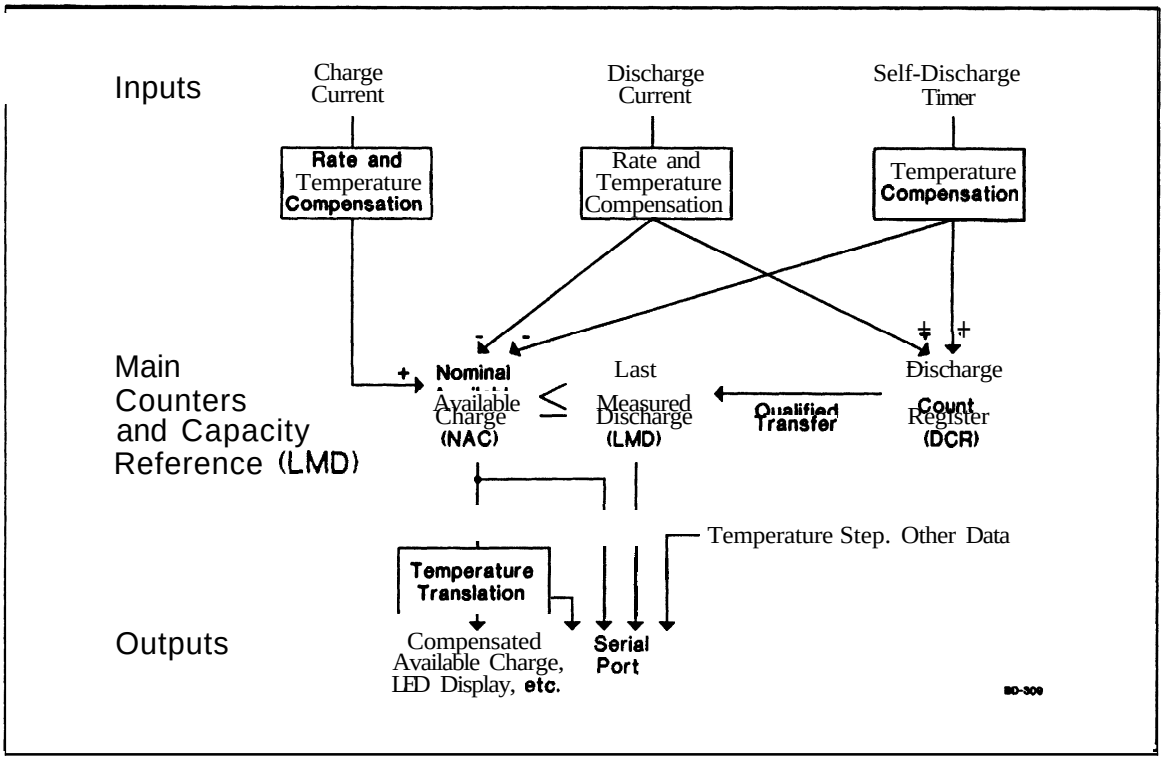


Figure 2. Operational Overview

2. Programmed Full Count (PFC) or initial battery capacity:

The initial LMD and gas gauge rate values are programmed by using $PROG_1$-$PROG_4$. The bq2050H is configured for a given application by selecting a PFC value from Table 2. The correct PFC may be determined by multiplying the rated battery capacity in mAh by the sense resistor value:

Battery capacity (mAh) • sense resistor (Ω) =

PFC (mVh)

Selecting a PFC slightly less than the rated capacity provides a conservative capacity reference until the bq2050H "learns" a new capacity reference.

Example: Selecting a PFC Value

Given:

Sense resistor = 0.05Ω
Number of cells = 2
Capacity = 1000mAh, Li-Ion battery, coke-anode
Current range = 50mA to 1A
Relative display mode
Serial port only
Self-discharge = NAC_{512} per day @ 25°C
Voltage drop over sense resistor = 2.5mV to 50mV
Nominal discharge voltage = 3.6V
High speed DQ

Table 1. bq2050H Programming

Pin Connection	$PROG_5$ Compensation/ Self-Discharge	$PROG_6$ NAC on Reset	$\overline{DISP}$ Display State
H	Table 4/Disabled	PFC, standard speed	LEDs disabled
Z	Table 4/ NAC_{512}	0, high speed	LEDs on when charging
L	Table 3/ NAC_{512}	0, standard speed	LEDs on for 4 sec.

Note: $PROG_5$ and $PROG_6$ states are independent.

Table 2. bq2050H Programmed Full Count mVh Selections

$PROG_x$		Programmed Full Count (PFC)	$PROG_4$ = L			$PROG_4$ = Z			Units
1	2		PROG3 = H	PROG3 = Z	PROG3 = L	PROG3 = H	PROG3 = Z	PROG3 = L	
-	-	-	SCALE = 1/80	SCALE = 1/160	SCALE = 1/320	SCALE = 1/640	SCALE = 1/1280	SCALE = 1/2560	mVh/ count
H	H	49152	614	307	154	76.8	38.4	19.2	mVh
H	Z	45056	563	282	141	70.4	35.2	17.6	mVh
H	L	40960	512	256	128	64.0	32.0	16.0	mVh
Z	H	36864	461	230	115	57.6	28.8	14.4	mVh
Z	Z	33792	422	211	106	53.0	26.4	13.2	mVh
Z	L	30720	384	192	96.0	48.0	24.0	12.0	mVh
L	H	27648	346	173	86.4	43.2	21.6	10.8	mVh
L	Z	25600	320	160	80.0	40.0	20.0	10.0	mVh
L	L	22528	282	141	70.4	35.2	17.6	8.8	mVh
V_{SR} equivalent to 2 counts/sec. (nom.)			90	45	22.5	11.25	5.6	2.8	mV

Therefore:

1000mAh • 0.05Ω = 50mVh

Select:

PFC = 30720 counts or **48mVh**
PROG1 = float
PROG2 = low
PROG3 = high
PROG4 = float
PROG5 = float
PROG6 = float

The initial full battery capacity is **48mVh** (960mAh) until the **bq2050H** ?earns° a new capacity with a qualified **discharge** from full **to EDV1.**

3. **Nominal Available Capacity (NAC):**

NAC counts up during charge **to** a **maximum** value of LMD and down during **discharge** and **self-discharge to 0. NAC is reset to 0 on init[illegible] and on the first** valid *charge* **following discharge** to **EDV1.** To prevent **overstatement of *charge during* periods** of overcharge, **NAC stops incrementing** when **NAC = LMD.**

4. **Discharge** Count Register (DCR):

The DCR counts up during discharge independent of NAC and could continue increasing after NAC has **decremented to 0. Prior to NAC = 0 (empty battery), both discharge** and **self-discharge increment the DCR** After NAC = 0, only discharge increments the DCR. The DCR **resets** to **0** when **NAC = LMD.** The **DCR does not** roll over but stops counting when it **reaches FFFFh.**

The DCR value becomes the new LMD value on the first charge after a valid **discharge to V_{EDV1} if:**

- No valid charge **initiations** (charges **greater than 256 NAC counts, where $V_{SRO} > V_{SRQ}$) occurred during the period between NAC = LMD and EDV1 detected.**
- **The self-discharge** count is not more than 4096 counts (8% **to** 18% of **PFC,** specific **percentage threshold** determined by **PFC).**
- The temperature **is ≥ 0°C** when the EDV1 level is reached **during discharge.**

The valid discharge flag **(VDQ) indicates** whether the **present discharge is** valid for LMD update. If the DCR update value is **less** than LMD by greater than 4096 counts, LMD will only be **modified** by 4096 counts. This prevents invalid **DCR** values from corrupting LMD.

5. **Scaled Available Energy (SAE):**

SAE is useful in determining the available energy within the battery, and may provide a more useful capacity reference in battery chemistries with eloped voltage **profiles** during discharge. SAE may be converted **to** a **mWh** value using the following **formula:**

$$E(mWh) = (SAEH * 256 + SAEL) * \frac{2.4 * SCALE * (R_{B1} + R_{B2})}{R_S * R_{B2}}$$

where R_{B1}, R_{B2} and R_S are **resistor values** in ohms. **SCALE** is the selected scale from Table 2. SAEH and SAEL **are** digital values read **via** DQ.

6. **Compensated Available Capacity (CAC)**

CAC counts similar to NAC, but contains the available capacity compensated for discharge rate and temperature.

Charge Counting

Charge activity is detected **based** on a positive voltage on the **V_{SR}** input. If charge activity **is** detected, the bq2050H increments **NAC** at a **rate** proportional to **V_{SR}** and, if enabled, activates an LED display. Charge actions increment the **NAC after compensation** for temperature.

The **bq2050H** determines charge activity **sustained** at a continuoue rate equivalent **to $V_{SRO} > V_{SRQ}$. A** valid charge **equates to sustained** charge activity greater than 256 **NAC** counts. Once a valid charge is detected, charge counting continues until **V_{SRO} (V_{SR} + V_{OS})** falls below **V_{SRQ}. V_{SRQ} is 210µV,** and is described in the Digital Magnitude Filter **section.**

Discharge Counting

Discharge activity is **detected based** on a negative voltage on the **V_{SR}** input. *All* **discharge** counts where **$V_{SRO} < V_{SRD}$ cause** the **NAC** register to decrement and the **DCR** to increment. **V_{SRD}** is **-200µV,** and is described in the Digital Magnitude Filter **section.**

Self-Discharge Estimation

The **bq2050H** continuously decrements **NAC and increments** DCR for **self-discharge** based *on* time **and temperature. The** self-discharge count **rate** is **programmed** to be a-nominal **1/512 • NAC per** day or disabled. **This** is the rate for a battery **whose** temperature is **between 20°–30°C.** The **NAC** register cannot be decremented below 0.

Count Compensations

Discharge Compensation

Corrections for the rate **of discharge,** temperature, **and anode type are made by adjusting an internal compensation factor. This factor is based on the measured rate of discharge of the** battery. **Tables** 3A **and** 3B **outline the correction** factor typically **used for** graphite anode Li-Ion batteries, and Tables 4A and

4B outline the factors typically used for *coke* anode Li-Ion batteries. The compensation factor is applied to CAC and is based on discharge rate and temperature.

Table 3A. Graphite Anode

Approximate Discharge Rate	Discharge Compensation Factor	Efficiency
< 0.5C	1.00	100%
≥ 0.5C	1.05	95%

Table 3B.

Temperature	Temperature Compensation Factor	Efficiency
≥ 10°C	1.00	100%
0°C to 10°C	1.10	90%
-10°C to 0°C	1.35	74%
≤ -10°C	2.50	40%

Table 4A. Coke Anode

Approximate Discharge Rate	Discharge Compensation Factor	Efficiency
<0.5C	1.00	100%
≥ 0.5C	1.15	86%

Table 4B.

Temperature	Temperature Compensation Factor	Efficiency
≥ 10°C	1.00	100%
0°C to 10°C	1.25	80%
-10°C to 0°C	2.00	50%
≤ -10°C	8.00	12%

Charge Compensation

The bq2050H applies the following temperature compensation to NAC during charge:

Temperature	Temperature Compensation Factor	Efficiency
< 10°C	0.95	95%
≥ 10°C	1.00	100%

This compensation applies to both types of Li-Ion cells.

Self-Discharge Compensation

The self-discharge compensation is programmed for a nominal rate of 1/512 • NAC per day. This is the rate for a battery within the 20–30°C temperature range. This rate varies across 8 ranges from <10°C to >70°C, changing with each higher temperature (approximately 10°C). See Table 5 below.

Table 5. Self-Discharge Compensation

Temperature Range	Typical Rate PROG5 = Z or L
< 10°C	NAC/2048
10–20°C	NAC/1024
20–30°C	NAC/512
30–40°C	NAC/256
40–50°C	NAC/128
50–60°C	NAC/64
60–70°C	NAC/32
> 70°C	NAC/16

Self-discharge may be disabled by connecting $PROG_5$ = H.

Digital Magnitude Filter

The bq2050H has a digital filter to eliminate charge and discharge counting below a set threshold. The bq2050H setting is 200µV for V_{SRD} and 210µV for V_{SRQ}.

Table 6. bq2050H Current-Sensing Errors

Symbol	Parameter	Typical	Maximum	Unib	Notes
Vos	Offset referred to V_{SR}	± 50	± 180	µV	$\overline{DISP}$ = V_{CC}.
INL	Integrated non-linearity error	± 2	± 4	%	Add 0.1% per °C above or below 25°C and 1% per volt above or below 4.25V.
INR	Integrated non-repeatability e——	± 1	± 2	%	Measurement repeatability given similar operating conditions.

2

Error Summary

Capacity Inaccurate

The LMD is susceptible to error on initialization or if no updates occur. On initialization, the LMD value includes the error between the programmed full capacity and the actual capacity. This error is present until a valid discharge occurs and LMD is updated (see the DCR description on page 7). The other cause of LMD error is battery wear-out. As the battery ages, the measured capacity must be adjusted to account for changes in actual battery capacity.

A Capacity Inaccurate counter (CPI) is maintained and incremented each time a valid charge occurs (qualified by NAC; see the CPI register description) and is reset whenever LMD is updated from the DCR. The counter does not wrap around but stops counting at 255. The capacity inaccurate flag (CI) is set if LMD has not been updated following 64 valid charges.

Current-Sensing Error

Table 5 illustrates the current-sensing error as a function of V_{SRO}. A digital filter eliminates charge and discharge counts to the NAC register when V_{SRO} is between V_{SRQ} and V_{SRD}.

Communicating With the bq2050H

The bq2050H includes a simple single-pin (DQ plus return) serial data interface. A host processor uses the interface to access various bq2050H registers. Battery characteristics may be easily monitored by adding a single contact to the battery pack. The open-drain DQ pin on the bq2050H should be pulled up by the host system, or may be left floating if the serial interface is not used.

The interface uses a command-based protocol, where the host processor sends a command byte to the bq2050H. The command directs the bq2050H to either store the next eight bits of data received to a register specified by the command byte or output the eight bite of data specified by the command byte.

The communication protocol is asynchronous return-to-one. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 333 bits/sec in standard communication mode and 5K bits/sec in high-speed mode (PROG6 = Z). The least-significant bit of a command or data byte is transmitted first. The protocol is simple enough that it can be implemented by moat host processors using either polled or interrupt processing. Data input from the bq2050H may be sampled using the pulse-width capture timers available on some microcontrollers.

If a communication error occurs, e.g. t_{CYCB} > 6ma (or 250µs for "H" specification), the bq2050H should be sent a BREAK to reinitiate the serial interface. A BREAK is detected when the HDQ pin is driven to a logic-low state for a time, t_B or greater. The HDQ pin should then be returned to its normal ready-high logic state for a time, t_{BR}. The bq2050H is now ready to receive a command from the host processor.

The return-to-one data bit frame consists of three distinct sections. The first section is used to start the transmission by either the host or the bq2050H taking the HDQ pin to a logic-low state for a period, $t_{STRH,B}$. The next section is the actual data transmission, where the data should be valid by a period, t_{DSU}, after the negative edge used to start communication. The data should be held for a period, t_{DV}, to allow the host or bq2050H to sample the data bit.

The final section is used to stop the transmission by returning the HDQ pin to a logic-high state by at least a period, t_{SSU}, after the negative edge used to start communication. The final logic-high state should be held until a period, tsv, to allow time to ensure that the bit transmission was stopped properly. The timings for data and break communication are given in the aerial communication timing specification and illustration sections.

Communication with the bq2050H is always performed with the least-significant bit being transmitted first. Figure 3 shows an example of a communication sequence to read the bq2050H NAC register.

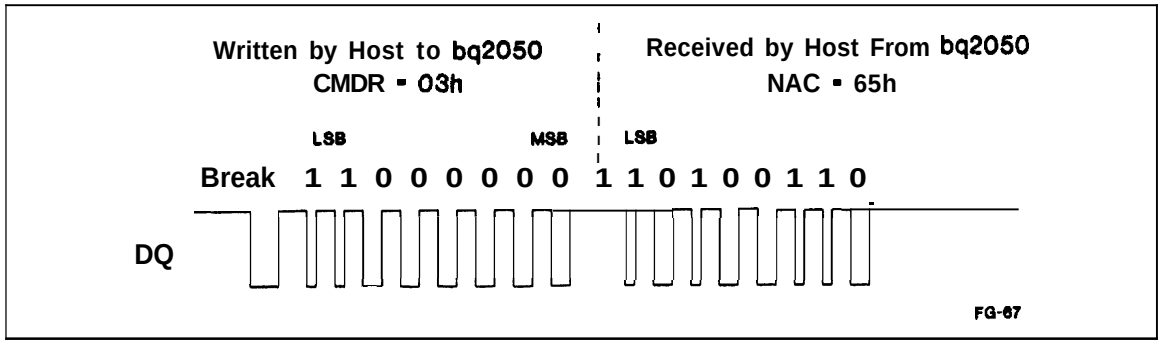


Figure 3. Typical Communication With the bq2050H

bq2050H Registers

The **bq2050H** command and **status** registers are **listed** in Table 7 and described below.

Command Register (CMDR)

The write-only CMDR register **is accessed** when eight valid command bits have been received by the **bq2050H**. The CMDR **register contains** two **fields:**

- W/$\overline{R}$ bit
- Command **address**

The W/$\overline{R}$ bit of the command register is used to select whether the received command is for a read or a write function.

The **W/$\overline{R}$** values are:

CMDR **Bits**							
7	6	5	4	3	2	1	*0*
W/$\overline{R}$	-						

Where W/$\overline{R}$ is:

0 **The bq2050H outputs the requested register contents specified by the address portion of CMDR.**

1 The following eight **bits** should be written to the register specified by the **address** portion of CMDR

The lower seven-bit field of CMDR **contains** the **address** portion of the register to be accessed. Attempts to write to invalid **addresses** are ignored.

CMDR **Bits**							
7	6	5	4	3	2	1	*0*
-	AD6	AD5	AD4	AD3	AD2	AD1	ADO (LSB)

Primary Status Flags Register (FLGS1)

The read-only **FLGS1** register **(address=01h)** contains the primary **bq2050H flags.**

The *charge* ***status*** flag (CHGS) **is asserted** when a valid charge rate **is** detected. Charge rate is deemed valid when **$V_{SRO} > V_{SRQ}$. A V_{SRO}** of **less** than **V_{SRQ}** or discharge activity **clears** CHGS.

The CHGS valuee are:

FLGS1 Bits

CHGS	-				-	-	-

Where CHGS is:

0 Either discharge activity detected or **$V_{SRO} < V_{SRQ}$**

1 **$V_{SRO} > V_{SRQ}$**

The *battery* replaced flag **(BRP) is** asserted whenever the **bq2050H is reset** either **by** application of **Vcc** or by a **serial** port command. BRP is reset when either a valid charge action increments NAC to be equal to LMD, or a valid charge action is **detected** after the **EDV1** flag **is** asserted. BRP = 1 signifies that the device **has** been **reset.**

The BRP valuee are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	BRP	-	-	-	-	-	-

Table 7. bq2050H Command and Status Registers

Symbol	Register Name	Loc. (hex)	Read/ Write	Control Field							
				7(MSB)	6	5	4	3	2	1	0(LSB)
CMDR	Command register	00h	Write	W/$\overline{R}$	AD6	AD5	AD4	AD3	AD2	AD1	AD0
FLGS1	Primary status flags register	01h	Read	CHGS	BRP	PSTAT	CI	VDQ	n/u	EDV1	EDVF
TMP	Temperature register	02h	Read	TMP3	TMP2	TMP1	TMP0	GG3	GG2	GG1	GG0
NACH	Nominal available capacity high byte register	03h	R/W	NACH7	NACH6	NACH5	NACH4	NACH3	NACH2	NACH1	NACH0
NACL	Nominal available capacity low byte register	17h	Read	NACL7	NACL6	NACL5	NACL4	NACL3	NACL2	NACL1	NACL0
BATID	Battery identification register	04h	R/W	BATID7	BATID6	BATID5	BATID4	BATID3	BATID2	BATID1	BATID0
LMD	Last measured discharge register	05h	R/W	LMD7	LMD6	LMD5	LMD4	LMD3	LMD2	LMD1	LMD0
FLGS2	Secondary status flags register	06h	Read	n/u	DR2	DR1	DR0	n/u	n/u	PSTAT1	OVLD
PPD	Program pin pull-down register	07h	Read	n/u	n/u	PPD6	PPD5	PPD4	PPD3	PPD2	PPD1
PPU	Program pin pull-up register	08h	Read	n/u	n/u	PPU6	PPU5	PPU4	PPU3	PPU2	PPU1
CPI	Capacity inaccurate count register	09h	Read	CPI7	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	CPI0
VSB	Battery voltage register	0Bh	Read	VSB7	VSB6	VSB5	VSB4	VSB3	VSB2	VSB1	VSB0
VTS	End-of-discharge threshold select register	0Ch	R/W	VTS7	VTS6	VTS5	VTS4	VTS3	VTS2	VTS1	VTS0
CACH	Compensated available capacity high byte register	0Dh	Read	CACH7	CACH6	CACH5	CACH4	CACH3	CACH2	CACH1	CACH0
CACL	Compensated available capacity low byte register	0Eh	Read	CACL7	CACL6	CACL5	CACL4	CACL3	CACL2	CACL1	CACL0
SAEH	Scaled available energy high byte register	0Fh	Read	SAEH7	SAEH6	SAEH5	SAEH4	SAEH3	SAEH2	SAEH1	SAEH0
SAEL	Scaled available energy low byte register	10h	Read	SAEL7	SAEL6	SAEL5	SAEL4	SAEL3	SAEL2	SAEL1	SAEL0
RST	Reset Register	39h	W	RST	0	0	0	0	0	0	0
RNAC	Relative NAC	11h	R	-	RNAC6	RNAC5	RNAC4	RNAC3	RNAC2	RNAC1	RNAC0

Note: n/u = not used

Where BRP is:

0 Battery is charged until NAC = LMD *or* discharged until the EDVl flag is asserted

1 bq2050H is reset

The *protector status* flag (PSTAT) provides information on the state of the overvoltage protector within the Li-Ion battery pack. The PSTAT flag is asserted whenever this input is high and is cleared when the input is low.

The PSTAT values are:

FLGSI Bits							
7	6	5	4	3	2	1	0
-	-	PSTAT	-		-	-	-

Where PSTAT is:

0 PSTAT input is low

1 PSTAT input is high

The ***capacity inaccurate*** flag (CI) is used to warn the user that the battery has been charged a substantial number of times since LMD has been updated. The CI flag is asserted on the 64th charge after the last LMD update or when the bq2050H is reset. The flag is cleared after an LMD update.

The CI values are:

FLGSI Bits							
7	6	5	4	3	2	1	0
		-	CI	-			

Where CI is:

0 When LMD is updated with a valid full discharge

1 After the 64th valid charge action with no LMD updates or the bq2050H is reset

The ***valid discharge*** flag (VDQ) is asserted when the bq2050H is discharged from NAC=LMD. The flag remains set until either LMD is updated or one of three actions that can clear VDQ occurs:

- The self-discharge count register (SDCR) has exceeded the maximum acceptable value (4096 counts) for an LMD update.
- A valid charge action sustained at $V_{SRO} > V_{SRQ}$ for at least 256 NAC counts.
- The EDV1 flag was set at a temperature below 0°C

The VDQ valuea are:

FLGSI Bib							
7	6	5	4	3	2	1	0
-	-	-	-	VDQ	-	-	-

Where VDQ is:

0 SDCR ≥ 4096, subsequent valid charge action detected, or EDVl is asserted with the temperature less than 0°C

1 On first discharge after NAC = LMD

The ***first end-of-discharge warning*** flag (EDVl) warns the user that the battery is almost empty. The first segment pin, SEG_1, is modulated at a 4Hz rate if the display is enabled once EDVl is asserted, which should warn the user that loss of battery power is imminent. The EDVl flag is latched until a valid charge has been detected. The EDVl threshold is externally controlled via the VTS register (see Voltage Threshold Register on this page).

The EDVl values are:

FLGSI Bits							
7	6	5	4	3	2	1	0
					-	EDVl	-

Where EDVl is:

0 Valid charge action detected, $V_{SB} \geq V_{TS}$

1 $V_{SB} < V_{TS}$ providing that the discharge rate is < 2C

The ***final end-of-discharge warning*** flag (EDVF) flag is used to warn that battery power is at a failure condition. All segment drivers are turned off. The EDVF flag is latched until a valid charge has been detected. The EMPTY pin is also forced to a high-impedance state on assertion of EDVF. The host system may pull EMPTY high, which may be used to disable circuitry to prevent deep-discharge of the battery. The EDVF threshold is set 50mV below the EDVl threshold.

The EDVF values are:

FLGSI Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	EDVF

Where EDVF is:

0 Valid charge action detected, $V_{SB} \geq (V_{TS} - 50mV)$

1 $V_{SB} < (V_{TS} - 50mV)$ providing the discharge rate is < 2C

Table 7. Temperature Register

TMP3	TMP2	TMP1	TMP0	Temperature
0	0	0	0	T < -30°C
0	0	0	1	-30°C < T < -20°C
0	0	1	0	-20°C < T < -10°C
0	0	1	1	-10°C < T < 0°C
0	1	0	0	0°C < T < 10°C
0	1	0	1	10°C < T < 20°C
0	1	1	0	20°C < T < 30°C
0	1	1	1	30°C < T < 40°C
1	0	0	0	40°C < T < 50°C
1	0	0	1	50°C < T < 60°C
1	0	1	0	60°C < T < 70°C
1	0	1	1	70°C < T < 80°C
1	1	0	0	T > 80°C

Temperature Register (TMP)

The read-only TMP register (address=02h) contains the battery temperature.

TMP Temperature Bits							
TMP4	TMP3	TMP2	TMP1	-	-	-	-

The bq2050H contains an internal temperature sensor. The temperature is used to set charge and discharge efficiency factors as well as to adjust the self-discharge coefficient. The temperature register contents may be tramlated as shown in Table 7.

The bq2050H calculates the gas gauge bits. GG3-GG0 as a function of CACH and LMD. The results of the calculation give available capacity in 1/16 increments from 0 to 15/16.

TMPGG Gas Gauge Bits							
7	6	5	4	3	2	1	0
-	-	-	-	GG3	GG2	GG1	GG0

Nominal Available Charge Registers (NACH/NACL)

The read/write NACH high-byte register (address=03h) and the read-only NACL low-byte register (address=17h) are the main gas gauging register for the bq2050H. The NAC registers are incremented during charge actions and decremented during discharge and self-discharge actions.

The correction factors for charge/discharge efficiency are applied automatically to NAC. NACH and NACL are set to 0 during a bq2050 reset.

Writing to the NAC registers affects the available charge counts and, therefore, affects the bq2050H gas gauge operation. Do not write the NAC registers to a value greater than LMD.

Battery Identification Register (BATID)

The read/write BATID register (address=04h) is available for use by the system to determine the type of battery pack. The BATID contents are retained as long as Vcc is greater than 2V. The contents of BATID have no effect on the operation of the bq2050H. There is no default setting for this register.

Last Measured Discharge Register (LMD)

LMD is a read/write register (address=05h) that the bq2050H uses as a measured full reference. The bq2050H adjusts LMD based on the measured discharge capacity of the battery from full to empty. In this way the bq2050H updates the capacity of the battery. LMD is set to PFC during a bq2050H reset.

Secondary Status Flags Register (FLGS2)

The read-only FLGS2 register (address=06h) contains the secondary bq2050H flags.

The discharge rate flags, DR2–0, are bits 6–4.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	DR2	DR1	DR0	-	-	-	

They are used to determine the current diecharge regime as follows:

DR2	DR1	DRO	Discharge Rate
0	0	0	DRATE < 0.5C
0	0	1	0.5C ≤ DRATE < 2C

The overload flag (OVLD) is asserted when a discharge rate in excess of 2C is detected. OVLD remains asserted as long as the condition persists and is cleared 0.5 seconds after the rate drops below 2C. The overload condition is used to stop sampling of the battery terminal characteristics for end-of-discharge determination.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-						-	OVLD

Program Pin Pull-Down Register (PPD)

The read-only PPD register (address=07h) contains some of the programming pin information for the bq2050H. The segment drivers, SEG_{1-6}, have a corresponding PPD register location. PPD_{1-6}. A given location is set if a pull-down resistor has been detected on its corresponding segment driver. For example, if SEG_1 and SEG_4 have pull-down resistors, the contents of PPD are xx001001.

Program Pin Pull-Up Register (PPU)

The read-only PPU register (address=08h) contains the rest of the programming pin information for the bq2050H. The segment drivers, SEG_{1-6}, have a corresponding PPU register location, PPU_{1-6}. A given location is set if a pull-up resistor has been detected on its corresponding segment driver. For example, if SEG_3 and SEG_6 have pull-up resistors, the contents of PPU are xx100100.

PPD/PPU Bib							
7	6	5	4	3	2	1	0
-	-	PPU_6	PPU_5	PPU_4	PPU_3	PPU_2	PPU_1
-	-	PPD_6	PPD_5	PPD_4	PPD_3	PPD_2	PPD_1

Capacity Inaccurate Count Register (CPI)

The read-only CPI register (address=09h) is ueed to indicate the number of times a battery has been charged without an LMD update. Because the capacity of a rechargeable battery varies with age and operating canditions, the bq2050H adapts to the changing capacity over time. A complete discharge from full (NAC=LMD) *to* empty (EDV1=1) *is* required to perform an LMD update assuming there have been no intervening valid charges, the temperature is greater than or equal to 0°C, and the self-discharge counter is less than 4096 counts.

The CPI register is incremented every time a valid charge is detected. When NAC > 0.94 • LMD, however, the CPI register increments on the first valid charge; CPI does not increment again for a valid charge until NAC < 0.94 • LMC. This prevents continuous trickle charging from incrementing CPI if self-diecharge decrements NAC. The CPI register increments to 255 without rolling over. When the contents of CPI are incremented to 64, the capacity inaccurate flag, CI, is asserted in the FLGS1 register. The CPI register is reset whenever an update of the LMD register is performed, and the CI flag is also cleared.

Battery Voltage Register (VSB)

The read-only battery voltage register is used to read the single-cell battery voltage on the SB pin. The VSB register (address = 0Bh) is updated approximately once per second with the present value of the battery voltage. V_{SB} = 24V • (VSB/256).

VSB Register Bits							
7	6	5	4	3	2	1	0
VSB7	VSB6	VSB5	VSB4	VSB3	VSB2	VSB1	VSBO

Voltage Threshold Register (VTS)

The end-of-discharge threshold voltages (EDV1 and EDVF) can be set using the VTS register (address = 0Ch). The read/write VTS register sets the EDVl trip point. EDVF is set 50mV below EDV1. The default value in the VTS register is A2h, representing EDVl = 1.52V and EDVF = 1.47V. EDVl = 2.4V • (VTS/256).

VTS Register Bits							
7	6	5	4	3	2	1	0
VTS7	VTS6	VTS5	VTS4	VTS3	VTS2	VTS1	VTS0

Compensated Available Charge Registers (CACH/CACL)

The read-only CACH high-byte register (address = 0Dh) and the read-only CACL low-byte register (address = 0Eh) represent the available charge compensated for diecharge rate and temperature. CACH and CACL use piece-wise corrections as outlined in Tables 3A, 3B, 4A, and 4B, and will vary as conditions change. The NAC and LMD registers are not affected by the discharge rate and temperature.

Scaled Available Energy Registers (SAEH/SAEL)

The read-only SAEH high-byte register (address = 0Fh) and the read only SAEL low-byte register (address = 10h) are used to scale battery voltage and CAC to a value which *can* be translated to watt-hours remaining under the present conditions. SAEL and SAEH may be converted to mWh using the formula on page 7.

Reset Register (RST)

The reset register (address = 39h) provides a means via software of initializing the bq2050H. A full bq2050H reset can be accomplished over the serial port by writing 80h to register 39h. Setting any other bit in the reset register is not allowed and will result in improper bq2050H operation. Resetting the bq2050H sets the following

- LMD = PFC
- CPI, VDQ, RNAC, NACH/L, CACH/L, SAEH/L = 0
- CI and BRP = 1

Note: NACH = PFC if $PROG_6$ = H

Relative NAC Register

The RNAC register (address = 11h) provides the relative battery etate-of-charge by dividing NACH by LMD. RNAC varies from 0 to 64h representing relative state-of-charge from 0 to 100%.

Reset Register (RST)

The reset register (address = 39h) enablea a software-controlled reset of the device. By writing the RST register contents from 00h to 80h, a bq2050H reset is performed. *Setting* any *bit other than the most-significant bit of the RST register is not allowed and results in improper operation of the bq2050H.*

Resetting the bq2050H seta the following:

- LMD = PFC
- CPI, VDQ, NACH, and NACL = 0
- CI and BRP = 1

Note: Self-discharge is disabled when $PROG_5$ = H.

Display

The bq2050H can directly display capacity information using low-power LEDs. If LEDs are used, the program pins should be resistively tied to V_{CC} or V_{SS} for a program high or program low, respectively.

The bq2050H displays the battery charge state in relative mode. In relative mode, the battery *charge* is represented as a percentage of the LMD. Each LED segment represents 20% of the LMD.

The capacity display is also adjusted for the present battery temperature. The temperature adjustment reflects the available capacity at a given temperature but does not affect the NAC register. The temperature adjustments are detailed in the CACH and CACL register descriptions.

When $\overline{DISP}$ is tied to V_{CC}, the SEG_{1-5} outputs are inactive. When $\overline{DISP}$ is left floating, the display becomes active whenever the bq2050H detects a charge in progress $V_{SRO} > V_{SRQ}$. When pulled low, the segment outputs become active for a period of four seconds, ± 0.5 seconds.

The segment outputa are modulated as two banks, with segmenta 1, 3, and 5 alternating with segments 2 and 4. The segment outputs are modulated at approximately 100Hz with each segment bank active for 30% of the period.

SEG_1 blinks at a 4Hz rate whenever V_{SB} has been detected to be below V_{EDV1} (EDV1 = 1), indicating a low-battery condition. V_{SB} below V_{EDVF} (EDVF = 1) disables the display output.

Microregulator

The bq2050H *can* operate directly from one cell. A micropower source for the bq2050H *can* be inexpensively built using the FET and an external resistor to accommodate a greater number of cells; see Figure 1.

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to Vss	-0.3	+7.0	V	
All other pins	Relative to Vss	-0.3	+7.0	V	
REF	Relative to Vss	-0.3	+8.5	V	Current limited by R1 (see Figure 1)
V_{SR}	Relative to Vss	-0.3	+7.0	V	Minimum 100Ω series resistor should be used to protect SR in case of a shorted battery (see the bq2050H application note for details).
T_{OPR}	Operating temperature	0	+70	°C	Commercial
		-40	+85	°C	Industrial

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage Thresholds ($T_A = T_{OPR}$; V = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDVF}	Final empty warning	1.44	1.47	1.50	V	SB, default
V_{EDV1}	First empty warning	1.49	1.52	1.55	V	SB, default
V_{SRO}	SR sense range	-300		+2000	mV	SR, V_{SR} + Vos
V_{SRQ}	Valid charge	210			µV	V_{SR} + Vos (see note)
V_{SRD}	Valid discharge			-200	µV	V_{SR} + Vos (see note)
V_{MCV}	Maximum single-cell voltage	2.20	2.25	2.30	V	SB

Note: Vos is affected by PC board layout. Roper layout guidelines should be followed for optimal performance. See "LayoutConsiderations."

DC Electrical Characteristics (T_A = T_{OPR})

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	3.0	4.25	6.5	V	V_{CC} excursion from < 2.0V to ≥ 3.0V initializes the unit.
V_{REF}	Reference at 25°C	5.7	6.0	6.3	V	I_{REF} = 5µA
	Reference at -40°C to +85°C	4.5	-	7.5	V	I_{REF} = 5µA
R_{REF}	Reference input impedance	2.0	5.0	-	MΩ	V_{REF} = 3V
I_{CC}	Normal operation	-	90	135	µA	V_{CC} = 3.0V, DQ = 0
		-	120	180	µA	V_{CC} = 4.25V, DQ = 0
		-	170	250	µA	V_{CC} = 6.5V, DQ = 0
V_{SB}	Battery input	0	-	V_{CC}	V	
R_{SBmax}	SB input impedance	10	-	-	MΩ	0 < V_{SB} < V_{CC}
I_{DISP}	$\overline{DISP}$ input leakage	-	-	5	µA	V_{DISP} = V_{SS}
I_{LCOM}	LCOM input leakage	-0.2	-	0.2	µA	$\overline{DISP}$ = V_{CC}
I_{RBI}	RBI data retention current	-	-	100	nA	V_{RBI} > V_{CC} < 3V
R_{DQ}	Internal pulldown	500	-	-	KΩ	
V_{SR}	Sense resistor input	-0.3	-	2.0	V	V_{SR} < V_{SS} = discharge; V_{SR} > V_{SS} = charge
R_{SR}	SR input impedance	10	-	-	MΩ	-200mV < V_{SR} < V_{CC}
V_{IH}	Logic input high	V_{CC} - 0.2	-	-	V	$PROG_1$–$PROG_6$
V_{IL}	Logic input low	-	-	V_{SS} + 0.2	V	$PROG_1$–$PROG_6$
V_{IZ}	Logic input Z	float	-	float	V	$PROG_1$–$PROG_6$
V_{OLSL}	SEG_X output low, low V_{CC}	-	0.1	-	V	V_{CC} = 3V, I_{OLS} ≤ 1.75mA SEG_1–SEG_5
V_{OLSH}	SEG_X output low, high V_{CC}	-	0.4	-	V	V_{CC} = 6.5V, I_{OLS} ≤ 11.0mA SEG_1–SEG_5
V_{OHLCL}	LCOM output high, low V_{CC}	V_{CC} - 0.3	-	-	V	V_{CC} = 3V, I_{OHLCOM} = -5.25mA
V_{OHLCH}	LCOM output high, high V_{CC}	V_{CC} - 0.6	-	-	V	V_{CC} = 6.5V, I_{OHLCOM} = -33.0mA
I_{IH}	$PROG_{1-6}$ input high current	-	1.2	-	µA	V_{PROG} = V_{CC}/2
I_{IL}	$PROG_{1-6}$ input low current	-	1.2	-	µA	V_{PROG} = V_{CC}/2
I_{OHLCOM}	LCOM source current	-33	-	-	mA	At V_{OHLCH} = V_{CC} - 0.6V
I_{OLS}	SEG_{1-5} sink current	-	-	11.0	mA	At V_{OLSH} = 0.4V
I_{OL}	Open-drain sink current	-	-	5.0	mA	At V_{OL} = V_{SS} + 0.3V DQ
V_{OL}	Open-drain output low	-	-	0.5	V	I_{OL} ≤ 5mA, DQ
V_{IHDQ}	DQ input high	2.5	-	-	V	DQ
V_{ILDQ}	DQ input low	-	-	0.8	V	DQ
R_{PROG}	Soft pull-up or pull-down resistor value (for programming)	-	-	200	KΩ	$PROG_1$–$PROG_6$
R_{FLOAT}	Float state external impedance	-	5		MΩ	$PROG_1$–$PROG_6$

Note: All voltages relative to V_{SS}.

Standard Serial Communication Timing Specification ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYCH}	Cycle time, host to bq2050H	3	-	-	ms	See note
t_{CYCB}	Cycle time, bq2050H to host	3	-	6	ms	
t_{STRH}	Start hold, host to bq2050H	5	-	-	ns	
t_{STRB}	Start hold, bq2050H to host	500	-	-	µs	
t_{DSU}	Data setup	-	-	750	µs	
t_{DH}	Data hold	750	-	-	µs	
t_{DV}	Data valid	1.50	-	-	ms	
t_{SSU}	Stop setup	-	-	2.25	ms	
t_{SH}	Stop hold	700	-	-	µs	
t_{SV}	Stop valid	2.95	-	-	ms	
t_B	Break	3	-	-	ms	
t_{BR}	Break recovery	1	-	-	ms	

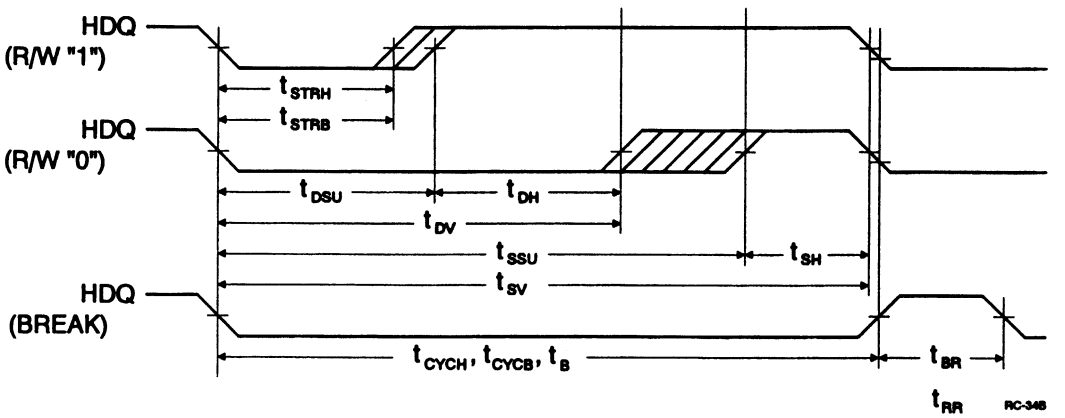
Note: The open-drain DQ pin should be pulled to at least V_{CC} by the host system for proper DQ operation. DQ may be left floating if the serial interface is not used.

High-Speed Serial Communication Timing Specification ($T_A = T_{OPR}$)

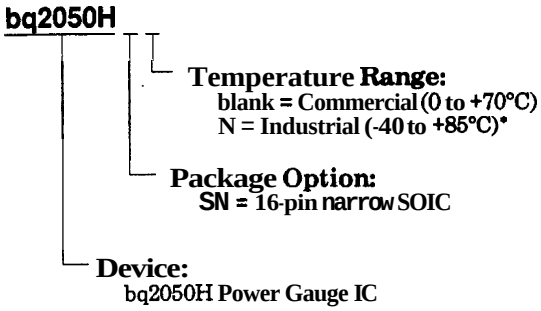
Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYCH}	Cycle time, host to bq2050H (write)	190	-	-	µs	See note
t_{CYCB}	Cycle time, bq2050H to host (read)	190	-	250	µs	
t_{STRH}	Start hold, host to bq2050H (write)	5	-	-	ns	
t_{STRB}	Start hold, bq2050H to host (read)	32	-	-	µs	
t_{DSU}	Data setup	-	-	50	µs	
t_{DH}	Data hold	50	-	-	µs	
t_{DV}	Data valid	95	-	-	µs	
t_{SSU}	Stop setup	-	-	145	µs	
t_{SH}	Stop hold	45	-	-	µs	
t_{SV}	Stop valid	185	-	-	µs	
t_B	Break	190	-	-	µs	
t_{BR}	Break recovery	40	-	-	µs	
t_{RR}	Read recovery	40	-	-	µs	Last bit of read to start of new cycle

Note: The open-drain DQ pin should be pulled to at least V_{CC} by the host system for proper DQ operation. DQ may be left floating if the serial interface is not used.

Serial Communication Timing Illustration



Ordering Information



* Contact factory for availability.

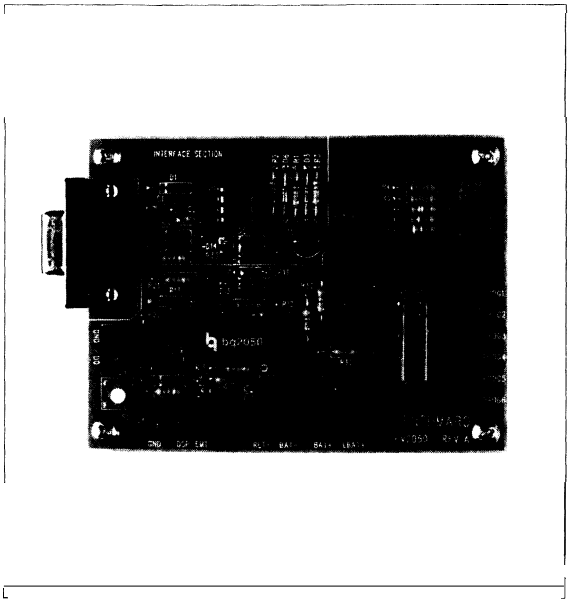
BENCHMARQ

Product Brief **EV2050/H**

Power Gauge™ Evaluation Board

Features

- bq2050 Power Gauge™ IC evaluation and development system
- RS-232 interface hardware for easy access to state-of-charge information via the serial port
- Alternative terminal block for direct connection to the serial port
- Battery state-of-charge monitoring for 1- to 5-cell (series) applications
- On-board voltage regulator for Power Gauge™ operation
- State-of-charge information displayed on bank of 5 LEDs
- Nominal capacity jumper-configurable
- Cell anode type (coke or graphite) jumper-configurable



General Description

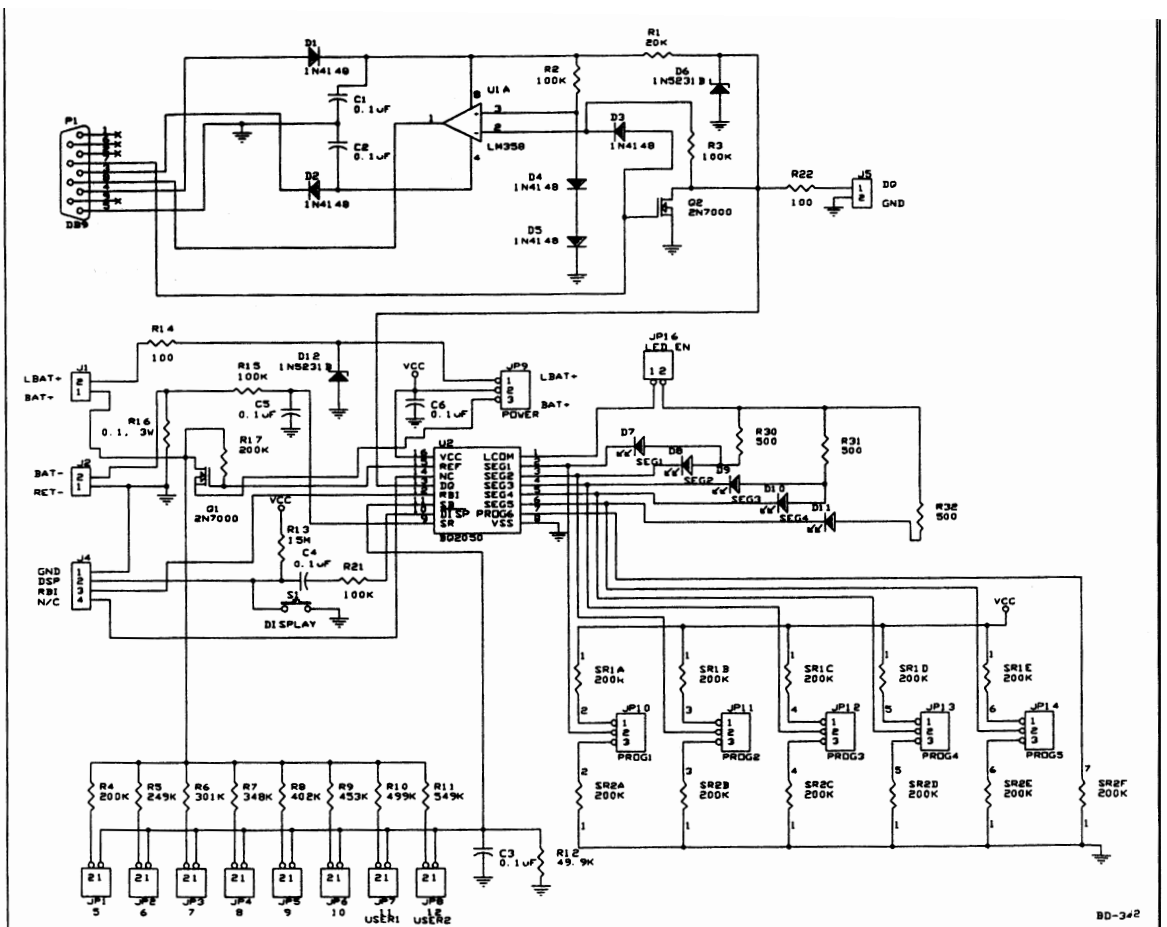
The EV2050/H Evaluation System provides a development and evaluation environment for the bq2050 or bq 2050H Power Gauge™ IC. The EV2050/H incorporates a bq2050, a sense resistor, and all other hardware necessary to provide a power monitoring function for 1 to 5 series Li-Ion cells.

Hardware for an RS-232 interface is included on the EV2050/H so that easy access to the state-of-charge information can be achieved via the serial port of the bq2050/H. Direct connection to the serial port of the bq2050/H is also made available for check-out of the final hardware/software implementation.

The menu-driven software provided with the EV2050/H displays chargeidischarge activity and allows user interface to the bq2050 from any standard DOS PC.

A full data sheet for this product is available on our web site (http:/iwww.benchmarq.com), or you may contact the factory for one.

EV2050/H Board Schematic



BENCHMARQ

bq2090

Gas Gauge IC With SMBus-Like Interface

Features

- **Provides** conservative and repeatable meaeurement of available charge in **NiCd, NiMH,** and Lithium Ion rechargeable batteries
- ➤ **Designed** for battery **pack** integration
  - **120µA** typical **operating** current
  - Small **size** enables implementations in as little ae **½ square** inch of PCB
- **Two-wire SMBus-like** interface
- ➤ **Measurements compensated** for current and **temperature**
- ➤ Contains self-discharge compensation **using** internal temperature **sensor**
- ➤ 16-pin narrow SOIC

General Description

The **bq2090** Gae Gauge IC With SMBus-like Interface is intended for battery-pack **or** in-eyetam installation to maintain an accurate record of available battery **charge,** The bq2090 directly **supports** capacity **monitoring** for NiCd, NiMH, and Lithium Ion bat-

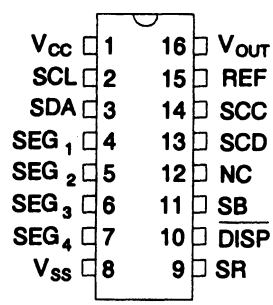
The bq2090 uses the SMBus protocol that supports *many* of the **Smart Battery** Data **(SBData)** commands. Battery state-of-charge, capacity remaining, **remaining time** and chem**istry are available** *over* the serial link **Battery-charge** state *can* be **directly** indicated using a **four-segment LED** display to graphically depict battery **full-to-empty in 25% increments.**

The bq2090 estimates **battery** self-dis**charge based on an internal timer and temperature sensor. The bq2090 also automatically** recalibrates, or 'learns' battery capacity in the full course of a **discharge cycle from full to empty.**

The **bq2090** may operate directly **from** three or four **nickel chemistry cells.** With the REF output and an external **transistor,** a **simple,** inexpensive regulator can be built to provide Vcc for other battery cell **configurations.**

An external E^2PROM ie **used** to program initial values into the bq2090 and is necessary for proper operation.

Pin Connections



16-Pin Narrow SOIC

PN-110

Pin Names

VOUT	**E^2PROM supply output**	SB	Battery sense input
SEG1	LED segment 1	**$\overline{DISP}$**	**Display** control input
SEG2	LED segment 2	SR	Sense **resistor** input
SEG3	LED segment 3	SCC	Serial communication clock
SEG4	LED segment 4	**SCD**	Serial communication data **input/output**
SCL	Serial memory clock		
SDA	Serial memory **data**	**Vcc**	**3.0–5.5V**
REF	Voltage reference **output**	**Vss**	**System ground**

Pin Descriptions

SEG_1–SEG_4 **LED display segment outputs**

Each output may activate an external LED to sink the current sourced from V_{CC}.

SCC **Serial communication clock**

This open-drain bidirectional pin is used to clock the data transfer to and from the bq2090.

SCD **Serial communication data**

This open-drain bidirectional pin is used to transfer address and data to and from the bq2090.

SCL **Serial memory clock**

This output is used to clock the data transfer between the bq2090 and the external non-volatile configuration memory.

SDA **Serial memory data and** address

This bi-directional pin is used to transfer address and data to and from the bq2090 and the external configuration memory.

NC **No connect**

V_{OUT} **Supply output**

This output supplies power to the external E^{2}PROM configuration memory.

SR **Sense resistor input**

The voltage drop (V_{SR}) across pins SR and V_{SS} is monitored and integrated over time to interpret charge and discharge activity. The SR input is connected to the sense resistor and the negative terminal of the battery. $V_{SR} < V_{SS}$ indicates diecharge, and $V_{SR} > V_{SS}$ indicates charge. The effective voltage drop, V_{SRO}, as seen by the bq2090 is $V_{SR} + V_{OS}$ (see Table 3).

$\overline{DISP}$ **Display control input**

$\overline{DISP}$ high disables the LED display. $\overline{DISP}$ floating allows the LED display to be active during charge or during discharge if the rate is greater than a user-programmable threshold. $\overline{DISP}$ low activates the display.

SB **Secondary battery input**

This input monitors the single-cell voltage potential through a high-impedance resistor divider network for end-of-discharge voltage (EDV) thresholds and maximum charge voltage (MCV).

REF **Reference output for regulator**

REF provides a reference output for an optional micro-regulator.

V_{CC} **Supply voltage input**

V_{SS} **Ground**

Functional Description

General Operation

The bq2090 determines battery capacity by monitoring the amount of charge input to or removed from a rechargeable battery. The bq2090 measures discharge and charge currents, estimates self-discharge and monitors the battery for low-battery voltage thresholds. The charge measurement is made by monitoring the voltage across a small-value series sense resistor between the negative battery terminal and ground. The available battery charge is determined by monitoring this voltage over time and correcting the measurement for the environmental and operating conditions.

Figure 1 shows a typical battery pack application of the bq2090 using the LED capacity display, the serial port. and an external E2PROM for battery pack programming information. The bq2090 must be configured and calibrated for the battery-specific information to ensure proper operation. Table 1 outlines the externally programmable functions available in the bq2090. Refer to the Programming the bq2090 section for further details.

An internal temperature sensor eliminates the need for an external thermistor—reducing cost and components. An internal, temperature-compensated time-base eliminates the need for an external resonator, further reducing cost and components. The entire circuit in Figure 1 can occupy less than ¾ square inch of board space.

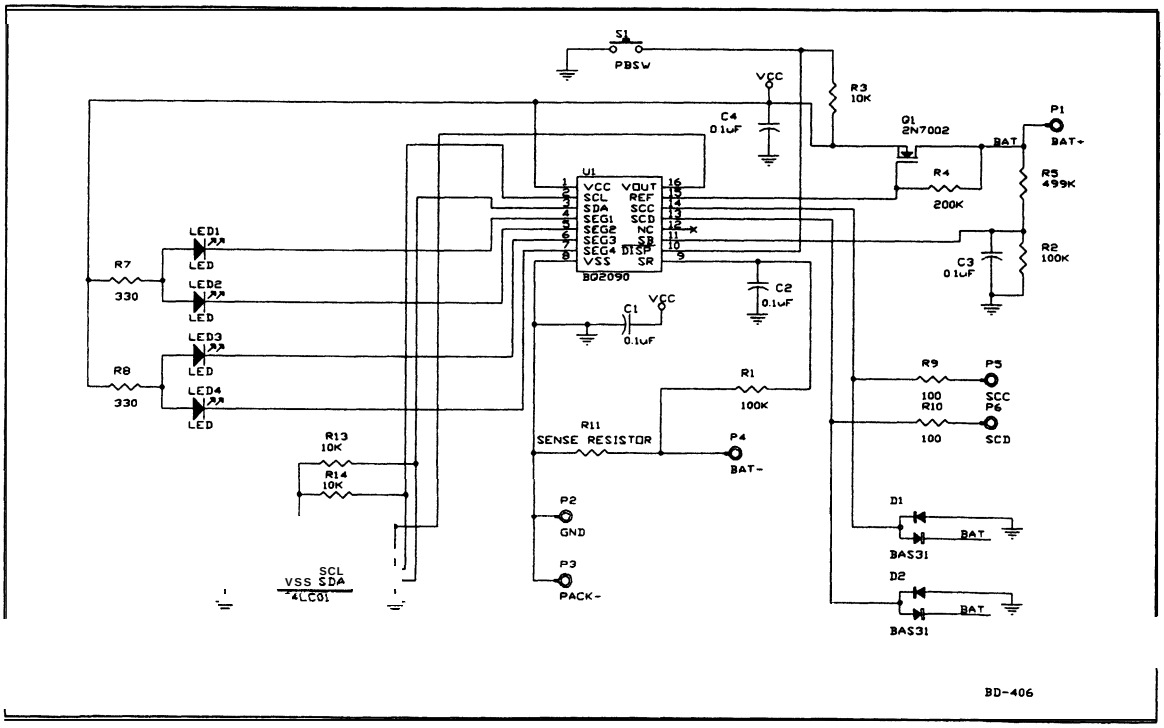


Figure 1. Battery Pack Application Diagram—LED Display

Table 1. Configuration Memory Programming Values

Parameter Name	Address	Length	Units
Design capacity	0x00/0x01	16 bits: low byte, high byte	mAh
Initial battery voltage	0x02/0x03	8 bits	N/A
Reserved	0x04/0x05	-	-
Reserved	0x06/0x07	-	-
Remaining Capacity Alarm	0x08/0x09	16 bits: low byte, high byte	mAh
FLAGS1	0x0a	8 bits	N/A
FLAGS2	0x0b	8 bits	N/A
Current measurement gain	0x0c/0x0d	16 bits: low byte, high byte	N/A
EDV_1	0x0e/0x0f	16 bits: low byte, high byte	mV
EDV_F	0x10/0x11	16 bits: low byte, high byte	mV
Temperature offset	0x12/0x13	16 bits: low byte, high byte	0.1°K
Self-discharge rate	0x14	16 bits: low byte, high byte	N/A
Digital filter	0x15	8 bits	mV
Current integration gain	0x16/0x17	16 bits: low byte, high byte	N/A
Discharge display threshold	0x18	8 bits	N/A
Battery voltage offset	0x19	8 bits	mV
Battery voltage gain	0x1a/0x1b	16 bits	N/A
Reserved	0x1c/0x31	-	-
Design voltage	0x32/0x33	16 bite: low byte, high byte	mV
Specification Information	0x34/0x35	16 bite: low byte, high byte	N/A
Manufacturer Date	0x36/0x37	16 bits: low byte, high byte	N/A
Serial number	0x38/0x39	16 bits: low byte, high byte	N/A
Reserved	0x3a/0x3f	-	-
Manufacturer name	0x40/0x4f	8 + 120 bits	N/A
Device name	0x50/0x5f	8 + 120 bits	N/A
Chemistry	0x60/0x6f	8 + 120 bits	N/A
Manufacturer data	0x70/0x7f	8 +120 bits	N/A

Note: N/A=Not applicable; data packed or coded. See Programming the bq2090 section for details.

Voltage Thresholds

In conjunction with monitoring V_{SR} for charge/discharge currents, the bq2090 monitors the battery potential through the SB pin. The voltage potential is determined through a resistor divider network per the following equation:

$$\frac{R_5}{R_2} = \frac{MBV}{2.25} - 1$$

where MBV is the maximum battery voltage, R_5 is connected to the positive battery terminal, and R_2 is connected to the negative battery terminal. should be rounded to the next highest integer. The battery voltage is monitored for the end-of-discharge voltage (EDV) and for maximum cell voltage (MCV) and for alarm warning conditions. EDV threshold levels are used to determine when the battery has reached an "empty' state, and the MCV threshold is wed for fault detection during charging. The battery voltage gain and two EDV thresholds are programmed via E^2PROM. See the Programming the bq2090 section for further details.

If V_{SB} is below either of the two EDV thresholds, the associated *flag* is latched and remains latched, independent of V_{SB}, until the next valid charge.

EDV monitoring may be disabled under certain conditions. If the discharge current is greater than 3A, EDV monitoring is disabled and resumes after the current falls below 1.5A.

Reset

The bq2090 is reeet when f i t connected to the battery pack. The bq2090 can also be reset with a command vver the serial port, as described in the Software Reset section.

Temperature

The bq2090 monitors temperature using an internal sensor. The temperature is used to adapt charge/discharge and self-dischargecompensations. Temperature may also be accessed over the serial port. See the Programming the bq2090 section for further details.

Layout Considerations

The bq2090 measures the voltage differential between the SR and Vss pins. Vos (the offset voltage at the SR pin) is greatly affected by PC board layout. For optimal results, the PC board layout should follow the strict rule of a single-point ground return. Sharing high-current ground with small signal ground causes undesirable noise on the small signal nodes. Additionally, in reference to Figure 1:

- The capacitors (C1, C3, and C4) should be placed as close as possible to the SB and Vcc pins, and their paths to Vss should be as short as possible. A high-quality ceramic capacitor of 0.1µf is recommended for Vcc.
- The sense resistor capacitor (C2) should be placed as cloee as possible to the SR pin.
- The sense resistor (R_{11}) should be as close as possible to the bq2090.
- The IC should be close to the cells for the beat temperature measurement.

Gas Gauge Operation

The operational overview diagram in Figure 2 illustrates the operation of the bq2090. The bq2090 accumulates a measure of charge and diecharge currents, as well as an estimation of self-discharge. Charge and discharge currents are temperature-compensated, and charge is rate-compensated. Self-discharge is only temperature-compensated.

The main counter, Remaining Capacity (RM), repreaenta the available battery capacity at any given time. Battery charging increments the RM register, whereas battery discharging and self-discharge decrement the RM register and increment the DCR (Discharge Count Register).

The Discharge-Count Register (DCR) is used to update the Full-Charge Capacity (FCC) register only if a complete battery discharge from full to empty occurs without any partial battery charges. Therefore, the bq2090 adapts ita capacity determination based on the actual conditions of discharge.

The battery's initial capacity is equal to the Design Capacity (DC). Until FCC is updated, RM counts up to, but not beyond, this threshold during subsequent charges.

1. **Full-Charge Capacity** or learned-battery capacity:

   FCC is the last measured discharge capacity of the battery. On initialization (application of Vcc or reset), FCC = DC. During subsequent discharges, the FCC is updated with the latest measured capacity in the *Discharge* Count Register (DCR), representing a discharge from full to below EDV1. A qualified discharge is necessary for a capacity transfer from the DCR to the FCC register. The FCC also serves as the 100% reference threshold used by the relative state-of-charge calculation and display.

2. Design Capacity (DC):

   The DC is the user specified battery capacity and is programmed by using an external E^2PROM. The DC also provides the 100% reference for the absolute display mode.

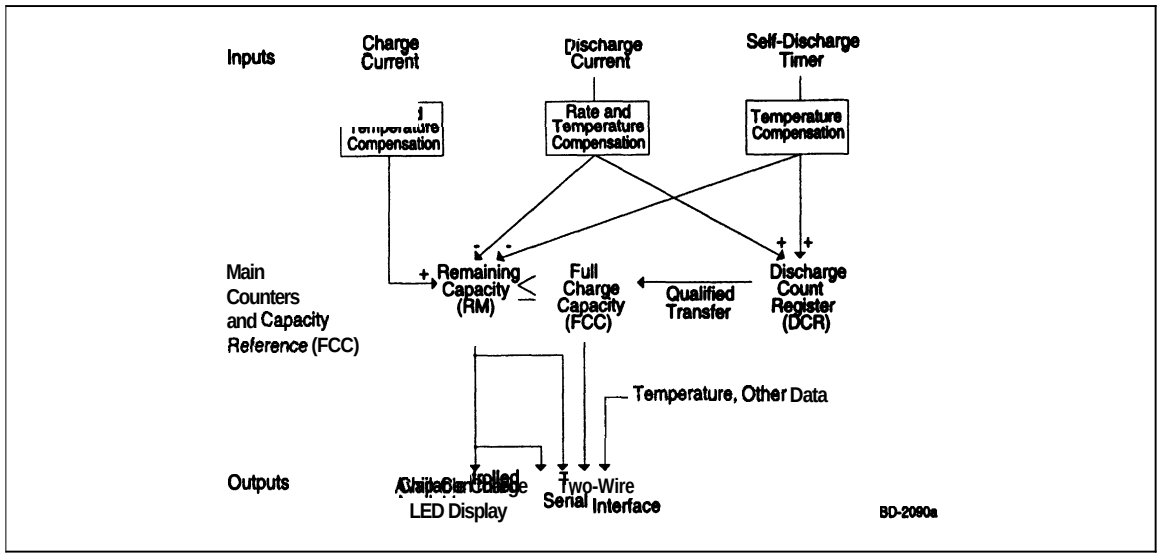


Figure 2. Operational Overview

3. Remaining Capacity **(RM):**

RM counts up during charge to a maximum **value of FCC and down during discharge and self-discharge** to 0. **RM is reset to 0 on initialization and when a valid charge is detected and EDV1=1. To prevent** overstatement of charge during periods of overcharge, RM stops incrementing when RM = FCC.

4. Discharge Count Register (DCR):

The DCR counts up during discharge independent of RM and can continue **increasing** after RM has decremented to 0. Prior to RM = 0 (empty battery), both discharge and self-discharge increment the DCR. After RM = 0, only discharge **increments** the DCR. The DCR resets to 0 when RM = FCC. The DCR does not roll over but stops counting when it reaches **FFFFh.**

The **DCR** value becomes the new **FCC value on the first** charge after a valid diecharge to V_{EDV1} **if:**

- No valid charge initiations **(charges** greater than 10mAh, where $V_{SRO} > V_{SRQ}$) **occurred** during the period between RM = FCC and **EDV1** detected.
- The self-discharge count is not more than 256mAh.

  The temperature is ≥ 273°K when the EDV1 level is reached during discharge.

The valid discharge flag (VDQ) indicates whether the present discharge is valid for FCC update.

Charge Counting

Charge activity is **detected** based on a **positive** voltage on **the** V_{SR} input. If charge activity is detected, the bq2090 **increments RM at a rate proportional to** V_{SRO} **and, if** enabled, activates an LED display. Charge actions **increment the RM after compensation for charge** rate **and temperature.**

The bq2090 determines charge activity **sustained** at a **continuous** rate equivalent **to** $V_{SRO} > V_{SRQ}$. A valid charge equates to sustained charge activity greater than 10 mAh. **Once** a valid charge is detected, charge counting continues until V_{SRO} falls below V_{SRQ}. V_{SRQ} is a programmable threshold as **described** in the Digital Magnitude Filter **section.**

Discharge Counting

All discharge counts where $V_{SRO} < V_{SRD}$ **cause the** RM register to decrement and the DCR to increment. Exceeding the user-programmable discharge display threshold, stored in external E^2PROM, activates the display, if enabled. V_{SRD} is a programmable threshold as described in the Digital Magnitude Filter section.

Self-Discharge Estimation

The **bq2090** continuously decrements RM and **increments DCR for self-discharge based on time and** temperature. The self-diecharge rate is dependent on the battery chemistry. The **bq2090** self-discharge estimation rate is externally programmed in E^2PROM

and can be programmed from 0 to 25% per day at 20°C. This rate doubles every 10°C from 0°C to 70°C.

Count Compensations

The bq2090 determines fast discharge when the discharge rate exceeds the programmed fast discharge rate. Charge activity is compensated for temperature and rate before updating the RM and/or DCR. Discharge rate is compensated for temperature before updating the RM register. Self-discharge estimation is compensated for temperature before updating RM or DCR.

Charge Compensation

Charge efficiency is compensated for rate, temperature, and battery chemistry. For Li-ion chemistry cells, the charge efficiency is unity for all cases. However, the charge efficiency for nickel chemistry cells is adjusted using the following equation:

$$Q_{EFF} = Q_{EB} + 0.125 * \frac{AverageCurrent()}{FullCapacity()}$$

where $Q_{EB} = 0.80$ if $T < 30°C$

$Q_{EB} = 0.75$ if $30°C \le T < 40°C$

$Q_{EB} = 0.60$ if $T \ge 40°C$

and $AverageCurrent() \le FullCapacity()$

$Q_{EFF} = Q_{EB} + 0.125$ if $AverageCurrent() > FullCapacity()$

Remaining Capacity Compensation

The bq2090 adjusts the RM ae a function of temperature. This adjustment accounts for the reduced capacity of the battery at colder temperatures. The following equation is used to adjust RM:

If $T \ge 6°C$

$RemainingCapacity() = NominalAvailableCapacity$

If $T < 5°C$

$RC() = NAC() (1 + TCC * (T - 5°C))$

where T = temperature °C

TCC = 0.016 for Li–Ion cells

TCC = 0.0004 for Ni chemistry cells

Digital Magnitude Filter

The bq2090 has a programmable digital filter to eliminate charge and discharge counting below a set threshold. Table 2 shows typical digital filter settings. The proper digital fiiter setting can be calculated using the following equation.

$$V_{SRD}\,(mV) = -45 / DMF$$

$$V_{SRQ}\,(mV) = -1.25 \cdot V_{SRD}$$

Table 2. Typical Digital Filter Settings

DMF	DMF Hex.	V_{SRD} (mV)	V_{SRQ} (mV)
75	4B	-0.60	0.75
100	64	-0.45	0.56
150 (default)	96	-0.30	0.38
175	AF	-0.26	0.32
200	C8	-0.23	0.28

Error Summary

Capacity Inaccurate

The FCC is susceptible to error on initialization or if no updates occur. On initialization, the FCC value includes the error between the design capacity and the actual capacity. This error is present until a valid discharge occurs and FCC is updated (see the DCR description). The other cause of FCC error is battery wear-out. As the battery ages, the measured capacity must be adjusted to account for changes in actual battery capacity. Periodic discharges from full to empty will minimize errors in FCC.

Current-Sensing Error

Table 3 illustrates the current-sensing error as a function of V_{SR}. A digital filter eliminates charge and discharge counts to the RM register when V_{SRO} is between V_{SRQ} and V_{SRD}.

Display

The bq2090 can directly display capacity information using low-power LEDs. The bq2090 displays the battery charge state in either absolute or relative mode. In relative mode, the battery charge is represented as a percentage of the FCC. Each LED segment represents 25% of the FCC.

In absolute mode, each segment represents a fixed amount of charge, based on the initial design capacity. In absolute mode, each segment represents 25% of the design capacity. As the battery wears out over time, it is possible for the FCC to be below the initial design capacity. In this case, all of the LEDs may not turn on in absolute mode, representing the reduction in the actual battery capacity.

The displayed capacity is compensated for the present battery temperature. The displayed capacity varies as temperature varies, indicating the available charge at the present conditions.

When $\overline{DISP}$ is tied to V_{CC}, the SEG_{1-4} outputs are inactive. When $\overline{DISP}$ is left floating, the display becomes active whenever the bq2090 recognizes a valid charge or if the discharge rate exceeds the programmed fast discharge display threshold. When pulled low, the segment outputs become active immediately for a period of approximately 4 seconds.

The segment outputa are modulated as two banks of three, with segments 1 and 3 alternating with segments 2 and 4. The segment outputa are modulated at approximately 100Hz with each segment bank active for 30% of the period.

SEG_1 blinks at a 4Hz rate whenever V_{SB} has been detected to be below V_{EDV1} ($EDV_1 = 1$), indicating a low-battery condition. V_{SB} below V_{EDVF} ($EDV_F = 1$) disables the display output.

Microregulator

The bq2090 can operate directly from three or four nickel chemistry cells. To facilitate the power rupply requirements of the bq2090, an REF output is provided to regulate an external low-threshold n-FET. A micropower source for the bq2090 can be inexpensively built using the FET and an external resistor; see Figure 1.

Communicating With the bq2090

The bq2090 includes a simple two-pin (SCC and SCD) bidirectional serial data interface. A host processor uses the interface to access various bq2090 registers; see Table 4. This allows battery characteristics to be easily monitored. The open-drain SCD and SCC pine on the bq2090 are pulled up by the host system, or may be connected to V_{SS}, if the serial interface is not wed.

The interface uses a command-based protocol, where the host processor sends the battery address and an eight-bit command byte to the bq2090. The command directs the bq2090 to either store the next data received to a register specified by the command byte or output the data specified by the command byte.

bq2090 Data Protocols

The host system, acting in the role of a Bus master, uses the read word and write word protocols to communicate integer data with the bq2090 (see Figure 3).

Host-to-bq2090 Message Protocol

The Bus Host communicates with the bq2090 using one of three protocols:

- Read word
- Writeword
- Read block

The particular protocol used is a function of the command. The protocols wed are shown in Figure 3.

Table 3. bq2090 Current-Sensing Errors

Symbol	Parameter	Typical	Maximum	Units	Notes
V_{OS}	Offset referred to V_{SR}	± 50	± 150	µV	$\overline{DISP}$ = Vcc.
INL	Integrated non-linearity error	± 2	± 4	%	Add 0.1% per °C above or below 25°C and 1% per volt above or below 4.25V.
INR	Integrated non-repeatability error	± 1	± 2	%	Measurement repeatability given similar operating conditions.

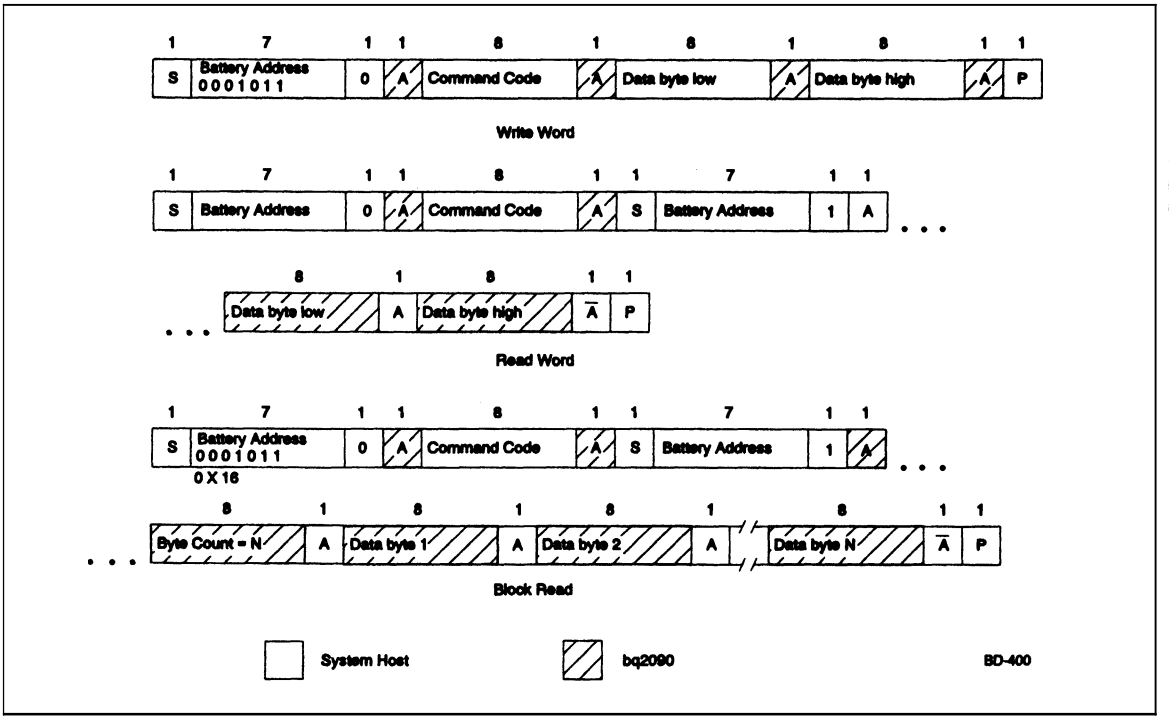


Figure 3. Host Communication Protocols

Host-to-bq2090 Messages (see Table 4)

Temperature() (0x08)

This read-only word returns the cell-pack's internal temperature (0.1°K).

Output: unsigned integer. Returns cell temperature in tenths of degrees Kelvin increments

Units: 0.1°K

Range: 0 to +500.0°K

Granularity: 0.5°K or better

Accuracy: ±3°K after calibration

Voltage() (0x09)

This read-only word returns the cell-pack voltage (mV).

Output: unsigned integer. Returns battery terminal voltage in mV

Units: mv

Range: 0 to 65,535 mV

Granularity: 0.2% of design voltage

Accuracy: ±1% of design voltage after calibration

Current() (0x0a)

This read-only word returns the current through the battery's terminals (mA).

Output: signed integer. Returns the charge/discharge rate in mA, where positive is for charge and negative is for-didurge

Units: mA

Range: 0 to 32,767 mA for charge or 0 to -32,768 mA for discharge

Granularity: 0.2% of the DesignCapacity() or better

Accuracy: ±1% of the Design Capacity after calibration

Table 4. bq2090 Register Functions

Function	Code	Access	Units	Defaults[1]
Temperature	0x08	read	0.1°K	
Voltage	0x09	read	mV	
Current	0x0a	read	mA	0000h
AverageCurrent	0x0b	read	mA	0000h
MaxError	0x0c	read	percent	2
RelativeStateOfCharge	0x0d	read	percent	0000h
AbsoluteStateOfCharge	0x0e	read	percent	0000h
RemainingCapacity	0x0f	read	mAh	0000h
FullChargeCapacity	0x10	read	mAh	E^2
RunTimeToEmpty	0x11	read	minutes	
AverageTimeToEmpty	0x12	read	minutes	
AverageTimeToFull	0x13	read	minutes	
Error Codes	0x16	read	number	0000h
CycleCount	0x17	read	count	0000h
DesignCapacity	0x18	read	mAh	E^2
DesignVoltage	0x19	read	mV	E^2
ManufactureDate	0x1b	read	unsigned int	E^2
SerialNumber	0x1c	read	number	E^2
Reserved	0x1d - Oxlf			
ManufacturerName	0x20	read	string	E^2
DeviceName	0x21	read	string	E^2
DeviceChemistry	0x22	read	string	E^2
ManufacturerData	0x23	read		E^2
FLAGS1 and FLAGS2	0x2c	read	unsigned int.	E^2

Note: 1. Defaults after reset or power-up.

AverageCurrent() (0x0b)

This read-only word returns a rolling average of the current through the battery's terminals. The AverageCurrent() function returns meaningful values after the battery's first minute of operation.

Output: signed integer. Returns the charge/discharge rate in mA, where positive is for charge and negative is for discharge

Units: mA

Range: 0 to 32,767 mA for charge or 0 to -32,768 mA for discharge

Granularity: 0.2% of the DesignCapacity() or better

Accuracy: ±1% of the Design Capacity after calibration

RelativeStateOfCharge() (0x0d)

This read-only word returns the predicted remaining battery capacity expressed as a percentage of FullChargeCapacity() (%). RelativeStateOfCharge() is only valid for battery capacities less than 5,000mAh.

Output: unsigned integer. Returns the percent of remaining capacity

units: %

Range: 0 to 100%

Granularity: 1% or better

AbsoluteStateOfCharge() (0x0e)

This read-only word returns the predicted remaining battery capacity expressed as a percentage of DesignCapacity() (%). Note that AbsoluteStateOfCharge can return values greater than 100%. Absolute StateOfCharge is only valid for battery capacities less than 5,000mAh.

Output: unsigned integer. Returns the percent of remaining capacity

units: %

Range: 0 to 65,535 %

Granularity: 1% or better

Accuracy: ±MaxError()

RemainingCapacity() (0x0f)

This read-only word returns the predicted remaining battery capacity. The RemainingCapacity() value is expressed in mAh.

Output: unsigned integer. Returns the estimated remaining capacity in mAh

Unite: mAh

Range: 0 to 65,535 mAh

Granularity: 0.2% of DesignCapacity() or better

FullChargeCapacity() (0x10)

This read-only word returns the predicted pack capacity when it is fully charged. FullChargeCapacity() defaults to the value programmed in the external E²PROM until a new pack capacity is learned.

Output: unsigned integer. Returns the estimated full *charge* capacity in mAh

Unite: mAh

Range: 0 to 65,535 mAh

Granularity 0.296 of design capacity or better

RunTimeToEmpty() (0x11)

This read-only word returns the predicted remaining battery life at the present rate of discharge (minutes). The RunTimeToEmpty() value is calculated based on Current().

Output: unsigned integer, Returns the minutes of operation left

Unite: minutes

Range: 0 to 65,534 minutes

Granularity 2 minutes or better

Invalid data indication: 65.535 indicates battery is being *charged*

AverageTimeToEmpty() (0x12)

This read-only word returns the predicted remaining battery life at the present average discharge rate (minutes). The AverageTimeToEmpty is calculated based on AverageCurrent().

Output: unsigned integer, Returns the minutes of operation left

Units: minutes

Range: 0 to 65,534 minutes

Granularity: 2 minutes or better

Invalid data indication: 65,535 indicates battery is being charged

AverageTimeToFull() (0x13)

This read-only word returns the predicted time until the Smart Battery reaches full charge at the present average charge rate (minutes). The AverageTimeToFull() is calculated based on AverageCurrent().

Output: unsigned integer. Returns the remaining time in minutes

Units: minutes

Range: 0 to 65,534 minutes

Granularity: 2 minutes or better

Invalid data indication: 65,535 indicates battery is not being charged

Battery Status() (0x16)

This read-only word returns the battery statue word.

Output: unsigned integer. Returns the status register with alarm conditions bitmapped as shown in Table 5.

Some of the Battery Status() flags (Remaining_Capacity_Alarm and Remaining–Time–Alarm) are calculated based on current. See Table 8 for definitions.

Table 5. Status Register

Alarm Bits	
0x8000	Not Meaningful
0x4000	Not Meaningful
0x2000	Not Meaningful
0x1000	Over_Temp_Alarm
0x0800	Terminate_Discharge_Alarm
0x0400	Reserved
0x0200	Remaining_Capacity_Alarm
0x0100	Remaining_Time_Alarm
Status Bits	
0x0080	Initialized
0x0040	Discharging
0x0020	Not Meaningful
0x0010	Fully Discharged
Error Code	
0x0000-0x000f	Reserved for error codes

CycleCount() (0x17)

This mad-only word returns the number of charge/discharge cycles the battery has *experienced* A charge/discharge cycle starts from a base value equivalent to the battery's state-of-charge, upon completion of a charge cycle. The bq2090 increments the cycle counter *during* the current charge cycle, if the battery has been discharged to below 85% of the state-of-charge at the end of the last charge cycle. A discharge > 0.5% is needed, preventing false reporting of small charge/discharge cycles.

Output: unsigned integer. Returns the count of charge/discharge cycles the battery has experienced

Units: cycles

Range: 0 to 65,535 cycles; 65,535 indicates battery has experienced 65,535 or more cycles

Granularity: 1 cycle

DesignCapacity() (0x18)

This read-only word returns the theoretical capacity of a new pack. The DesignCapacity() value is expressed in mAh at the nominal discharge rate.

Output: unsigned integer. Returns the battery capacity in mAh

unite: mAh

Range: 0 to 65,536 mAh

DesignVoltage() (0x19)

This read-only word returns the theoretical voltage of a new pack (mV).

Output: unsigned integer. Returns the battery's normal terminal voltage in mV

Units: mV

Range: 0 to 65,535 mV

ManufactureDate() (0x1b)

This read-only word returns the date the cell was manufactured in a packed integer word. The date is packed as follows: (year - 1980), month, day.

Field	Bits Used	Formal	Allowable Vdue
Day	0–4	5-bit binary value	1–31 (corresponds to date)
Month	5–8	4bit binary value	1–12 (corresponds to month number)
Year	9–15	7-bit binary value	0 • 127 (corresponds to year biased by 1980)

SerialNumber() (Oxlc)

This read-only word returns a serial number. This number, when combined with the ManufacturerName(), the DeviceName(), and the ManufactureDate(), uniquely identifies the battery.

Output: unsigned integer

ManufacturerName() (0x20)

This read-only string returns a character string where the first byte is the number of characters available. The maximum number of characters is 15. The character string contains the battery manufacturer's name. For example, "Benchmarq" identifies the battery pack manufacturer as Benchmarq.

Output: string or ASCII character string

DeviceName() (0x21)

This read-only string returns a character string where the first byte is the number of characters available. The maximum number of characters is 15. The 15-byte character string contains the battery's name. For example, a DeviceName() of "bq2090" indicates that the battery is a model bq2090.

Output: string or ASCII character string

DeviceChemistry() (0x22)

This read-only string returns a character string where the first byte is the number of characters available. The maximum number of characters is 15. The 15-byte character string contains the battery's chemistry. For example, If the DeviceChemistry() function returns "NiMH," the battery pack contains nickel-metal hydride cells.

Output: string or ASCII character string

FLAGS1&2() (0x2c)

This read-only register returns an unsigned integer representing the internal status registers of the bq2090. The MSB represents FLAGS2, and the LSB represents FLAGS1. See Table 6 for the bit description for FLAGS1&2.

FLAGS2

The Display *Mode* flag (DMODE), Bit 7, determines whether the bq2090 displays Relative or Absolute capacity.

The DMODE values are:

FLAGS2 Bits							
7	6	5	4	3	2	1	0
DMODE	-	-	-	-	-	-	-

Where DMODE is:

0 Selects Absolute display

1 Selects Relative display

The *Fast* Discharge flag (FDQ), Bit 6, is set when the discharge rate exceeds the programmed level and is cleared when the rate drops below this level.

The FDQ values are:

FLAGS2 Bits							
7	6	5	4	3	2	1	0
-	FDQ	-	-	-	-	-	-

Table 6. Bit Description for FLAGS1 and FLAGS2

	(MSB) 7	6	5	4	3	2	1	0 (LSB)
FLAGS2	DMODE	FDQ	CHM			-	LTF	
FLAGS1	-		VQ	WRINH	VDQ	SEDV	EDV1	EDVF

- = Reserved

Where **FDQ** is:

0 **AverageCurrent < Discharge** display **threshold**

1 **AverageCurrent >** Discharge **display threshold**

The ***Chemistry*** flag **(CHM),** Bit 5, **selects Li-Ion** or Nickel compensation **factors.**

The **CHM** values are:

FLAGS2 Bits							
7	6	5	4	3	2	1	0
-	-	CHM	-	-	-	-	-

Where **CHM** is:

0 Selects Nickel

1 Selects Li-Ion

Bit 4 is reserved and should be initialized to zero for proper bq2090 operation.

Bit 3 is reserved.

Bit 2 **is** reserved.

The ***Low-Tempemturn Fault*** flag **(LTF),** Bit 1, is set when **temperature<0°C** and cleared when **temperature>5°C.**

The LTF values are:

FLAGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	LTF	-

Where LTF **is:**

0 Temperature **>5°C**

1 Temperature **<0°C**

Bit 0 is **reserved.**

FLAGS1

Bit 7 is reaewed.

Bit 6 is reaerved.

The Valid ***Charge*** flag (VQ), Bit 5, is set when $V_{SRO} \geq V_{SRQ}$ and **10mAh** of charge has accumulated. This bit is cleared during a discharge and when $V_{SRO} \leq V_{SRQ}$.

The VQ values are:

FLAGS1 Bits							
7	6	5	4	3	2	1	0
-	-	VQ	-	-	-	-	-

Where VQ is:

0 $V_{SRO} \leq V_{SRQ}$

1 VSRO ≥ VSRQ and **10mAh** of charge has accumulated

The *Write* Inhibit **flag** (WRINH), Bit 4, allows or inhibits writes to all **registers.**

The WRINH valuea are:

FLAGS1 Bits							
7	6	5	4	3	2	1	0
		-	WRINH	-	-	-	-

Where WRINH is:

0 Allows writes to **all registers**

1 **Inhibits** all writes and secures the **bq2090 from invalid/undesired** writes.

WRINH may **be** cleared by writing Manufacturer Access()=**0xXX37** and forcing the SB pin to **ground.**

The Valid Discharge **flag** (VDQ), Bit 3, is set when a valid discharge is occurring (discharge cycle valid for learning new full charge capacity) and cleared if a partial charge is detected, EDVl is asserted when **T<0°C,** or self-discharge accounts for more than 256mAh of the **discharge.**

The VDQ values are:

FLAGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	VDQ	-	-	-

Where **VDQ** is:

0 **Self-discharge** is greater than 256mAh, EDVl = 1 when **T<0°C** or VQ = 1

1 On first discharge after **RM=FCC**

The *Stop EDV* flag (SEDV), Bit 2, is set when the discharge current>3A and cleared when the discharge current falls below 1.5A.

The SEDV values are:

FLAGS1 Bits							
7	6	5	4	3	2	1	0
				-	SEDV	-	-

Where SEDV is:

0 Current < 1.5A

1 Current > 3A

The First *End-of-Discharge Voltage* flag (EDV1), Bit 1, is set when Voltage()<EDV1=1 if SEDV=0 and cleared when VQ=1 and Voltage()>EDV1.

The EDV1 values are:

FLAGS1 Bits							
7	6	5	4	3	2	1	0
					-	EDV1	-

Where EDV1 is:

0 VQ = 1 and Voltage ()> EDV1

1 Voltage()< EDV1 and SEDV = 0

The Final End-of-Discharge Voltage flag (EDVF). Bit 0, is set when Voltage()<EDVF=1 if SEDV=0 and cleared when VQ=1 and Voltage()>EDVF.

The EDVF values are:

FLAGS1 Bits							
7	6	5	4	3	2	1	0
						-	EDVF

Where EDVF is:

0 VQ = 1 and Voltage > EDVF

1 Voltage < EDVF and SEDV = 0

ManufacturerData() (0x23)

This read-only string allows access to an up to 15-byte manufacturer data string.

Output: block data—data whose meaning is assigned by the Smart Battery's manufacturer

2

Software Reset

The bq2090 can be reset over the serial port by confirming that the WRINH bit is set to zero in FLAGS1, writing MaxError() (0x0c) to any value other than 2, and writing the reset register (0x44) to 8000, causing the bq2090 to reinitialize and read the default values from the external E^{2}PROM. See the WRINH bit description if WRINH is set to 1.

Error Codes and Status Bits

Error codes and status bite are listed in Table 7 and Table 8, respectively,

bq2090 Critical Messages

Whenever the bq2090 detects a critical condition, it becomes a bus master and sends Alarm Warning() messages to the Bus Host, as appropriate, notifying it of the critical condition(s). The message sent by the Alarm Warning() function is similar to the message returned by the BatteryStatus() function. The bq2090 continues broadcasting the AlarmWarning() messages at 8-second intervals until the critical condition(s) has been corrected.

AlarmWarning() (0x16)

The bq2090, acting as a bus master device to the Bus Host, sends this message to notify it that one or more alarm conditions exist. Alarm Warning() is repeated at 8-second intervals until the condition(s) causing the alarm has been corrected.

Table 7. Error Codes (BatteryStatus() (0x16))

Error	Code	Access	Description
OK	0x0000	read/write	bq2090 processed the function code without detecting any errors
Busy	0x0001	read/write	bq2090 is unable to process the function code at this time
NotReady	0x0002	read/write	bq2090 cannot read or write the data at this time–try again later
UnsupportedCommand	0x0003	read/write	bq2090 does not support the requested function code
AccessDenied	0x0004	write	bq2090 detected an attempt to write to a read-only function code
Overflow/Underflow	0x0005	read/write	bq2090 detected a data overflow or underflow
BadSize	0x0006	write	bq2090 detected an attempt to write to a function code with an incorrect size data block
UnknownError	0x0007	read/write	bq2090 detected an unidentifiable error

Note: Reading the bq2090 after an error clears the error code.

Table 8. Status Bits

Alarm Bits		
BR Name	**Set When:**	**Rent When:**
OVER_TEMP_ALARM	bq2090 detects that its internal temperature is greater than 60°C	Internal temperature falls back into the acceptable range
TERMINATE_DISCHARGE_ALARM	bq2090 determines that it has supplied all the charge that it can without being damaged (that is, continued use will result in permanent capacity loss to the battery)	Battery reaches a state of charge sufficient for it to once again safely supply power
REMAINING_CAPACITY_ALARM	bq2090 detects that the RemainingCapacity() is lees than that set by the RemainingCapacity() function	Either the value set by the RemainingCapacityAlarm() function is lower than the Remaining Capacity() or the RemainingCapacity() is increased by charging
REMAINING_TIME_ALARM	bq2090 detects that the eetimated remaining time at the preeent discharge rate is less than that set by the RemainingTimeAlarm() function	Either the value set by the RemainingTimeAlarm() function is lower than the AverageTimeToEmpty() or the AverageTimeToEmpty() is increased by charging
Status Bits		
Bit Name	**Set When:**	**Reset When:**
INITIALIZED	bq2090 is set when the bq2090 has reached a full or empty state	Battery detects that power-on or user-initiated reset has occurred
DISCHARGING	bq2090 determines that it is not being charged	Battery detects that it is being charged
FULLY_DISCHARGED	bq2090 determines that it has supplied all the charge that it can without being damaged (that is, continued use will result in permanent capacity loss to the battery)	RelativeStateOfCharge() is greater than or equal to 20%

Programming the bq2090

The bq2090 requires the proper programming of an external E^2PROM for proper device operation. Each module can be calibrated for the greatest accuracy, or general "default" values can be used. A programming kit (interface board, software, and cable) for an IBM-compatible PC is available from Benchmarq. Please contact Benchmarq for further detail

The bq2090 uses a 24C01 or equivalent serial E^2PROM for storing the various initial values, calibration data, and string information. Table 1 outlines the parameters and addresses for this information. Tables 9 and 10 detail the various register contents and show an example program value for an 1800mAh NiMH battery pack, using a 50mΩ sense resistor.

Table 9. Example Register Contents

Description	E^2PROM Address		E^2PROM Hex Contents		Example Values	Notes
	Low Byte	High Byte	Low Byte	High Byte		
Design Capacity	0x00	0x01	08	07	1800mAh	This sets the initial full charge battery capacity stored in FCC. FCC is updated with the actual full to empty discharge capacity after a valid discharge from RM = FCC to Voltage() = EDV1.
Initial Battery Voltage	*0x02*	0x03	30	2a	10800mV	This register is used to adjust the battery voltage. Comparing the valuea read from the bq2090 to two known input voltages allows the bq2090 to calibrate the battery voltage to within 1%. This action adjusts for errors in the resistor-dividers used for the SB input and bq2090 offset errors.
Reserved	0x04	0x05	ff	ff		This register function is reserved.
Reserved	0x06	0x07	ff	ff		This register function is reserved.
Remaining Capacity Alarm	0x08	0x09	b4	*00*	180mAh	This value represents the low capacity alarm value.
FLAGS1	0x0a		10			This enables writes to all registers and should be set to 10h prior to pack shipment to inhibit undesirable writes to the bq2090.
FLAGS2	0x0b		80		Li-Ion = a0h NiMH = 80h	See FLAGS2 register for the bit description and the proper value for programming FLAGS2. Selects relative display mode and Lithium Ion compensation factors.
Current Measurement Gain[1]	0x0c	0x0d	77	01	18.75/.05	The current gain measurement and current integration gain are related and defined for the bq2090 current measurement. 0x0c = 18.75/sense resistor value in ohms.
EDV1	0x0e	0x0f	16	db	9450mV (1.05V/cell)	The value programmed is the two's complement of the threshold voltage in mV.
EDVF	0x10	0x11	d8	dc	9000mV (1.0V/cell)	The value programmed is the two's complement of the threshold voltage in mV.

Note: 1. Can be adjusted to calibrate the battery pack.

Table 9 Example Register (Continued)

Description	E²PROM Address		E²PROM Hex Contents		Example Values	Notes
	Low Byte	High Byte	Low Byte	High Byte		
Temperature Offset[1]	0x12	0x13	28	15	541.6	The default value is 540.1K.
Self-Discharge Rate	0x14		f0		.15C	This packed field is the 2s complement of ((RM/4)/(RM/x)) where RM/x is the desired self-discharge rate per day at room temperature.
Digital Filter	0x15		fa		.18mV	This field is used to set the digital magnitude filter as described in Table 2.
Current Integration Gain	Ox16	0x17	40	00	3.2/.05	This field represents the following: 3.2/sense resistor in ohms. It is used by the bq2090 to scale the measured voltage values on the SR pin in mA and mAh. This register also compensates for variations in the reported sense resistor value.
Discharge Display Threshold	0x18		fb		Ifd = C/10 = 180mA 45/(180 * .05) = 5 2s(5) = fb	This packed field is the 2's complement of the desired voltage on SR which activates the LED display. fdqthr = 2's(-45/(Ifd*Rs)) where Ifd is the desired fast discharge current and Rs is the sense resistor value in ohms. This is only valid when DISP = Z.
Battery Voltage Offset[1]	0x19		00		0mV	This value is used to adjust the voltage offset measured at the SB input.
Voltage Gain[1]	0x1a	0x1b	09	05	9.02	Voltage gain is packed as two units. For example, R5/R2 = 9.09 would be stored as: whole number stored in 0x1a (=09h) and the decimal component stored in 0x1b as 256 * 0.02 = 05.
Reserved	0x1c 0x1e	Oxld 0x1f	ff 00	ff 00		This register is reserved.
Design Voltage	0x32	0x33	30	2a	10800mV	This is nominal battery pack voltage.
Specification Information	0x34	0x35	00	00		This is the default value for this register.
Manufacturer Date	0x36	0x37	a1	20	May 1,1996 = 8353	Packed per the ManufactureDate() description, which represents May 1,1996 in this example.
Serial Number	0x38	0x39	12	27	10002	This contains the pack serial number, if desired.

Note: 1. Can be adjusted to calibrate the battery pack.

Table 10. Example Program Values

String Description	Address	0x ?0	Ox ?1	Ox ?2	Ox ?3	Ox ?4	0x ?5	0x ?6	0x ?7	0x ?8	0x ?9-?f
Reserved	0x3a-0x3f	00	00	00	00	00	00	00	00	00	00
Manufacturer's Name	0x40-0x4f	09	42 B	45 E	4e N	43 C	48 H	4d M	41 A	52 R	51 Q
Device Name	0x50-0x5f	08	42 B	51 Q	32 2	30 0	39 9	30 0	41 A	33 3	00-00
Chemistry	0x60-0x6f	04	4e N	69 I	4d M	48 H	00	00	00	00	00-00
Manufacturer's Data	0x70-0x7f	04	44 D	52 R	31 1	35 5	00	00	00	00	00-00

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to Vss	-0.3	+7.0	V	
All other pins	Relative to Vss	-0.3	+7.0	V	
REF	Relative to Vss	-0.3	+8.5	V	Current limited by R1 (see Figure 1)
V_{SR}	Relative to Vss	-0.3	+7.0	V	Minimum 100Ω aeries resistor should be used to protect SR in case of a shorted battery (see the bq2090 application note for details).
T_{OPR}	Operating temperature	0	+70	°C	Commercial

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage Thresholds (TA = TOPR; V = 3.0 to 5.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
E_{VSB}	Battery voltage error relative to SB	-50mV		50mV	V	See note

Note: The accuracy of the voltage measurement may be improved by adjusting the battery voltage offset and gain, stored in external E^2PROM. For proper operation, V_{CC} ahould be 1.5V greater than V_{SB}.

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	3.0	4.25	5.5	V	V_{CC} excursion from < 2.0V to ≥ 3.0V initializes the unit.
V_{REF}	Reference at 25°C	5.7	6.0	6.3	V	I_{REF} = 5µA
	Reference at -40°C to +85°C	4.5		7.5	V	I_{REF} = 5µA
R_{REF}	Reference input impedance	2.0	5.0		Ma	V_{REF} = 3V
I_{CC}	Normal operation		90	135	µA	V_{CC} = 3.0V
			120	180	µA	V_{CC} = 4.25V
			170	250	µA	V_{CC} = 5.5V
V_{SB}	Battery input	0		V_{CC}	V	
R_{SBmax}	SB input impedance	10			MΩ	0 < V_{SB} < V_{CC}
I_{DISP}	$\overline{DISP}$ input leakage			5	µA	V_{DISP} = V_{SS}
I_{LVOUT}	Vow output leakage	-0.2		0.2	µA	E^2PROM off
V_{SR}	Sense resistor input	-0.3		2.0	V	V_{SR} < V_{SS} = discharge; V_{SR} > V_{SS} = charge
R_{SR}	SR input impedance	10			Ma	-200mV < V_{SR} < V_{CC}
V_{IH}	Logic input high	1.4		5.5	V	SCL, SDA, SCC, SCD
V_{IL}	Logic input low	-0.5		0.6V	V	SCL, SDA, SCC, SCD
V_{OL}	Data, clock output low			0.4	V	I_{OL}=350µA, SDA, SCD
I_{OL}	Sink current	100		350	µA	V_{OL}≤0.4V, SDA, SCD
V_{OLSL}	SEG_X output low, low V_{CC}		0.1		V	V_{CC} = 3V, I_{OLS} ≤ 1.75mA SEG_1–SEG_4
V_{OLSH}	SEG_X output low, high V_{CC}		0.4		V	V_{CC} = 5.5V, I_{OLS} ≤ 11.0mA SEG_1–SEG_4
V_{OHVL}	V_{OUT} output, low V_{CC}	V_{CC} - 0.3	-		V	V_{CC} = 3V, I_{VOUT} = -5.25mA
V_{OHVH}	V_{OUT} output, high V_{CC}	V_{CC} - 0.6	-		V	V_{CC} = 5.5V, I_{VOUT} = -33.0mA
I_{VOUT}	Vow source current	-33			mA	At V_{OHVH} = V_{CC} - 0.6V
I_{OLS}	SEG_X sink current			11.0	mA	At V_{OLSH} = 0.4V

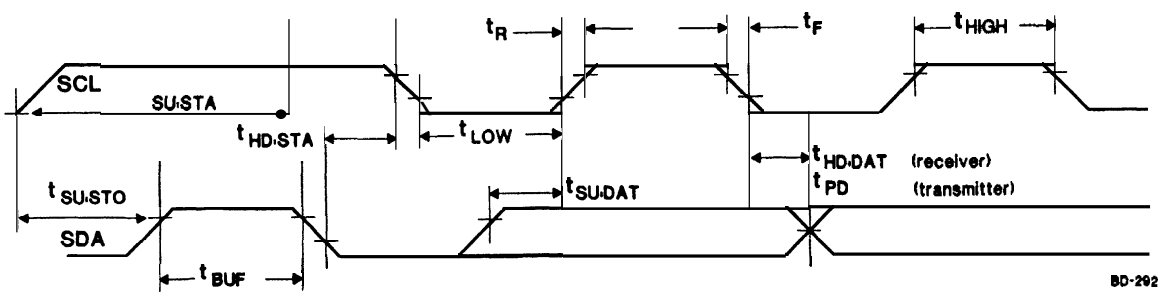
Note: All voltages relative to Vss.

AC Specifications

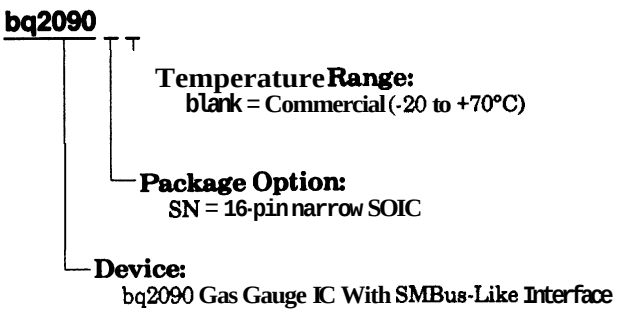
Symbol	Parameter	Min	Max	Units	Notes
F_{SMB}	SMBus operating frequency	10	100	KHz	
T_{BUF}	Bus free time between stop and start condition	4.7			
$T_{HD:STA}$	Hold time after (repeated) start condition	4.0		µs	
$T_{SU:STA}$	Repeated start condition setup time	250		ns	SCD
		4.7		µs	External Memory
$T_{SU:STO}$	Stop condition setup time	4.0		µs	
$T_{HD:DAT}$	Data hold time	0		ns	
$T_{SU:DAT}$	Data setup time	250	40	ns	
T_{EXT1}	Data buffering time addresses 0x00-0x18 per character		40	ms	
T_{EXT2}	String buffering time addresses 0x19-0x23 per character		15	me	40 ms for first character
T_{PD}	Data output delay time	300	3500	ns	External memory only. See Note.
T_{LOW}	Clock low period	4.7		µs	
T_{HIGH}	Clock high period	4.0		µs	
T_F	Clock/Data fall time		300	ns	
T_R	Clock/data rise time		1000	ns	

Note: The external memory must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the fallingedge of SCL to avoid unintended generation of START or STOP conditions.

Bus Timing Data



Ordering Information



Notes

BENCHMARQ

Preliminary **bq2091**

Gas Gauge IC With SMBus-Like Interface

Features

- Provides conservative and repeatable measurement of available charge in NiCd, NiMH, and Li-Ion rechargeable batteries
- Supports SBData charge control commands for Li-Ion, NiMH, and NiCd chemistries
- Designed for battery pack integration
  - 120µA typical operating current
  - Small size enables implementations in as little as ¾ *square* inch of PCB
- Two-wire SMBus-like interface
- Measurements compensated for current and temperature
- Programmable self-discharge and charge compensation
- 16-pin narrow SOIC

General Description

The **bq2091** Gas Gauge IC with **SMBus-Like** Interface is intended for battery-pack *or* in-system installation to maintain an accurate record of available battery charge. The **bq2091** directly supports capacity monitoring for NiCd, NiMH, and Li-Ion battery chemistries.

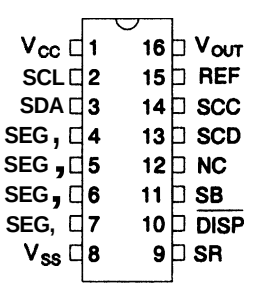
The **bq2091** uses the **SMBus** protocol that supports many of the Smart Battery Data (SBData) commands. The **bq2091** also supports SBData charge control. Battery state-of-charge, capacity remaining, remaining time and chemistry *are* available over the serial link. Battery-charge state can be directly indicated using a four-segment LED display to graphically depict battery full-to-empty in 25% increments.

The **bq2091** estimates battery self-discharge based on an internal timer and temperature sensor and user programmable rate information stored in external E^2PROM. The **bq2091** also automatically recalibrates, or "learns" battery capacity in the full course of a discharge cycle from full to empty.

The **bq2091** may operate directly from three or four nickel chemistry cells. With the REF output and an external transistor, a simple, inexpensive regulator can be built to provide Vcc for other battery cell configurations.

An external E^2PROM is used to program initial values into the **bq2091** and is necessary for proper operation.

Pin Connections



16-Pin Narrow SOIC

PN-110

Pin Names

V_{OUT}	E^2PROM supply output	SB	Battery sense input
SEG_1	LED segment 1	$\overline{DISP}$	Display control input
SEG_2	LED segment 2	SR	Sense resistor input
SEG_3	LED segment 3	SCC	Serial communication clock
SEG_4	LED segment 4	SCD	Serial communication data input/output
SCL	Serial memory clock		
SDA	Serial memory data	V_{CC}	3.0–5.5V
REF	Voltage reference output	V_{SS}	System ground

Pin Descriptions

SEG_1–SEG_4 **LED display segment outputs**

Each output may activate an external LED to sink the current sourced from V_{CC}.

SCC **Serial communication clock**

This open-drain bidirectional pin is used to clock the data transfer to and from the bq2091.

SCD **Serial communication data**

This open-drain bidirectional pin is used to transfer address and data to and from the bq2091.

SCL **Serial memory clock**

This output is used to clock the data transfer between the bq2091 and the external non-volatile configuration memory.

SDA **Serial memory data and address**

This bi-directional pin is used to transfer address and data to and from the bq2091 and the external configuration memory.

NC **No connect**

V_{OUT} **Supply output**

This output supplies power to the external E^2PROM configuration memory.

SR **Sense resistor input**

The voltage drop (V_{SR}) across pins SR and V_{SS} is monitored and integrated over time to interpret charge and discharge activity. The SR input is connected to the sense resistor and the negative terminal of the battery. $V_{SR} < V_{SS}$ indicates discharge, and $V_{SR} > V_{SS}$ indicates charge. The effective voltage drop, V_{SRO}, as seen by the bq2091 is $V_{SR} + V_{OS}$ (see Table 3 on page 8).

$\overline{DISP}$ **Display control input**

$\overline{DISP}$ high disables the LED display. $\overline{DISP}$ floating allows the LED display to be active during charge if the rate is greater than 100mA. DISP low activates the display.

SB **Secondary battery input**

This input monitors the cell pack voltage as a single-cell potential through a high-impedance resistor divider network. The cell pack voltage is reported in the SBD register function Voltage0(0x09) and is compared to end-of-discharge voltage and charging voltage parameters.

REF **Reference output for regulator**

REF provides a reference output for an optional micro-regulator.

V_{CC} **Supply voltage input**

V_{SS} **Ground**

Functional Description

General Operation

The bq2091 determines battery capacity by monitoring the amount of charge input to or removed from a rechargeable battery. The bq2091 measures discharge and charge currents, estimates self-discharge and monitors the battery for low-battery voltage thresholds. The charge measurement is made by monitoring the voltage across a small-value series sense resistor between the battery's negative terminal and ground. The available battery charge is determined by monitoring this voltage over time and correcting the measurement for the environmental and operating conditions.

Figure 1 shows a typical battery pack application of the bq2091 using the LED capacity display, the aerial port, and an external E^{2}PROM for battery pack programming information. The bq2091 muet be configured and calibrated for the battery-specific information to ensure proper operation. Table 1 outlines the externally programmable functions available in the bq2091. Refer to the Programming the bq2091 section for further details.

An internal temperature sensor eliminates the need for an external thermistor—reducing cost and components. An internal, temperature-compensated time-base eliminates the need for an external resonator, further reducing cost and components. The entire circuit in Figure 1 can occupy less than ¾ square inch of board space.

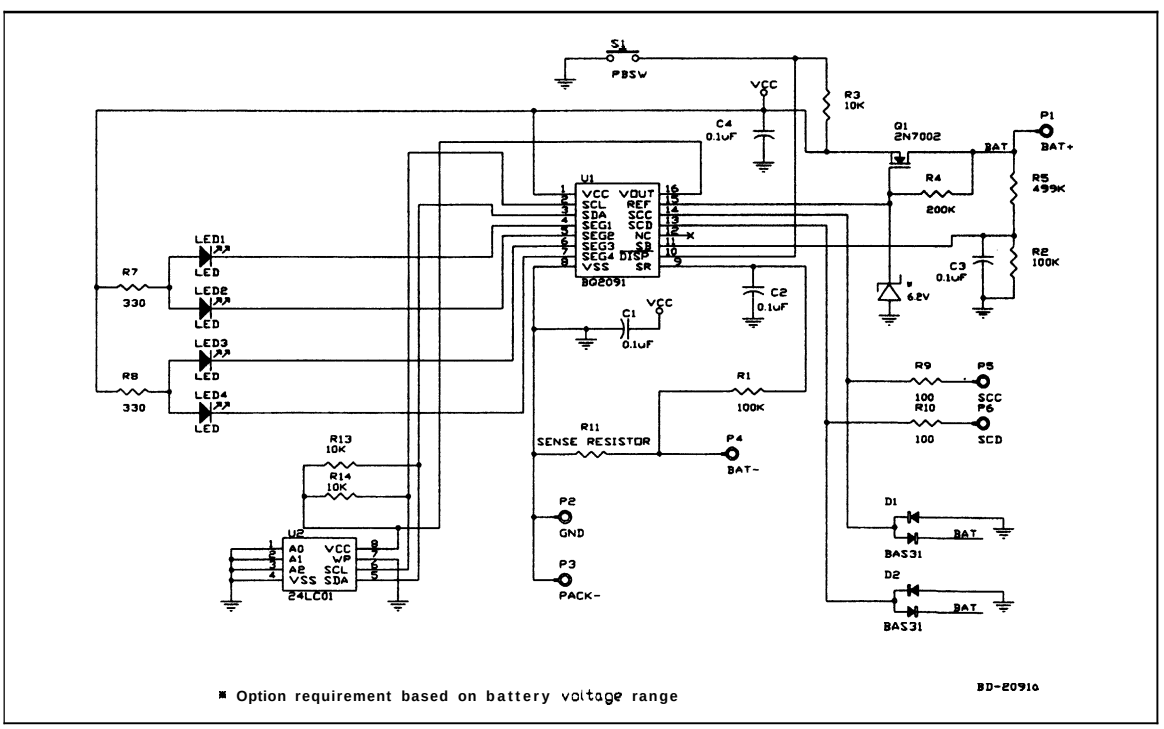


Figure 1. Battery Pack Application Diagram—LED Display

Table 1. Configuration Memory Programming Values

Parameter Name	Address	Length	Unb
Design capacity	0x00/0x01	16 bite: low byte, high byte	mAh
Initial battery voltage	0x02/0x03	16 bite: low byte, high byte	mV
Fast charging current	0x04/0x05	16 bite: low byte, high byte	mA
Fast charging voltage	0x06/0x07	16 bit: low byte, high byte	mV
Remaining capacity alarm	0x08/0x09	16 bite: low byte, high byte	mAh
FLAGS1	0x0a	8 bits	N/A
FLAGS2	0x0b	8 bite	N/A
Current measurement gain	0x0c/0x0d	16 bits: low byte, high byte	N/A
EDV_1	0x0e/0x0f	16 bits: low byte, high byte	mV
EDV_F	0x10/0x11	16 bits: low byte, high byte	mV
Temperature offset	0x12	8 bite	0.1°K
Maximum charge temperature/ΔT/Δt	0x13	8 bits	°C
Self-discharge rate	0x14	8 bits	N/A
Digital filter	0x15	8 bits	mV
Current integration gain	0x16/0x17	16 bits: low byte, high byte	N/A
Full charge percentage	0x18	8 bits	N/A
Charge compensation	0x19	8 bite	N/A
Battery voltage offset	0x1a	8 bits	mV
Battery voltage gain	0x1b/0x1c	16 bits: high byte, low byte	N/A
Serial number	0x1d/0x1e	16 bite: low byte, high byte	N/A
Charge cycle count	0x1f/0x20	16 bite: low byte, high byte	N/A
Maintenance charge current	0x22/0x23	16 bite: low byte, high byte	mA
Reserved	0x24/0x31	–	–
Design voltage	0x32/0x33	16 bits: low byte, high byte	mV
Specification information	0x34/0x35	16 bits: low byte, high byte	N/A
Manufacturer date	0x36/0x37	16 bits: low byte, high byte	N/A
Reserved	0x38/0x3f	–	–
Manufacturer name	0x40/0x4f	8 + 120 bits	N/A
Device name	0x50/0x5f	8 + 120 bits	N/A
Chemistry	0x60/0x6f	8 + 120 bite	N/A
Manufacturer data	0x70/0x7f	8 +120 bite	N/A

Note: N/A=Not applicable; data packed or coded. See Programming the bq2091 section for details.

Voltage Thresholds

In conjunction with monitoring V_{SR} for charge/discharge currents, the bq2091 monitors the battery potential through the SB pin. The voltage potential is determined through a resistor divider network per the following equation:

$$\frac{R_5}{R_2} = \frac{MBV}{2.25} - 1$$

where MBV is the maximum battery voltage, R_5 is connected to the positive battery terminal, and R_2 is connected to the negative battery terminal. R_5/R_2 should be rounded to the next highest integer. The battery voltage is monitored for the end-of-discharge voltage (EDV) and for maximum cell voltage (MCV) and for alarm warning conditions. EDV threshold levels are used to determine when the battery has reached an 'empty' state, and the MCV threshold is used for fault detection during charging. The battery voltage gain and two EDV thresholds are programmed via E^2PROM. See the Programming the bq2091 section for further details.

If V_{SB} is below either of the two EDV thresholds, the associated flag is latched and remains latched, independent of V_{SB}, until the next valid charge.

EDV monitoring may be disabled under certain conditions. If the discharge current is greater than approximately 6A, EDV monitoring is disabled and resumes after the current falls below 6A.

Reset

The bq2091 is reset when f i i connected to the battery pack. The bq2091 can also be reset with a command over the serial port, as described in the Software Reset section.

Temperature

The bq2091 monitors temperature using an internal sensor. The temperature is used to adapt charge/discharge and self-discharge compensations as well as maximum temperature and $\Delta T/\Delta t$ during bq2091 controlled charge. Temperature may also be accessed over the serial port. See the Programming the bq2091 section for further details.

Layout Considerations

The bq2091 measures the voltage differential between the SR and Vss pins. V_{OS} (the offset voltage at the SR pin) is greatly affected by PC board layout. For optimal results, the PC board layout should follow the strict rule of a single-point ground return. Sharing high-current ground with small signal ground causes undesirable noise on the small signal nodes. Additionally, in reference to *Figure* 1:

- The capacitors (C1, C3, and C4) should be placed as close as possible to the SB and V_{CC} pins, and their paths to V_{SS} should be as short as possible. A high-quality ceramic capacitor of 0.1µf is recommended for V_{CC}.
- The sense resistor capacitor (C2) should be placed as close as possible to the SR pin.
- The sense resistor (R_{11}) should be as *close* as possible to the bq2091.
- The IC should be close to the cells for the best temperature measurement.
- An optional zener may be necessary to ensure V_{CC} is not above the maximum rating during operation.

Gas Gauge Operation

The operational overview diagram in Figure 2 illustrates the operation of the bq2091. The bq2091 accumulates a measure *of* charge and discharge currents, as well as an estimation of self-discharge. Charge currents are compensated for temperature and state-of-charge. Self-discharge is only temperature-compensated.

The main counter, Remaining Capacity (RM), represents the available battery capacity at *any* given time. Battery charging increments the RM register, whereas battery discharging and self-discharge decrement the RM register and increment the DCR (Discharge *Count* Register).

The Diharge-Count Register (DCR) is used to update the Full-Charge Capacity (FCC) register only if a complete battery discharge from full to empty occurs without any partial battery charges. Therefore, the bq2091 adapta its capacity determination based on the actual conditions of discharge.

The battery's initial capacity is equal to the Design Capacity (DC). Until FCC is updated, RM counts up to, but not beyond, this threshold during subsequent *charges*.

1. Full-Charge Capacity or learned-battery capacity:

   FCC is the last measured discharge capacity of the battery. *On* initialization (application of V_{CC} or reset), FCC = DC. During subsequent discharges, the FCC is updated with the latest measured capacity in the Discharge Count Register (DCR), representing a discharge from full to below EDV1. A qualified discharge is necessary for a capacity transfer from the DCR to the FCC register. The FCC also serves as the 100% reference threshold wed by the relative state-of-charge calculation and display.

2. Design Capacity (DC):

   The DC is the user specified battery capacity and is programmed by wiring an external E²PROM. The DC also provides the 100% reference for the absolute display mode.

3. Remaining Capacity (RM):

   RM counts up during charge to a maximum value of FCC and down during discharge and self-discharge to 0. RM is reset to 0x0A when EDV1 = 1 and a valid charge is detected. To prevent overstatement of charge during periods of overcharge, RM stops incrementing when RM = FCC. RM may optionally be written to a user-defined value when fully charged when the battery pack is under bq2091 charge control. See bq2091 charge control for further details.

4. Discharge Count Register (DCR):

   The DCR counts up during discharge independent of RM and can continue increasing after RM has decremented to 0. Prior to RM = 0 (empty battery), both discharge and self-discharge increment the DCR. After RM = 0, only discharge increments the DCR. The DCR resets to 0 when RM = FCC. The DCR does not roll over but stops counting when it reaches FFFFh.

   The DCR value becomes the new FCC value on the first charge after a valid discharge to V_{EDV1} if:

   - No valid charge initiations (charges greater than 10mAh, where $V_{SRO} > V_{SRQ}$) occurred during the period between RM = FCC and EDV1 detected.
   - The self-discharge count is not more than 256mAh.
   - The temperature is ≥ 273°K when the EDV1 level is reached during discharge.

   The valid discharge flag (VDQ) indicates whether the present discharge is valid for FCC update. FCC cannot be modified by greater than -512mAh during any single cycle.

Charge Counting

Charge activity is detected based on a positive voltage on the VSR input. If charge activity is detected, the bq2091 increments RM at a rate proportional to V_{SRO} and, if enabled, activates an LED display. Charge actions increment the RM after compensation for charge rate and temperature.

The bq2091 determines charge activity sustained at a continuous rate equivalent to $V_{SRO} > V_{SRQ}$. A valid charge equates to sustained charge activity greater than 10 mAh. Once a valid charge is detected, charge counting continues until V_{SRO} falls below V_{SRQ}. V_{SRQ} is a programmable threshold as described in the Digital Magnitude Filter section.

Discharge Counting

All discharge counts where $V_{SRO} < V_{SRD}$ cause the RM register to decrement and the DCR to increment. V_{SRD} is a programmable threshold as described in the Digital Magnitude Filter section.

Self-Discharge Estimation

The bq2091 continuously decrements RM and increments DCR for self-discharge based on time and temperature. The self-discharge rate is dependent on the battery chemistry. The bq2091 self-discharge estimation rate is externally programmed in E²PROM and can be programmed from 0 to 25% per day at 20°C. This rate doubles every 10°C from 0°C to 70°C.

Charge Control

The bq2091 supports SBD charge control by broadcasting ChargingCurrent() and ChargingVoltage() to the Smart Charger address. Smart Charger broadcasts can be disabled by writing bit 14 of BatteryStatus() to 1. The bq2091-based charge control can be disabled by setting bit 4 in Flags2 (MSB of 0x2f) to 1. See Programming the bq2091 for further details. If RM is below the full charge percentage, the bq2091 will broadcast the fast charge current and voltage to the Smart Charger, if enabled. The bq2091 will broadcast the maintenance current valuea (trickle rate) if Voltage() is below EDVF.

The bq2091 internal charge control is compatible with Li-Ion and Nickel-based chemistries. For Li-Ion, the bq2091 will broadcast the required charge current and voltage according to the values programmed in the external E²PROM. During a valid charge (VQ = 1), if Current (0x0a) falls below 50mA while Voltage (0x09) is within 256mV of the charging voltage, the bq2091 will signal a valid charge termination where the Terminate-Charge and Fully-Charged bit is set in Battery Status.

For nickel-based chemistries, the bq2091 will broadcast the required charge current and voltage according to the programmed values in the external E²PROM. Maximum Temperature and AT/& are used as valid charge termination methods. Note: Nickel-based chemistries require a charge voltage higher than the maximum cell voltage during charge to ensure constant current charging. During a valid charge (VQ = 1), if the bq2091 determines a maximum temperature or AT/& rate greater than the programmed value, the Terminate Charge and Fully-Charged bit will be set in Battery Status.

Once the bq2091 determines a valid charge termination condition, charging current is set to 0 until this condition ceases (ΔT/Δt, MaxT, min. current). After a valid charge

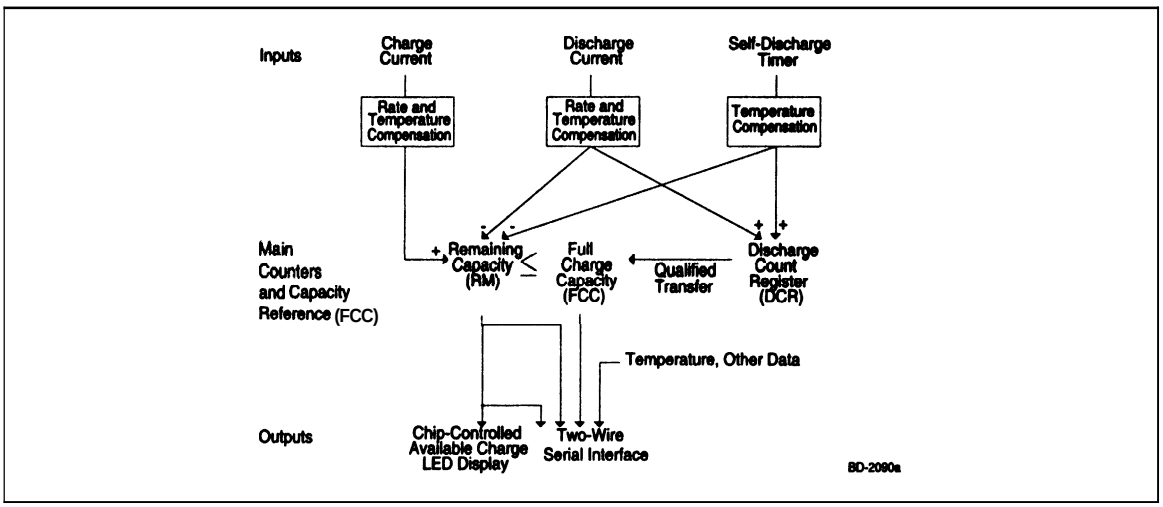


Figure 2. Operational Overview

termination and the terminate condition ceases, maintenance (trickle) charge current and voltage will be broadcast to the Smart Charger. This process continues until RM falls below the full charge percentage. The bq2091 will then request the fast charge current and voltage to the Smart Charger.

During fast charge, the bq2091 will suspend charge by requesting zero current and setting the Terminate-Charge-Alarm bit in Battery Statue. Charge is suspended if the actual charge current is 25% greater than the programmed charged current. If the programmed charge current is less than 1024mA, overcurrent suspend will occur if the actual charge current is 256mA greater than the programmed value. Charge is also suspended if the actual battery voltage is 5% greater than the programmed charge voltage. If the battery temperature is greater than the programmed maximum temperature prior to charge, then the bq2091 will suspend charge requests until the temperature falls below 50°C.

After a valid charge termination, RM may optionally be set to a value from 0 to 100% of the Full Charge Capacity. If RM is below the value programmed in Full Charge Percent, RM will be set to Full Charge Percent upon valid charge termination. If RM is above the Full Charge Percent, RM is not mo ed. This value also is used to determine when the bq2091 broadcasts fast charge or maintenance charge information.

Count Compensations

Charge activity is compensated for temperature and state-of-charge before updating the RM and/or DCR. RM is compensated for temperature before updating the RM register. Self-discharge estimation is compensated for temperature before updating RM or DCR.

Charge Compensation

Charge efficiency is compensated for state-of-charge. temperature, and battery chemistry. For Li-ion chemistry cells, the charge efficiency is unity for all cases. However, the charge efficiency for nickel chemistry cells is adjusted using the following equation:

$$RM = RM * (Q_{EFC} - Q_{ET})$$

where RelativeStateofCharge ≤ FullChargePercentage

and Q_{EFF} is the programmed fast charge efficiency varying from .75 to .99.

$$RM = RM \_ (Q_{ETC} - Q_{ET})$$

where RelativeStateofCharge ≥ FullChargePercentage

and Q_{ETC} is the programmed maintenance (trickle) charge efficiency varying from .50 to .97.

Q_{ET} is used to adjust the charge efficiency as the battery temperature increases according to the following:

$Q_{ET} = 0$ if $T < 30°C$

$Q_{ET} = 0.02$ if $30°C \le T < 40°C$

$Q_{ET} = 0.05$ if $T \ge 40°C$

Remaining Capacity Compensation

The bq2091 adjusts the RM as a function of temperature. This adjustment accounts for the reduced capacity of the battery at colder temperatures. The following equation is used to adjust RM:

If T ≥ 5°C

RemainingCapacity () = NominalAvailableCapacity()

If T < 5°C

RM() = NAC() (1 + TCC * (T - 5°C))

where T = temperature °C

TCC = 0.016 for Li–Ion cells

TCC = 0.0004 for Ni chemistry cells

RM will adjust upward to NominalAvailableCapacity() as the temperature increases.

Digital Magnitude Filter

The bq2091 has a programmable digital filter to eliminate charge and discharge counting below a set threshold. Table 2 shows typical digital filter settings. The proper digital filter setting can be calculated using the following equation.

$$V_{SRD}\ (mV) = -45 / DMF$$

$$V_{SRQ}\ (mV) = -1.25 * V_{SRD}$$

Table 2. Typical Digital Filter Settings

DMF	DMF Hex.	V_{SRD} (mV)	V_{SRQ} (mV)
75	4B	-0.60	0.75
100	64	-0.45	0.56
150 (default)	96	-0.30	0.38
175	AF	-0.26	0.32
200	C8	-0.23	0.28

Error Summary

Capacity Inaccurate

The FCC is susceptible to error on initialization or if no updates occur. On initialization, the FCC value includes the error between the design capacity and the actual capacity. This error is present until a valid discharge occurs and FCC is updated (see the DCR description on page 6). The other cause of FCC error is battery wear-out. As the battery ages, the measured capacity must be adjusted to account for changes in actual battery capacity. Periodic diecharges from full to empty will minimize errors in FCC.

Current-Sensing Error

Table 3 illustrates the current-sensing error as a function of V_{SR}. A digital filter eliminates charge and discharge counts to the RM register when V_{SR} is between V_{SRQ} and V_{SRD}.

Display

The bq2091 can directly display capacity information using low-power LEDs. The bq2091 displays the battery charge state in either absolute or relative mode. In relative mode, the battery charge is repreaented as a percentage of the FCC. Each LED segment represents 25% of the FCC.

In absolute mode, each segment represents a fixed amount of charge, based on the initial design capacity. In absolute mode, each segment represents 25% of the design capacity. As the battery wears out over time, it is possible for the FCC to be below the initial design capacity. In this case, all of the LEDs may not turn on in absolute mode, representing the reduction in the actual battery capacity.

The displayed capacity is compensated for the present battery temperature. The displayed capacity varies as temperature varies, indicating the available charge at the present conditions.

When $\overline{DISP}$ is tied to V_{CC}, the SEG_{1-4} outputs are inactive. When $\overline{DISP}$ is left floating, the display becomes active whenever the bq2091 recognizes a valid charge. When pulled low, the segment outputs become active immediately for a period of approximately 4 seconds.

The segment outputs are modulated as two banks of three, with segments 1 and 3 alternating with segments 2 and 4. The segment outputs are modulated at approximately 100Hz with each segment bank active for 30% of the period.

SEG_1 blinks at a 4Hz rate whenever V_{SB} has been detected to be below V_{EDV1} (EDV_1 = 1), indicating a low-battery condition. V_{SB} below V_{EDVF} (EDV_F = 1) disables the display output.

Microregulator

The bq2091 can operate d i l y from three or four nickel chemistry cells. To facilitate the power supply requirements of the bq2091, an REF output is provided to regulate an external low-threshold n-FET. A micropower source for the bq2091 can be inexpensively built using the FET and an external resistor; see Figure 1.

Note that an optional zener diode may be necessary to limit V_{CC} during *charge*.

Communicating With the bq2091

The bq2091 includes a simple two-pin (SCC and SCD) bidirectional eerial data interface. A hoet processor uses the interface to access various bq2091 registers; see Table 4. This allows battery characteristics to be easily monitored. *The* open-drain SCD and SCC pins on the bq2091 are pulled up by the host system, or may be connected to V_{SS}, if the serial interface lb not used.

The interface uses a command-baaed protocol, where the host processor sends the battery address and an eight-bit command byte to the bq2091. *The* command directs the bq2091 to either store the next data received to a register specified by the command byte or output the data specified by the command byte.

bq2091 Data Protocols

The host system, acting in the role of a Bue master, uses the read word and write word protocols to communicate integer data with the bq2091 (see Figure 3).

Host-to-bq2091 Message Protocol

The Bus Host communicates with the bq2091 using one of three protocols:

- Read word
- Writeword
- Read block

The particular protocol used is a function of the command. The protocols used are shown in Figure 3.

Host-to-bq2091 Messages (see Table 4)

ManufacturerAccess() (0x00)

This optional function is not operational fur the bq2091.

RemainingCapacityAlarm() (0x01)

This function sets or returns the low-capacity alarm value. When RM falls below the RemainingCapacity-Alarm() value programmed from the external E^2PROM, the RemainingCapacityAlarm bit is set in BatteryStatus()(0x16). The system may alter this alarm during operation.

Input/Output: unsigned integer. This sets/returns the value where the Remaining Capacity Alarm bit is set in Battery Status.

RemainingTimeAlarm() (0x02)

This function sets or returns the low remaining time alarm value. When the AverageTimeToEmpty() (0x12) falls below this value, the Remaining Time Alarm bit in Battery Status is set. The default value fur thie register is ten minutes. The system may alter this alarm during operation.

Input/Output: unsigned integer. This sets/re- t w the value where the Remaining Time Alarm bit is set in Battery Status.

BatteryMode() (0x03)

This read/write word selects the various battery operational modes. The bq2091 supports the battery capacity information specified in mAh. This function also determines whether the bq2091 charging values are broadcasted to the Smart Battery Charger address when the battery requires charging.

Table 3. bq2091 Current-Sensing Errors

Symbol	Parameter	Typical	Maximum	Units	Notes
V_{OS}	Offset referred to V_{SR}	± 50	± 150	µV	$\overline{DISP}$ = V_{CC}.
INL	Integrated non-linearity error	± 2	± 4	%	Add 0.1% per °C above or below 25°C and 1% per volt above or below 4.25V.
INR	Integrated non-repeatability error	± 1	± 2	%	Measurement repeatability given similar operating conditions.

Temperature() (0x08)

This read-only word returns the cell-pack's internal temperature (0.1°K).

Output: unsigned integer. Returns cell temperature in tenths of degrees Kelvin increments

Units: 0.1°K

Range: 0 to +500.0°K

Granularity: 0.5°K or better

Accuracy: ±3°K after calibration

Voltage() (0x09)

This read-only word returns the cell-pack voltage (mV).

Output: unsigned integer. Returns battery terminal voltage in mV

Units: mV

Range: 0 to 65,535 mV

Granularity: 0.2% of design voltage

Accuracy: ±1% of design voltage after calibration

Current() (0x0a)

This read-only word returns the current through the battery's terminals (mA).

Output: signed integer. Returns the charge/discharge rate in mA, where positive is for charge and negative is for discharge

Units: mA

Range: 0 to 32,767 mA for charge or 0 to -32,768 mA for discharge

Granularity 0.2% of the DesignCapacity() or better

Accuracy: ±1% of the Design Capacity after calibration

AverageCurrent() (0x0b)

This read-only word returns a rolling average of the current through the battery's terminals. The AverageCurrent() function returns meaningful values after the battery's first minute of operation.

Output: signed integer. Returns the charge/discharge rate in mA, where positive is for charge and negative is for discharge

units: mA

Range: 0 to 32,767 mA for charge or 0 to 92,768 mA for discharge

Granularity: 0.2% of the DesignCapacity() or better

Accuracy: *1% of the Design Capacity after calibration

RelativeStateOfCharge() (0x0d)

This read-only word returns the predicted remaining battery capacity expressed as a percentage of FullChargeCapacity() (%). RelativeStateOfCharge() is only valid for battery capacities less than 10,400mAh.

Output: unsigned integer. Returns the percent of remaining capacity

Unite: %

Range: 0 to 100%

Granularity: 1% or better

AbsoluteStateOfCharge() (0x0e)

This read-only word returns the predicted remaining battery capacity expressed as a percentage of DesignCapacity() (%). Note that AbsoluteStateOfCharge can return values greater than 100%. **Absolute StateOfCharge is only valid for battery capacities less than 10,400mAh.**

Output: unsigned integer. Returns the percent of remaining capacity

Units: %

Range: 0 to 65,535 %

Granularity. 1% or better

Accuracy: ±MaxError()

RemainingCapacity() (0x0f)

This read-only word returns the predicted remaining battery capacity. The RemainingCapacity() value is expressed in mAh.

Output: unsigned integer. Returns the estimated remaining capacity in mAh

Units: mAh

Range: 0 to 65,535 mAh

Granularity 0.2% of DesignCapacity() or better

FullChargeCapacity() (0x10)

This read-only word returns the predicted pack capacity when it is fully charged. FullChargeCapacity() defaults

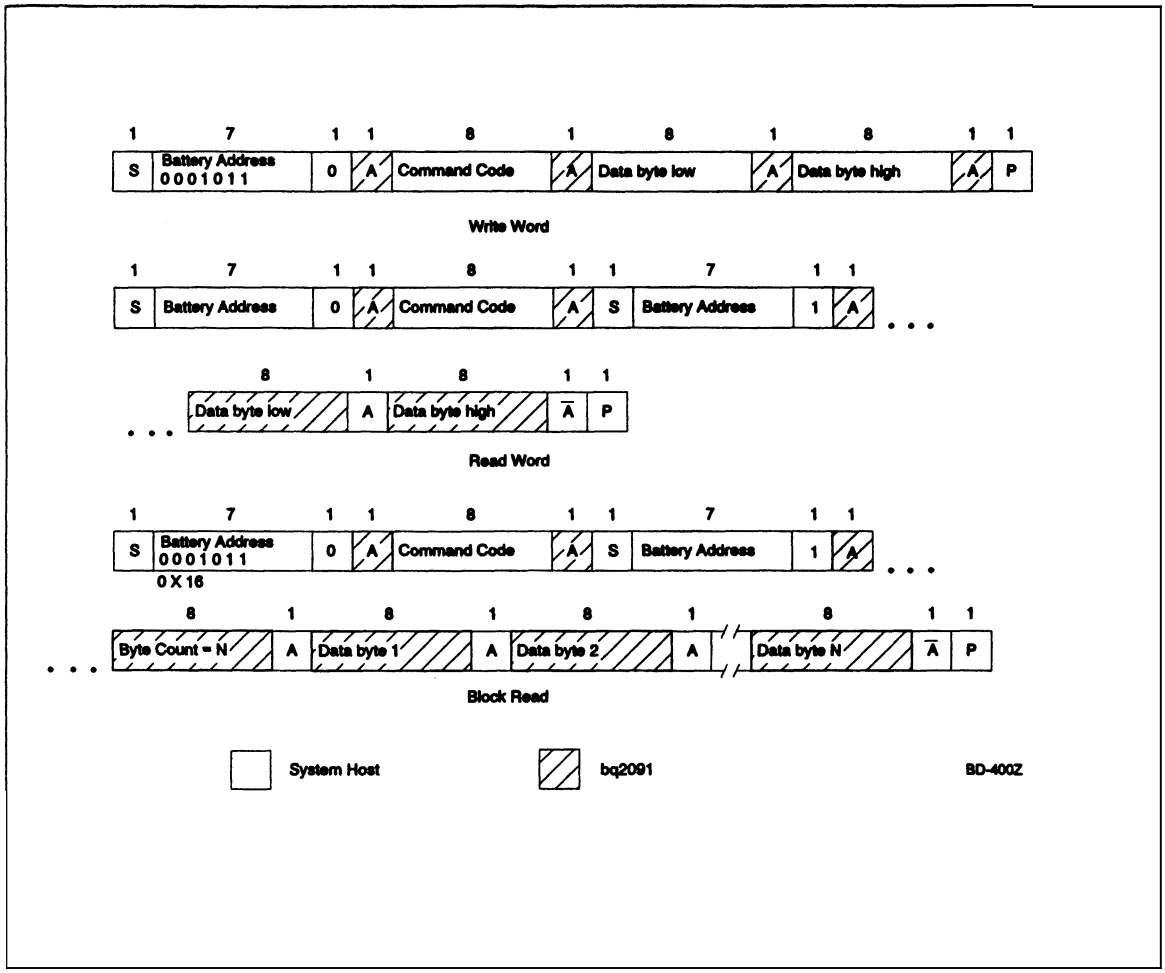


Figure 3. Host Commun˙cation Protocols

Table 4. **bq2091** Register Functions

Function	Code	Access	Units	Defaults[1]
ManufacturerAccess	0x00	read/write		
RemaningCapacityAlarm	0x01	read/write	unsigned int.	E^2
RemainingTimeAlarm	0x02	read/write	unsigned int.	10
BatteryMode	0x03	read	bit flag	
Temperature	0x08	read	0.1°K	
Voltage	0x09	read	mV	
Current	0x0a	read	mA	0000h
AverageCurrent	0x0b	read	mA	0000h
MaxError	0x0c	read	percent	100
RelativeStateOfCharge	0x0d	read	percent	0000h
AbsoluteStateOfCharge	0x0e	read	percent	0000h
RemainingCapacity	0x0f	read	mAh	0000h
FullChargeCapacity	0x10	read	mAh	E^2
RunTimeToEmpty	0x11	read	minutes	
AverageTimeToEmpty	0x12	read	minutes	
Reserved	0x13			
ChargingCurrent	0x14	read	mA	E^2
ChargingVoltage	0x15	read	mV	E^2
Battery Status	0x16	read	number	0000h
CycleCount	0x17	read	count	E^2
DesignCapacity	0x18	read	mAh	E^2
DesignVoltage	Ox19	read	mV	E^2
ManufactureDate	0x1b	read	unsigned int	E^2
SerialNumber	Oxlc	read	number	E^2
Reserved	0x1d - Oxlf			
ManufacturerName	0x20	read	string	E^2
DeviceName	0x21	read	string	E^2
DeviceChemistry	*0x22*	read	string	E^2
ManufacturerData	0x23	read	string	E^2
FLAGS1 and FLAGS2	0x2f	read	bit flag	E^2
Endof DischargeVoltage1	0x3e	read	mV	E^2
EndofDischargeVoltageFinal	0x3f	read	mV	E^2

Note: 1. Defaults after reset or power-up.

to the value programmed in the external E^2PROM until a new pack capacity is learned.

Output: unsigned integer. Returns the estimated full charge capacity in mAh

Units: mAh

Range: 0 to 65,536 mAh

Granularity: 0.2% of design capacity or better

RunTimeToEmpty() (0x11)

This read-only word returns the predicted remaining battery life at the present rate of discharge (minutes). The RunTimeToEmpty() value is calculated based on Current().

Output: unsigned integer. Returns the minutes of operation left

Unite: minutes

Range: 0 to 65,534 minutes

Granularity: 2 minutes or better

Invalid data indication: 65,535 indicates battery is being *charged*

AverageTimeToEmpty() (0x12)

This read-only word returns the predicted remaining battery life at the present average discharge rate (minutes). The AverageTimeToEmpty is calculated based on AverageCurrent().

Output: unsigned integer. Returns the minutes of operation left

Unite: minutes

Range: 0 to 65,534 minutes

Granularity: 2 minutes or better

Invalid data indication: 65,535 indicates battery is being charged

ChargingCurrent() (0x14)

If enabled, the bq2091 sends the desired charging rate in mA to the Smart Battery Charger.

Output: unsigned integer. Transmits/returns the maximum charger *output* current in mA

Units: mA

Range: *0 to* 65,534 mA

Granularity: 0.2% of the design capacity or better

Accuracy: ±0.2% of the design capacity

Invalid data indication: 65,535 indicates that the Smart Charger should operate as a voltage source outside its maximum regulated *current*

ChargingVoltage() (0x15)

If enabled, the bq2091 sends the desired voltage in mV to the Smart Battery Charger.

Output: unsigned integer. Transmits/returns the charger voltage output in mV

Units: mV

Range: 0 to 65,534mV

Granularity: 0.2% of the design voltage or better

Accuracy: ±0.2% of the design voltage

Invalid data indication: 65,535 indicatea that the Smart Battery Charger should operate as a current source outside its maximum regulated voltage range.

BatteryStatus() (0x16)

This read-only word returns the battery status word.

Output: unsigned integer. Returns the status register with alarm conditions bitmapped as shown in Table 6.

Some of the Battery Status() flags (Remaining_Capacity_Alarm and Remaining–Time–Alarm) are calculated based on current. See Table 8 for definitions.

CycleCount() (0x17)

This read-only word returns the number of charge/discharge cycles the battery has experienced. A charge/discharge cycle starts from a base value equivalent to the battery's state-of-charge, upon completion of a charge cycle. The bq2091 increments the cycle counter during the current charge cycle, if the battery has been discharged to below *86% of* the state-of-charge at the end of the last charge cycle. A discharge > 0.5% is needed, preventing false reporting of small charge/discharge cycles.

Output: unsigned integer. Returns the count of charge/discharge cycles the battery has experienced

Units: cycles

Range: 0 to 65,535 cycles; 66,535 indicates battery has experienced 65,535 or more cycles

Granularity 1 cycle

DesignCapacity() (0x18)

This read-only word returns the theoretical capacity of a new pack. The DesignCapacity() value is expressed in mAh at the nominal discharge rate.

Output: unsigned integer. Returns the battery capacity in mAh

Units: mAh

Range: 0 to 65,535 mAh

DesignVoltage() (0x19)

This read-only word returns the theoretical voltage of a new pack (mV).

Output: unsigned integer. Returns the battery's normal terminal voltage in mV

Units: mV

Range: 0 to 65,535 mV

ManufactureDate() (0x1b)

This read-only word returns the date the cell was manufactured in a packed integer word. The date is packed as follows: (year - 1980), month, day.

Field	Bits Used	Format	Allowable Value
Day	0–4	5-bit binary value	1–31 (corresponds to date)
Month	5–8	4-bit binary value	1–12 (corresponds to month number)
Year	9–15	7-bit binary value	0 • 127 (corresponds to year biased by 1980)

SerialNumber() (0x1c)

This read-only word returns a serial number. This number, when combined with the ManufacturerName(), the DeviceName(), and the ManufactureDate(), uniquely identifies the battery.

Output: unsigned integer

ManufacturerName() (0x20)

This read-only string returns a character string where the first byte is the number of charactera available. The maximum number of characters is 15. The character string contains the battery manufacturer's name. For example, "Benchmarq" identifii the battery pack manufacturer as Benchmarq.

Output: string or ASCII character string

Table 5. Status Register

Alarm Bits	
0x8000	Overcharge Alarm
0x4000	Terminate Charge Alarm
0x2000	Reserved
0x1000	Over Temp Alarm
0x0800	Terminate Discharge Alarm
0x0400	Reserved
0x0200	Remaining Capacity Alarm
0x0100	Remaining Time Alarm
Status Bits	
0x0080	Initialized
0x0040	Discharging
0x0020	Fully Charged
0x0010	Fully Discharged
Error Code	
0x0000-0x000f	Reserved for error codes

DeviceName() (0x21)

This read-only string returns a character string where the first byte is the number of characters available. The maximum number of characters is 15. The 15-byte character string contains the battery's name. For example, a DeviceName() of "bq2091" indicates that the battery is a model bq2091.

Output: string or ASCII character string

DeviceChemistry() (0x22)

This read-only string returns a character string where the first byte is the number of characters available. The maximum number of charactere is 15. The 15-byte character string contains the battery's chemistry. For example, if the DeviceChemistry() function returns "NiMH," the battery pack contains nickel-metal hydride cells.

Output: string or ASCII character string

ManufacturerData() (0x23)

This read-only string allows access to an up to 15-byte manufacturer data string.

Output: block data—data whose meaning is assigned by the Smart Battery's manufacturer

EndofDischargeVoltage1() (0x3e)

This read-only word returns the **first end of discharge** voltage **programmed** for the **pack.**

Output: unsigned **integer.** Returns **battery** end-**of-discharge voltage programmed in E²PROM in mV.**

EndofDischargeVoltageF() (0x3f)

This read-only word **returns** the final **end-of-discharge voltage programmed** for **the** pack.

Output: unsigned **integer. Returns** battery final **end-of-discharge** voltage programmed in **E²PROM** in **mV.**

FLAGS1&2() (0x2c)

This read-only register returns an unsigned **integer** representing the internal statue **registers** of **the bq2091.** The **MSB represents** FLAGS2, and the LSB **represents FLAGS1.** See Table 6 for the bit description for **FLAGS1&2.**

FLAGS2

The *Display* Mode flag (@MODE), Bit 7, **determines** whether **the bq2091** displays Relative or **Absolute** capacity.

The DMODE values are:

FLAGS2 Bits							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DMODE	-	-	-	-	-	-	-

Where DMODE **is:**

0 **Selects Absolute** display

1 **Selects Relative display**

Bit 6 is **reserved.**

The Chemistry flag **(CHM),** Bit 5, **selects Li-Ion** or N i l compensation **factors.**

The **CHM values** are:

FLAGS2 Bib							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
-	-	**CHM**	-	-	-	-	-

Where CHM is:

0 **Selects Nickel**

1 Selects **Li-Ion**

Bit 4, the Charge *Control* **flag (CC), determines** whether a **bq2091-based charge termination** will **set** RM to a **user-**defined **programmable** full *charge* capacity.

The CC **values** are:

FLAGS2 Bib							
7	**6**	5	**4**	**3**	**2**	**1**	**0**
-	-	-	**CC**	-	-	-	-

Where CC is:

0 RM is not modified on valid **bq2091** charge termination

1 **RM is set to a programmable percentage of the** FCC when **a** valid **bq2091 charge** termina· **tion occurs**

Bit 3 is reserved.

Bit 2, **the *Overvoltage flag* (OV),** is **set** when **the** bq2091 detects **a** peck voltage **5%** greater **than** the **programmed** charging **voltage. This** bit **is cleared** when **the pack** volt-***age* falls** 5% below the **programmed charging** voltage.

The OV values **are:**

FLAGS2 Bits							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
-	-	-	-	-	**OV**	-	-

Where OV is:

0 **BatteryVoltage() < 1.05 • ChargingVoltage**

1 **BatteryVoltage() ≥ 1.05 • ChargingVoltage**

Table 6. Bit Description for FLAGS1 and FLAGS2

	(MSB) 7	**6**	**5**	**4**	**3**	**2**	**1**	**0 (LSB)**
FLAGS2	DMODE		**CHM**	CC		OV	**LTF**	**OC**
FLAGS1	**ΔT/Δt1**	**ΔT/Δt0**	**VQ**	**WRINH**	**VDQ**	SEDV	**EDV1**	EDVF

- = Reserved

Bit 1, the Low *Temperature* Fault flag **(LTF),** is set when **temperature<0°C** and cleared when **temperature>5°C.**

The LTF values are:

FLAGS2 Bits								
7	6	5	4	3	2	1	0
					-	LTF	-

Where LTF is:

0 **Temperature>5°C**

1 **Temperature<0°C**

Bit 0, the *Overcurrent* flag (OC), is **set** when the average current **is** 25% greater than the programmed charging current. **If** the charging **current is** programmed **less** than **1024mA, overcurrent** is set if the average **current** is 256mA greater than the programmed charging current. This flag is cleared when the average current falls below **256mA.**

The OC values are:

FLAGS2 Bits							
7	6	5	4	3	2	1	0
						-	OC

Where OC is:

0 Average current **is** less than 1.25 * **charging** current or **less** than **256mA** if charging current is programmed **less** than **1024mA**

1 Average current exceeds 1.25 • charging current or **256mA** if the charging current **is** programmed leas than **1024mA. This** bit **is** cleared if average **current<256mA**

FLAGS1

Bit 7 and bit 6, the ***Delta Temperature*** flags, signify whether the **bq2091 is** sensing a valid **ΔT/Δt** for charge termination. Both **bits** must transition to a **1** to signify that the rise in battery temperature exceeds the programmed rate threshold. The bits are clear if the rate of temperature falls below the programmed **ΔT/Δt** rate.

The $\Delta T/\Delta t_0$, $\Delta T/\Delta t_1$ values are:

FLAGSI Bits							
7	6	5	4	3	2	1	0
$\Delta T/\Delta t_1$	$\Delta T/\Delta t_0$	-	-	-	-	-	-

Where $\Delta T/\Delta t_0$, $\Delta T/\Delta t_1$ is:

0 Temperature < **Programmed ΔT/Δt** rate

1 Temperature > Programmed **ΔT/Δt** rate

The Valid Charge flag (VQ), Bit **5,** is set when $V_{SRO} \geq V_{SRQ}$ and **10mAh** of charge has accumulated. This bit **is** cleared during a discharge and when $V_{SRO} \leq V_{SRQ}$.

The VQ values are:

FLAGS1 Bits							
7	6	5	4	3	2	1	0
-	-	VQ	-	-	-	-	-

Where VQ is:

0 $V_{SRO} \leq V_{SRQ}$

1 VSRO ≥ VSRQ and **10mAh** of charge has accumulated

The ***Write Inhibit* flag** (WRINH), Bit 4, allows or inhibits writes to **all** registers.

The **WRINH values** are:

FLAGSI Bits							
7	6	5	4	3	2	1	0
		-	WRINH	-	-	-	-

Where WRINH **is:**

0 Allows writes to **all registers**

1 Inhibits all writes and secures the bq2091 from **invalid/undesired** writes.

WRINH should be set at the time of pack assembly and tested to prevent normally read-write registers from accidental over-writing.

The ***Valid Discharge*** flag ***(VDQ),*** Bit 3, is set when a valid discharge **is occurring** (discharge cycle valid for learning new full charge capacity) and cleared if a partial charge is detected, EDV1 is **asserted** when **T<0°C,** or self-discharge accounts for more than **256mAh** of the discharge.

The VDQ **values** are:

FLAGS1 Bits							
7	6	5	4	3	2	1	0
			-	VDQ	-	-	-

Where VDQ is:

0 Self-discharge **is** greater than **256mAh,** EDV1 = 1 when **T<0°C** or VQ = 1

1 On first discharge after **RM=FCC**

The Stop ***EDV*** flag **(SEDV),** Bit 2, is set when the discharge **current>6.15A** and cleared when the discharge current falls below **6.15A.**

The SEDV values are:

FLAGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	SEDV	-	-

Where SEDV is:

0 Current<6.15A

1 Current>6.15A

The First End-of-Discharge Voltage flag (EDV1), Bit 1, b set when Voltage()<EDV1=1 if SEDV=0 and cleared when VQ=1 and Voltage()>EDV1.

The EDVl values are:

FLAGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	EDV1	-

Where EDVl is:

0 VQ = 1 and Voltage ()> EDVl

1 Voltage() < EDVl and SEDV = 0

The *Final End-of-Discharge Voltage* flag *(EDVF)*, Bit 0, is set when Voltage()<EDVF=1 if SEDV=0 and cleared when VQ=1 and Voltage()>EDVF.

The EDVF values are:

FLAGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	EDVF

Where EDVF is:

0 VQ = 1 and Voltage > EDVF

1 Voltage < EDVF and SEDV = 0

Software Reset

The bq2091 *can* be reset over the serial port by confirming that the WRINH bit is set to zero in FLAGS1, writing MaxError() (0x0c) to any value other than 2. and writing the reset register (0x44) to 8009, causing the bq2091 to reinitialize and read the default values from the external E^2PROM.

Error Codes and Status Bits

Error codes and status bits are listed in Table 7 and Table8, respectively.

Programming the bq2091

The bq2091 requires the proper programming of an external E^2PROM for proper device operation. Each module can be calibrated for the greatest accuracy, or general "default" values can be used. A programming kit (interface board, software, and cable) for an IBM-compatible PC is available from Benchmarq. Please contact Benchmarq far further detail

The bq2091 uses a 24C01 or equivalent serial E^2PROM for storing the various initial values, calibration data, and string information. Table 1 outlines the parameters and addresses for thb information. Tables 9 and 10 detail the various register contents and show an example program value for an 1800mAh NiMH battery pack, using a 50mΩ sense resistor.

Table 7. Error Codes (BatteryStatus() (0x16))

Error	Code	Access	Description
OK	0x0000	read/write	bq2091 processed the function code without detecting any errors
Busy	0x0001	read/write	bq2091 is unable to process the function code at this time
NotReady	0x0002	read/write	bq2091 cannot read or write the data at this time—try again later
UnsupportedCommand	0x0003	read/write	bq2091 does not support the requested function code
AccessDenied	0x0004	write	bq2091 detected an attempt to write to a read-only function code
Overflow/Underflow	0x0005	read/write	bq2091 detected a data overflow or underflow
BadSize	0x0006	write	bq2091 detected an attempt to write to a function code with an incorrect size data block
UnknownError	0x0007	read/write	bq2091 detected an unidentifiable error

Note: Reading the bq2091 after an error clears the error code.

Table 8. Status Bits

Alarm Bits		
Bit Name	**Set When:**	**Reset When:**
OVER_CHARGE_ALARM	BQ2091 detects over-temperature, ΔT/Δt, or minimum charge current conditions exist (Note: valid charge termination).	A discharge occurs or when ΔT/Δt, over-temperature, or minimum current ceases during charge.
TERMINATE_CHARGE_ALARM	bq2091 detects over-current, over-voltage, over-temperature, or ΔT/Δt conditions exist during charge. Charging current is set to zero, indicating a charge suspend.	A discharge occurs or when all conditions causing the event cease.
ΔT/Δt_ALARM	bq2091 detects the rate-of-temperature increase is above the programmed value (valid termination)	The temperature rise falls below the programmed rate.
OVER_TEMP_ALARM	bq2091 detects that its internal temperature is greater than the programmed value (valid termination).	Internal temperature falls below 50°C.
TERMINATE_DISCHARGE_ALARM	bq2091 determines that it has supplied all the charge that it can without being damaged (EDVF).	Battery reaches a state of charge sufficient for it to once again safely supply power.
REMAINING_CAPACITY_ALARM	bq2091 detects that the RemainingCapacity() is less than that set by the RemainingCapacity() function.	Either the value set by the RemainingCapacityAlarm() function is lower than the Remaining Capacity() or the RemainingCapacity() is increased by charging.
REMAINING_TIME_ALARM	bq2091 detects that the estimated remaining time at the present discharge rate is less than that set by the RemainingTimeAlarm() function.	Either the value set by the RemainingTimeAlarm() function is lower than the AverageTimeToEmpty() or the AverageTimeToEmpty() is increased by charging.
Status Bits		
Bit Name	**Set When:**	**Reset When:**
INITIALIZED	bq2091 is set when the bq2091 has reached a full or empty state.	Battery detects that power-on or user-initiated reset has occurred.
DISCHARGING	bq2091 determines that it is not being charged.	Battery detects that it is being charged.
FULLY–CHARGED	bq2091 determines a valid charge termination. RM will then be set to full charge percentage if necessary.	RM discharges below the full charge percentage
FULLY_DISCHARGED	bq2091 determines that it has supplied all the charge that it can without being damaged (that is, continued use will result in permanent capacity loss to the battery)	RelativeStateOfCharge() is greater than or equal to 20%

Table 9. Example Register Contents

Description	E^2PROM Address		E^2PROM Hex Contents		Example Values	Notes
	Low Byte	High Byte	Low Byte	High Byte		
Design Capacity	0x00	0x01	08	07	1800mAh	This sets the initial full charge battery capacity stored in FCC. FCC is updated with the actual full to empty discharge capacity after a valid discharge from RM = FCC to Voltage() = EDV1.
Initial Battery Voltage	0x02	0x03	30	2a	10800mV	This register is used to adjust the battery voltage. Comparing the values read from the bq2091 to two known input voltages allows the bq2091 to calibrate the battery voltage to within 1%. This action adjusts for errors in the resistor-dividers used for the SB input and bq2091 offset errors.
Fast charging current	0x04	0x05	08	07	1800mA	This register is used to set the fast charge current for the Smart Charger.
Fast charging	0x06	0x07	c4	3b	15300mV	This register is used to set the fast charge voltage for the Smart Charger.
Remaining Capacity Alarm	0x08	0x09	b4	00	180mAh	This value represents the low capacity alarm value.
FLAGS1	0x0a		10			This enables writes to all registers and should be set to 10h prior to pack shipment to inhibit undesirable writes to the bq2091.
FLAGS2	0x0b		b0		Li-Ion = a0h NiMH = 80h	See FLAGS2 register for the bit description and the proper value for programming FLAGS2. Selects relative display mode, Lithium Ion compensation factors, and enables bq2091 Smart Charger control.
Current Measurement Gain[1]	0x0c	0x0d	ee	02	37.5/.05	The current gain measurement and current integration gain are related and defined for the bq2091 current measurement. 0x0c = 37.5/sense resistor value in o h .
EDV1	0x0e	0x0f	16	db	9450mV (1.05V/cell)	The value programmed is the two's complement of the threshold voltage in mV.
EDVF	0x10	0x11	d8	dc	9000mV (1.0V/cell)	The value programmed is the two's complement of the threshold voltage in mV.

Note: 1. Can be adjusted to calibrate the battery pack.

Table 9. Example Register Contents (Continued)

Description	E^2PROM Address		E^2PROM Hex Contents		Example Values	Notes
	Low Byte	High Byte	Low Byte	High Byte		
Temperature Offset[1]	0x12		32		5.0°C	The default value is 0x80 (12.8° + nominal value). Actual temp (20°C) = Nominal temp. (15°C) - temp. offset (5°C) where temperature determined by the bq2091 can be adjusted from 0° to 25.5° (Temperature offset (0-255) * .1)+ nominal value temp.
Maximum Charge Temperature, ΔT/Δt	0x13		87		61.2°C (74 - (8 • 1.6)) ΔT/Δt = 7	Maximum charge temperature is 74 - (mt * 1.6)°C (upper nibble). ΔT/Δt rate is in the lower nibble and varies from 0 to 15, where 0 is more sensitive than 15. Typical value is 7.
Self-Discharge Rate	0x14		f0		.15C	This packed field is the 2's complement of ((RM/4)/(RM/x)) where RM/x ia the desired self-discharge rate per day at room temperature.
Digital Filter	0x15		fa		.18mV	This field is used to set the digital magnitude filter as described in Table 2.
Current Integration Gain[1]	0x16	0x17	40	00	3.2/.05	This field repreaenta the following: 3.2/sense resistor in ohms. It is used by the bq2091 to scale the measured voltage values on the SR pin in mA and mAh. This register also compensates for variations in the reported sense resistor value.
Full Charg Percentage	0x18		a0		98%=60 2.3(60)=a0	This packed field is the 2's complement of the desired value in RM when the bq2091 determines a full charge termination. If RM is below this value. RM is set to this value. If RM is above this value, then RM is not adjusted.
e Charge Compensation	0x19		bd		85% = maintenance comp. 95% = fast charge comp.	This packed value is used to set the fast charge and maintenance *charge* efficiency for nickel-based batteries. The upper nibble adjusts the maintenance charge compensation; the lower nibble adjusts the fast charge compensation. Maintenance, upper nibble = (eff% * 256 - 128)/8 Fast *charge*, lower nibble = (eff% * 256 - 192)/4
Battery Voltage Offset[1]	0x1a		00		0mV	Thie value is used to adjust the battery voltage offset according to the following: Voltage offset (mV) = V_{SB} * 1000 + V_{OFF}) * no. of cells
Voltage Gain[1]	Oxlb	Oxlc	09	05	9.02	Voltage gain is packed as two unite. For example, R5/R2 = 9.09 would be stored as: whole number stored in 0x1a (=09h) and the decimal component stored in 0x1b as 256 * 0.02 = 05.
Serial Number	Osld	0x1e	12	27	10002	This contains the optional pack serial number.

Note: 1. Can be adjusted to calibrate the battery pack.

Table 9. Example Register Contents (Continued)

Description	E²PROM Address		E²PROM Hex Content8		Example Values	Notes
	Low Byte	High Byte	Low Byte	High Byte		
Charge Cycle Count	0x1f	0x20	00	00	0	This field contains the charge cycle count and should be set to zero for a new battery.
Reserved	0x21					
Maintenance Charge Current	0x22	0x23	64	00	100mA	This field contains the desired maintenance current after fast charge termination by the bq2091.
Reserved	0x24	0x31				
Design Voltage	0x32	0x33	30	2a	10800mV	This is nominal battery pack voltage.
Specification Information	0x34	0x35	00	00		This is the default value for this register.
Manufacturer Date	0x36	0x37	a1	20	May 1, 1996 = 8363	Packed per the ManufactureDate() description, which represents May 1,1996 in this example.

Table 10. Example Register Contents (String Data)

String Description	Address	0x ?0	0x ?1	0x ?2	0x ?3	0x ?4	0x ?5	0x ?6	0x ?7	0x ?8	0x ?9-?f
Reserved	0x38-0x3f	00	00	00	00	00	00	00	00	00	00
Manufacturer's Name	0x40-0x4f	09	42 B	45 E	4e N	43 C	48 H	4d M	41 A	52 R	51 Q
Device Name	0x50-0x5f	08	42 B	51 Q	32 2	30 0	39 9	31 1	41 A	34 4	00-00
Chemistry	0x60-0x6f	04	4e N	69 I	4d M	48 H	00	00	00	00	00-00
Manufacturer's Data	0x70-0x7f	04	44 D	52 R	31 1	35 5	00	00	00	00	00-00

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to V_{SS}	-0.3	+7.0	V	
All other pins	Relative to V_{SS}	-0.3	+7.0	V	
REF	Relative to V_{SS}	-0.3	+8.5	V	Current limited by R1 (see Figure 1)
V_{SR}	Relative to V_{SS}	-0.3	+7.0	V	Minimum 100Ω series resistor should be used to protect SR in case of a shorted battery (see the bq2091 application note for details).
T_{OPR}	Operating temperature	0	+70	°C	Commercial

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may *affect* device reliability.

DC Voltage Thresholds ($T_A = T_{OPR}$; V = 3.0 to 5.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
E_{VSB}	Battery voltage error relative to SB	-50mV		50mV	V	See note

Note: . The accuracy of the voltage measurement may be improved by adjusting the battery voltage offset and gain, stored in external E²PROM. For proper operation, V_{CC} should be 1.5V greater than V_{SB}.

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	3.0	4.25	5.5	V	V_{CC} excursion from < 2.0V to ≥ 3.0V initializes the unit.
V_{REF}	Reference at 25°C	6.7	6.0	6.3	V	I_{REF} = 5µA
	Reference at -40°C to +85°C	4.5		7.5	V	I_{REF} = 5µA
R_{REF}	Reference input impedance	2.0	5.0		MΩ	V_{REF} = 3V
I_{CC}	Normal operation		90	135	µA	Vcc = 3.0V
			120	180	µA	V_{CC} = 4.25V
			170	250	µA	Vcc = 5.5V
V_{SB}	Batteryinput	0		V_{CC}	V	
R_{SBmax}	SB input impedance	10	-	-	MΩ	0 < V_{SB} < V_{CC}
I_{DISP}	$\overline{DISP}$ input leakage	-	-	5	µA	V_{DISP} = V_{SS}
I_{LVOUT}	V_{OUT} output leakage	-0.2		0.2	µA	E^2PROM off
V_{SR}	Sense resistor input	-0.3		2.0	V	V_{SR} < Vss = discharge; V_{SR} > V_{SS} = charge
R_{SR}	SR input impedance	10			MΩ	-200mV < V_{SR} < V_{CC}
V_{IH}	Logic input high	1.4		5.5	V	SCL, SDA, SCC, SCD
V_{IL}	Logic input low	-0.5		0.6V	V	SCL, SDA, SCC, SCD
V_{OL}	Data, clock output low			0.4	V	I_{OL}=350µA, SDA, SCD
I_{OL}	Sink current	100		350	µA	V_{OL}≤0.4V, SDA, SCD
V_{OLSL}	SEG_X output low, low Vcc		0.1		V	Vcc = 3V, I_{OLS} ≤ 1.75mA SEG_1–SEG_4
V_{OLSH}	SEG_X output low, high V_{CC}	-	0.4	-	V	Vcc = 5.5V, I_{OLS} ≤ 11.0mA SEG_1–SEG_4
V_{OHVL}	V_{OUT} output, low Vcc	V_{CC} - 0.3	-		V	V_{CC} = 3V, I_{VOUT} = -5.25mA
V_{OHVH}	V_{OUT} output, high Vcc	V_{CC} - 0.6	-		V	V_{CC} = 5.5V, I_{VOUT} = -33.0mA
I_{VOUT}	V_{OUT} source current	-33	-	-	mA	At V_{OHVH} = V_{CC} - 0.6V
I_{OLS}	SEG_X sink current			11.0	mA	At V_{OLSH} = 0.4V

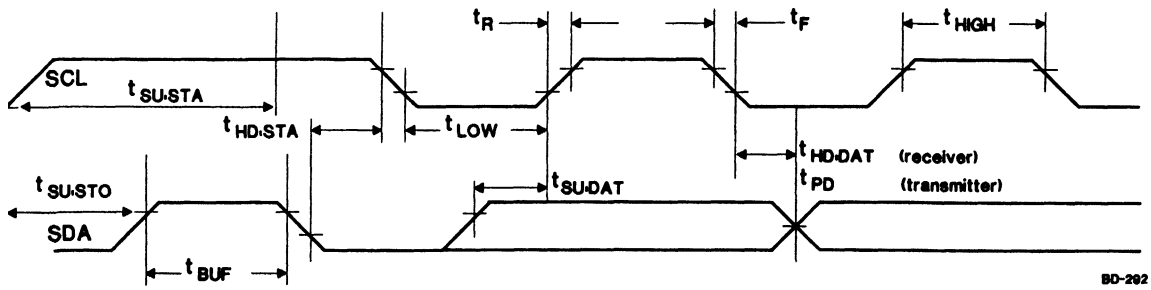
Note: All voltages relative to V_{SS}.

AC Specifications

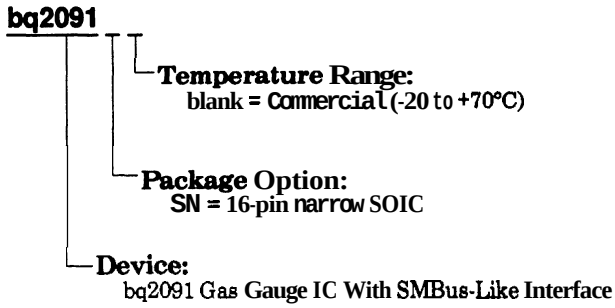
Symbol	Parameter	Min	Max	Units	Notes
F_{SMB}	SMBus operating frequency	10	100	KHz	
T_{BUF}	Bus free time between stop and start condition	4.7		µs	
$T_{HD:STA}$	Hold time after (repeated) start condition	4.0		µs	
$T_{SU:STA}$	Repeated start condition eetup time	250		ns	SCD
		4.7		µs	External Memory
$T_{SU:STO}$	Stop condition setup time	4.0		µs	
$T_{HD:DAT}$	Data hold time	0		ns	
$T_{SU:DAT}$	Data setup time	250	40	ns	
T_{EXT1}	Data buffering time addresses 0x00-0x18 per character		40	ma	
T_{EXT2}	String buffering time addresses 0x19-0x23 per character		15	ms	40 ms for first character
T_{PD}	Data output delay time	300	3500	ns	External memory only. See Note.
T_{LOW}	Clock low period	4.7		µs	
T_{HIGH}	Clock high period	4.0			
T_F	Clock/Data fall time		300	ns	
T_R	Clock/data rise time		1000	ns	

Note: The external memory must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

Bus Timing Data



Ordering Information



bq2110

NiCd or NiMH Gas Gauge Module

Features

- Complete bq2010 Gas Gauge solution for NiCd or NiMH battery packs
- Battery information available over a single-wire bidirectional serial port
- Battery state-of-charge monitoring for 4- to 12-cell series applications
- On-board regulator allows direct connection to the battery
- "L" version includes push-button activated LEDs to display state-of-charge information
- Nominal capacity and cell chemistry pre-configured
- Compact size for battery pack integration

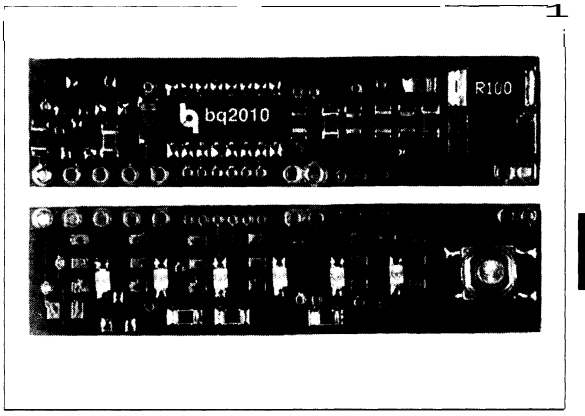
General Description

The bq2110 Gas Gauge Module provides a complete and compact solution for capacity monitoring of NiCd and NiMH battery packs. Designed for battery pack integration, the bq2110 incorporates a bq2010 Gas Gauge IC, a current sense resistor, and all other components necessary to accurately monitor and display the capacity of 4 to 12 series cells. The bq2110L includes six surface-mounted LEDs to display remaining capacity in 20% increments of the learned capacity (relative mode) or programmed capacity (absolute mode). The sixth LED is used in absolute mode to represent an overfull condition (charge above the programmed capacity). The LEDs are activated with the onboard push-button switch.

Contacts are provided on the bq2110 for direct connection to the battery stack (BAT+, BAT-), the serial communications port (DQ), and the empty indicator (EMPTY). Please refer to the bq2010 data sheet for the specifics on the operation of the Gas Gauge.

Benchmarq configures the bq2110 based on the information requested in Table 1. The configuration defines the number of series cells, the nominal battery pack capacity, the self-discharge rate, and the LED display mode.

The onboard sense resistor accurately measures charge and discharge activity of the battery pack. The resistor value and type should be specified on the configuration sheet. The two options available are a 3W through hole type or a 1W surface mount type. Please refer to the application note entitled "A Tutorial for Gas Gauging" to select the proper value.



A module development kit is also available for the bq2110. The bq2110B-KT or bq2110LB-KT includes one configured module and the following:

1) A serial interface board that allows connection to the RS-232 port of an AT-compatible computer.
2) Menu-driven software with the bq2110 to display charge/discharge activity and to allow user interface to the bq2010 from any standard DOS PC.
3) Source code for the TSR.

Pin Descriptions

P1	**DQ/Serial communication port**
P2	**BAT+/Battery positive/pack positive**
P3	**No connect**
P4	**EMPTY/Empty indicator output**
P5	**GND/Ground**
P6	**PACK-Pack negative**
P7	**BAT-Battery negative**

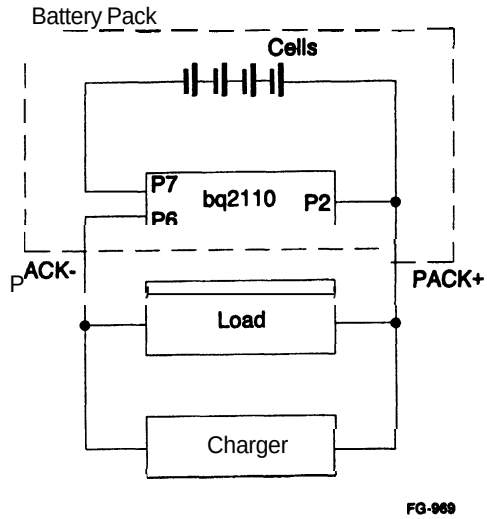
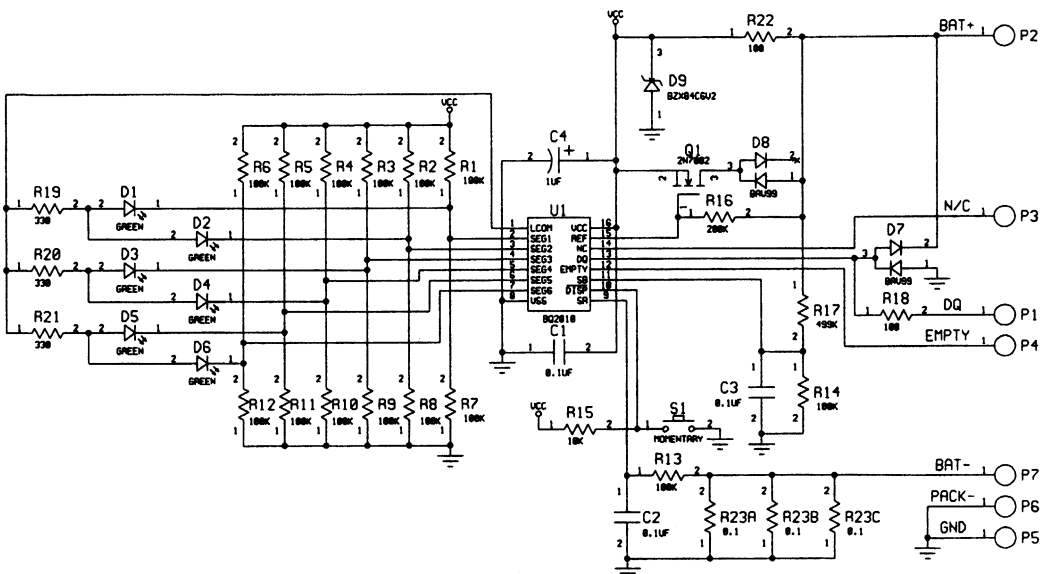


Figure 1. Module Connection Diagram

Table 1. bq2110 Module Configuration

Customer **Name:**	
Contact:	Phone:
Address:	
Sales Contact:	Phone:
Number of series battery cells (4–12)	
Battery type **(NiCd** or **NiMH)**	
Battery pack capacity **(mAh)**	
Discharge rate into load (A)	M i n . **Avg.** **Max.**
Sense resistor size in **mΩ** (0.1 **Ω** standard)	
Sense resistor type: **(Thru-hole (3W)** or surface mount (1W))	
Display mode (absolute or relative)	
LEDs and switch (Y/N)	

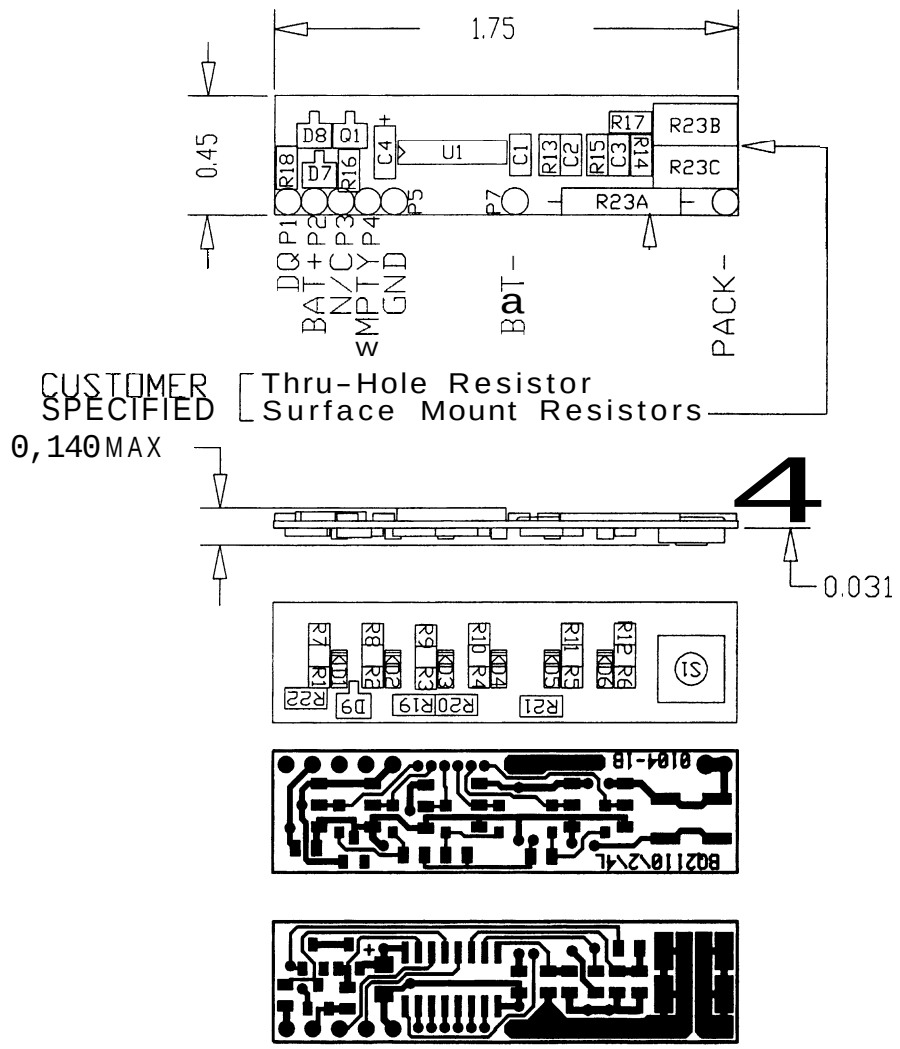
bq2110 Schematic



BD-963

Note: Schematic shows components which may not be placed on the board, depending upon the configuration.

bq2110 Board



BD-340

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Conditions
V_{CC}	Relative to V_{SS}	-0.3	+7.0	V	bq2010
All other pins	Relative to V_{SS}	-0.3	+7.0	V	bq2010
P_{SR}	Continuous sense resistor power dissipation		3	W	Thru-hole sense resistor
			1	W	Surface mount sense resistors
T_{OPR}	Operating temperature	0	+70	°C	Commercial
T_{STR}	Storage temperature	-40	+85	°C	

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
NumCell	Number of series cells in battery pack	4		12		
BAT+	Positive terminal of pack	GND	NumCell * 1.2V	NumCell * 1.8V	V	
BAT-	Negative terminal of pack	GND - 0.3		GND+2.0	V	
I_{CC}	Supply current at BAT+ terminal (no external loads)	-	200	300	µA	
R_{DQ}	Internal pull-down	500k			Ω[1]	
I_{OL}	Open-drain sink current DQ, EMPTY			5.0	mA[1]	
V_{OL}	Open-drain output low, DQ, EMPTY			0.5	V'	I_{OL} < 5mA
V_{IHDQ}	DQ input high	2.5			V[1]	
V_{ILDQ}	DQ input low			0.8	V[1]	
V_{OS}	Voltage offset			150	µV[1]	

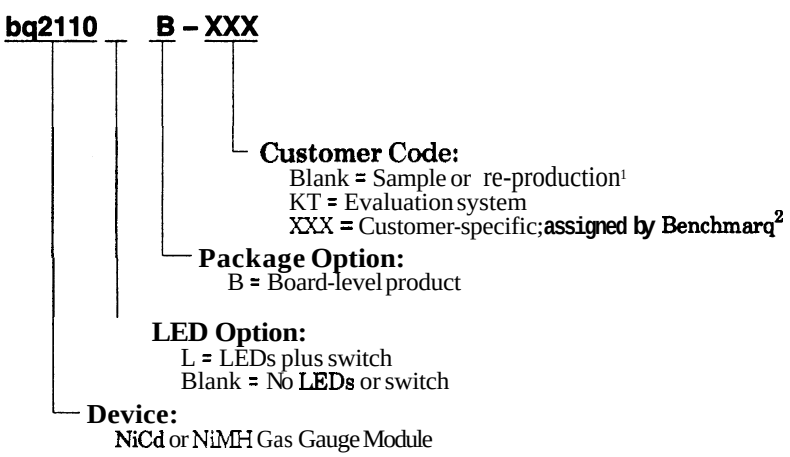
Note: 1. Characterized on PCB. IC 100% tested.

DC Voltage Thresholds ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDVF}	Final empty warning	0.93	0.95	0.97	V	BAT+/NumCell[1]
V_{EDV1}	F i t empty warning	1.03	1.05	1.07	V	BAT+/NumCell[1]
V_{MCV}	Maximum single-cell voltage	2.20	2.25	2.30	V	BAT+/NumCell[1]
V_{SRO}	Sense resistor range	-300		+2000	mV	$V_{SR} + V_{OS}$[2]
V_{SRQ}	Valid charge	375			µV	$V_{SR} + V_{OS}$ [2,3]
V_{SRD}	Valid discharge			-300	µV	$V_{SR} + V_{OS}$ [2,3]

Notes:
1. At SB input of bq2010
2. At SR input of bq2010.
3. Default value; value set in DMF register.

Ordering Information



Notes:
1. Requires configuration sheet (see Table 1)
2. Example production part number: bq2110LB-001

NiCd Gas Gauge Module with LEDs for High Discharge Rates

Features

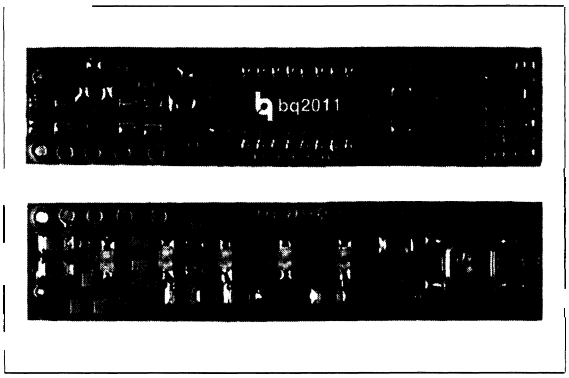
- ➤ Complete bq2011 Gas Gauge solution for NiCd packs in high discharge rate applications
- ➤ Five surface-mounted LEDs to display state-of-charge information
- ● Battery state-of-charge monitoring for 4- to 12-cell series applications
- ● On-board regulator allows direct connection to the battery
- ➤ Battery information available over a single-wire bidirectional serial port
- ● Nominal capacity pre-configured
- ● Compact size for battery pack integration

General Description

The bq2111L Gas Gauge Module provides a complete and compact solution for capacity monitoring of NiCd battery packs in high discharge rate applications such as power tools. Designed for battery pack integration, the bq2111L incorporates a bq2011 Gas Gauge IC, five surface-mounted LEDs, and the other discrete components necessary to monitor and display accurately the capacity of 4 to 12 series cells. The only external component required is a low-value sense resistor connected between GND and PACK-. Contacts are also provided on the bq2111L for direct connection to the battery stack and the serial communications port (DQ). The battery stack should be connected between BAT+ and GND. Please refer to the bq2011 data sheet for the specifics on the operation of the Gas Gauge.

Benchmarq configures the bq2111L based on the information requested in Table 1. The configuration defines the number of series cells and the nominal battery pack capacity. The bq211L module uses the absolute LED display to indicate battery capacity. In this mode, the remaining capacity is represented as a percentage of the programmed capacity.

The bq2111L can operate directly from four series cells within the pack using the LBAT+ supply input. For four series cell applications or applications using the on-board regulator, LBAT+ should be connected to BAT+. Please refer to Figure 1 for module connection illustrations.



A module development kit is also available for the bq2111L. The bq2111LB-KT includes one configured module and the following:

1) A serial interface board that allows connection to the RS-232 port of an AT-compatible computer.

2) Menu-driven software with the bq2111L to display charge/discharge activity and to allow user interface to the bq2011 from any standard DOS PC.

3) Source code for the TSR.

Pin Descriptions

P1	**DQ/Serial communication port**
P2	**BAT+/Battery positive/Pack positive**
P3	**LBAT+/Four-cell power**
P4	**PACK-Pack negative**
P5	**GND/Ground**

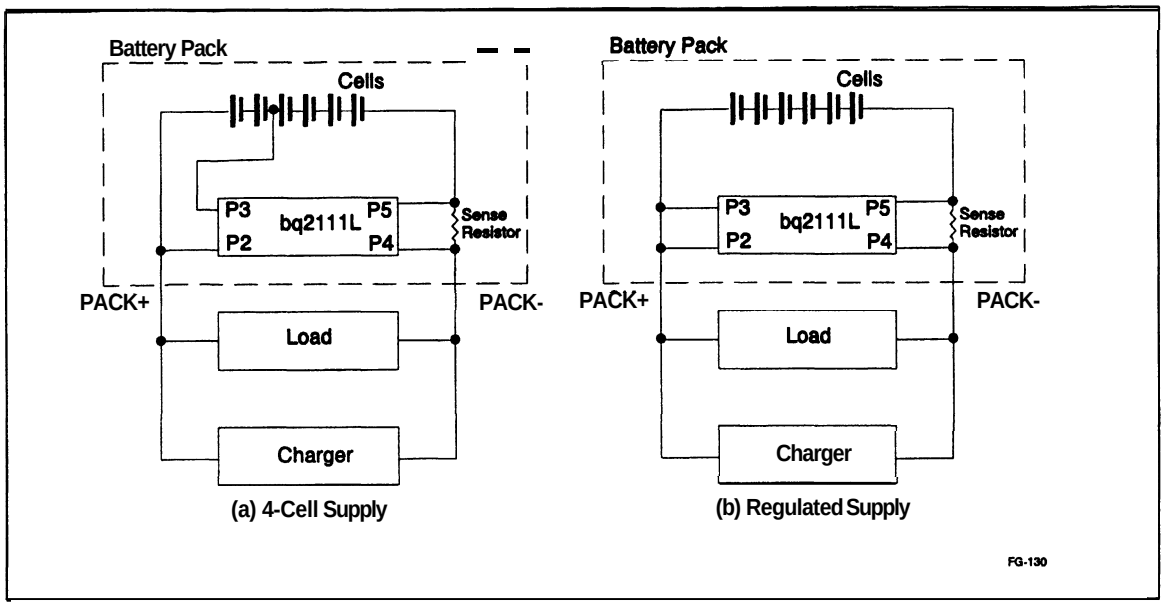


Figure 1. Module Connection Diagram

Table 1. bq2111L Module Configuration

Customer Name: _____

Contact: _____ Phone: _____

Address: _____

_____

Sales Contact: _____ Phone: _____

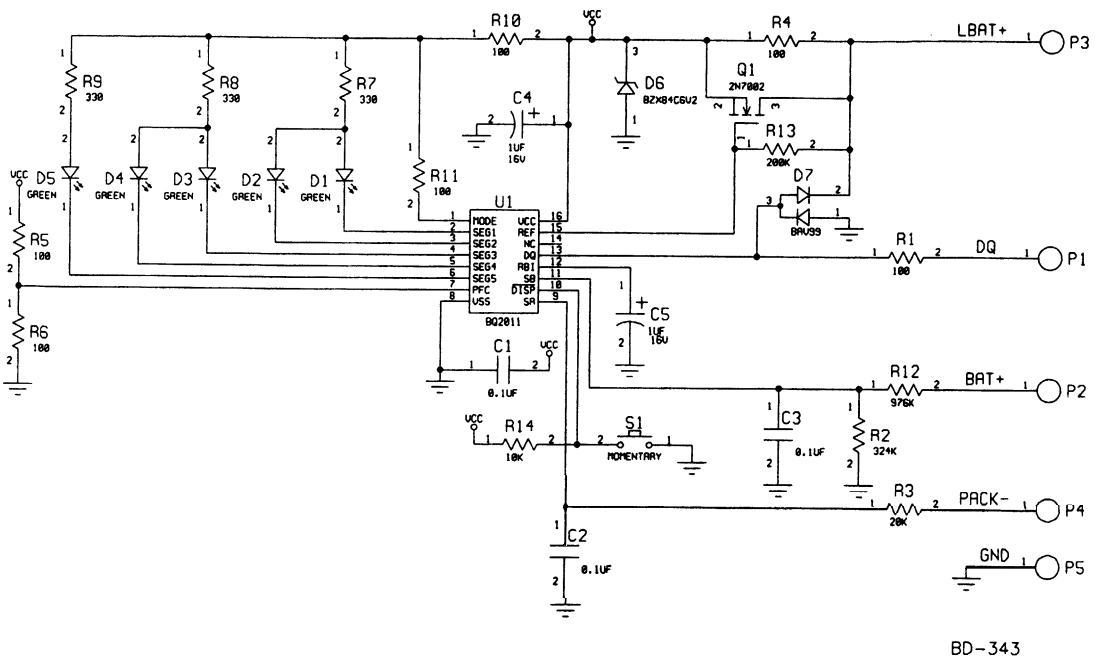
Number of series battery cells (4–12) _____

Sense resistor size in mΩ (0.005Ω standard)' _____

Battery pack capacity (mAh) _____

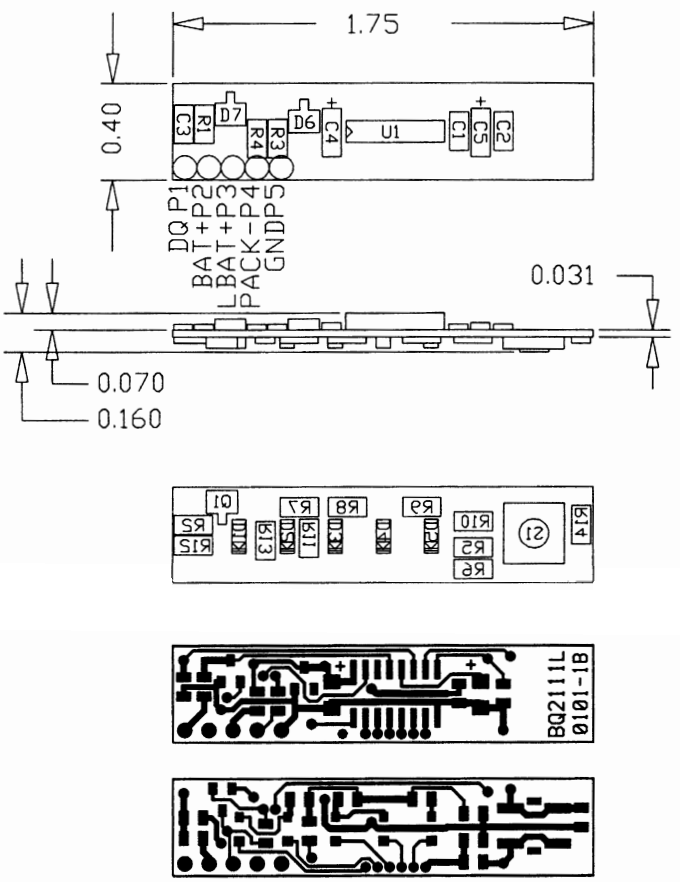
Note: 1. Sense resistor is not included with board.

bq2111L Example Schematic



Note: Schematic shows components which may not be placed on the board, depending upon the configuration.

bq2111L Board



BD-344

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to V_{SS}	-0.3	+7.0	V	bq2011
All other pine	Relative to Vss	-0.3	+7.0	V	bq2011
T_{OPR}	Operating temperature	0	+70	°C	Commercial
T_{STR}	Storage temperature	-40	+85	°C	

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

3

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
NumCell	Number of series cells in battery pack	4	-	12	-	
BAT+	Positive terminal of pack	GND	NumCell * 1.2V	NumCell * 1.8V	V	
V_{SR}	Voltage across the sense resistor, P4 to P5	-0.3		2	V	
V_{CC}	Supply voltage (direct cell operation) LBAT+	3.0	4.8	7.2	V	
I_{CC}	Supply current at BAT+ terminal (no external loads)	-	120	250	µA	
R_{DQ}	Internal pull-down	500k		-	Ω[1]	
I_{OL}	Open-drain sink current DQ			5.0	mA[1]	
V_{OL}	open-drain output low, DQ			0.5	V[1]	I_{OL} < 5mA
V_{IHDQ}	DQ input high	2.5			V[1]	
V_{ILDQ}	DQ input low			0.8	V[1]	
Vos	Voltage offset			150	µV[1]	

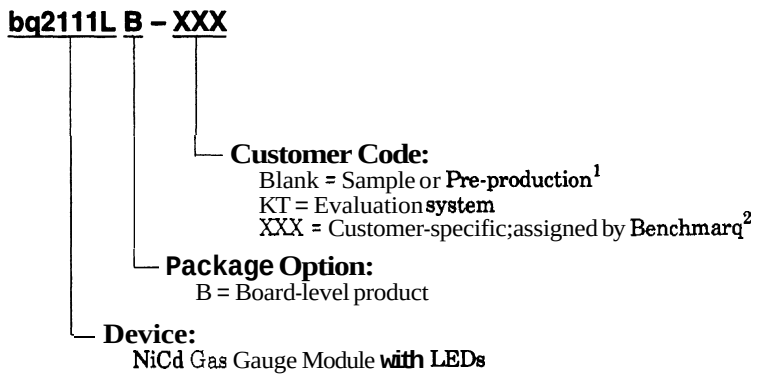
Note: 1. Characterized on PCB, IC 100% tested.

DC Voltage Thresholds ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDV}	Final empty warning	0.87	0.90	0.93	V	BAT+/NumCell[1]
V_{MCV}	Maximum single-cell voltage	1.95	2.0	2.05	V	BAT+/NumCell[1]
V_{SR1}	Discharge compensation threshold	20	50	75	mV	$V_{SR} + V_{OS}$[2]
V_{SR2}	Discharge compensation threshold	70	100	125	mV	$V_{SR} + V_{OS}$[2]
V_{SR3}	Discharge compensation threshold	120	150	175	mV	$V_{SR} + V_{OS}$[2]
V_{SR4}	Discharge compensation threshold	220	253	275	mV	$V_{SR} + V_{OS}$[2]
V_{SRO}	Sense resistor sense range	-300		+2000	mV	$V_{SR} + V_{OS}$[2]
V_{SRQ}	Valid charge			-400	µV	$V_{SR} + V_{OS}$[2]
V_{SRD}	Valid discharge	500			µV	$V_{SR} + V_{OS}$[2]

Notes: 1. At SB input of bq2011
2. At SR input of bq2011

Ordering Information

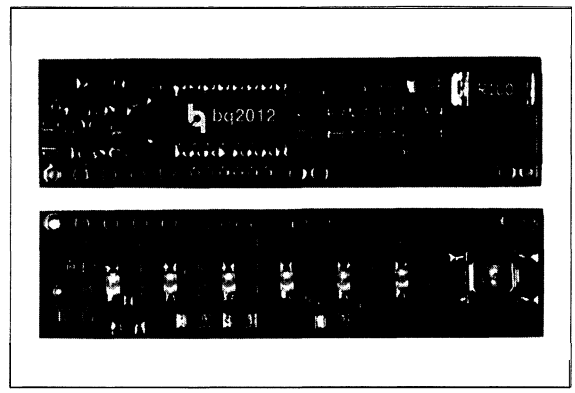


Notes: 1. Requires configuration sheet (see Table 1)
2. Example production part number bq2111LB-001

NiCd or NiMH Gas Gauge Module With Slow Charge Control

Features

- ➤ Complete bq2012 Gas Gauge solution for NiCd or NiMH battery packs
- ➤ Output for slow charge control of battery pack
- ➤ Battery information available over a single-wire bidirectional serial port
- ➤ Battery state-of-charge monitoring for 4- to 12-cell series applications
- ➤ On-board regulator allows direct connection to the battery
- ● "L" version includes push-button activated LEDs to display state-of-charge information
- ● Nominal capacity and cell chemistry pre-configured
- ● Compact size for battery pack integration



General Description

The bq2112 Gas Gauge Module provides a complete and compact solution for capacity monitoring of NiCd and NiMH battery packs. Designed for battery pack integration, the bq2112 incorporates a bq2012 Gas Gauge IC, a current sense resistor, and all other components necessary to accurately monitor and display the capacity of 3 to 12 series cells. The bq2112L includes six surface-mounted LEDs to display remaining capacity in 20% increments of the learned capacity (relative mode) or programmed capacity (absolute mode). The sixth LED is used in absolute mode to represent an overfull condition (charge above the programmed capacity). The LEDs are activated with the onboard push-button switch.

Contacts are provided on the bq2112 for direct connection to the battery stack (BAT+, BAT-), the serial communications port (DQ), the empty indicator (EMPTY), and the charge control output ($\overline{CHG}$). Please refer to the bq2012 data sheet for the specifics on the operation of the Gas Gauge.

Benchmarq configures the bq2112 based on the information requested in Table 1. The configuration defines the number of series cells, the nominal battery pack capacity, the self-discharge rate, and the LED display mode.

The onboard sense resistor accurately measures charge and discharge activity of the battery pack. The resistor value and type should be specified on the configuration sheet. The two options available are a 3W through hole type or a 1W surface mount type. Please refer to the application note entitled "A Tutorial for Gas Gauging" to select the proper value.

A module development kit is also available for the bq2112. The bq2112B-KT or bq2112LB-KT includes one configured module and the following:

1) A serial interface board that allows connection to the RS-232 port of an AT-compatible computer.
2) Menu-driven software with the bq2112 to display charge/discharge activity and to allow user interface to the bq2012 from any standard DOS PC.
3) Source code for the TSR.

Pin Descriptions

P1	**DQ/Serial communication port**
P2	**BAT+/Battery positive/pack positive**
P3	**$\overline{CHG}$/Charge control output**
P4	**EMPTY/Empty indicator output**
P5	**GND/Ground**
P6	**PACK-/Pack negative**
P7	**BAT-Battery negative**

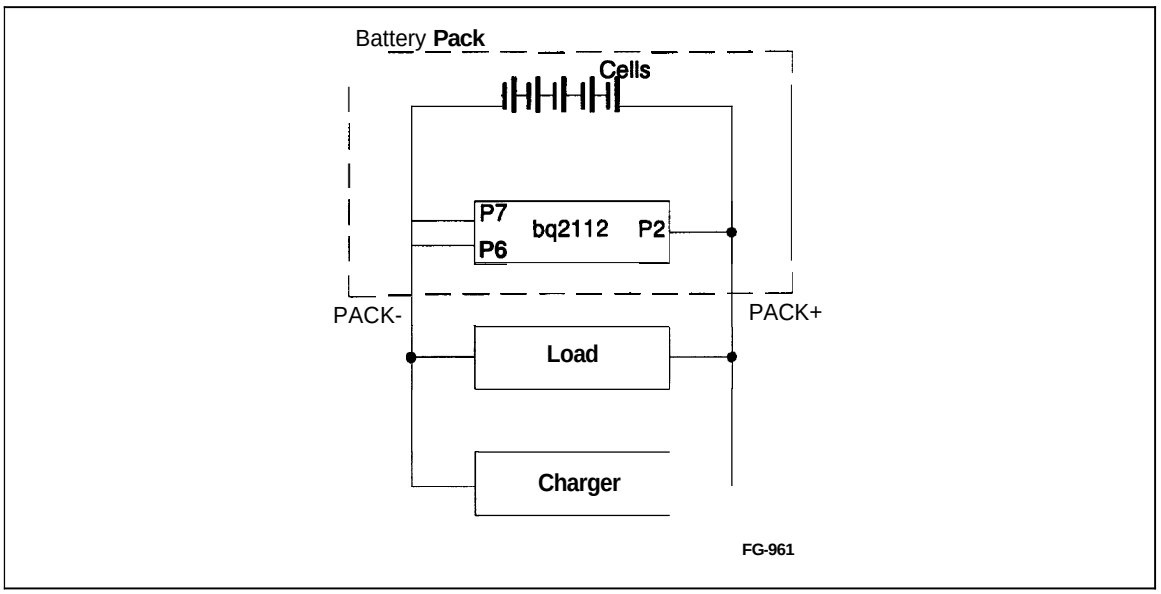
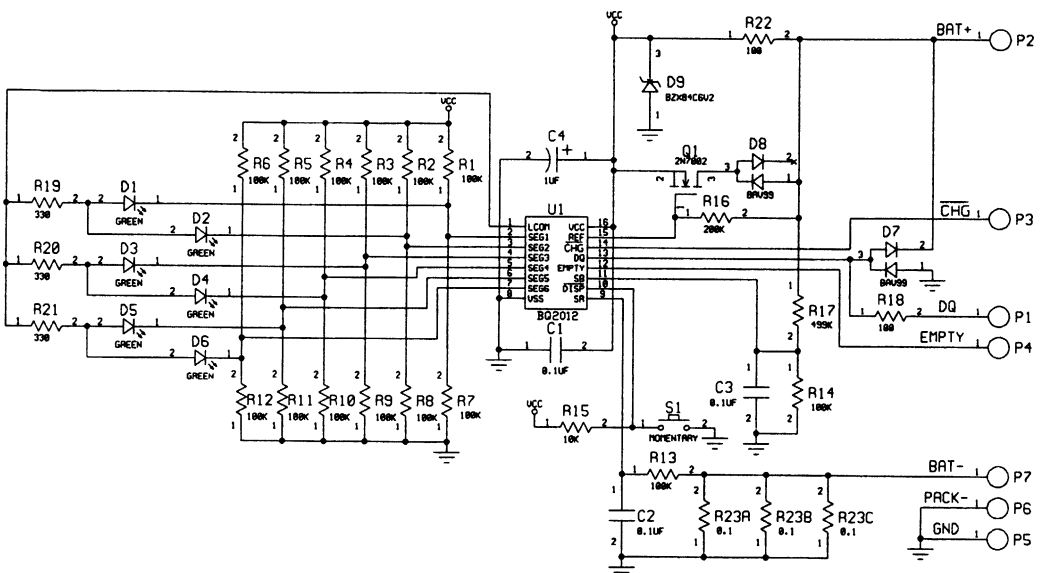


Figure 1. Module Connection Diagram

Table 1. bq2112 Module Configuration

Customer Name:	
Contact:	Phone:
Address:	
Sales Contact:	Phone:
Number of series battery cells (4–12)	
Battery type (NiCd or NiMH)	
Battery pack capacity (mAh)	
Discharge rate into load (A)	Min. Avg.____ Max.____
Sense resistor size in mΩ (0.1Ω standard)	
Sense resistor type: (Thru-hole (3W) or surface mount (1W))	
Display mode (absolute or relative)	
LEDs and switch (Y/N)	

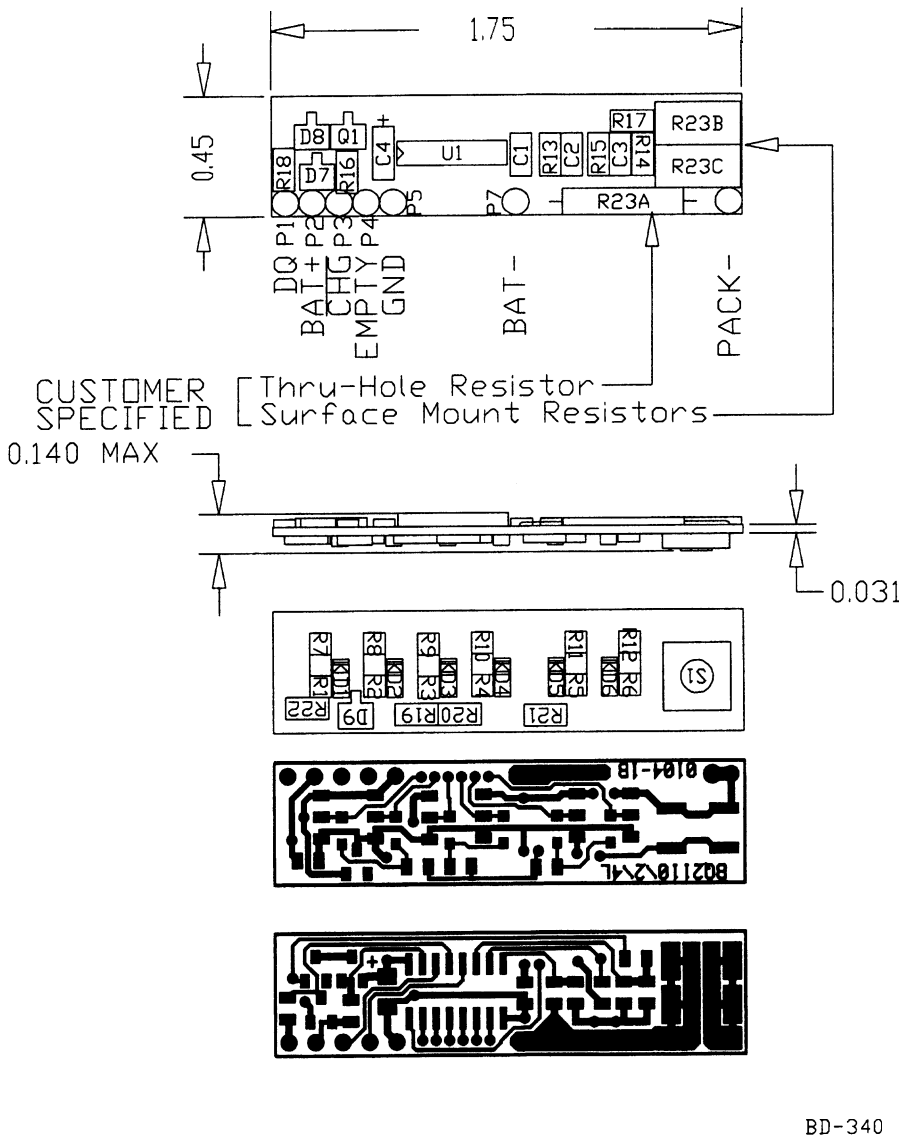
bq2112 Schematic



BD-964

Note: Schematic shows components which may not be placed on the board, depending upon the configuration.

bq2112 Board



Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Conditions
Vcc	Relative to Vss	-0.3	+7.0	V	bq2012
All other pine	Relative to Vss	-0.3	+7.0	V	bq2012
PSR	Continuous sense resistor power dissipation		3	W	Thru-hole sense resistor
			1	W	Surface mount sense resistor
TOPR	Operating temperature	0	+70	°C	Commercial
TSTR	Storage temperature	-40	+85	°C	

Note: Permanent device damage may *occur* if Absolute **Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to condition beyond the operational limits for extended periods of time may affect device reliability.

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
NumCell	Number of series cells in battery pack	4		12		
BAT+	Positive terminal of pack	GND	NumCell • 1.2V	NumCell • 1.8V	V	
BAT-	Negative terminal of pack	GND - 0.3		GND+2.0	V	
ICC	Supply current at BAT+ terminal (no external loads)	-	200	300	µA	
RDQ	Internal pull-down	500k			Ω[1]	
IOL	Open-drain sink current DQ, EMPTY, CHG			5.0	mA[1]	
VOL	Open-drain output low, DQ, E r n , CHG			0.5	V[1]	IOL < 5mA
VIHDQ	DQ input high	2.5			V[1]	
VILDQ	DQ input low			0.8	V[1]	
VOS	Voltage offset			150	µV[1]	

Note: 1. Characterized on PCB, IC 100% tested.

DC Voltage Thresholds ($T_A = T_{OPR}$)

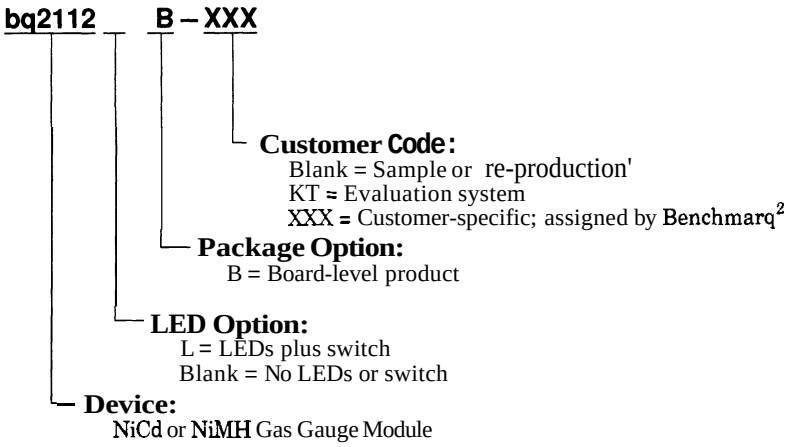
Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDVF}	Final empty warning	0.93	0.95	0.97	V	BAT+/NumCell[1]
V_{EDV1}	First empty warning	1.03	1.05	1.07	V	BAT+/NumCell[1]
V_{MCV}	Maximum single-cell voltage	2.20	2.25	2.30	V	BAT+/NumCell[1]
V_{SRO}	Sense resistor range	-300		+2000	mV	$V_{SR} + V_{OS}$[2]
V_{SRQ}	Valid charge	375			µV	$V_{SR} + V_{OS}$ [2,3]
V_{SRD}	Valid discharge			-300	µV	$V_{SR} + V_{OS}$ [2,3]

Notes: 1. At SB input of bq2012.

2. At SR input of bq2012.

3. Default value; value set in DMF register.

Ordering Information



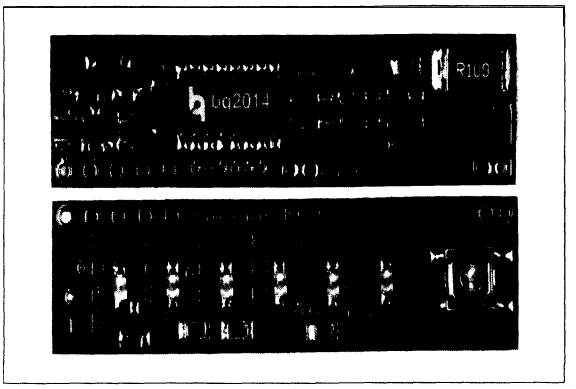
Notes: 1. Requires configuration sheet (see Table 1)

2. Example production part number: bq2110LB-002

NiCd or NiMH Gas Gauge Module With Charge Control Output

Features

- Complete bq2014 Gas Gauge solution for NiCd or NiMH battery packs
- Charge control output allows communication to external charge controller (bq2004)
- Battery information available over a single-wire bidirectional serial port
- Battery state-of-charge monitoring for 4- to 12-cell series applications
- On-board regulator allows direct connection to the battery
- "L" version includes push-button activated LEDs to display state-of-charge information
- Nominal capacity and cell chemistry pre-configured
- Compact size for battery pack integration



General Description

The bq2114 Gas Gauge Module provides a complete and compact solution for capacity monitoring of NiCd and NiMH battery packs. Designed for battery pack integration, the bq2114 incorporates a bq2014 Gas Gauge IC, a current sense resistor, and all other components necessary to accurately monitor and display the capacity of 4 to 12 series cells. The bq2114L includes five surface-mounted LEDs to display remaining capacity in 20% increments of the learned capacity (relative mode) or programmed capacity (absolute mode). The LEDs are activated with the onboard push-button switch.

Contacts are provided on the bq2114 for direct connection to the battery stack (BAT+, BAT-), the serial communications port (DQ), the empty indicator (EMPTY), and the charge control output (CHG). Please refer to the bq2014 data sheet for the specifics on the operation of the Gas Gauge.

Benchmarq configures the bq2114 based on the information requested in Table 1. The configuration defines the number of series cells, the nominal battery pack capacity, the self-discharge rate, and the LED display mode.

The onboard sense resistor accurately measures charge and discharge activity of the battery pack. The resistor value and type should be specified on the configuration sheet. The two options available are a 3W through hole type or a 1W surface mount type. Please refer to the application note entitled "A Tutorial for Gas Gauging" to select the proper value.

A module development kit is also available for the bq2114. The bq2114B-KT or bq2114LB-KT includes one configured module and the following:

1) A serial interface board that allows connection to the RS-232 port of an AT-compatible computer.
2) Menu-driven software with the bq2114 to display charge/discharge activity and to allow user interface to the bq2014 from any standard DOS PC.
3) Source code for the TSR.

Pin Descriptions

P1	**DQ/Serial communication port**
P2	**BAT+/Battery positive/pack positive**
P3	**CHG/Charge control output**
P4	**EMPTY/Empty indicator output**
P5	**GND/Ground**
P6	**PACK-/Pack negative**
P7	**BAT-/Battery negative**

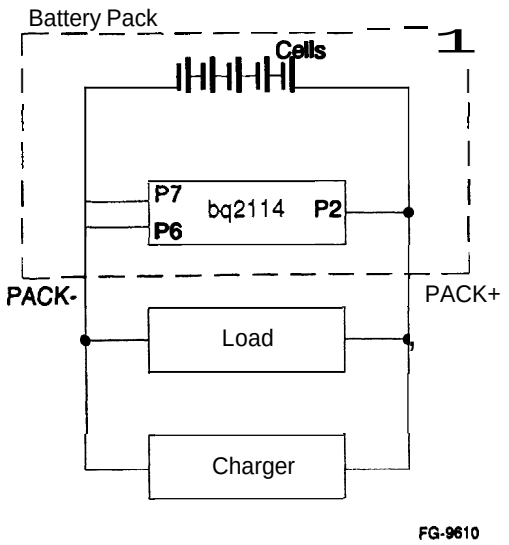
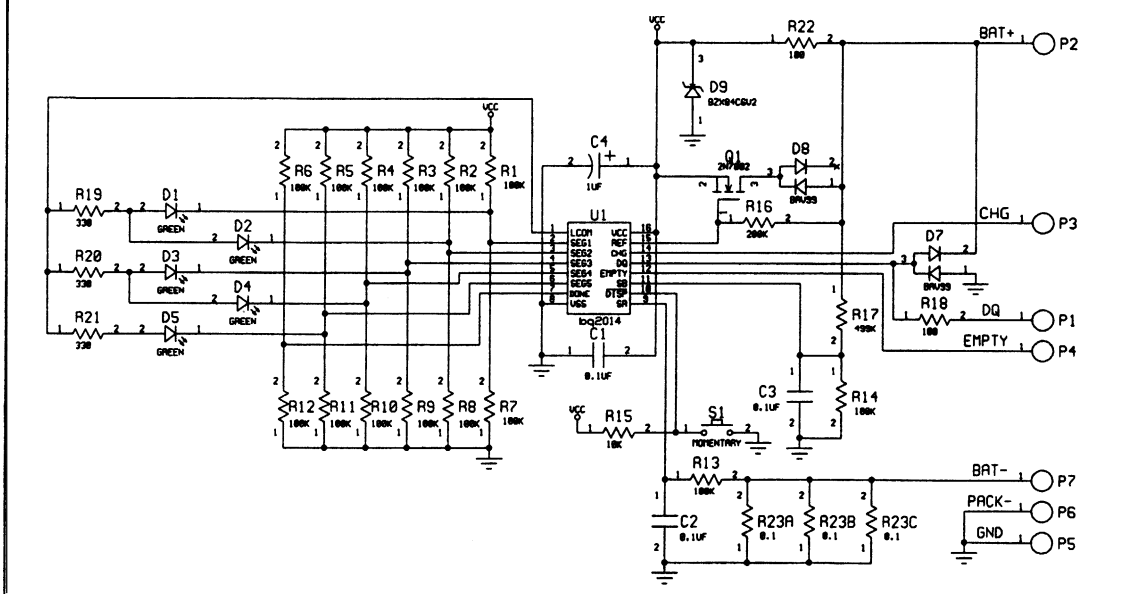


Figure 1. Module Connection Diagram

Table 1. bq2114 Module Configuration

Customer Name:	
Contact:	Phone:
Address:	
Sales Contact:	Phone:
Number of series battery cells (4–12)	
Battery type (NiCd or NiMH)	
Battery pack capacity (mAh)	
Discharge rate into load (A)	Min. Avg.____ Max.____
Sense resistor size in mΩ (0.1Ω standard)	
Sense resistor type: (Thru-hole (3W) or surface mount (1W))	
Display mode (absolute or relative)	
LEDs and switch (Y/N)	

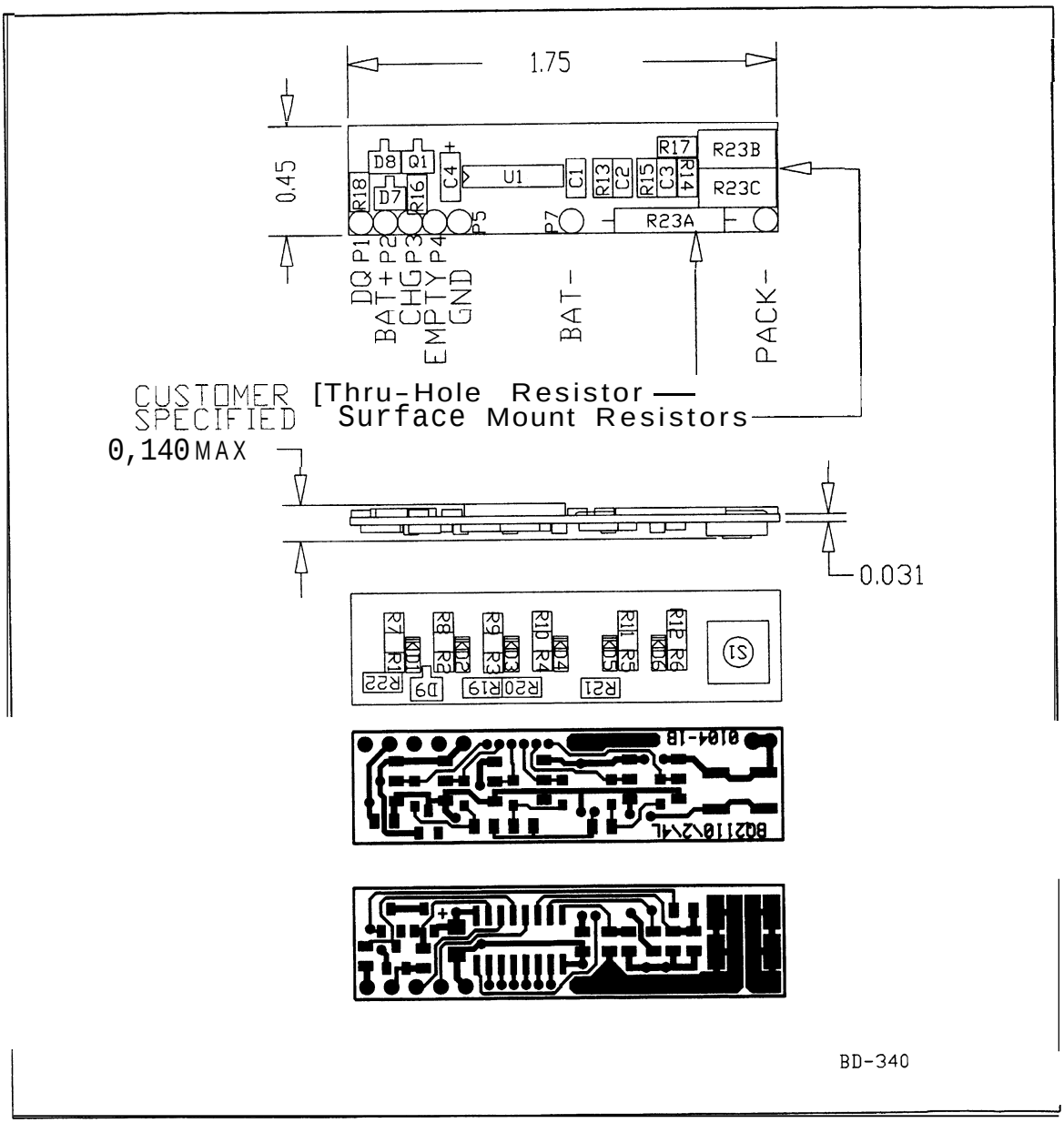
bq2114 Schematic



BD-965

Note: Schematic shows components which may not be placed on the board, depending upon the configuration.

bq2114 Board



BD-340

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Conditions
V_{CC}	Relative to V_{SS}	-0.3	+7.0	V	bq2014
All other pins	Relative to V_{SS}	-0.3	+7.0	V	bq2014
P_{SR}	Continuous sense resistor power dissipation		3	W	Thru-hole sense resistor
			1	W	Surface mount sense resistor
T_{OPR}	Operating temperature	0	+70	°C	Commercial
T_{STR}	Storage Temperature	-40	+85	°C	

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

3

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
NumCell	Number of series cells in battery pack	4		12		
BAT+	Positive terminal of pack	GND	NumCell * 1.2V	NumCell * 1.8V	V	
BAT-	Negative terminal of pack	GND - 0.3		GND+2.0	V	
I_{CC}	Supply current at BAT+ terminal (no external loads)		200	300	µA	
R_{DQ}	Internal pull-down	500k			Ω[1]	
I_{OL}	Open-drain sink current DQ, EMPTY, CHG			5.0	mA[1]	
V_{OL}	Open-drain output low, DQ, EMPTY, CHG			0.5	V[1]	I_{OL} < 5mA
V_{IHDQ}	DQ input high	2.5			V[1]	
V_{ILDQ}	DQ input low			0.8	V[1]	
V_{OS}	Voltage offset			150	µV[1]	

Note: 1. Characterized on PCB, IC 100% tested.

DC Voltage Thresholds ($T_A = T_{OPR}$)

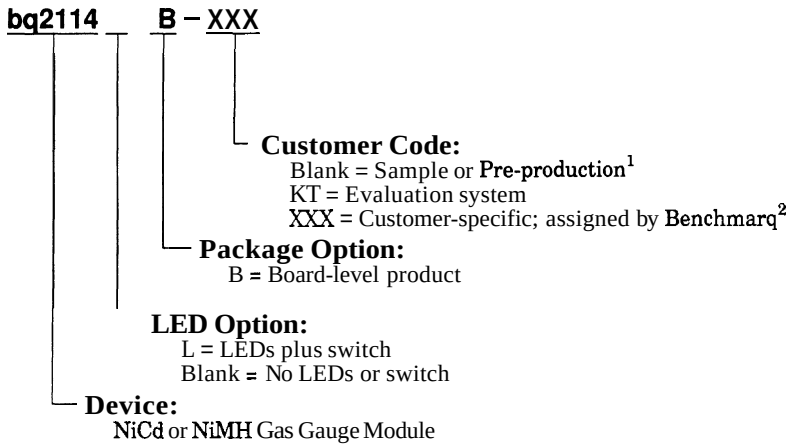
Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDVF}	Final empty warning	0.93	0.95	0.97	V	BAT+/NumCell[1]
V_{EDV1}	First empty warning	1.03	1.05	1.07	V	BAT+/NumCell[1]
V_{MCV}	Maximum single-cell voltage	2.20	2.25	2.30	V	BAT+/NumCell[1]
V_{SRO}	Sense resistor range	-300	-	+2000	mV	$V_{SR} + V_{OS}$[2]
V_{SRQ}	Valid charge	375	-	-	µV	$V_{SR} + V_{OS}$ [2, 3]
V_{SRD}	Valid discharge	-	-	-300	µV	$V_{SR} + V_{OS}$ [2, 3]

Notes: 1. At SB input of bq2014.

2. At SR input of bq2014.

3. Default value; value set in DMF register.

Ordering Information



Notes: 1. Requires configuration sheet (see Table 1)

2. Example production part number: bq2110LB-003

bq2150

Li-Ion Gas Gauge Module

Features

- ➤ Complete bq2050 Gas Gauge solution for Li-Ion battery packs
- ● Battery information available over a single-wire bidirectional serial port
- ● Battery state-of-charge monitoring for 2- to 4-cell senes applications
- ● On-board regulator allows direct connection to the battery
- ● 'L version includes push-button activated LEDs to display state-of-charge information
- ● Nominal capacity pre-configured
- ● Compact size for battery pack integration

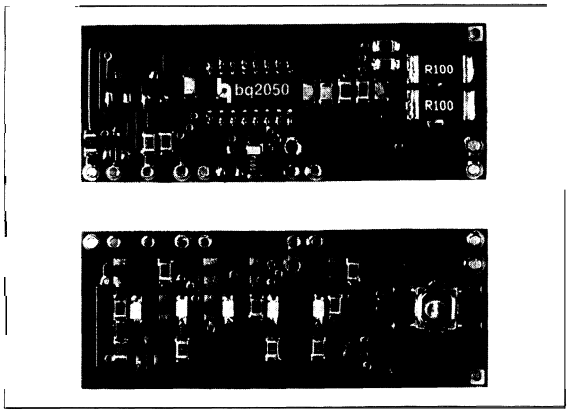
General Description

The bq2150 Gas Gauge Module provides a complete and compact solution for capacity monitoring of Li-Ion battery packs. Designed for battery pack integration, the bq2150 incorporates a bq2050 Gas Gauge IC, a current sense resistor, and all other components necessary to accurately monitor and display the capacity of 2 to 4 series cells.

The bq2150L includes five LEDs to display remaining capacity in 20% increments of the learned capacity. The LEDs are activated with the onboard push-button switch.

Contacts are provided on the bq2150 for direct connection to the battery stack (BAT+, BAT-) and the serial communications port (DQ). The RBI input provides backup power to the bq2050 in the event that the cells are removed or the battery is turned off. The bq2150 has a 1µF capacitor onboard connected to RBI to supply backup power for about an hour. In battery packs that use high-side FETs to control the charge/discharge of the Li-Ion cells, the RBI input can be wired to a single cell to provide prolonged data retention times. The SD input allows an external signal (active low) to turn the bq2050 IC off to minimize internal current consumption of the battery pack and maximize storage life of the pack in the system. When turned off, the bq2050 is non-functional, and the RBI power source maintains register information. Please refer to the bq2050 data sheet for the specifics on the operation of the Gas Gauge.

Benchmarq configures the bq2150 based on the information requested in Table 1. The configuration defines the number of series cells, the nominal battery pack capacity, and the Li-Ion battery type (coke or graphite anode).



The onboard sense resistor accurately measures the charge and discharge activity of the battery pack. The sense resistor value should also be specified on the configuration sheet. The sense resistor value depends on the application. The two options available are a 3W through-hole type and a 1W surface-mount type. Please refer to the application note entitled "A Tutorial for Gas Gauging," to select the proper value.

A module development kit is also available for the bq2150. The bq2150B-KT or the bq2150LB-KT includes one configured module and the following:

1) A serial interface board that allows connection to the RS-232 port of an AT-compatible computer.
2) Menu-driven software to display charge/discharge activity and to allow user interface to the bq2050 from any standard DOS PC.
3) Source code for the TSR.

Pin Descriptions

P1	**DQ/Serial Communications port**
P2	**No connect**
P3	**BAT+/Battery positive/pack positive**
P4	**SD/Shutdown**
P5	**RBI/Register backup input**
P6	**GND/Ground**
P7	**PACK-/Pack negative**
P8	**BAT-Battery negative**

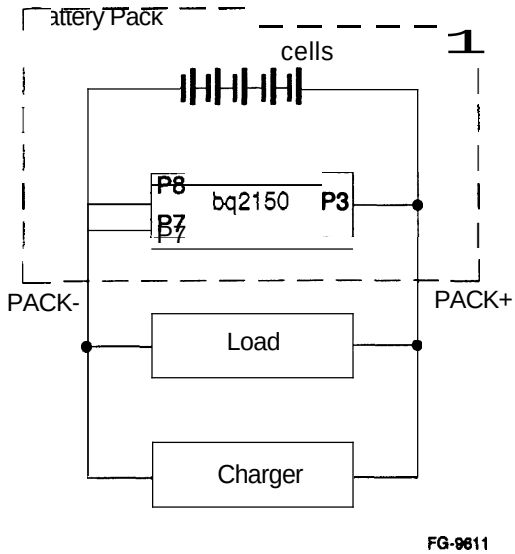


Table 1. bq2150 Module Configuration

Customer Name: _____

Contact: _____ Phone: _____

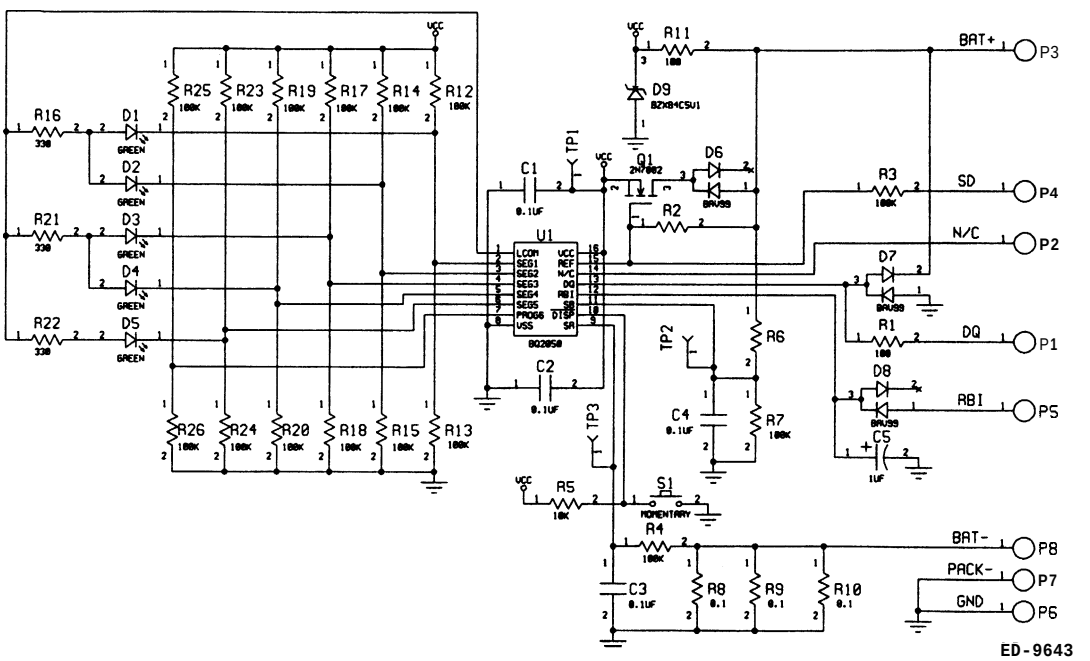
Address: _____

_____

Sales Contact: _____ Phone: _____

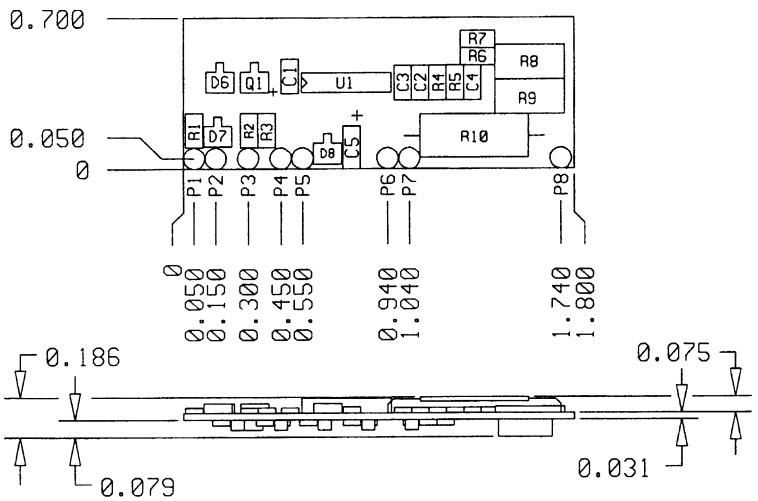
Number of series battery cells (2– 4)	_____
Coke or graphite cell anode	_____
Battery pack **capacity (mAh)**	_____
Discharge rate into load (A)	min. _____ avg. _____ **max.** _____
Sense resistor size in **mΩ** (0.1 standard)	_____
Sense resistor type **(Thru-hole** (3W) or surface-mount **(1W))**	_____
Nominal Available Capacity after reset (Programmed Capacity or Zero)	_____
Self-discharge compensation **(Y/N)**	_____
LEDs and switch (Y/N)	_____

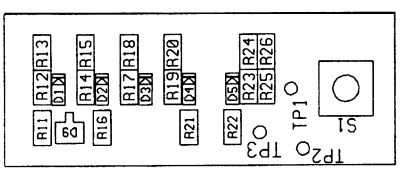
bq2150 Schematic

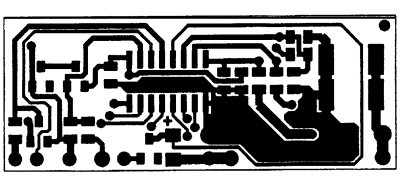


Note: Schematic shows components which may not be placed on the board, depending upon the configuration.

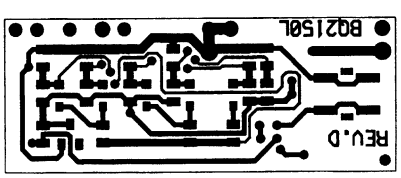
bq2150 Board







LAYER 1



LAYER 2

BD-9656

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Conditions
V_{CC}	Relative to V_{SS}	-0.3	+7.0	V	bq2050
All other pins	Relative to V_{SS}	-0.3	+7.0	V	bq2050
P_{SR}	Continuous sense resistor power dissipation		3	W	Thru-hole sense resistor
		-	1	W	Surface-mount sense resistor
T_{OPR}	Operating temperature		+70	°C	Commercial
T_{STR}	Storage temperature	-40	+85	°C	

Note: Permanent device damage may occur if **Absolute Maximum Ratings are** exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
NumCell	Number of series cells in battery pack	2		4		
BAT+	Positive terminal of pack	GND	NumCell * 3.6V	NumCell * 5.4V	V	
BAT-	Negative terminal of pack	GND - 0.3		GND+2.0	V	
I_{CC}	Supply current at BAT+ terminal (no external loads)	-	200	300	µA	
R_{DQ}	Internal pull-down	500k			Ω[1]	
I_{OL}	Open-drain sink current DQ	-		5.0	mA[1]	
V_{OL}	Open-drain output low, I_{OL} DQ	-	-	0.5	V[1]	I_{OL} < 5mA
V_{IHDQ}	DQ input high	2.5			V[1]	
V_{ILDQ}	DQ input low			0.8	V[1]	
V_{OS}	Voltage offset			150	µV[1]	

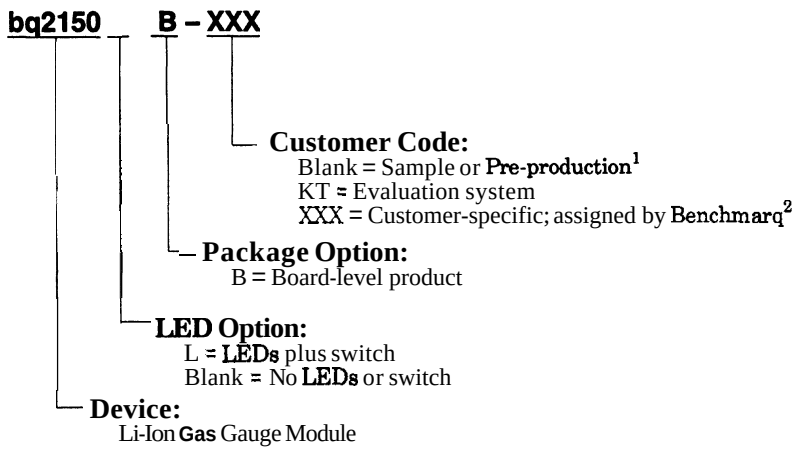
Note: 1. Characterized on PCB, IC 100% tested.

DC Voltage Thresholds ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDVF}	Final empty warning	1.45	1.47	1.49	V	BAT+/(2*NumCell)[1]
V_{EDV1}	First empty warning	1.50	1.52	1.55	V	BAT+/(2*NumCell)[1]
V_{MCV}	Maximum single-cell voltage	2.20	2.25	2.30	V	BAT+/(2*NumCell)[1]
V_{SRO}	Sense range	-300		+2000	mV	SR, $V_{SR} + V_{OS}$[2]
V_{SRQ}	Valid charge	210			µV	$V_{SR} + V_{OS}$ [2, 3]
V_{SRD}	Valid discharge			-200	µV	$V_{SR} + V_{OS}$ [2, 3]

Note:
1. At SB input of bq2050
2. At SR input of bq2050.
3. Default value; value set in DMF register.

Ordering Information



Notes:
1. Requires configuration sheet (Table 1)
2. Example production part number: bq2150LB-001

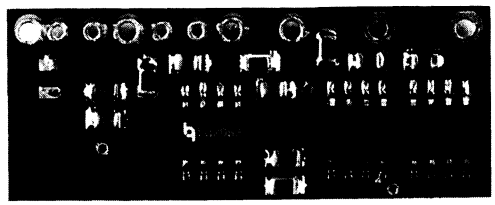
BENCHMARQ

bq2153

Li-Ion Pack Supervisor Module

Features

- Complete and compact lithium-ion pack supervisor
- Provides overvoltage, undervoltage, and overcurrent protection for three or four series Li-Ion cells
- ➤ Designed for battery pack integration
  - On-board charge and discharge control FETs
  - Direct connection for series battery terminals
  - Measures 1.40 X 0.56 inches
- Low standby and operating currents
- Low on-resistance FETs



3

General Description

The bq2153 provides a complete solution for the supervision of three or four series Li-Ion cells. Designed for battery pack integration, the bq2153 incorporates a bq2053 Pack Supervisor, two FETs, and all other components required to monitor overvoltage, undervoltage, and overcurrent conditions. The board provides direct connections for the negative and positive terminals of each cell. See Table 2. Please refer to the bq2053 data sheet for specific information on the operation of the bq2053.

Benchmarq configures the bq2153 based on the information requested in Table 1.

Pin Descriptions

1P	**Battery 1 positive input/pack positive**
1N	**Battery 1 negative input**
2N	**Battery 2 negative input**
3N	**Battery 3 negative input**
4N	**Battery 4 negative input**
PK-	**Pack negative**

Table 1. bq2153 Module Configuration

Customer Name: _____

Contact: _____ Phone: _____

Address: _____

_____

Sales Contact: _____ Phone: _____

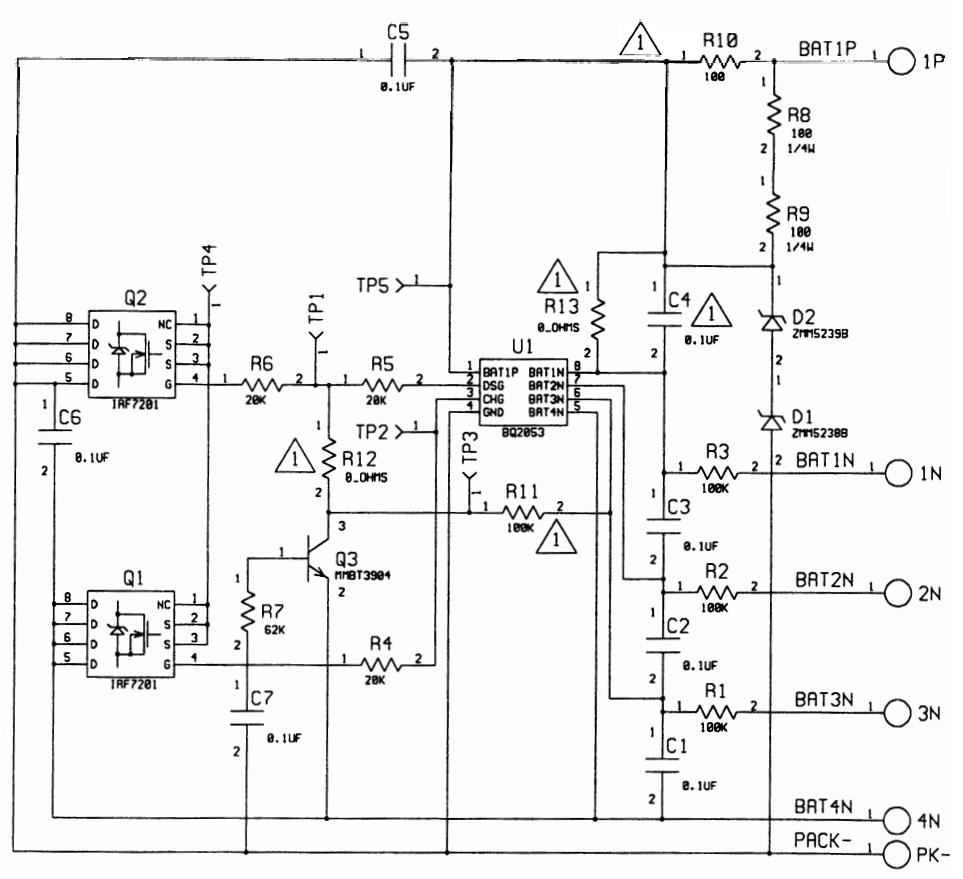
Number of series cells (3 or 4) _____

Overvoltage threshold (4.25V default) _____

Table 2. Pin Connections

Number of Cells	On-board Configuration	External Connections
3 cells	1N tied to 1P	1P – Positive terminal of first call
		2N – Negative terminal of first cell
		3N – Negative terminal of second cell
		4N– Negative terminal of third cell
4 cells		1P – Positive terminal of first cell
		1N – Negative terminal of first cell
		2N – Negative terminal of second cell
		3N– Negative terminal of third cell
		4N – Negative terminal of fourth cell

bq2153 Schematic

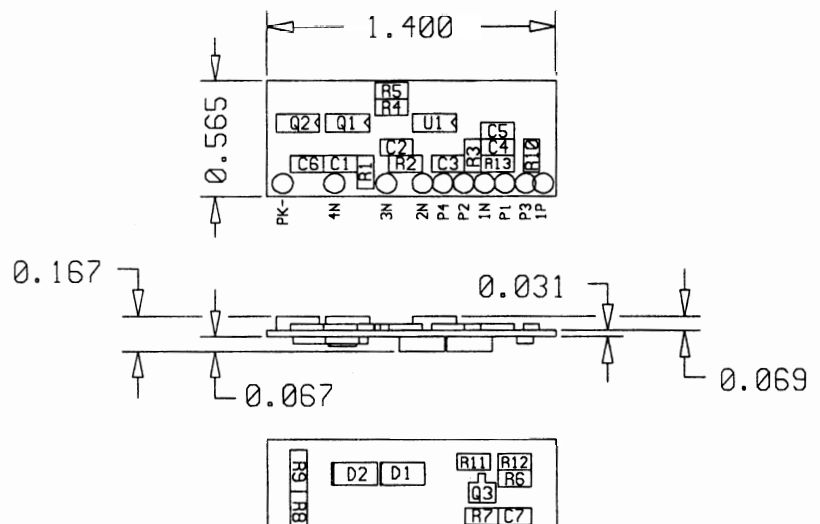


Notes:

1. **Component may or may not be placed depending on the configuration.**

BD-2153b

bq2153 Board



BD-2153a

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_T	Voltage applied on any pin relative to 1P	-.18 to +0.31	V	
T_{OM}	Operating temperature	0 to +70	°C	Commercial
T_{STG}	Storage temperature	-40 to +85	°C	

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should e ed to l Recommended DC Operating liti detailed in this data sheet. Exposure to conditions beyond th l limits for ded periods f ti may affect levi li

3

DC Electrical Characteristics ($T_A = T_{OPR}$)

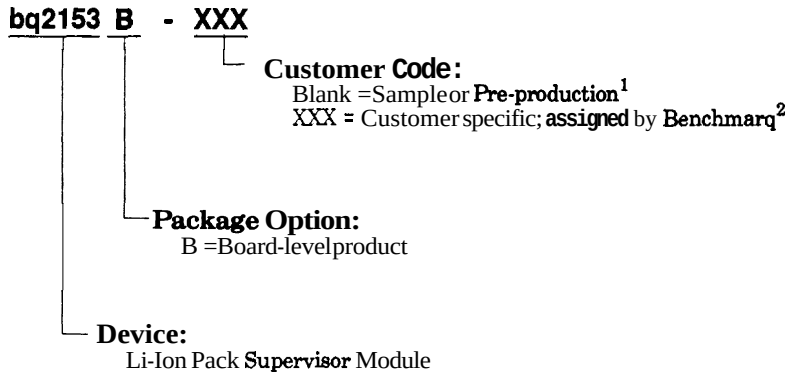
Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
V_{OP}	Operating voltage, 1P to 4N	6.0		18	V	
I_{CC}	Operating current 3-cell		12	25	µA	
	Operating current 4-cell		25	40	µA	
I_{CCLP}	Low power current			1	µA	
$R_{1N, 2N, 3N}$	Battery input impedance		10		MΩ	
R_{FET}	FET on resistance			50	mΩ	Per FET
I_D	Continuous charge/discharge current		2	4	A	

DC Thresholds ($T_A = T_{OPR}$)

Symbol	Parameter	Value	Tolerance	Unit
V_{OV}	Overvoltage limit	4.25	± 1.5%	V
V_{CE}	Charge enable voltage	Vov - 100mV	± 50mV	V
V w	Undervoltage limit	2.3	± 100mV	V
V_{OC}	Overcurrent limit, 4N to PK-	± 250	± 25	mV

Note: Standard device. Contact Benchmarq for different threshold options.

Ordering Information



Notes:
1. Requires configuration sheet (see Table 1)
2. Example production part number: bq2153B-001

BENCHMARQ

bq2164

NiCd or NiMH Gas Gauge Module with Fast Charge Control

Features

- ➤ Complete bq2004/bq2014 battery management solution for NiCd or NiMH pack
- ➤ Accurate battery state-of-charge monitoring
- ● Reliable fast charge termination
- ● Automatic full capacity calibration
- ➤ Battery information available over a single-wire bi-directional serial port
- ➤ Nominal capacity, cell chemistry, and charge control parameters pre-configured
- ➤ Compact size for battery pack integration

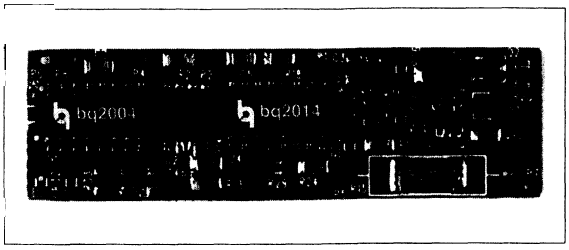
General Description

The bq2164 Gas Gauge Module provides a complete and compact battery management solution for NiCd and NiMH battery packs. Designed for battery pack integration, the bq2164 combines the bq2014 Gas Gauge IC with the bq2004 Fast Charge IC on a small printed circuit board. The board includes all the necessary components to accurately monitor the capacity and reliably terminate fast charge of 5 to 10 series cells.

The gas gauge IC uses the onboard sense resistor to track charge and discharge activity of the battery pack. The fast charge IC gates a current-limited or constant-current charging supply connected to PACK+. Charging termination is based on $\Delta T/\Delta t$ or $-\Delta V/PVD$, maximum temperature, time, and voltage. The bq2004 signals charge completion to the bq2014 to indicate full capacity. The charge complete signal to the gas gauge eliminates the need to fully cycle the battery pack to initially calibrate full pack capacity.

Contacts are provided on the bq2164 for direct connection to the battery stack (BAT+, BAT-), the gas gauge's communications port (DQ), and the thermistor (THERM+, THERM). The thermistor is required for temperature fast charge termination. Please refer to the bq2004 and bq2014 data sheets for the specifics on the operation of the gas gauge and the fast charge ICs.

Benchmarq configures the bq2164 based on the information requested in Table 1. The configuration defines the number of series cells, the nominal battery pack capacity, the self-discharge rate, and the fast charge control parameters. The control parameters depend on the charge rate, cell chemistry and termination technique specified in the configuration table. They consist of the fast



3

charge hold-off, safety timers, and the pulse trickle rate as shown in the bq2004 data sheet. The bq2164 is optimized for temperature termination with the thermistor provided with the development kit.

The sense resistor value and type should also be specified on the configuration sheet. The two options available are a 3W through-hole type or a 1W surface-mount type. Please refer to the application note entitled "A Tutorial for Gas Gauging" to select the proper value.

A module development kit is also available for the bq2164. The bq2164B-KT includes one configured module and the following:

1) A serial interface board that allows connection to the RS-232 port of an AT-compatible computer.
2) Menu-driven software with the bq2164 to display charge/discharge activity and to allow user interface to the bq2014 from any standard DOS PC.
3) Source code for the TSR.
4) A Philips 10K NTC Thermistor type 2322-640-63103.

Pin Description

P1	DQ/Serial communication port
P2	BAT+/Battery positive
P3	PACK+/Pack positive
P4	PACK-Pack negative
P5	BAT-Battery negative
P6	THERM+/Thermistor positive
P7	THERM-/Thermistor negative
P8	MOD/Fast charge control output

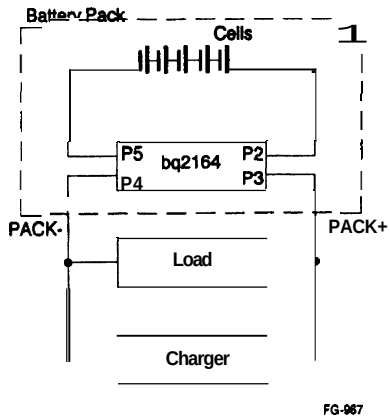


Figure 1. Module Connection Diagram

Table 1. bq2164 Module Configuration

Customer Name: _____

Contact: _____ Phone: _____

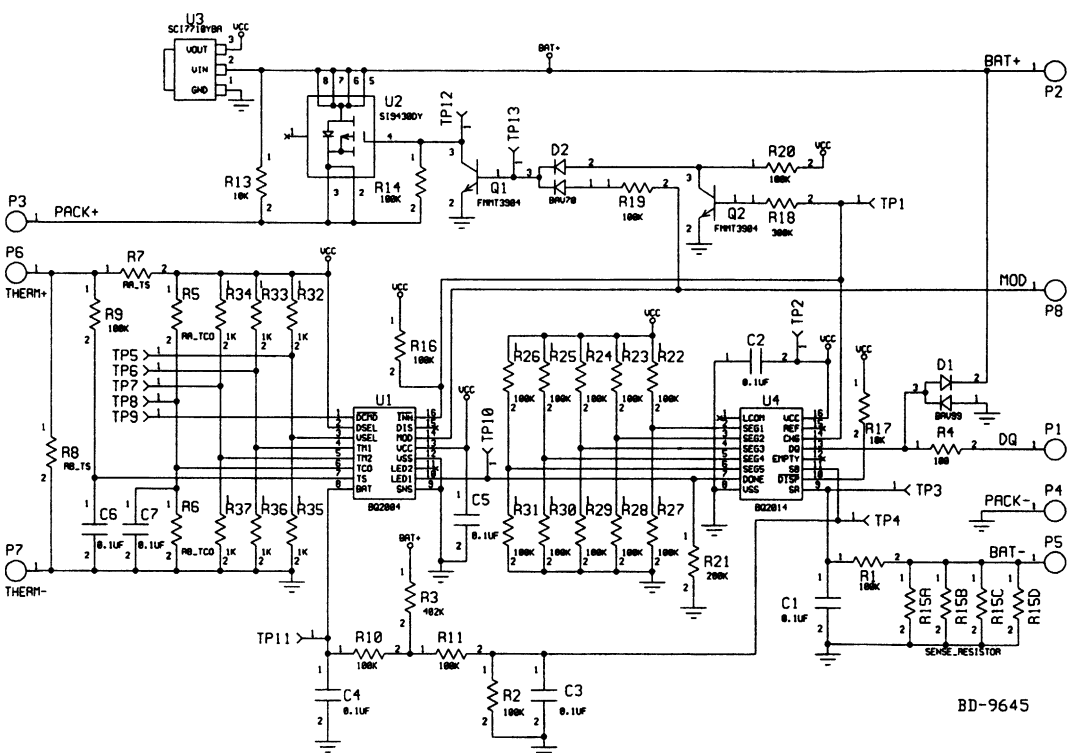
Address: _____

_____

Sales Contact: _____ Phone: _____

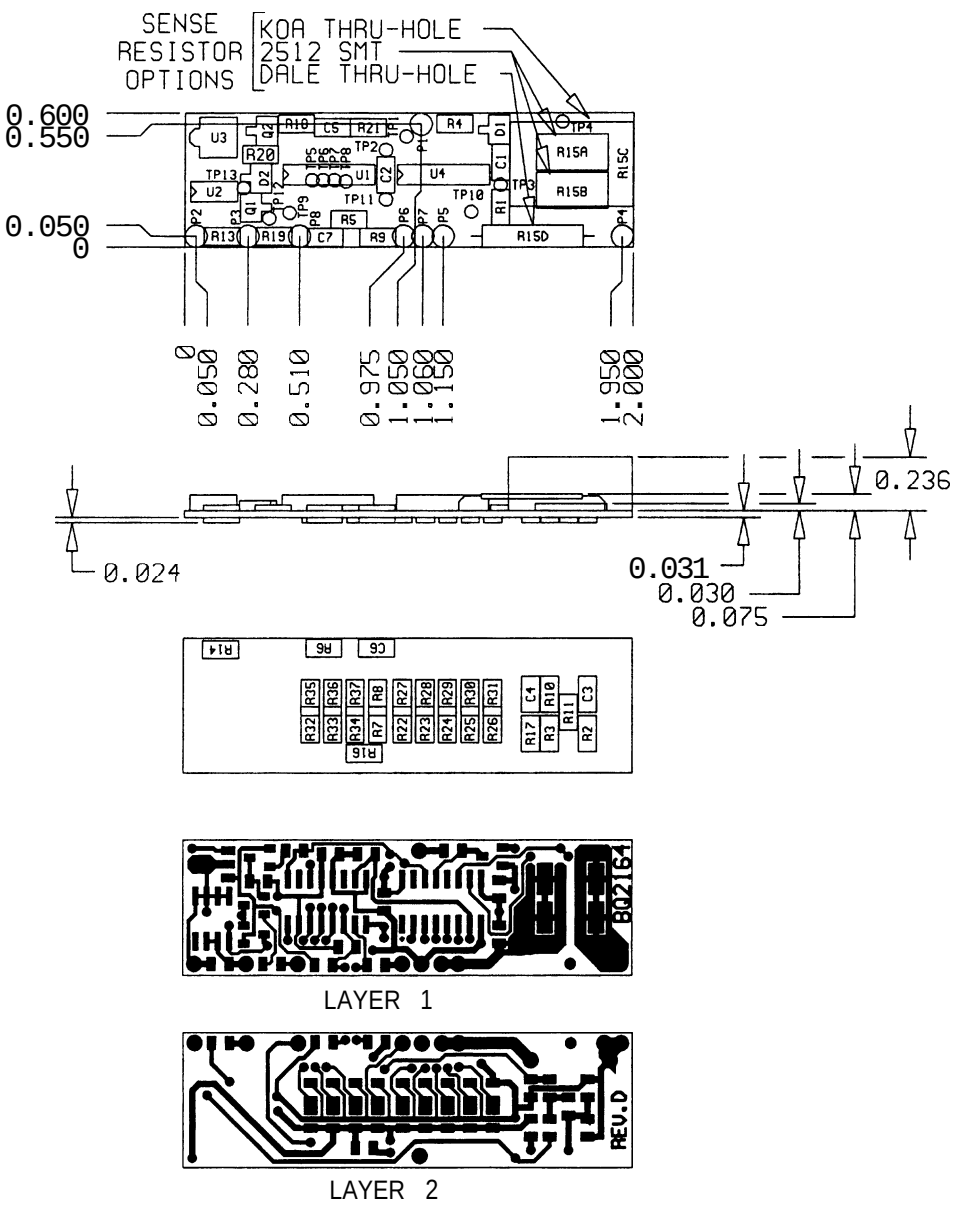
Number of series battery cells (5–10)	_____
Battery type (NiCd or NiMH)	_____
Battery pack capacity (mAh)	_____
Discharge rate into load (A)	Min. _____ **Avg.** _____ Max. _____
Sense resistor type: (Thru-hole (3W) or surface-mount(1W))	_____
Sense resistor size in m a (0.1Ω standard)	_____
Fast charge current (A)	_____
Charge voltage (V)	_____
Temperature termination (enabled/disabled)	_____
PVD or –AV termination	_____

bq2164 Schematic



Note: Schematic shows components which may not be placed on the board, depending upon the configuration.

bq2164 Board



Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
P_{SR}	Continuous sense resistor power dissipation	-	3	W	Thru-hole sense resistor
		-	1	W	Surface-mount sense resistor
V_{CHG}	Charging voltage	-	20	V	
T_{OPR}	Operating temperature	0	+70	°C	Commercial
T_{STR}	Storage temperature	-40	+85	°C	

Note: Permanent device damage may occur if Absolute **Maximum Ratings** are **exceeded.** Functional operation should be limited to the Recommended DC Operating Conditions detailed in **this** data sheet. **Exposure** to conditions beyond the operational limits for extended periods of time may ***affect*** device **reliability.**

3

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
NumCell	Number of cells in battery pack	5		10		
BAT+	Positive terminal of pack	GND	NumCell * 1.2V	NumCell * 1.8V	V	
BAT-	Negative terminal of pack	GND - 0.3		GND+2.0	V	
I_{CC}	Supply current at BAT+ terminal (no external loads)		200	300	µA	
I_{CHG}	Charge current			2	A	
I_{DSCHG}	Discharge current			2	A	
R_{DQ}	Internal pull-down	500k			Ω[1]	
I_{OL}	Open-drain sink current DQ			5.0	mA[1]	
V_{OL}	Open-drain output low, DQ	-		0.5	V[1]	I_{OL} < 5mA
V_{IHDQ}	DQ input high	2.5			V[1]	
V_{IHDQ}	DQ input low			0.8	V[1]	
V_{OS}	Voltage offset			150	µV[1]	

Note: **1.** Characterized on **PCB,** IC 100% tested.

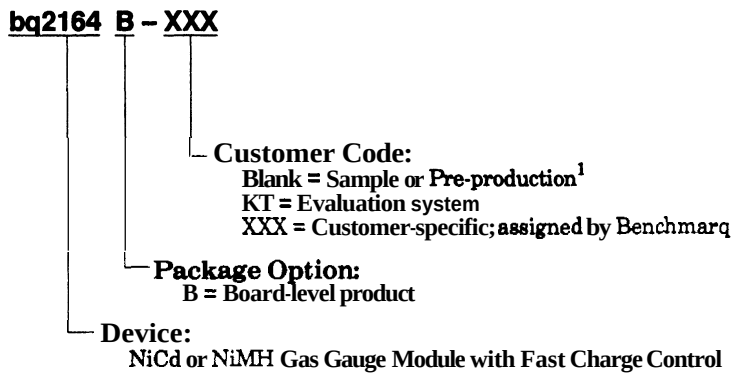
DC Voltage and Temperature Thresholds ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDVF}	Final empty warning	0.93	0.95	0.97	V	BAT+/NumCell[1]
V_{EDV1}	First empty warning	1.03	1.05	1.07	V	BAT+/NumCell[1]
V_{MCV}	Maximum single-cell voltage	2.20	2.25	2.30	V	BAT+/NumCell[1]
V_{SRO}	SR sense range	-300		+2000	mV	$V_{SR} + V_{OS}$[2]
V_{SRQ}	Valid charge	375			µV	$V_{SR} + V_{OS}$ [2,3]
V_{SRD}	Valid discharge			-300	µV	$V_{SR} + V_{OS}$ [2,3]
V_{SR1}	Discharge compensation threshold	-120	-150	-180	mV	$V_{SR} + V_{OS}$[2]
T_{LTF}	Low-temperature charging fault		10		°C	Low-temperature charge inhibit/terminate[4]
T_{HTF}	High-temperature charging fault		45		°C	High-temperature charge inhibit
V_{EDVC}	Minimum charging cell voltage		1		V	Minimum cell voltage to initiate charge
V_{MCVC}	Maximum charging cell voltage		2		V	Maximum cell voltage to initiate or continue charge
$R_{\Delta T/\Delta t}$	ΔT/Δt charge termination rate	-	1	-	°C/ min.	@ 30°C
T_{TCO}	Maximum charging temperature		50		°C	High-temperature charge termination

Notes:

1. At SB input of bq2014.
2. At SR input of bq2014.
3. Default value; value set in DMF register.
4. PVD termination disables the low-temperature fault charge termination.

Ordering Information



Notes:
1. Requires configuration sheet (Table 1)
2. Example production part number: bq2164B-001

Notes

BENCHMARQ

bq2165

Li-Ion Gas Gauge Module with Pack Supervisor

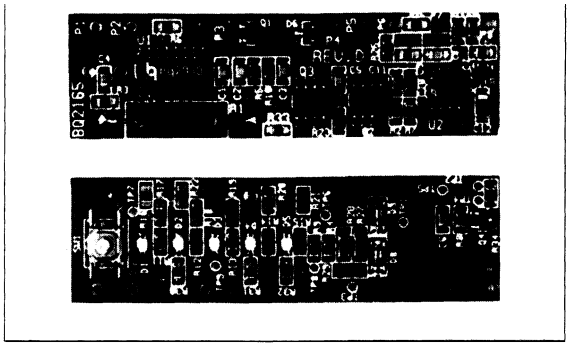
Features

- ➤ Compact, production-ready lithium ion gas gauge and protection solution for three or four series cells
- Accurate measurement of available battery capacity
- Provides overvoltage, undervoltage, and overcurrent protection
- Designed for battery pack integration
  - Small size
  - Includes bq2050 and bq2053 ICs
  - On-board charge and discharge control FETs
  - Low operating current for minimal battery drain
- Battery capacity available through single-wire serial port
- "L" version includes 5 push-button activated LEDs to display state-of-charge information

The bq2165 Gas Gauge Module provides a complete and compact battery management solution for Li-Ion battery packs. Designed for battery pack integration, the bq2165 combines the bq2050 Power Gauge IC with the bq2053 Supervisor IC on a small printed circuit board. The board includes all the necessary components to accurately monitor battery capacity and protect the cells from overvoltage, undervoltage, and overcurrent conditions. The board works with three or four Li-Ion series cells.

The Power Gauge IC uses the on-board sense resistor to track charge and discharge activity of the battery pack. Critical battery information can be accessed through the serial communications port at DQ. The supervisor circuit consists of the bq2053 and two FETs. The bq2053 controls the FETs to protect the batteries during charge/discharge cycles and short circuit conditions. The bq2165 provides contacts for the positive and negative terminals of each battery in the stack. Please refer to the bq2050 and bq2053 data sheets for the specifics on the operation of the power gauge and supervisor ICs.

Benchmarq configures the bq2165 based on the information requested in Table 1. The configuration defines the number of series cells, the nominal battery pack capacity, the self-discharge rate, the Li-Ion battery type (coke or graphite anode), and the threshold limits. The sense resistor value should also be specified on the configuration sheet. The sense resistor value depends on the application. Please refer to the application note entitled "A Tutorial for Gas Gauging" to select the proper value. Refer to page 5 for the bq2165 physical dimensions.



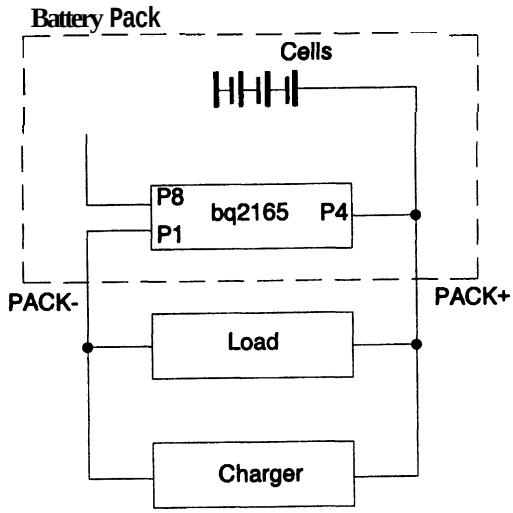
The bq2165L includes five LEDs to display remaining capacity in 20% increments of the learned capacity. The LEDs are activated with the onboard push-button switch.

A module development kit is also available for the bq2165. The bq2165B-KT or the bq2165LB-KT includes one configured module and the following:

1) A serial interface board that allows connection to the RS-232 port of any AT-compatible computer.
2) Menu driven software to display charge/discharge activity and to allow user interface to the bq2050 from any standard DOS PC.
3) Source code for the TSR.

Pin Descriptions

P1/P2	**Pack negative**
P3	**DQ/Serial communications port**
P4	**BAT_{1P}/Battery 1 positive input/pack positive**
P5	**BAT_{1N}/Battery 1 negative input**
P6	**BAT_{2N}/Battery 2 negative input**
P7	**BAT_{3N}/Battery 3 negative input**
P8	**BAT_{4N}/Battery 4 negative input**



FG-9612

Table 1. bq2165 Module Configuration

Customer Name: _____

Contact: _____ Phone: _____

Address: _____

_____

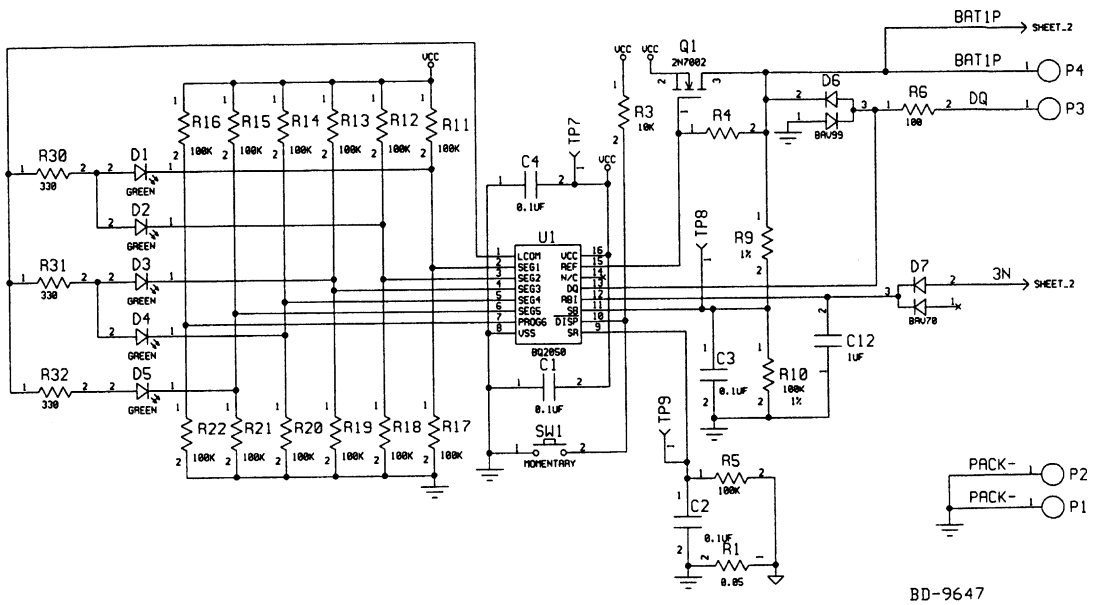
Sales Contact: _____ Phone: _____

Number of series cells (3 or 4)	_____
Coke or graphite cell anode	_____
Battery pack capacity (mAh)	_____
Discharge rate into load (A)	min. _____ avg. _____ max. _____
Sense resistor value in mΩ (0.1Ω standard)	_____
Nominal Available Capacity after reset (Programmed Capacity or Zero)	_____
Self-discharge compensation (Y/N)	_____
Overvoltage threshold (4.25V default)	_____
LEDs and switch (Y/N)	_____

Table 2. Intermediate Pin Connections

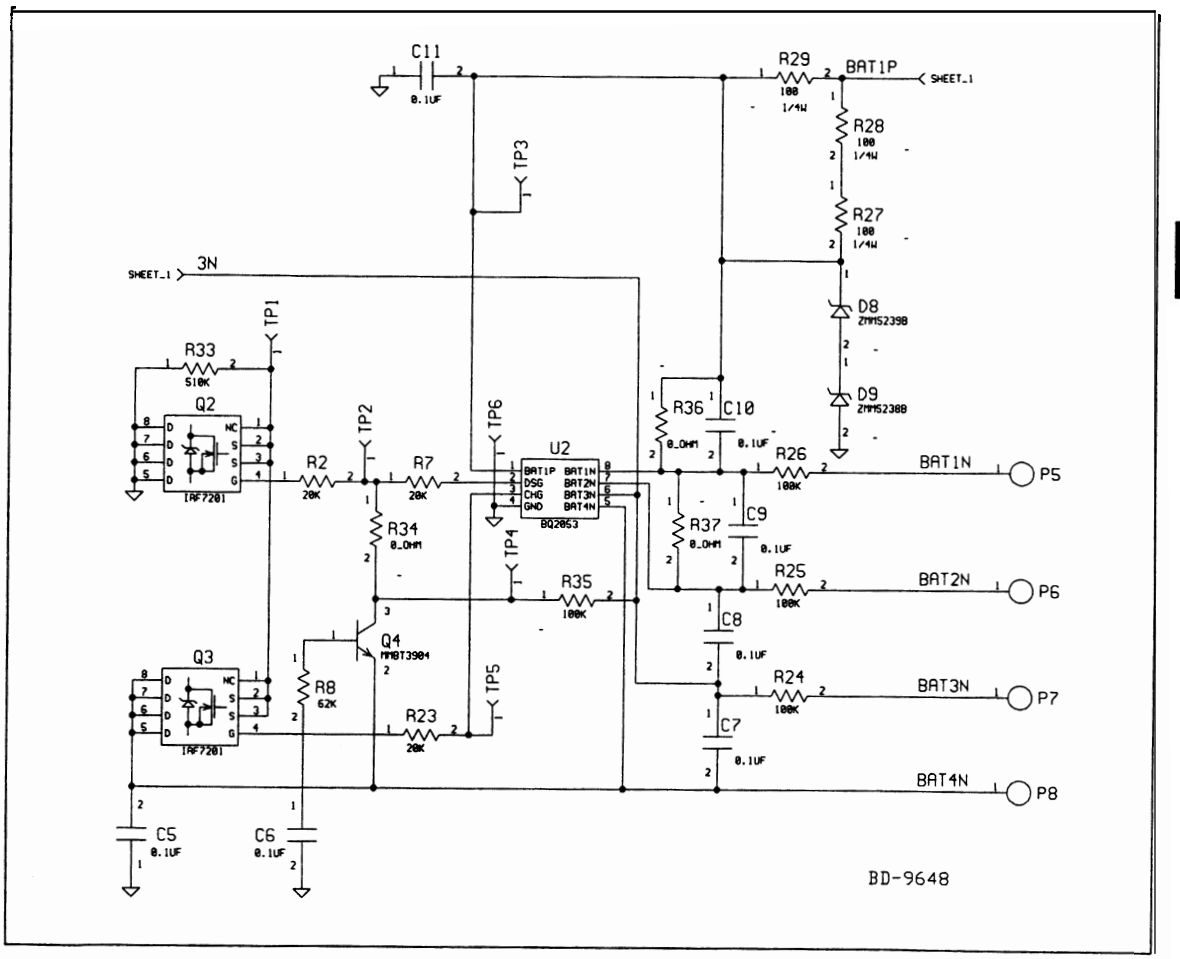
Number of Cello	On-board Configuration	External Connections
3 cells	1N tied to 1P	1P – Positive terminal of first cell
		2N – Negative terminal of first cell
		3N – Negative terminal of second cell
		4N– Negative terminal of third cell
4 cells		1P – Positive terminal of first cell
		1N – Negative terminal of first cell
		2N – Negative terminal of second cell
		3N– Negative terminal of third cell
		4N – Negative terminal of fourth cell

bq2165 Schematic

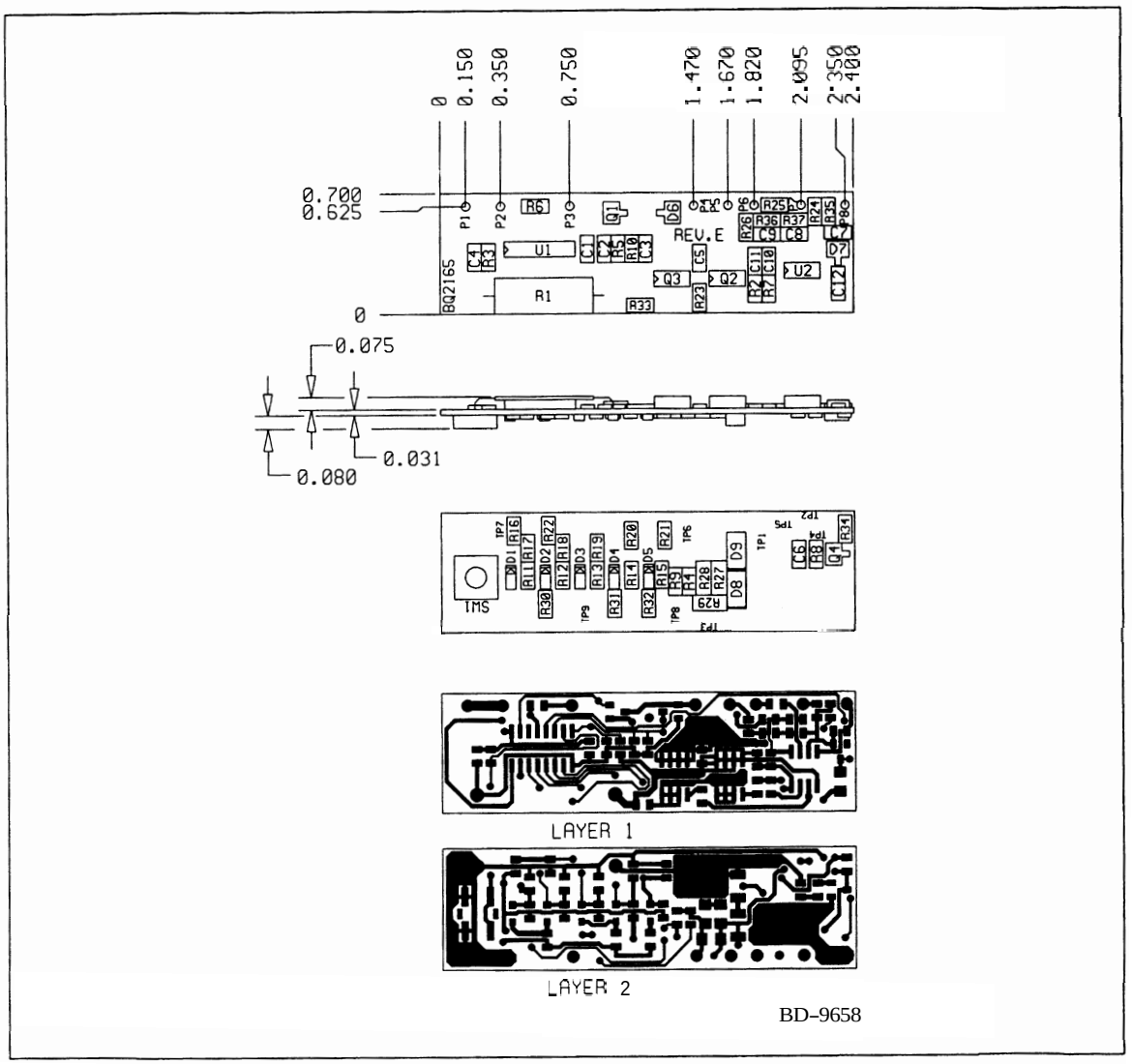


Note: Schematic shows components which may not be placed on the board, depending upon the configuration.

bq2165 Schematic Continued



bq2165 Board



Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Conditions
V_T	Voltage applied on *any* contact relative to BAT_{1P}	-18	+0.31	V	
P_{SR}	Continuous sense resistor power dissipation		3	W	
T_{OPR}	Operating temperature	0	+70	°C	
T_{STG}	Storage temperature	-40	+85	°C	

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may *affect* device reliability.

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
NumCell	Number of series cells in battery pack	3		4		
BAT+	Positive terminal of pack	GND	NumCell * 3.6V	NumCell * 4.1V	V	
BAT-	Negative terminal of pack	GND - 0.3		GND+2.0	V	
I_{CC}	Supply current at BAT_{1P} terminal (no external loads)		200	300	µA	
R_{DQ}	Internal pull-down	500k		-	Ω[1]	
I_{OL}	Open-drain sink current DQ			5.0	mA[1]	
V_{OL}	Open-drain output low, DQ			0.5	V[1]	I_{OL} < 5mA
V_{IHDQ}	DQ input high	2.5			V[1]	
V_{IHDQ}	DQ input low			0.8	V[1]	
V_{OS}	Voltage offset			150	µV[1]	
$R_{BAT1N, 2N, 3N}$	Battery input impedance		10		mΩ	
R_{FET}	FET on resistance			50	mΩ	Per FET
I_D	Continuous charge/discharge current	-	2	4	A	

Note: 1. Characterized on PCB, IC 100% tested.

DC Voltage Thresholds ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDVF}	Final empty warning	1.45	1.47	1.49	V	BAT+/(2*NumCell)[1]
V_{EDV1}	First empty warning	1.50	1.52	1.55	V	BAT+/(2*NumCell)[1]
V_{MCV}	Maximum single-cell voltage	2.20	2.25	2.30	V	BAT+/(2*NumCell)[1]
V_{SRO}	SR sense range	-300		+2000	mV	SR, $V_{SR} + V_{OS}$[2]
V_{SRQ}	Valid charge	210			µV	$V_{SR} + V_{OS}$ [2,3]
V_{SRD}	Valid discharge			-200	µV	$V_{SR} + V_{OS}$ [2,3]

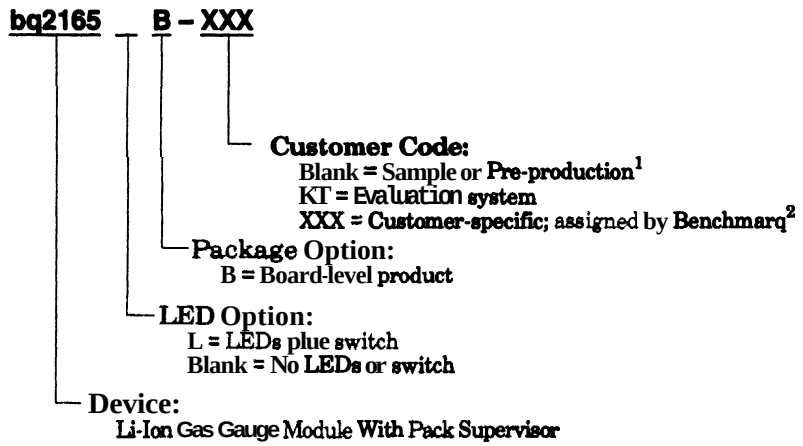
Notes:
1. At SB input of bq2050
2. At SR input of bq2050.
3. Default value; value set in DMF register.

DC Thresholds ($T_A = T_{OPR}$)

Symbol	Parameter	Value	Tolerance	Unit
V_{OV}	Overvoltage limit	4.25	± 1.5%	V
V_{CE}	Charge enable voltage	V_{OV} - 100mV	± 50mV	V
V_{UV}	Undervoltage limit	2.3	± 100mV	V
V_{OC}	Overcurrent limit, BAT4N to PACK-	± 250	± 25	mV

Note: Standard device. Contact Benchmarq for different threshold options.

Ordering Information



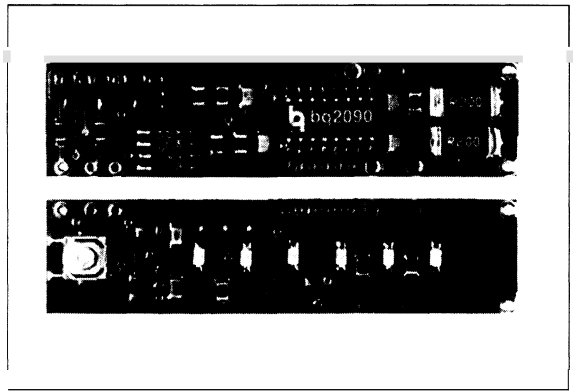
Notes:
1. Requires configuration sheet (see Table 1)
2. Example production part number: bq2165LB-001

Notes

Smart Battery Module with SMBus-Like interface and LEDs

Features

- Complete smart battery solution for NiCd, NiMH, and Li-Ion battery packs
- Accurate measurement of available battery capacity
- Designed for battery pack integration:
  - Small size
  - Includes bq2090, configuration E^2PROM, and sense resistor
  - Four onboard state-of-charge LEDs with push-button activation
  - Low operating current for minimal battery drain
- Critical battery information available over two-wire serial port



A module development kit is also available for the bq2190L. The bq2190LB-KT includes one configured module and the following:

1) An EV2090 serial interface board allowing connection to the RS-232 port of any AT-compatible computer.
2) Menu-driven software to display charge/discharge activity and to allow user interface to the bq2090 and serial E^2PROM from any standard Windows 3.x PC.

General Description

The bq2190L Smart Battery Module provides a complete solution for the design of intelligent battery packs. The bq2190L uses the SMBus protocol and supports many of the Smart Battery Data commands in the SMB/SBD specifications. Designed for battery pack integration, the bq2190L combines the bq2090 Gas Gauge IC with a serial E^2PROM on a small printed circuit board. The board includes all the necessary components to monitor accurately battery capacity and to communicate critical battery parameters to the host system or battery charger. The bq2190L also includes four LEDs. The push-button switch activates the LEDs to show remaining battery capacity in 25% increments.

Contacts are provided on the bq2190L for direct connection to the battery stack (BAT+, BAT-) and the two-wire interface (SMBC, SMBD). Please refer to the bq2090 data sheet for specific information on the operation of the Gas Gauge and communication interface.

Benchmarq configures the bq2190L based on the information requested in Table 1. The configuration defines the pack voltage, capacity, and chemistry. The Smart Battery Module uses the onboard sense resistor to track charge and discharge activity of the battery pack. The sense resistor value and type should also be specified on the configuration sheet. The two options available are a 3W through-hole type or a 1W surface-mount type. The value depends on the application. Please refer to the application note entitled "A Tutorial for Gas Gauging" to select the proper value.

Pin Descriptions

P1	**BAT+/Battery positive**
P2	**GND/Ground**
P3	**Pack negative**
P4	**BAT-Battery negative**
P5	**SMBC/Communications clock**
P6	**SMBD/Serial data**

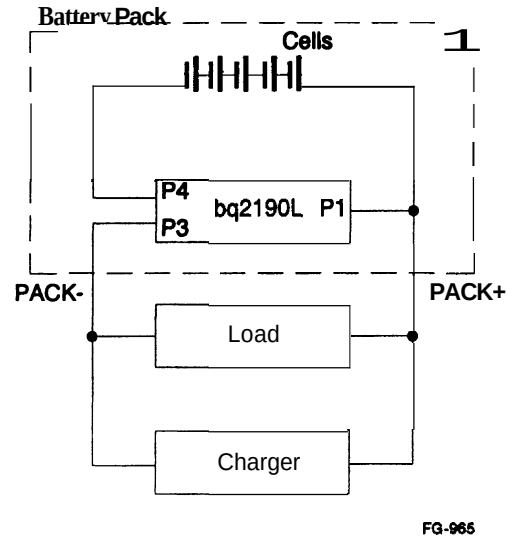
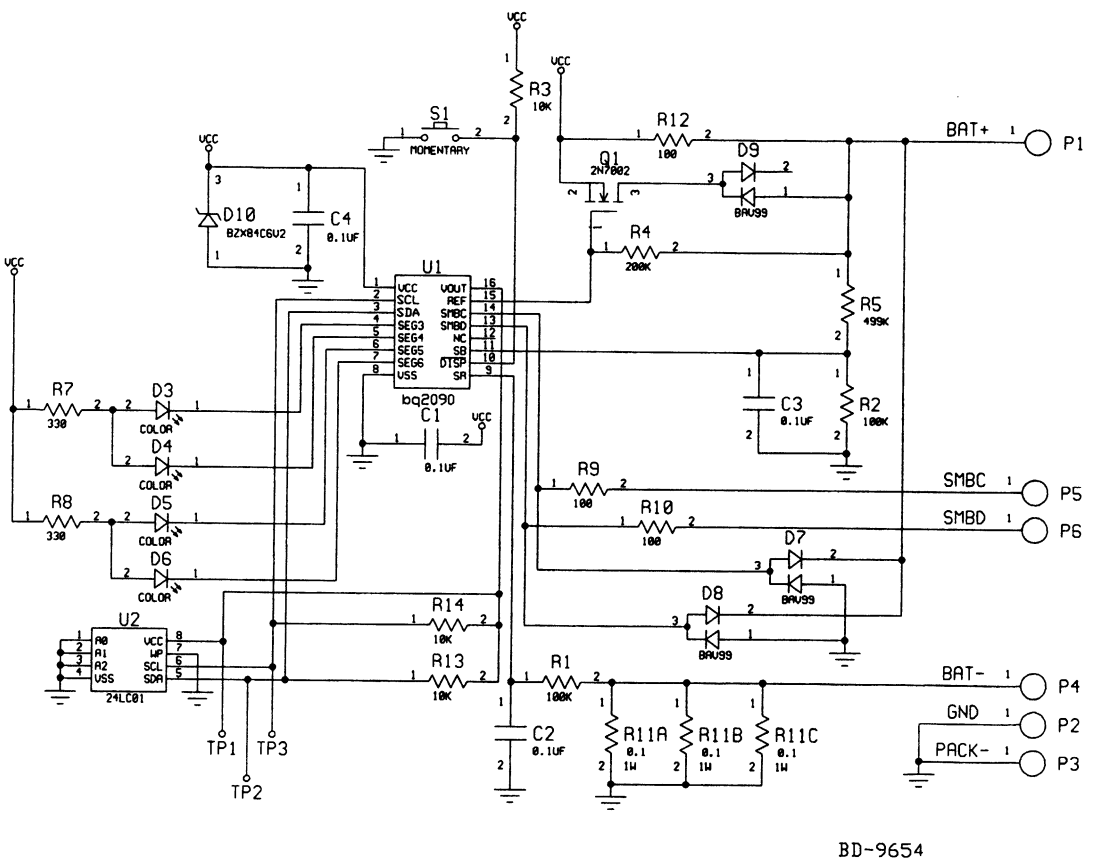


Figure 1. Module Connection Diagram

Table 1. bq2190L Module Configuration

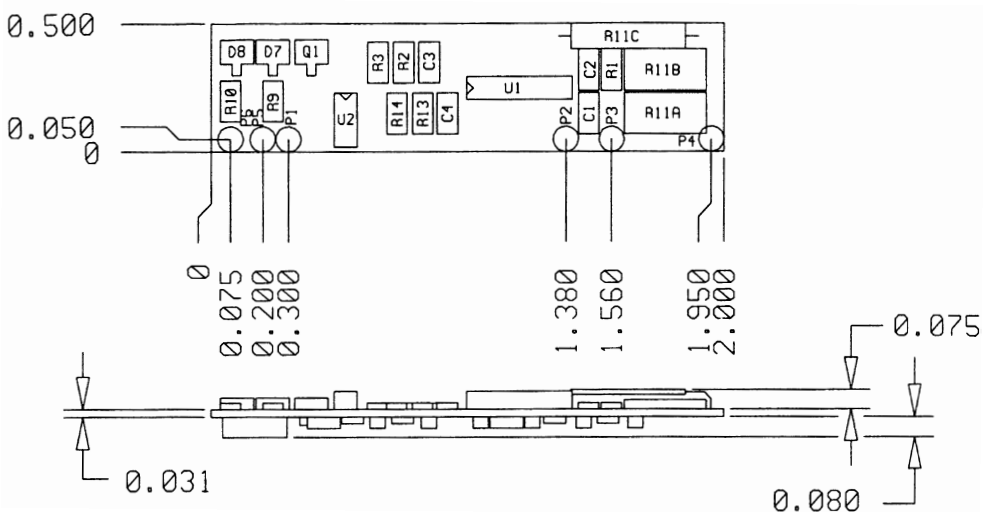
Design capacity (mAh)	
Remaining capacity alarm	
Sense resistor size in mΩ (0.1Ω standard)	
Sense resistor type: (Thru-hole (3W) or Surface Mount (1W))	
End of discharge voltage 1 (mV)	
End of discharge voltage 2 (mV)	
Battery chemistry	
Design voltage	
Manufacturer date	
Serial number	
Manufacturer name	
Device name	
Manufacturer data	
Display mode (absolute or relative)	

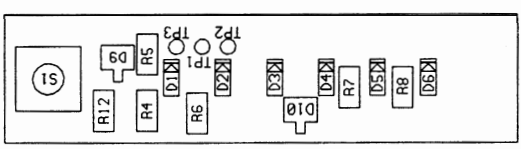
bq2190L Schematic

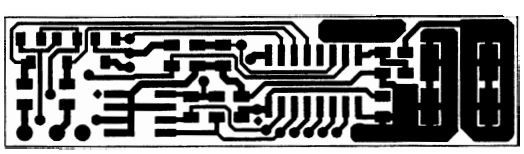


Note: Schematic shows components which may not be placed on the board, depending upon the co guration.

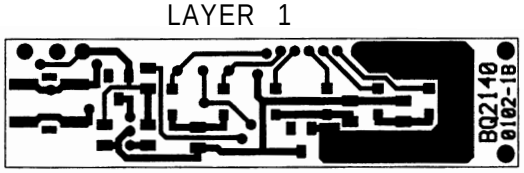
bq2190L Board







LAYER 1



LAYER 2

BD-9655

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Conditions
V_{CC}	Relative to V_{SS}	-0.3	+7.0	V	bq2090
All other pins	Relative to V_{SS}	-0.3	+7.0	V	bq2090
P_{SR}	Continuous sense resistor power dissipation		3	W	Thru-hole sense resistor
			1	W	Surface mount sense resistor
T_{OPR}	Operating temperature	0	+70	°C	Commercial
T_{STR}	Storage Temperature	-40	+85	°C	

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device *mliabii*.

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbd	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
BAT+	Positive terminal of pack	GND	14.4	21.6	V	
BAT-	Negative terminal of pack	GND - 0.3		GND+2.0	V	
I_{CC}	Supply current at BAT+ terminal (no external loads)	-	200	300	µA	
I_{OL}	Open-drain sink current			350	µA[1]	
V_{OL}	Open-drain output low			0.4	V[1]	
V_{IH}	Input high	1.4		5.5	V[1]	SMBC, SMBD
V_{IL}	Input low	-0.5		0.6	V[1]	SMBC, SMBD

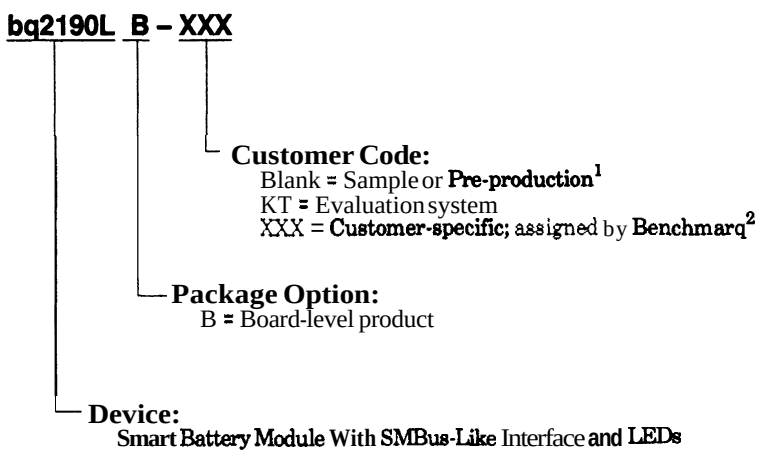
Note: 1. Characterized on PCB, IC 100% tested.

DC Voltage Thresholds ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
E_{VSB}	Battery voltage error	-60		+50	mV	Note1
V_{SRO}	Sense resistor range	-300		+2000	mV	Note2
V_{SRQ}	Valid charge	380			µV	Note 2, 3
V_{SRD}	Valid discharge			-300	µV	Note 2, 3

Notes:
1. At SB input of bq2090.
2. At SR input of bq2090.
3. Default value; value set in DMF register.

Ordering Information

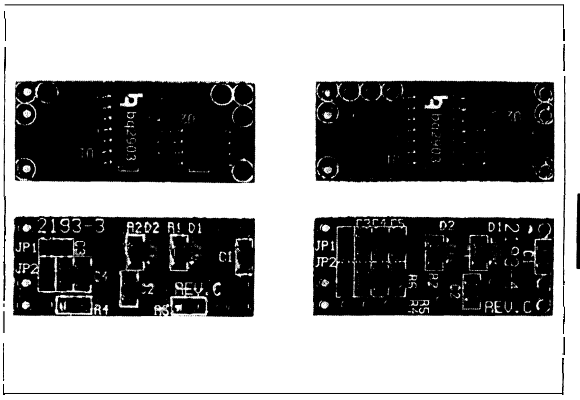


Notes:
1. Requires configuration sheet (see Table 1)
2. Example production part number: bq2190LB-001

Rechargeable Alkaline Charger Module

Features

- Complete charge control for three or four rechargeable alkaline cells
- PCB includes:
  - bq2903 alkaline charge chip
  - LEDs
  - Discharge FET
- Direct connections for individual battery terminal and DC input
- Provides pre-charge qualification, fast charge termination, and over-discharge protection
- Onboard LEDs indicate charge status and fault conditions



General Description

The bq2193L Charge Module provides a complete and compact solution for charge and discharge control of three or four rechargeable alkaline cells. Designed for in-system integration, the bq2193L incorporates a bq2903 Charge Controller IC, two status LEDs, and a discharge FET. It provides direct connections for the negative and positive terminals of each cell, the DC charging supply (DC+, DC-), and the load (LOAD+, LOAD-). Please refer to the bq2903 data sheet for more specific information on the operation of the Charge Controller.

Benchmarq configures the bq2193L based on the information requested in Table 1. The configuration defines the number of series cells, the discharge rate capability, and the end-of-discharge voltage. The board is available as a three-cell (bq2193L-3) or–four-cell (bq2193L-4) version.

Pin Descriptions

LOAD+	**Positive side of load**
BAT+	**Positive terminal of battery 1**
BAT1N	**Negative terminal of battery 1**
BAT2N	**Negative terminal of battery 2**
BAT3N	**NA (version 3); Negative terminal of battery 3 (version 4)**
BAT-	**Negative terminal of battery 3 (version 3); Negative terminal of battery 4 (version 4)**
DC+	**Positive side of charger**
DC-	**Negative side of charger**
LOAD-	**Negative side of load**

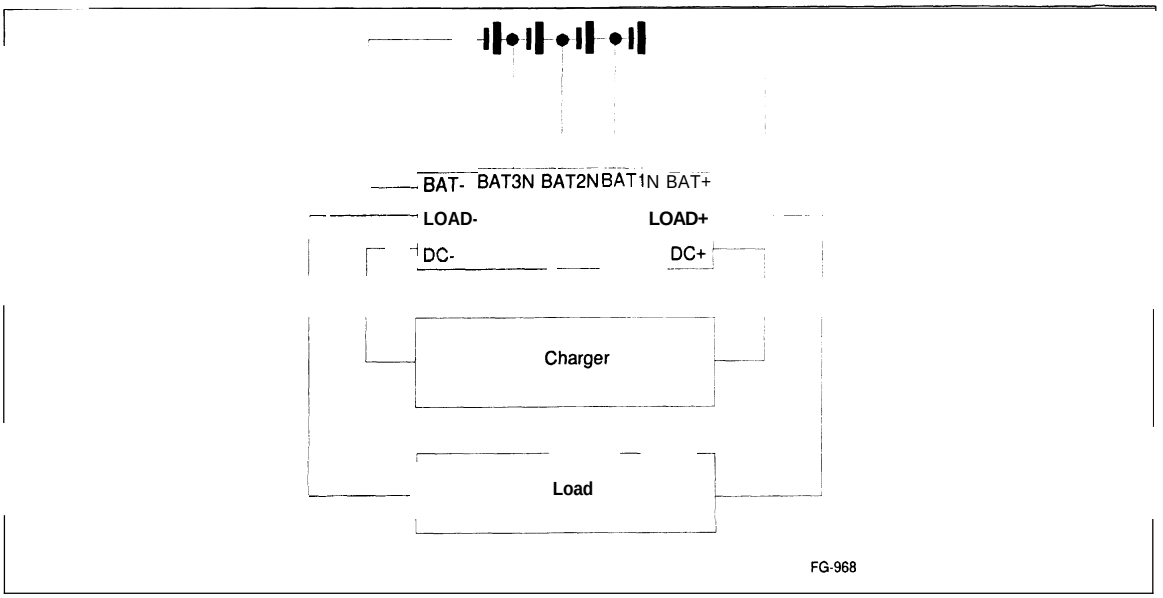


Figure 1. Module Connection Diagram

Table 1. bq2193 Module Configuration

Customer Name: _____

Contact: _____ Phone: _____

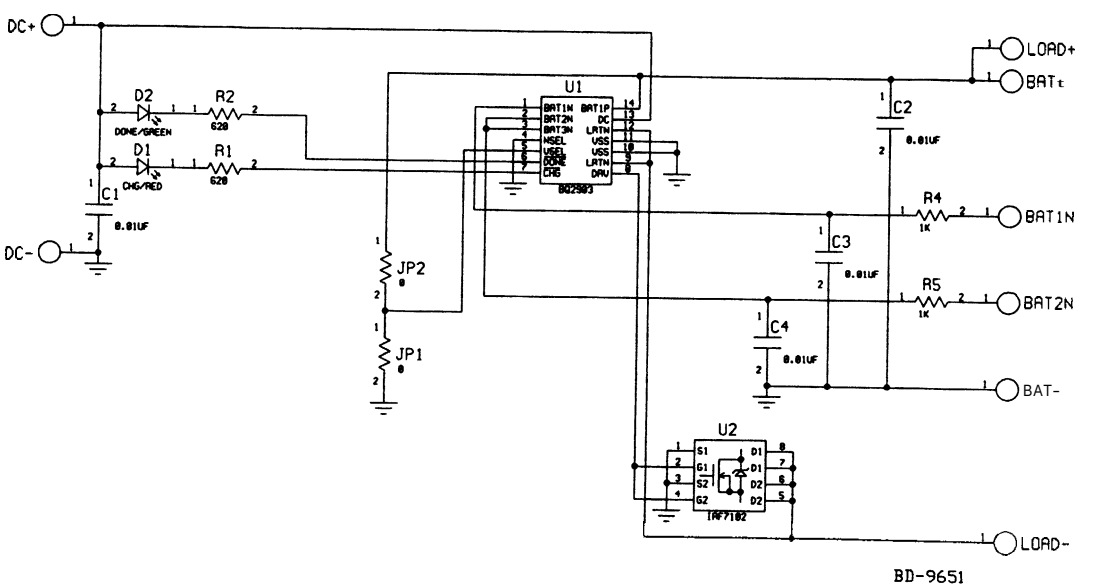
Address: _____

_____

Sales Contact: _____ Phone: _____

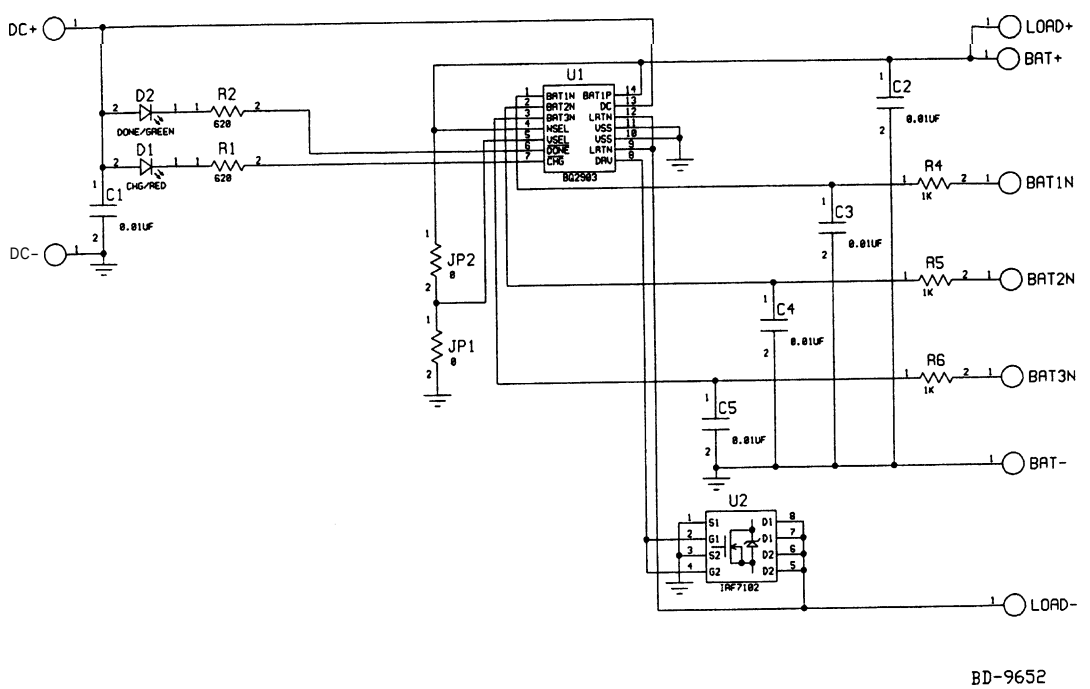
Number of battery cells (3-4)	_____
Load current (mA)	_____
End-of-discharge voltage (1.1V, 1.0V, or 0.9V)	_____

bq2193-3 Schematic



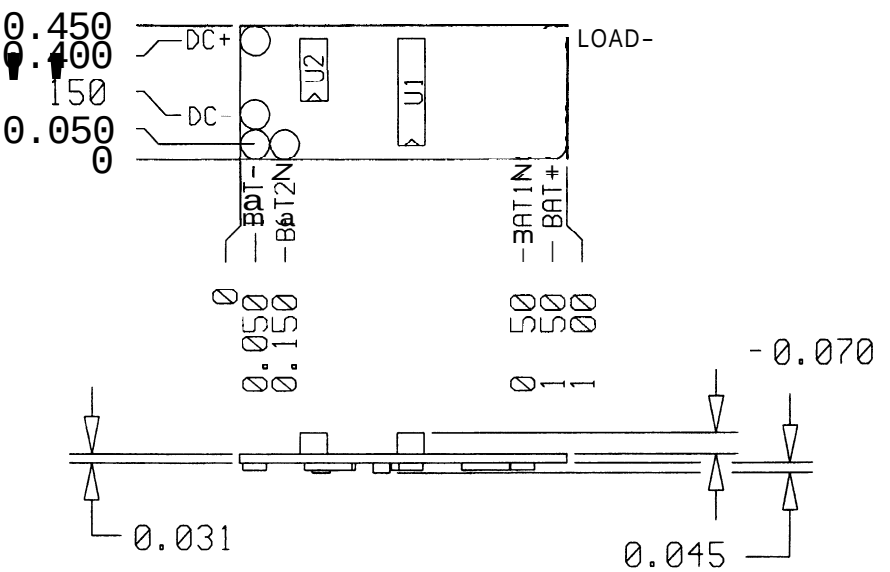
Note: Schematic shows components which may not be placed on the board, depending upon the configuration.

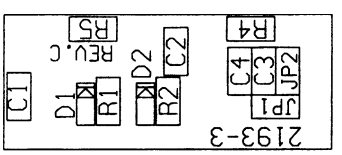
bq2193-4 Schematic

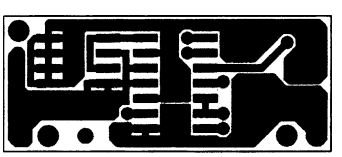


Note: Schematic shows components which may not be placed on the board, depending upon the configuration.

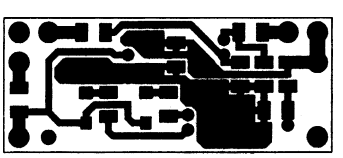
bq2193-3 Board







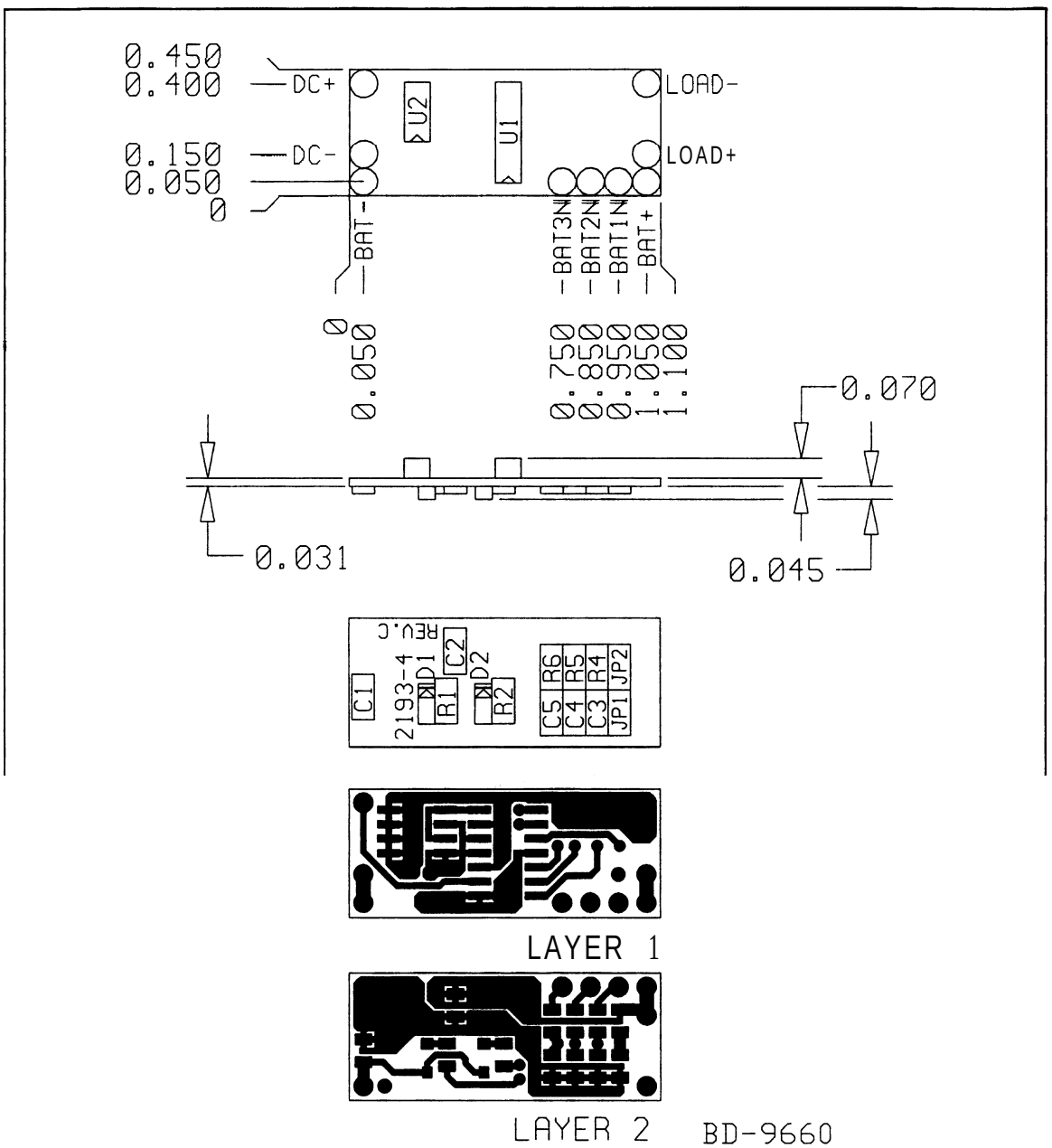
LAYER 1



LAYER 2

BD-9659

bq2193-4 Board



Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Conditions
DC_{IN}	V_{DC}	-0.3	11.0	V	
V_T	DC threshold voltage applied on any pin, excluding DC pin	-0.3	11.0	V	
T_{OM}	Operating ambient temperature	0	+70	°C	Commercial
I_{DC}	DC charging current		400	mA	
I_{LOAD}	Discharge current		1.3	A	

Note: Permanent device damage may occur if **Absolute Maximum Ratings are** exceeded. Functional operation should be limited to the **Recommended** DC Operating Conditions detailed in this data sheet. **Exposure** to conditions beyond the operational limits for extended periods of time may affect device reliabii.

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{CC}	Supply current			14	mA	V_{DC} = 10.0V[1]
I_{SB1}	Standby current		25	40	µA	VDC = 0, $V_{OCV} > V_{EDV}$[2]
I_{SB2}	Standby current			1	µA	$V_{DC} = 0$ $V_{OCV} < V_{EDV}$
R_{DSON}	Discharge on resistance		0.25		Ω	Note 3
I_{LOAD}	Discharge current			1	A	Note3
I_{DC}	DC charging current			300	mA	
V_{OP}	Operating voltage	2.7		10	V	Note 4

Note:
1. CHG/DONE LED on.
2. V_{OCV} = cell open circuit voltage.
3. Includes N-FET.
4. The minimum charge voltage is 2.0V per cell.

DC Thresholds (T_A = 25°C; V_{DC} = 10V)

Symbol	Parameter	Rating	Tolerance	Unit	Notes
V_{MAX}	Maximum cell open-circuit voltage	1.63	±3%	V	$V_{OCV} > V_{MAX}$ inhibits or terminates charge pulses
V_{EDV}	End-of-discharge voltage	0.90	±5%	V	
		1.00	±5%	V	
		1.10	±5%	V	
V_{FLT}	Maximum cell closed-circuit voltage	3.00	±5%	V	$V_{CCV} > V_{FLT}$ terminates charge, indicates fault
V_{MIN}	Minimum battery voltage	0.40	±5%	V	Vocv < V_{MIN} inhibits charge
V_{CE}	Charge enable	1.40	±5%	V	$V_{OCV} < V_{CE}$ on all cells re-initiates charge

Notes: Each parameter above has a temperature coefficient associated with it. To determine the coefficient for each parameter, use the following formula:

$$\text{Tempco} = \frac{\text{Parameter Rating}}{1.63} * -0.5\text{mV/°C}$$

The tolerance for these temperature coefficients is 10%.

EDV depends on configuration.

Vocv = cell open circuit voltage.

Ordering Information

bq2193L B – XXX

Customer Code:
Blank = Sample or Pre-production[1]
KT = Evaluation system
XXX = Customer-specific; assigned by Benchmarq[2]

Package Option:
B = Board-level product

Device:
Rechargeable Alkaline Charger Module

Notes:
1. Requires configuration sheet (see Table 1)
2. Example production part number: bq2193LB-001

BENCHMARQ

bq2201

SRAM Nonvolatile Controller Unit

Features

- Power monitoring and switching for 3 volt battery-backup applications
- Write-protect control
- 3 volt primary cell inputs
- Less than 10 ns chip enable propagation delay
- 5% or 10% supply operation

General Description

The CMOS bq2201 SRAM Nonvolatile Controller Unit provides all necessary functions for converting a standard CMOS SRAM into nonvolatile read/write memory.

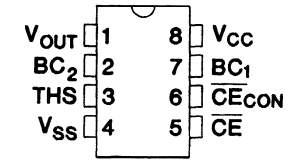
A precision comparator monitors the 5V Vcc input for an out-of-tolerance condition. When out of tolerance is detected, a conditioned chip enable output is forced inactive to write-protect any standard CMOS SRAM.

During a power failure, the external SRAM is switched from the V_{CC} supply to one of two 3V backup supplies. On a subsequent power-up, the SRAM is write-protected until a power-valid condition exists.

The bq2201 is footprint- and timing-compatible with industry standards with the added benefit of a chip enable propagation delay of less than 10ns.

4

Pin Connections



8-Pin Narrow DIP or SOIC

PN-17

Pin Names

V_{OUT}	Supply output
BC_1-BC_2	3 volt primary backup cell inputs
THS	Threshold select input
$\overline{CE}$	Chip enable active low input
$\overline{CE}_{CON}$	Conditioned chip enable output
V_{CC}	+5 volt supply input
V_{SS}	Ground

Functional Description

An external CMOS static RAM can be battery-backed using the V_{OUT} and the conditioned chip enable output pin from the bq2201. As V_{CC} slews down during a power failure, the conditioned chip enable output $\overline{CE}_{CON}$ is forced inactive independent of the chip enable input $\overline{CE}$.

This activity unconditionally write-protects external SRAM as V_{CC} falls to an out-of-tolerance threshold V_{PFD}. V_{PFD} is selected by the threshold select input pin, THS.

If THS is tied to Vss, power-fail detection occurs at 4.62V typical for 5% supply operation. If THS is tied to V_{OUT}, power-fail detection occurs at 4.37V typical for 10% supply operation. The THS pin must be tied to V_{SS} or V_{OUT} for proper operation.

If a memory access is in process during power-fail detection, that memory cycle continues to completion before the memory is write-protected. If the memory cycle is not terminated within time t_{WPT}, the $\overline{CE}_{CON}$ output is unconditionally driven high, write-protecting the memory.

As the supply continues to fall past V_{PFD}, an internal switching device forces V_{OUT} to one of the two external backup energy sources. $\overline{CE}_{CON}$ is held high by the V_{OUT} energy source.

During power-up. V o w is switched back to the V_{CC} supply as V_{CC} rises above the backup cell input voltage sourcing V_{OUT}. The $\overline{CE}_{CON}$ output is held inactive for time t_{CER} (120 ma maximum) —+ the supply has reached V_{PFD}, independent of the CE input, to allow for processor stabilization.

During power-valid operation, the $\overline{CE}$ input is fed through to the $\overline{CE}_{CON}$ output with a propagation delay of less than 1 0 ns. Nonvolatility is achieved by hardware hookup as shown in Figure 1.

Energy Cell Inputs—BC_1, BC_2

Two primary backup energy source inputs are provided on the bq2201. The BC_1 and BC_2 inputs accept a 3V primary battery, typically some type of lithium chemistry. If no primary cell is to be used on either BC_1 or BC_2, the unused input should be tied to Vss.

If both inputs are used, during power failure the V_{OUT} output is fed only by BC_1 as long as it is greater than 2.5V. If the voltage at BC_1 falls below 2.5V, an internal isolation switch automatically switches V o w from BC_1 to BC_2.

To prevent battery drain when there is no valid data to retain, V_{OUT} and $\overline{CE}_{CON}$ are internally isolated from BC_1 and BC2 by either:

- Initial connection of a battery to BC_1 or BC_2, or
- Presentation of an ieolation signal on $\overline{CE}$.

A valid isolation signal requires $\overline{CE}$ low as V_{CC} crosses both V_{PFD} and V_{SO} during a power-down. Between these two points in time, $\overline{CE}$ must be brought to the point of (0.48 to 0.52)•V_{CC} and held for at least 700ns. The isolation signal is invalid if $\overline{CE}$ exceeds 0.54•V_{CC} at any point between V_{CC} crossing V_{PFD} and V_{SO}. See Figure 2.

The appropriate battery is connected to V_{OUT} and $\overline{CE}_{CON}$ immediately on subsequent application and removal of V_{CC}.

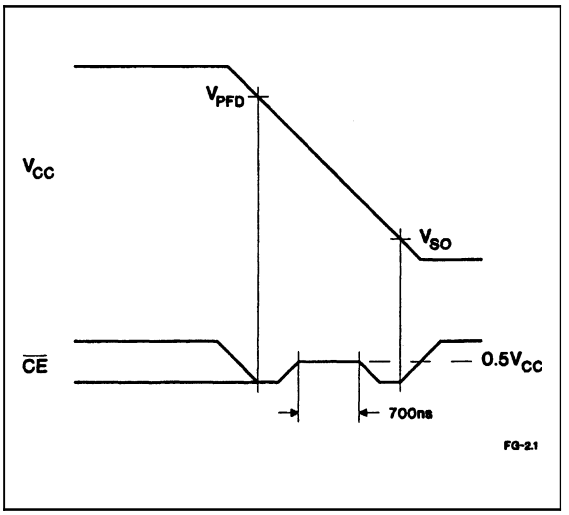


Figure 2. Battery Isolation Signal

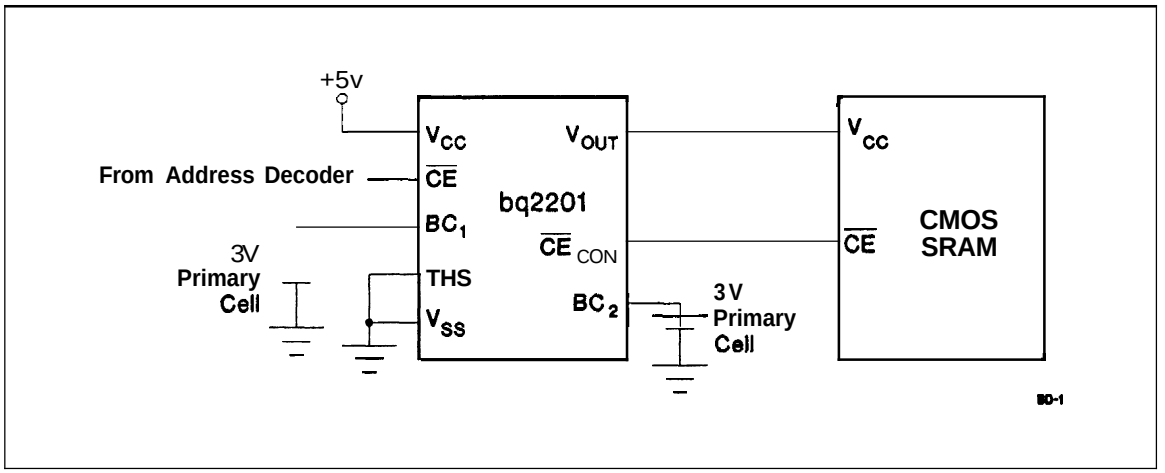


Figure 1. Hardware Hookup (5% Supply Operation)

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on Vcc relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
		-40 to +85	°C	Industrial "N"
T_{STG}	Storage temperature	-55 to 125	°C	
T_{BIAS}	Temperature under bias	-40 to +85	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds
I_{OUT}	V_{OUT} current	200	mA	

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may *affect* device reliability.

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
Vcc	Supply voltage	4.75	5.0	5.5	V	THS = V_{SS}
		4.50	5.0	5.5	V	THS = V_{OUT}
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3		0.8	V	
VIH	Input high voltage	2.2	-	V_{CC} + 0.3	V	
V_{BC1}, V_{BC2}	Backup cell voltage	2.0		4.0	V	
THS	Threshold select	-0.3	-	Vcc + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC}.

DC Electrical Characteristics ($T_A = T_{OPR}$, V_{CC} = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 1	µA	$V_{IN} = V_{SS}$ to V_{CC}
V_{OH}	Output high voltage	2.4			V	I_{OH} = -2.0 mA
V_{OHB}	V_{OH}, BC supply	V_{BC} - 0.3			V	$V_{BC} > V_{CC}$, I_{OH} = -10µA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 4.0 mA
I_{CC}	Operating supply current		3	5	mA	No load on V_{OUT} and $\overline{CE}_{CON}$.
V_{PFD}	Power-fail detect voltage	4.55	4.62	4.75	V	THS = V_{SS}
		4.30	4.37	4.50	V	THS = V_{OUT}
V_{SO}	Supplyswitch-over voltage	-	V_{BC}	-	V	
I_{CCDR}	Data-retention mode current	-	-	100	nA	V_{OUT} data-retention current to additional memory not included.
V_{OUT1}	V_{OUT} voltage	V_{CC} - 0.2			V	$V_{CC} > V_{BC}$, I_{OUT} = 100mA
		V_{CC} - 0.3			V	$V_{CC} > V_{BC}$, I_{OUT} = 160mA
V_{OUT2}	V_{OUT} voltage	V_{BC} -0.3	-	-	V	$V_{CC} < V_{BC}$, I_{OUT} = 100µA
V_{BC}	Active backup cell voltage		V_{BC2}		V	$V_{BC1} < 2.5V$
			V_{BC1}		V	$V_{BC1} > 2.5V$
I_{OUT1}	V_{OUT} current	-	-	160	mA	$V_{OUT} > V_{CC}$ - 0.3V
I_{OUT2}	Vomcurrent		100		µA	$V_{OUT} > V_{BC}$ - 0.2V

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC}.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
C_{IN}	Input capacitance			8	pF	Input voltage = 0V
C_{OUT}	Output capacitance			10	pF	Output voltage = 0V

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0 V to 3.0 V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	*See* Figure 3

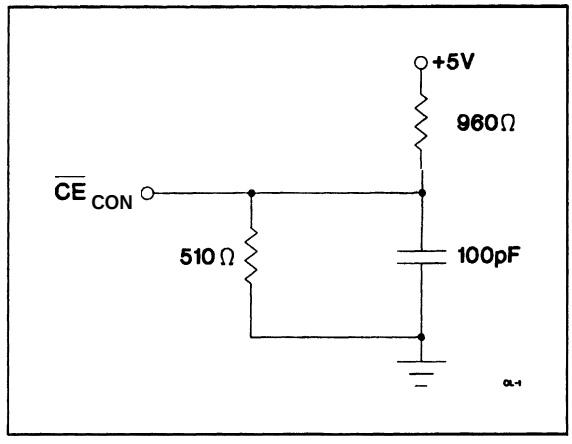


Figure 3. Output Load

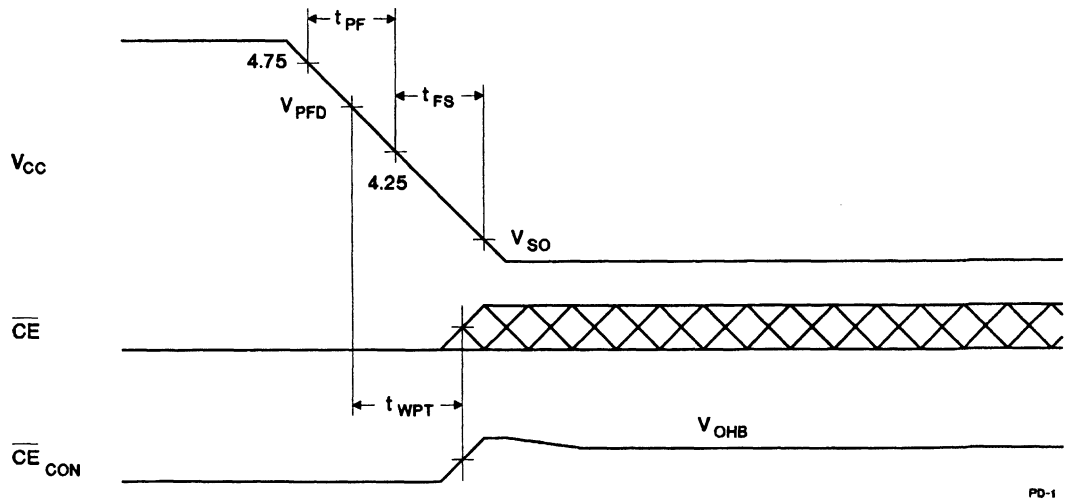
Power-Fail Control ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{PF}	V_{CC} slew, 4.75V to 4.25V	300			µs	
t_{FS}	V_{CC} slew, 4.25V to V_{SO}	10			µs	
t_{PU}	V_{CC} slew, 4.25V to 4.75V	0			µs	
t_{CED}	Chip enable propagation delay	-	7	10	ns	
t_{CER}	Chip enable recovery	40	80	120	ms	Time during which SRAM is write-protected after V_{CC} passes V_{PFD} on power-up.
t_{WPT}	Write-protecttime	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.

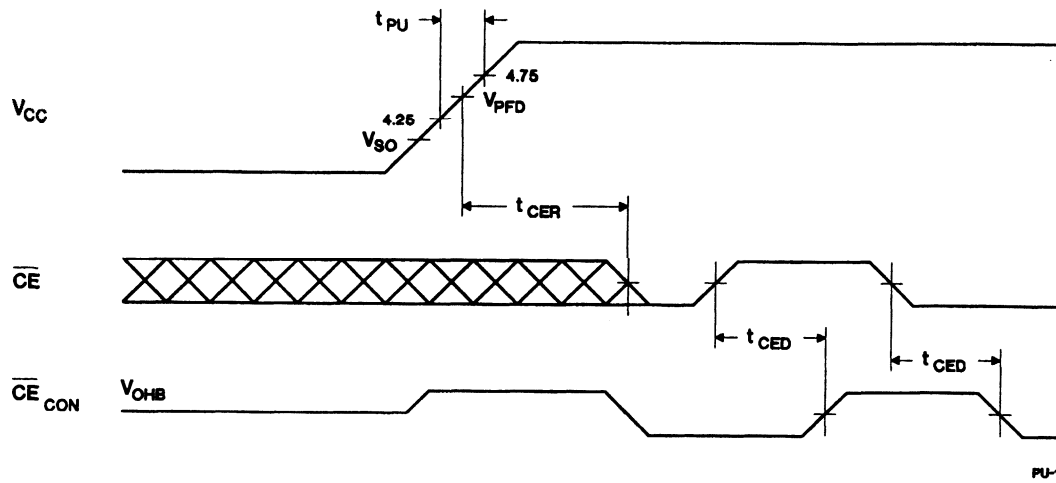
Note: Typical values indicate operation at T_A = 25°C.

Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

Power-Down Timing



Power-Up Timing



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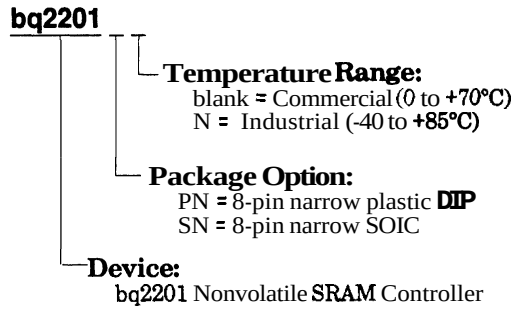
Data Sheet Revision History (Sept. 1991 Changes From Sept. 1990)

Added industrial temperature range.

Ordering Information



BENCHMARQ

bq2202

SRAM NV Controller With Reset

Features

- Power monitoring and switching for nonvolatile control of SRAMs
- Write-protect control
- Input decoder allows control of up to 2 banks of SRAM
- 3V primary cell input
- 3V rechargeable battery input/output
- Reset output for system power-on reset
- Less than 10ns chip enable propagation delay
- 5% or 10% supply operation

General Description

The CMOS bq2202 SRAM Nonvolatile Controller With Reset provides all the necessary functions for converting one or two banks of standard CMOS SRAM into nonvolatile read/write memory.

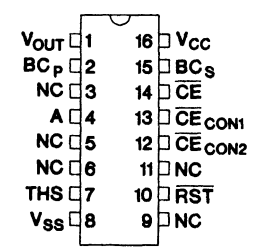
A precision comparator monitors the 5V V_{CC} input for an out-of-tolerance condition. When out of tolerance is detected, the two conditioned chip enable outputs are forced inactive to write-protect both banks of SRAM.

Power for the external SRAMs is switched from the V_{CC} supply to the battery-backup supply as V_{CC} decays. On a subsequent power-up, the V_{OUT} supply is automatically switched from the backup supply to the V_{CC} supply. The external SRAMs are write-protected until a power-valid condition exists. The reset output provides power-fail and power-on resets for the system.

During power-valid operation, the input decoder selects one of two banks of SRAM.

4

Pin Connections



16-Pin Narrow DIP or SOIC

PN-22

Pin Names

V_{OUT}	Supply output
$\overline{RST}$	Reset output
THS	Threshold select input
$\overline{CE}$	Chip enable active low input
$\overline{CE}_{CON1}$, $\overline{CE}_{CON2}$	Conditioned chip enable outputs
A	Bank select input
BC_P	3V backup supply input
BC_S	3V rechargeable backup supply input/output
NC	No connect
V_{CC}	+5 volt supply input
V_{SS}	Ground

Functional Description

Two banks of CMOS static RAM can be battery-backed using the V_{OUT} and conditioned chip enable output pins from the bq2202. As the voltage input V_{CC} slews down during a power failure, the two conditioned chip enable outputs, $\overline{CE}_{CON1}$ and $\overline{CE}_{CON2}$, are forced inactive independent of the chip enable input $\overline{CE}$.

This activity unconditionally write-protects external SRAM as V_{CC} falls to an out-of-tolerance threshold V_{PFD}. V_{PFD} is selected by the threshold select input pin, THS. If THS is tied to V_{SS}, the power-fail detection occurs at 4.62V typical for 5% supply operation. If THS is tied to V_{OUT}, power-fail detection occurs at 4.37V typical for 10% supply operation. The THS pin must be tied to V_{SS} or V_{OUT} for proper operation.

If a memory access is in process to any of the two external banks of SRAM during power-fail detection, that memory cycle continues to completion before the memory is write-protected. If the memory cycle is not terminated within time t_{WPT} (150µsec maximum), the two chip enable outputs are unconditionally driven high, write-protecting the controlled SRAMs.

As the supply continues to fall past V_{PFD}, an internal switching device forces V_{OUT} to the internal backup energy source. $\overline{CE}_{CON1}$ and $\overline{CE}_{CON2}$ are held high by the V_{OUT} energy source.

During power-up, V_{OUT} is switched back to the 5V supply as V_{CC} rises above the backup cell input voltage sourcing V_{OUT}. Outputs $\overline{CE}_{CON1}$ and $\overline{CE}_{CON2}$ are held inactive for time t_{CER} (120ms maximum) after the power supply has reached V_{PFD}, independent of the $\overline{CE}$ input, to allow for processor stabilization.

During power-valid operation, the $\overline{CE}$ input is passed through to one of the two $\overline{CE}_{CON}$ outputs with a propagation delay of less than 10 ns. The $\overline{CE}$ input is output on one of the two $\overline{CE}_{CON}$ output pins depending on the level of bank select input A, as shown in the Truth Table.

Bank select input A is usually tied to a high-order address pin so that a large nonvolatile memory can be designed using lower-density memory devices. Nonvolatility and decoding are achieved by hardware hookup as shown in Figure 1.

The reset output ($\overline{RST}$) goes active within t_{PFD} (150 µsec maximum) after V_{PFD}, and remains active for a minimum of 40ms (120ms maximum) after power returns valid The $\overline{RST}$ output can be used as the power-on reset for a microprocessor. Access to the external RAM may begin when $\overline{RST}$ returns inactive.

Energy Cell Inputs—BC_P, BC_S

Two backup energy source inputs are provided on the bq2202—a primary cell BC_P and a secondary cell BC_S. The primary cell input is designed to accept any 3V primary battery (non-rechargeable), typically some type of lithium chemistry. If a primary cell is not to be used, the BC_P pin should be grounded. The secondary cell input BC_S is designed to accept constant-voltage current-limited rechargeable cells.

During normal +5V power valid operation, 3.3V is output on the BC_S pin and is current-limited internally.

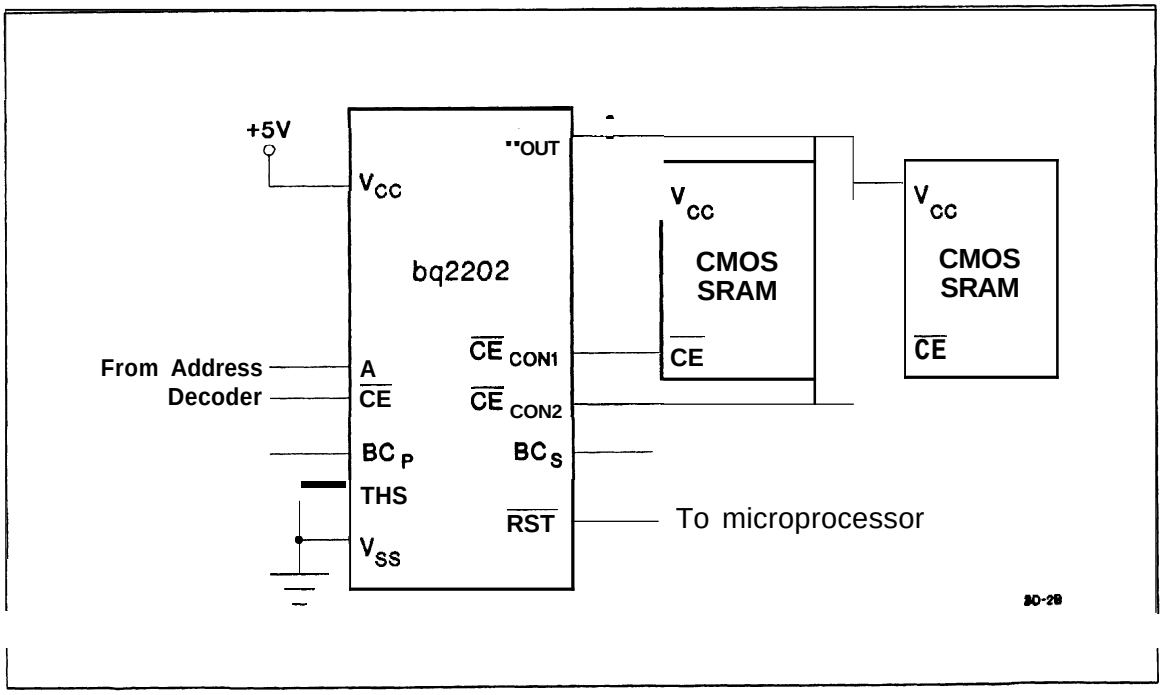


Figure 1. Hardware Hookup (5% Supply Operation)

If a secondary cell is not to be used, the BC_S pin must be tied directly to Vss. If both inputs are used, during power failure the V_{OUT} and $\overline{CE}_{CON}$ outputs are forced high by the secondary call ao long aa it is greater than 2.5V. Only the secondary call is loaded by the data retention current of the SRAM until the voltage at the BC_S pin falls below 2.5V. When and if the voltage at BC_S falls below 2.5V, an internal isolation switch automatically transfers the load from the secondary cell to the primary cell.

To prevent battery drain when there is no valid data to retain, V_{OUT}, $\overline{CE}_{CON1}$, and $\overline{CE}_{CON2}$ are internally isolated from BC_P and BC_S by either:

- Initial connection of a battery to BC_P or BC_S or

  Presentation of an isolation signal on $\overline{CE}$.

A valid isolation signal requires $\overline{CE}$ low as V_{CC} crosses both V_{PFD} and V_{SO} during a power-down. Between these two points in time, $\overline{CE}$ must be brought to V_{CC}*(0.48 to 0.52) and held for at least 700ns. The isolation signal is invalid if $\overline{CE}$ exceeds V_{CC}*0.54 at any point between V_{CC} crossing V_{PFD} and V_{SO}. See Figure 2.

The battery is connected to V_{OUT}, $\overline{CE}_{CON1}$, and $\overline{CE}_{CON2}$ immediately on subsequent application and removal of VCC.

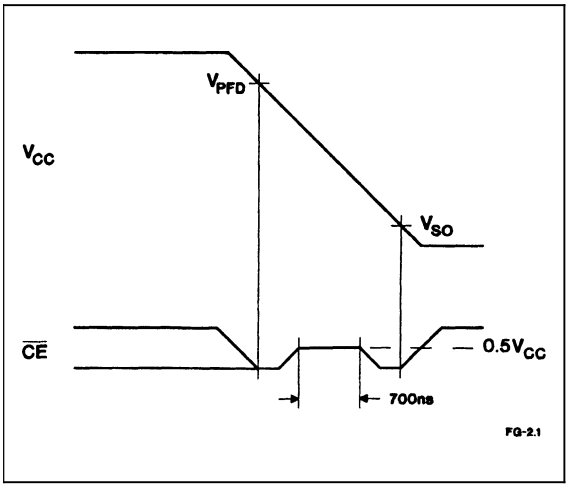


Figure 2. Battery Isolation Signal

4

Truth Table

Input		Output	
$\overline{CE}$	A	$\overline{CE}_{CON1}$	$\overline{CE}_{CON2}$
H	X	H	H
L	L	L	H
L	H	H	L

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on Vcc relative to Vss	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
		-40 to +85	°C	Industrial "N"
T_{STG}	Storage temperature	-55 to +125	°C	
T_{BIAS}	Temperature under bias	-40 to 85	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds
I_{OUT}	V_{OUT} current	200	mA	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. **Exposure** to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.75	5.0	5.5	V	THS = V_{SS}
		4.50	5.0	5.5	V	THS = V_{OUT}
V_{BCP}	Backup cell input voltage	2.0		4.0	V	$V_{CC} < V_{BC}$
V_{BCS}		2.5		4.0		
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3		0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	
THS	Threshold select	-0.3	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C, Vcc = 5V or V_{BC}.

DC Electrical Characteristics (T_A = TOPR, V_{CC} = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current			± 1	µA	$V_{IN} = V_{SS}$ to V_{CC}
V_{OH}	Output high voltage	2.4			V	I_{OH} = -2.0 mA
V_{OHB}	V_{OH}, backup supply	V_{BC} - 0.3			V	$V_{BC} > V_{CC}$, I_{OH} = -10µA
V_{OL}	Output low voltage			0.4	V	I_{OL} = 4.0 mA
I_{CC}	Operating supply current		3	6	mA	No load on V_{OUT}, $\overline{CE}_{CON1}$, and $\overline{CE}_{CON2}$
V_{PFD}	Power-fail detect voltage	4.65	4.62	4.75	V	THS = V_{SS}
		4.30	4.37	4.50	V	THS = V_{OUT}
V_{SO}	Supply switch-over voltage		V_{BC}		V	
I_{CCDR}	Data-retention mode current			100	nA	No load on V_{OUT}, $\overline{CE}_{CON1}$, and $\overline{CE}_{CON2}$
V_{OUT1}	V_{OUT} voltage	V_{CC} - 0.2			V	$V_{CC} > V_{BC}$, I_{OUT} = 100mA
		V_{CC} - 0.3			V	$V_{CC} > V_{BC}$, I_{OUT} = 160mA
V_{OUT2}	Vow voltage	V_{BC} - 0.2			V	$V_{CC} < V_{BC}$, I_{OUT} = 100µA
V_{BC}	Active backup cell voltage		V_{BCS}		V	V_{BCS} > 2.5V
			V_{BCP}		V	V_{BCS} < 2.5V
R_{BCS}	BCs charge output internal resistance	500	1000	1750	Ω	$V_{BCSO} \geq$ 3.0V
V_{BCSO}	BCs charge output voltage	3.0	3.3	3.6	V	$V_{CC} > V_{PFD}$, $\overline{RST}$ inactive, full charge or no load
I_{OUT1}	V_{OUT} current			160	mA	Vow ≥ V_{CC} - 0.3V
I_{OUT2}	V_{OUT} current		100		µA	Vow ≥ V_{BC} - 0.2V

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC}.

Capacitance (T_A = 25°C, F = 1 MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
C_{IN}	Input capacitance			8	pF	Input voltage = 0V
C_{OUT}	Output capacitance			10	pF	Output voltage = 0V

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0 V to 3.0 V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figure 3

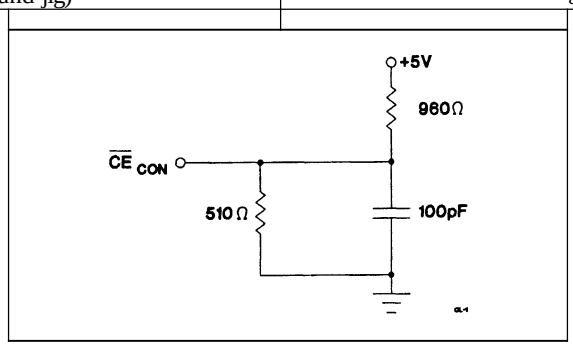


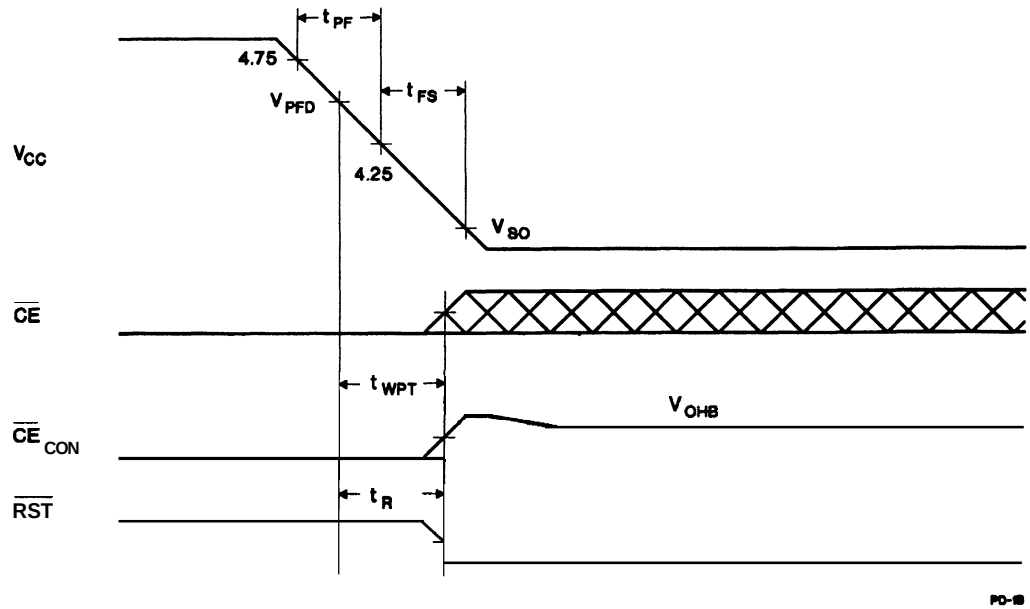
Figure 3. Output Load

Power-Fail Control ($T_A = T_{OPR}$)

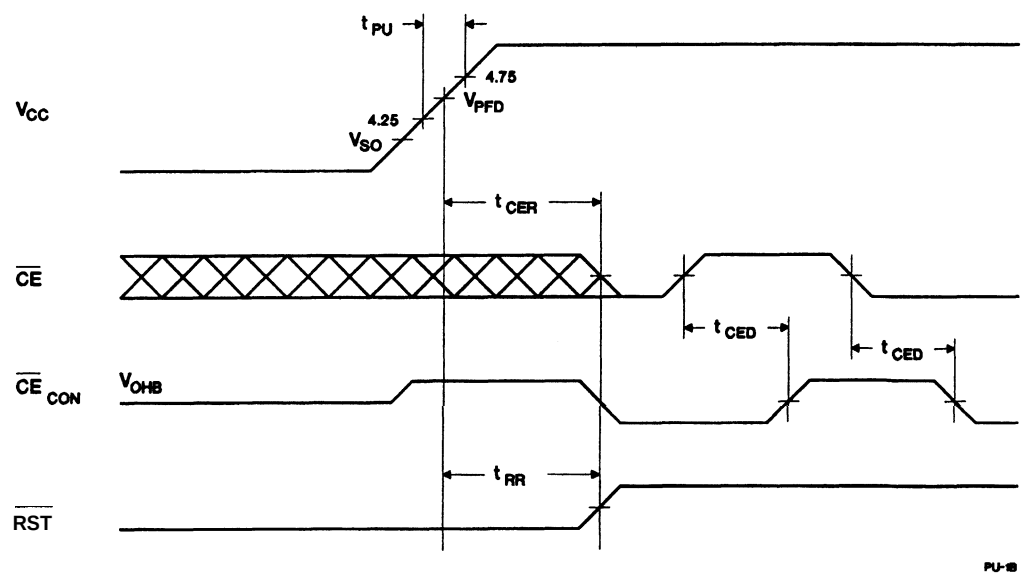
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{PF}	V_{CC} slew 4.75 to 4.25 V	300	-	-	µs	
t_{FS}	V_{CC} slew 4.25 V to V_{SO}	10	-	-	µs	
t_{PU}	V_{CC} slew 4.25 to 4.75 V	0		-	µs	
t_{CED}	Chip-enable propagation delay		7	10	ns	
t_{CER}	Chip-enable recovery time	t_{RR}	-	t_{RR}	ms	Time during which SRAM is write-protected after V_{CC} passes VPFD on power-up
t_{RR}	V_{PFD} to $\overline{RST}$ inactive	40	80	120	ms	Time, after V_{CC} becomes valid, before $\overline{RST}$ is cleared
t_{AS}	Input A set up to $\overline{CE}$	0		-	ns	
t_{WPT}	Write-protect time	t_R	-	t_R	µs	Delay after V_{CC} slews down past VPFD before SRAM is write-protected
t_R	V_{PFD} to $\overline{RST}$ active	40	100	150	µs	Delay after V_{CC} slews down past VPFD before $\overline{RST}$ is active

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.

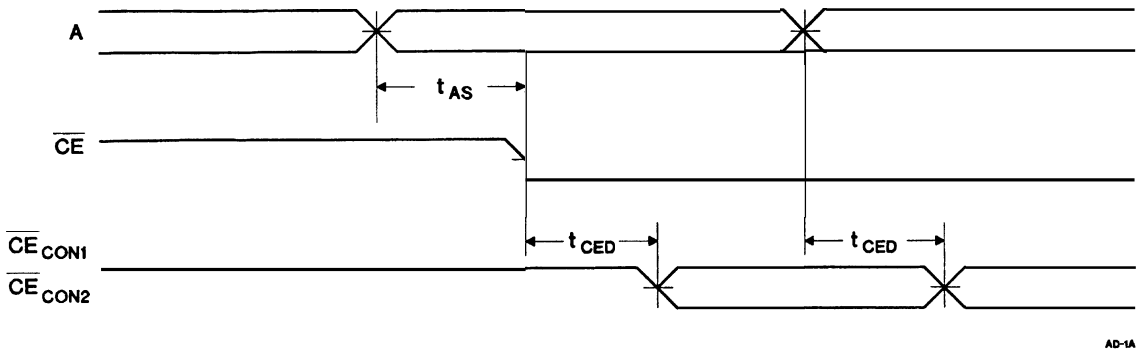
Power-Down Timing



Power-Up Timing



Address-Decode Timing



Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	2	Deleted last sentence	Clarification
1	6	V_{BCSO}—BCs charge output voltage	Was 3.15 min, 3.3 typ, 3.45 max; is 3.0 min, 3.3 typ, 3.6 max
2	5	Maximum charge output internal resistance (R_{BCS}) changed to 175022	Was 1500Ω

Note: Change 1 = Dec. 1992 B changes from Sept. 1991 A.
Change 2 = Nov. 1994 C changes from Dec. 1992 B.

Ordering Information

bq2202 _ _

Temperature Range:
blank = Commercial (0 to +70°C)
N = Industrial (-40 to +85°C)

Package Option:
PN = 16-pin narrow plastic DIP
SN = 16-pin narrow SOIC

Device:
bq2202 SRAM Nonvolatile Controller With Reset

BENCHMARQ

bq2203A

NV Controller With Battery Monitor

Features

- Power monitoring and switching for nonvolatile control of SRAMs
- Write-protect control
- Battery-low and battery-fail indicators
- Reset output for system power-on reset
- Input decoder allows control of up to 2 banks of SRAM
- 3V primary cell input
- 3V rechargeable battery inpuvoutput

General Description

The CMOS bq2203A SRAM Nonvolatile Controller With Battery Monitor provides all the necessary functions for converting one or two banks of standard CMOS SRAM into nonvolatile read/write memory. The bq2203A is compatible with the Personal Computer Memory Card International Association (PCMCIA) recommendations for battery-backed static RAM memory cards.

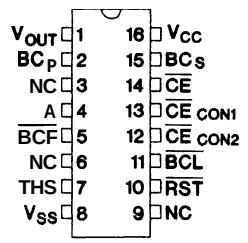
A precision comparator monitors the 5V V_{CC} input for an out-of-tolerance condition. When out of tolerance is detected, the two conditioned chip enable outputs are forced inactive to write-protect both banks of SRAM.

Power for the external SRAMs is switched from the V_{CC} supply to the battery-backup supply as V_{CC} decays. On a subsequent power-up, the V_{OUT} eupply is automatically switched from the backup supply to the V_{CC} supply. The external SRAMs are write-protected until a power-valid condition e d . The reset output provides power-fail and power-on resets for the system. The battery monitor indicates battery-low and battery-fail conditions.

During power-valid operation, the input–decoder selects one of two banks of SRAM.

4

Pin Connections



16-Pin Narrow DIP or SOIC

PN-26

Pin Names

V_{OUT}	Supply output
$\overline{RST}$	Reset output
THS	Threshold select input
$\overline{CE}$	Chip enable active low input
$\overline{CE}_{CON1}$, $\overline{CE}_{CON2}$	Conditioned chip enable outputs
A	Bank select input
$\overline{BCF}$	Battery fail push-pull output
$\overline{BCL}$	Battery low push-pull output
BC_P	3V backup supply input
BC_S	3V rechargeable backup supply input/output
NC	No conned
V_{CC}	+5 volt supply input
V_{SS}	Ground

Functional Description

Two banks of CMOS static RAM can be battery-backed using the V_{OUT} and the conditioned chip enable output pins from the bq2203A. As the voltage input V_{CC} slews down during a power failure, the two conditioned chip enable outputs, $\overline{CE}_{CON1}$ and $\overline{CE}_{CON2}$, are forced inactive independent of the chip enable input $\overline{CE}$.

This activity unconditionally write-protects external SRAM as V_{CC} falls to an out-of-tolerance threshold V_{PFD}. V_{PFD} is selected by the threshold select input pin, THS. If THS is tied to V_{SS}, the power-fail detection occurs at 4.62V typical for 5% supply operation. If THS is tied to V_{CC}, power-fail detection occurs at 4.37V typical for 10% supply operation. The THS pin must be tied to V_{SS} or V_{CC} for proper operation.

If a memory access is in process to any of the two external banks of SRAM during power-fail detection, that memory cycle continues to completion before the memory is write-protected. If the memory cycle is not terminated within time t_{WPT} (150µs maximum), the two chip enable outputs are unconditionally driven high, write-protecting the controlled SRAMs.

As the supply continues to fall past V_{PFD}, an internal switching device forces V_{OUT} to the external backup energy source. $\overline{CE}_{CON1}$ and $\overline{CE}_{CON2}$ are held high by the V_{OUT} energy source.

During power-up, V_{OUT} is switched back to the 5V supply as V_{CC} rises above the backup cell input voltage sourcing V_{OUT}. Outputs $\overline{CE}_{CON1}$ and $\overline{CE}_{CON2}$ are held inactive for time t_{CER} (120ms maximum) after the power supply has reached V_{PFD}, independent of the $\overline{CE}$ input, to allow for processor stabilization.

During power-valid operation, the $\overline{CE}$ input is passed through to one of the two $\overline{CE}_{CON}$ outputs with a propagation delay of less than 10ns. The $\overline{CE}$ input is output on one of the two $\overline{CE}_{CON}$ output pins depending on the level of bank select input A, as shown in the Truth Table.

Bank select input A is usually tied to a high-order address pin so that a large nonvolatile memory can be designed using lower-density memory devices. Nonvolatility and decoding are achieved by hardware hookup as shown in Figure 1.

The reset output ($\overline{RST}$) goes active within t_{PFD} (150µs maximum) after V_{PFD}, and remains active for a minimum of 40ms (120ms maximum) after power returns valid. The $\overline{RST}$ output can be used as the power-on reset for a microprocessor. Access to the external RAM may begin when $\overline{RST}$ returns inactive.

Energy Cell Inputs—BC_P, BC_S

Two backup energy source inputs are provided on the bq2203A—a primary cell BC_P and a secondary cell BC_S. The primary cell input is designed to accept any 3V primary battery (non-rechargeable), typically some type of Lithium chemistry. If a primary cell is not to be used, the BC_P pin should be tied to V_{SS}. The secondary cell input BC_S is designed to accept constant-voltage current-limited rechargeable cells.

During normal +5V power valid operation, 3.3V typical is output on the BC_S pin and is current-limited internally. Although this charging method can be used with various 3V secondary cells, it is specifically designed for a Panasonic VL (vanadium-lithium) series of rechargeable cells.

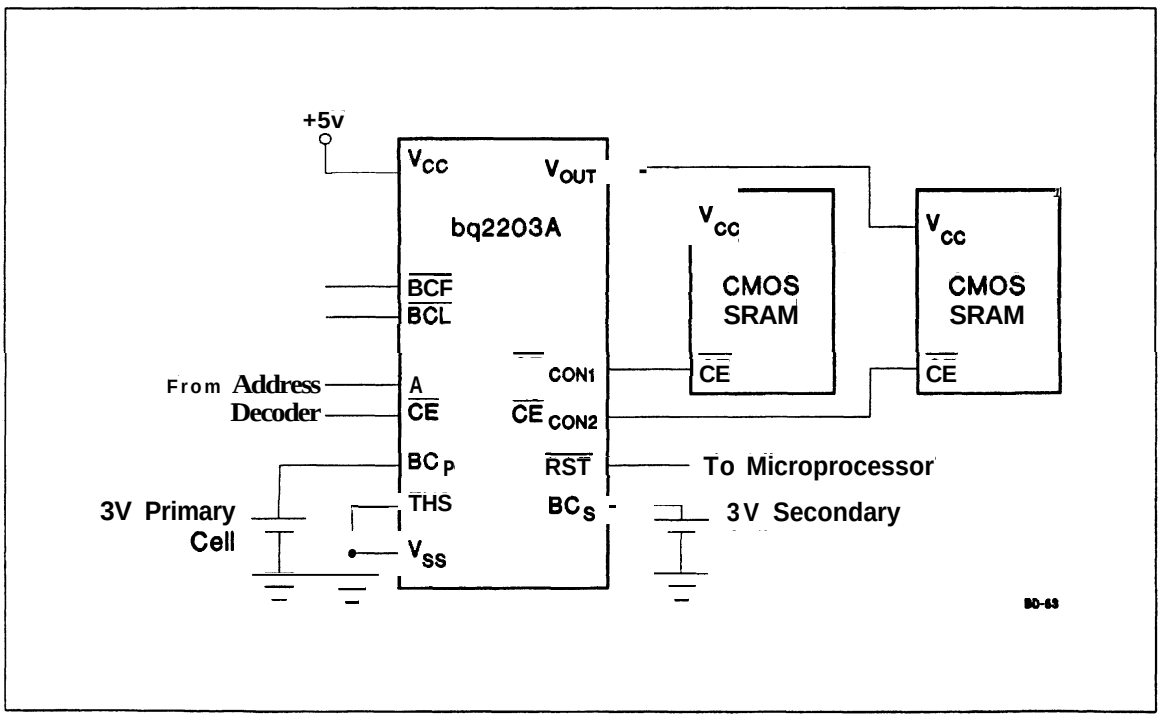


Figure 1. Hardware Hookup (5% Supply Operation)

If a secondary cell is not to be used, the BC_S pin must be tied directly to V_{SS}.

V_{CC} falling below V_{PFD} starts the comparison of BC_S and BC_P. The BC input comparison continues until V_{CC} rises above V_{SO}. Power to V_{OUT} begins with BC_S and switches to BC_P only when BC_S is less than BC_P minus V_{BSO}. The controller alternates to the higher BC voltage when the difference between the BC input voltages is greater than V_{BSO}. Alternating the backup batteries allows one-at-a-time battery replacement and efficient use of both backup batteries.

To prevent battery drain when there is no valid data to retain, V_{OUT}, $\overline{CE}_{CON1}$, and $\overline{CE}_{CON2}$ are internally isolated from BC_P and BC_S by either:

- Initial connection of a battery to BC_P *or* BC_S (V_{CC} grounded) or
- Presentation of an isolation signal on $\overline{CE}$.

A valid isolation signal requires $\overline{CE}$ low as V_{CC} crosses both V_{PFD} and V_{SO} during a power-down. Between these two points in time, $\overline{CE}$ must be brought to V_{CC}*(0.48 to 0.52) and held for at least 700ns. The isolation signal is invalid if $\overline{CE}$ exceeds V_{CC}*0.54 at any point between V_{CC} crossing V_{PFD} and V_{SO}. See Figure 2.

The isolation function is terminated and the appropriate battery is connected to V_{OUT}, $\overline{CE}_{CON1}$, and $\overline{CE}_{CON2}$ by powering Vcc up through V_{PFD}.

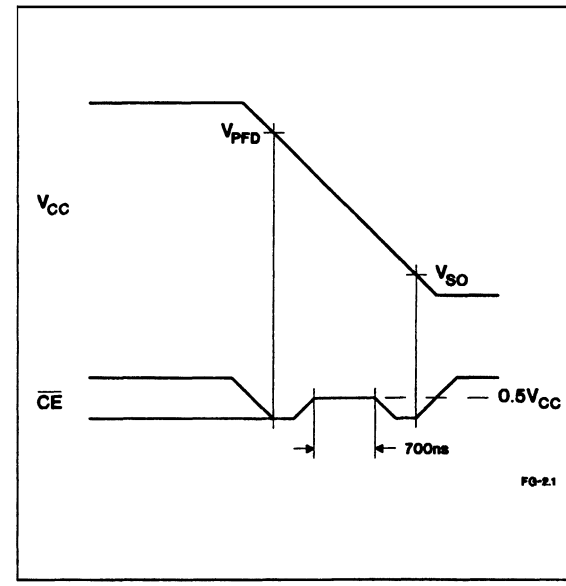


Figure 2. Battery Isolation Signal

Battery Monitor —$\overline{BCL}$, $\overline{BCF}$

As V_{CC} rises past V_{PFD}, the battery voltage on BC_P is compared with a dual voltage reference. The result of this comparison is latched internally, and output after t_{BC} when V_{CC} rises past V_{PFD}. If the battery voltage on BC_P is below V_{BL}, then $\overline{BCL}$ is asserted low. If the battery is below V_{BF}, then $\overline{BCL}$ and $\overline{BCF}$ are asserted low. The results of this comparison remain latched until Vcc falls below V_{PFD}.

Truth Table

Input		Output	
$\overline{CE}$	A	$\overline{CE}_{CON1}$	$\overline{CE}_{CON2}$
H	X	H	H
L	L	L	H
L	H	H	L

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on Vcc relative to Vss	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding Vcc relative to Vss	-0.3 to 7.0	V	$V_T \le V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to 70	°C	Commercial
		-40 to +85	°C	"N" Industrial
T_{STG}	Storage temperature	-55 to 125	°C	
T_{BIAS}	Temperature under bias	-40 to 85	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds
I_{OUT}	V_{OUT} current	200	mA	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbd	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.75	5.0	5.5	V	THS = V_{SS}
		4.50	5.0	5.5	V	THS = V_{CC}
V_{BCP}	Backup cell input voltage	2.0		4.0	V	$V_{CC} < V_{BC}$
V_{BCS}		2.0		4.0	V	$V_{CC} < V_{BC}$
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3		0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	
THS	Threshold select	-0.3	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C, Vcc = 5V.

DC Electrical Characteristics (T_A = TOPR, V_{CC} = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current			± 1	µA	V_{IN} = V_{SS} to V_{CC}
V_{OH}	Output high voltage	2.4			V	I_{OH} = -2.0 mA
V_{OHB}	VOH, backup supply	V_{BC} - 0.3			V	V_{BC} > Vcc, I_{OH} = -10µA
V_{OL}	Output low voltage			0.4	V	I_{OL} = 4.0 mA
I_{CC}	Operating supply current		3	6	mA	No load on outputs
V_{PFD}	Power-fail detect voltage	4.55	4.62	4.75	V	THS = V_{SS}
		4.30	4.37	4.50	V	THS = V_{CC}
V_{SO}	Supply switch-over voltage		V_{BC}		V	
I_{CCDR}	Data-retention mode current			100	nA	No load on outputs
V_{BC}	Active backup cell voltage		V_{BCS}		V	V_{BCS} > V_{BCP} + V_{BSO}
			V_{BCP}		V	V_{BCP} > V_{BCS} + V_{BSO}
V_{BSO}	Battery switch-over voltage	0.25	0.4	0.6	V	
R_{BCS}	BCs charge output internal resistance	500	1000	1750	Ω	V_{BCSO} ≥ 3.0V
V_{BCSO}	BCs charge output voltage	3.15	3.3	3.5	V	V_{CC} > V_{PFD}, $\overline{RST}$ inactive, full charge or no load
I_{OUT1}	Vowrcurrent			160	mA	V_{OUT} 2 V_{CC} - 0.3V
I_{OUT2}	VOUT current		100		µA	V_{OUT} ≥ V_{BC} - 0.2V
V_{BL}	Voltage battery low	2.3		2.5	V	BCP input only
V_{BF}	Voltage battery fail	2.0		2.2	V	BCP input only

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC}.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbd	Parameter	Minimum	Typical	Maximum	Unit	Conditions
C_{IN}	Input capacitance			8	pF	Input voltage = OV
C_{OUT}	Output capacitance			10	pF	Output voltage = 0V

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0 V to 3.0 V
Input rise and fall times	5ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figure 3

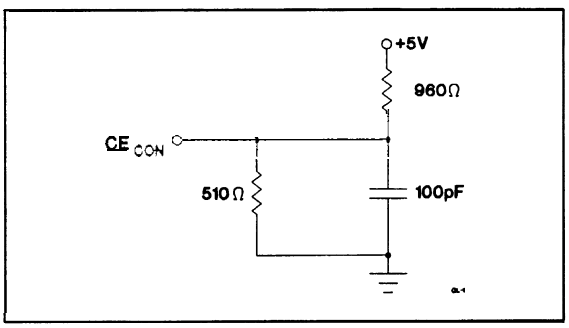


Figure 3. Output Load

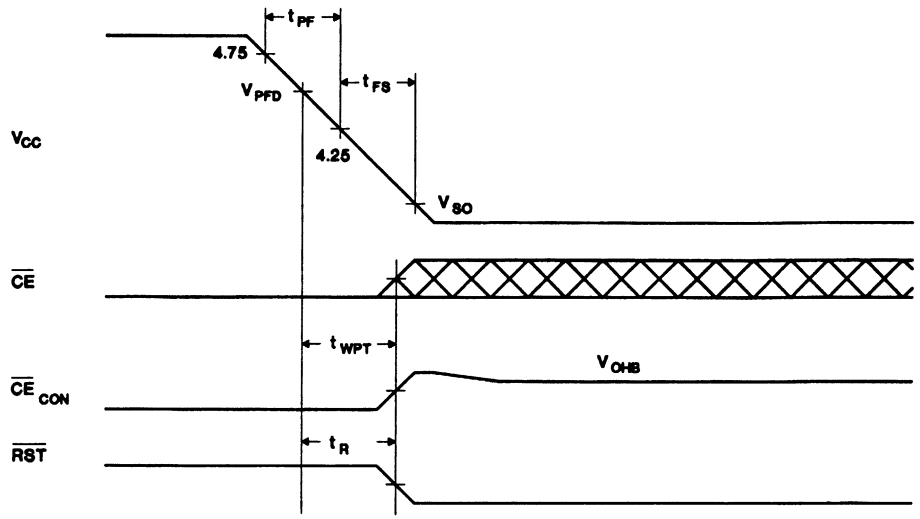
Power-Fail Control (T_A = TOPR)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{PF}	V_{CC} slew 4.75 to 4.25 V	300	-	-	µs	
t_{FS}	V_{CC} slew 4.25 V to Vso	10	-	-	µs	
t_{PU}	V_{CC} slew 4.25 to 4.75 V	0		-	µs	
t_{CED}	Chip-enable propagation delay		7	10	ns	
t_{CER}	Chip-enable recovery time	40	80	120	ms	Time during which SRAM is write-protected after V_{CC} passes V_{PFD} on power-up
t_{RR}	V_{PFD} to $\overline{RST}$ inactive	t_{CER}	-	t_{CER}	ms	Time, after V_{CC} becomes valid, before $\overline{RST}$ is cleared
t_{AS}	Input A set up to $\overline{CE}$	0		-	ns	
t_{WPT}	Write-protect time	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected
t_R	V_{PFD} to $\overline{RST}$ active	t_{WPT}	-	t_{WPT}	µs	Delay after V_{CC} slews down past V_{PFD} before $\overline{RST}$ is active
t_{BC}	V_{PFD} to $\overline{BCL}/\overline{BCF}$ active	t_{CER}	-	t_{CER}	ms	Delay after V_{CC} slews up past V_{PFD} before $\overline{BCL}$ or $\overline{BCF}$ is active

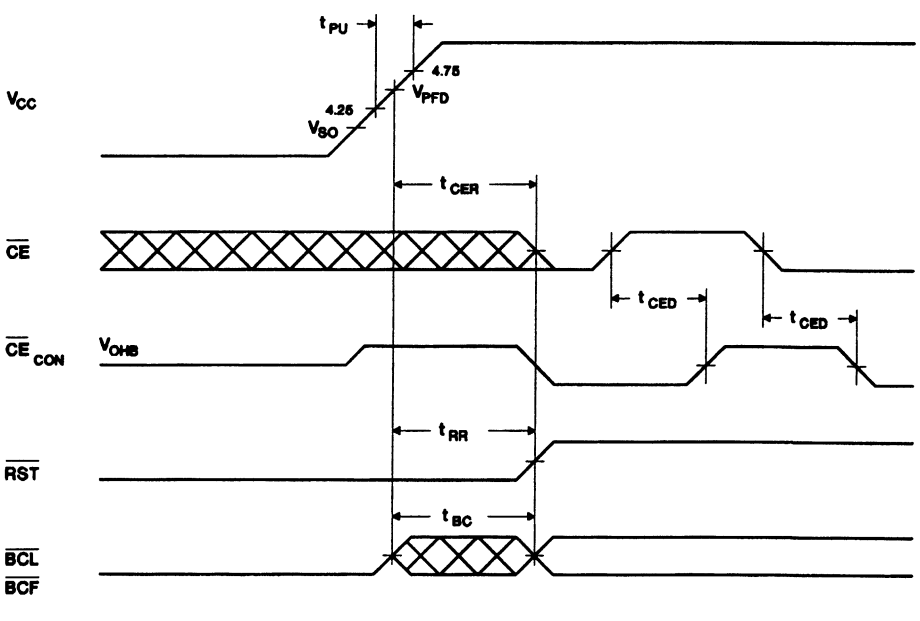
Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.

Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

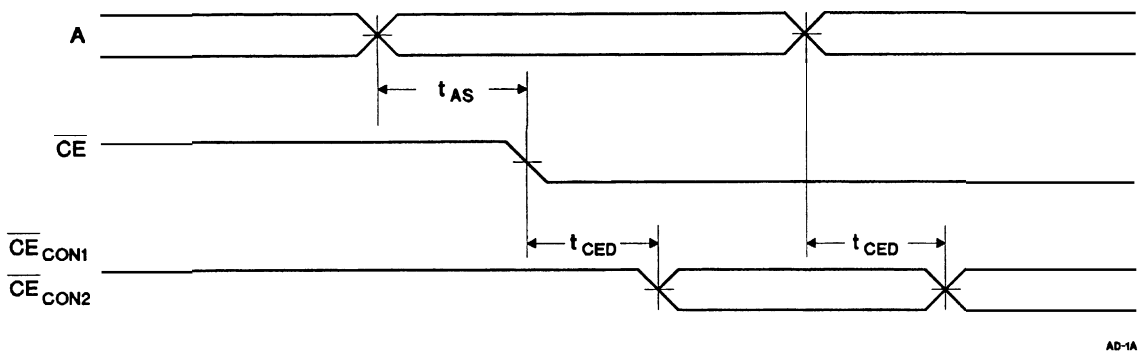
Power-Down Timing



Power-Up Timing



Address-Decode Timing



Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1		Data sheet changed from "Preliminary" to "Final"	
1	5	Maximum charge output internal resistance (R_{BCS}) changed to 1750Ω	Was 1500Ω

Note: Change 1 = Nov. 1994 B changes from Dec. 1992.

Ordering Information

bq2203A _ _

Temperature Range:
blank = Commercial (0 to +70°C)
N = Industrial (-40 to +85°C)*

Package Option:
PN = 16-pin plastic DIP Narrow
SN = 16-pin SOIC Narrow

Device:
bq2203A SRAM Nonvolatile Controller
With Battery Monitor and Reset

'Contact factory for availability.

BENCHMARQ

bq2204A

X4 SRAM Nonvolatile Controller Unit

Features

- Power monitoring and switching for 3 volt battery-backup applications
- Write-protect control
- 2-input decoder allows control for up to 4 banks of SRAM
- 3 volt primary cell inputs
- Less than 10 ns chip enable propagation delay
- 5% or 10% supply operation

General Description

The CMOS bq2204A SRAM Nonvolatile Controller Unit provides all necessary functions for converting up to four banks of standard CMOS SRAM into nonvolatile read/write memory.

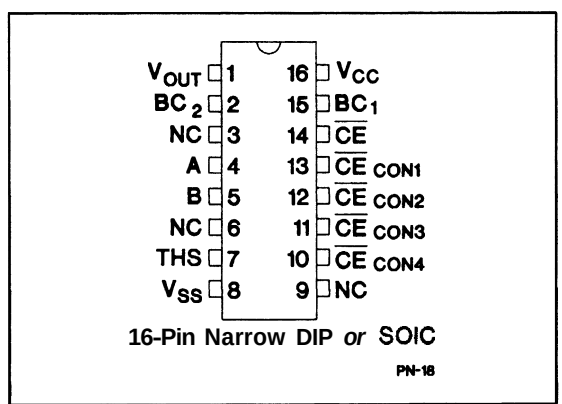
A precision comparator monitors the 5V Vcc input for an out-of-tolerance condition. When out of tolerance is detected, the four conditioned chip enable outputs are forced inactive to write-protect up to four banks of SRAM.

During a power failure, the external SRAMs are switched from the Vcc supply to one of two 3V backup supplies. On a subsequent power-up, the SRAMs are write-protected until a power-valid condition exists.

During power-valid operation, a two-input decoder transparently selects one of up to four banks of SRAM.

4

Pin Connections



16-Pin Narrow DIP or SOIC

PN-18

Pin Names

V_{OUT}	Supply output
BC_1-BC_2	3 volt primary backup cell inputs
THS	Threshold select input
$\overline{CE}$	Chip enable active low input
$\overline{CE}_{CON1}$-$\overline{CE}_{CON4}$	Conditioned chip enable outputs
A-B	Decoder inputs
NC	No connect
V_{CC}	+5 volt supply input
VSS	Ground

Functional Description

Up to four banks of CMOS static RAM can be battery-backed using the V_{OUT} and conditioned chip enable output pins from the bq2204A. As V_{CC} slews down during a power failure, the conditioned chip enable outputs $\overline{CE}_{CON1}$ through $\overline{CE}_{CON4}$ are forced inactive independent of the chip enable input $\overline{CE}$.

This activity unconditionally write-protects the external SRAM as V_{CC} falls below an out-of-tolerance threshold V_{PFD}. V_{PFD} is selected by the threshold select input pin, THS. If THS is tied to V_{SS}, the power-fail detection occurs at 4.62V typical for 5% supply operation. If THS is tied to V_{CC}, power-fail detection occurs at 4.37V typical for 10% supply operation. The THS pin must be tied to V_{SS} or V_{CC} for proper operation.

If a memory access is in process to any of the four external banks of SRAM during power-fail detection, that memory cycle continues to completion before the memory is write-protected. If the memory cycle is not terminated within time t_{WPT}, all four chip enable outputs are unconditionally driven high, write-protecting the controlled SRAMs.

As the supply continues to fall past V_{PFD}, an internal switching device forces V_{OUT} to one of the two external backup energy sources. $\overline{CE}_{CON1}$ through $\overline{CE}_{CON4}$ are held high by the V_{OUT} energy source.

During power-up, V_{OUT} is switched back to the 5V supply as V_{CC} rises above the backup cell input voltage sourcing V_{OUT}. Outputs $\overline{CE}_{CON1}$ through $\overline{CE}_{CON4}$ are held inactive for time t_{CER} (120 ma maximum) after the power supply has reached V_{PFD}, independent of the $\overline{CE}$ input, to allow for processor stabilization.

During power-valid operation, the $\overline{CE}$ input is passed through to one of the four $\overline{CE}_{CON}$ outputs with a propagation delay of less than 10 ns. The $\overline{CE}$ input is output on one of the four $\overline{CE}_{CON}$ output pins depending on the level of the decode inputs at A and B as shown in the Truth Table.

The A and B inputs are usually tied to high-order address pins so that a large nonvolatile memory can be designed using lower-density memory devices. Nonvolatility and decoding are achieved by hardware hookup as shown in Figure 1.

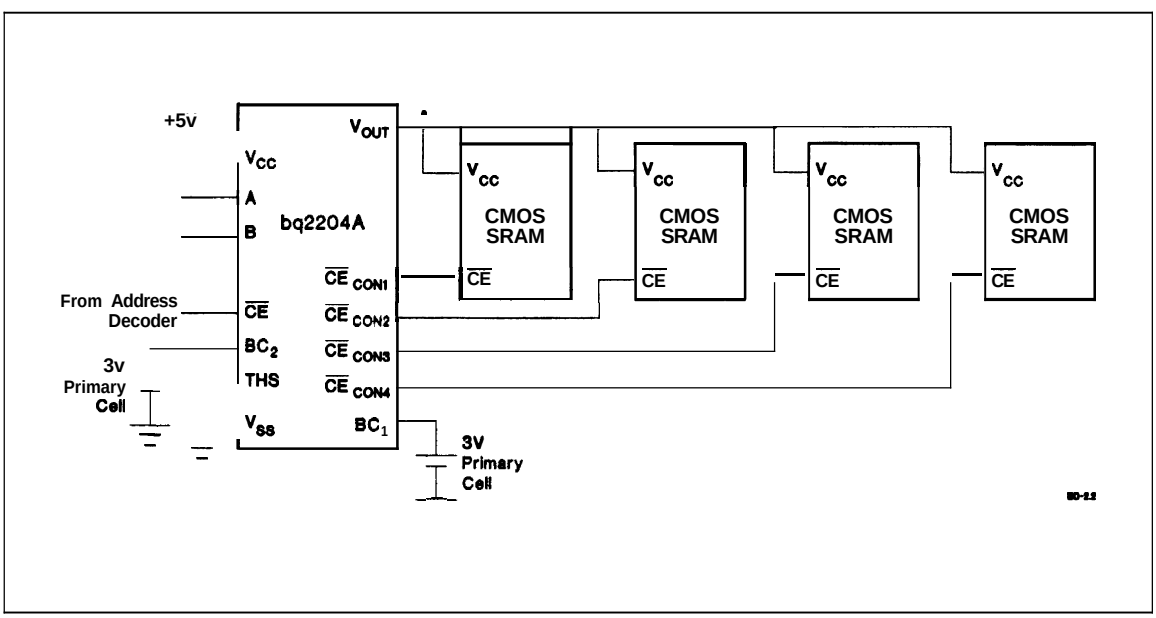


Figure 1. Hardware Hookup (5% Supply Operation)

Energy Cell Inputs—BC_1, BC_2

Two backup energy source inputs are provided on the bq2204A. The BC_1 and BC_2 inputs accept a 3V primary battery (non-rechargeable), typically some type of lithium chemistry. If no primary cell is to be used on either BC_1 or BC_2, the unused input should be tied to vss.

Vcc falling below V_{PFD} starts the comparison of BC_1 and BC_2. The BC input comparison continues until V_{CC} rises above Vso. Power to V_{OUT} begins with BC_1 and switches to BC_2 only when V_{BC1} is less than V_{BC2} minus V_{BSO}. The controller only alternates to the higher BC voltage when the difference between the BC input voltages is greater than V_{BSO}. Alternating the backup batteries allows one-at-a-time battery replacement and efficient use of both backup batteries.

To prevent battery drain when there is no valid data to retain, V_{OUT} and $\overline{CE}_{CON1-4}$ are internally isolated from BC_1 and BC_2 by either:

- Initial connection of a battery to BC_1 or BC_2, or
- Presentation of an isolation signal on $\overline{CE}$.

A valid isolation signal requires $\overline{CE}$ low as V_{CC} crosses both V_{PFD} and V_{SO} during a power-down. Between these two points in time, $\overline{CE}$ must be brought to the point of (0.48 to 0.52)*V_{CC} and held for at least 700ns. The isolation signal is invalid if $\overline{CE}$ exceeds 0.54*V_{CC} at any point between Vcc crossing V_{PFD} and V_{SO}. See Figure 2.

The appropriate battery is connected to V_{OUT} and $\overline{CE}_{CON1-4}$ immediately on subsequent application and removal of V_{CC}.

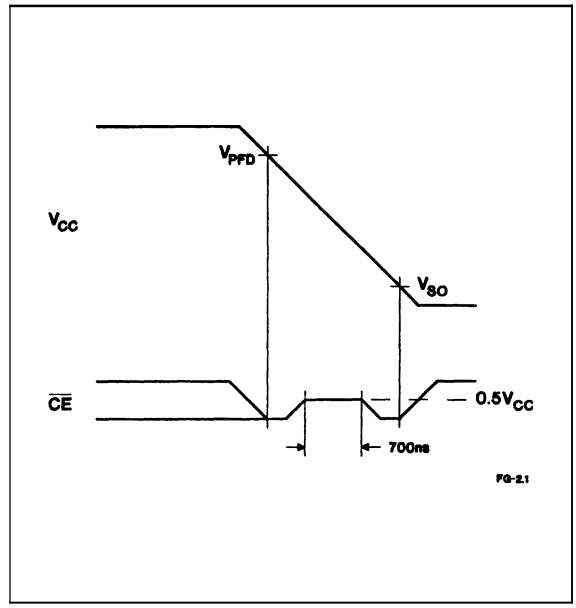


Figure 2. Battery Isolation Signal

4

Truth Table

Inputs			Outputs			
$\overline{CE}$	A	B	$\overline{CE}_{CON1}$	$\overline{CE}_{CON2}$	$\overline{CE}_{CON3}$	$\overline{CE}_{CON4}$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \le V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
		-40 to +85	°C	Industrial "N"
T_{STG}	Storage temperature	-65 to +125	°C	
T_{BIAS}	Temperature under bias	-40 to +85	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds
I_{OUT}	V_{OUT} current	200	mA	

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbd	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.75	5.0	5.5	V	THS = V_{SS}
		4.50	5.0	5.5	V	THS = V_{CC}
Vss	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3		0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	
V_{BC1}, V_{BC2}	Backup cell voltage	2.0		4.0	V	$V_{CC} < V_{BC}$
THS	Threshold select	-0.3	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC}.

DC Electrical Characteristics (T_A = TOPR, VCC = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current			± 1	µA	$V_{IN} = V_{SS}$ to V_{CC}
V_{OH}	Output high voltage	2.4			V	I_{OH} = -2.0 mA
V_{OHB}	V_{OH}, BC supply	V_{BC} - 0.3			V	$V_{BC} > V_{CC}$, I_{OH} = -10µA
V_{OL}	Output low voltage			0.4	V	I_{OL} = 4.0 mA
I_{CC}	Operating supply current		3	6	mA	No load on outputs.
V_{PFD}	Power-fail detect voltage	4.55	4.62	4.75	V	THS = V_{SS}
		4.30	4.37	4.50	V	THS = V_{CC}
V_{SO}	Supply switch-over voltage		V_{BC}		V	
I_{CCDR}	Data-retention mode current			100	nA	V_{OUT} data-retention current to additional memory not included.
V_{BC}	Active backup cell voltage		V_{BC1}		V	$V_{BC1} > V_{BC2} + V_{BSO}$
			V_{BC2}		V	$V_{BC2} > V_{BC1} + V_{BSO}$
V_{BSO}	Battery switch-over voltage	0.25	0.4	0.6	V	
I_{OUT1}	V_{OUT} current			160	mA	$V_{OUT} > V_{CC}$ - 0.3V
I_{OUT2}	V_{OUT} current		100		µA	$V_{OUT} > V_{BC}$ - 0.2V

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC}.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
C_{IN}	Input capacitance			8	pF	Input voltage = 0V
C_{OUT}	Output capacitance			10	pF	Output voltage = 0V

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0 V to 3.0 V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figure 3

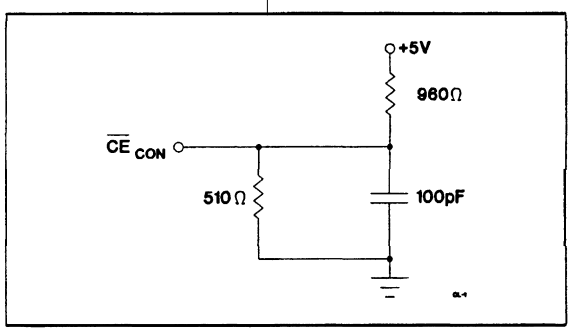


Figure 3. Output Load

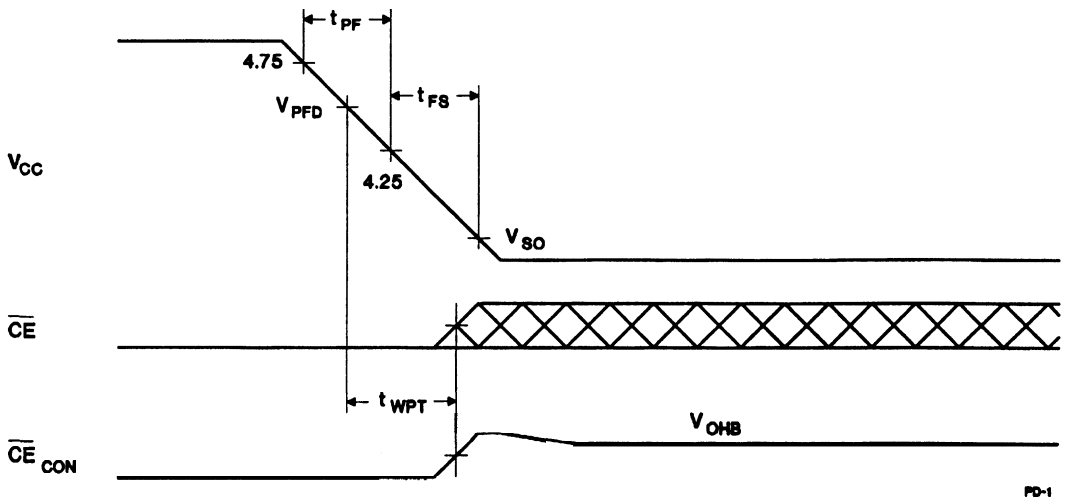
Power-Fail Control (TA = TOPR)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{PF}	V_{CC} slew, 4.75V to 4.25V	300	-	-	µs	
t_{FS}	Vcc slew, 4.25V to Vso	10			µs	
t_{PU}	V_{CC} slew, 4.25V to 4.75V	0			µs	
t_{CED}	Chip enable propagation delay		7	10	ns	
t_{AS}	A,B set up to $\overline{CE}$	0			ns	
t_{CER}	Chip enable recovery	40	80	120	ma	Time during which SRAM is write-protected after Vcc passes V_{PFD} on power-up.
t_{WPT}	Write-protect time	40	100	150	µs	Delay after Vcc slews down past V_{PFD} before SRAM is write-protected.

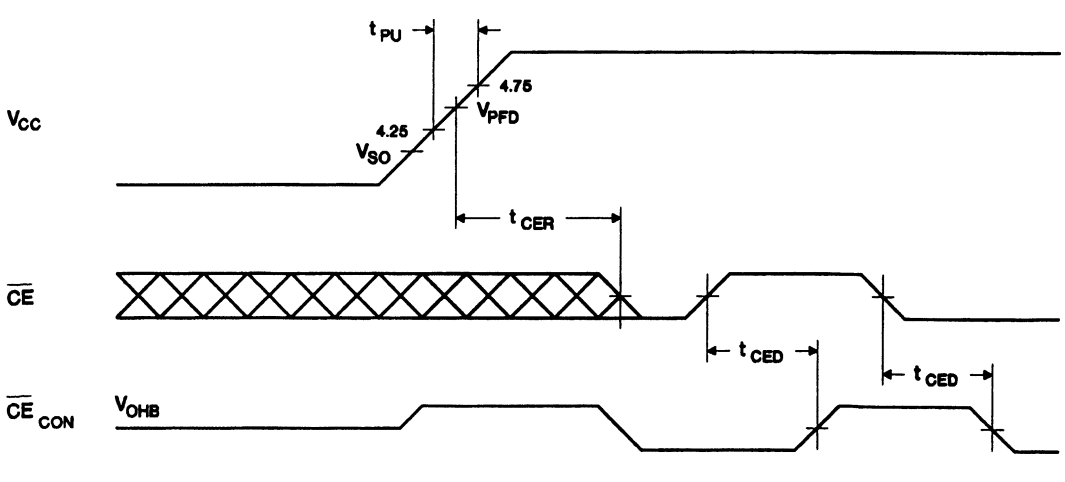
Note: Typical values indicate operation at T_A = 25°C, Vcc = 5V.

Caution: **Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode *may* affect data integrity.**

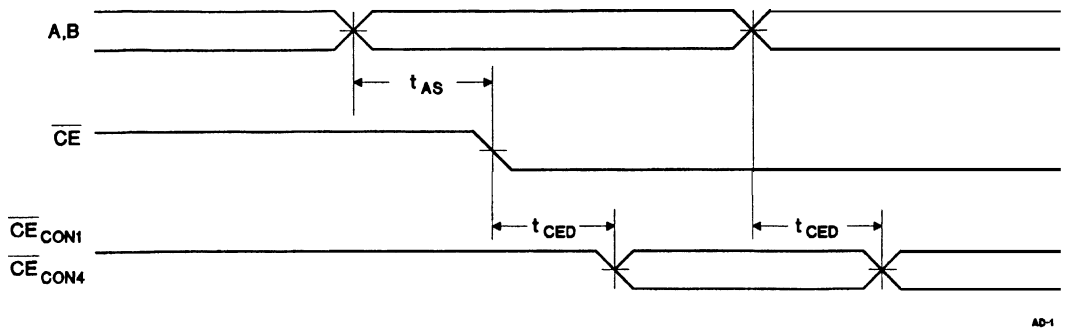
Power-Down Timing



Power-Up Timing



Address-Decode Timing



Data Sheet Revision History

Change No.	Page No.	Description of Change	Nature of Change
1	All	bq2204A replaces bq2204.	
1	1, 4–5	10% tolerance requires the THS pin to be tied to Vcc, not VOUT.	
1	3	Energy cell input selection process alternates between BC_1 and BC2.	

Note: Change 1 = Dec. 1992 changes from Sept. 1991

Ordering Information

bq2204A

Temperature Range:
blank = Commercial (0 to +70°C)
N = Industrial (-40 to +85°C)

Package Option:
PN = 16-pin narrow plastic DIP
SN = 16-pin narrow SOIC

Device:
bq2204A Nonvolatile SRAM Controller

BENCHMARQ

bq2502

Integrated Backup Unit

Features

- Power monitoring, backup supply, and switching for 3V battery-backup applications
- Write-protect control
- Input decoder allows control of up to 2 banks of SRAM
- 3V backup power output
- Internal 130mAh lithium coin cell
- Reset output for system power-on reset
- Less than 10ns chip enable propagation delay
- 5% or 10% supply operation

General Description

The CMOS bq2502 Integrated Backup Unit provides all the necessary functions for converting one or two banks of standard CMOS SRAM into nonvolatile read/write memory.

A precision comparator monitors the 5V V_{CC} input for an out-of-tolerance condition. When out of tolerance is detected, the two conditioned chip enable outputs are forced inactive to write-protect both banks of SRAM.

Power for the external SRAMs is switched from the Vcc supply to the internal battery-backup supply as V_{CC} decays. On a subsequent power-up, the V_{OUT} supply is automatically switched from the internal lithium supply to the V_{CC} supply.

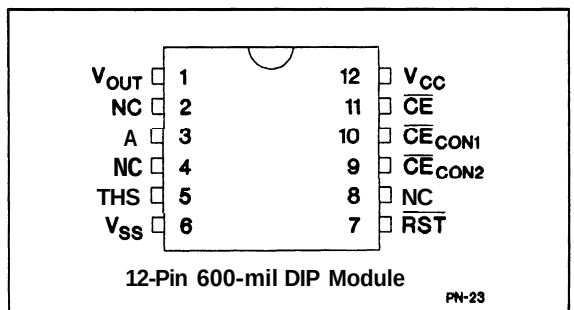
The external SRAMs are write-protected until a power-valid condition exists. The reaet output provides power-fail and power-on resets for the system.

During power-valid operation, the input decoder selects one of two banks of SRAM.

The internal lithium cell is initially electrically isolated, protecting the battery from accidental discharge. Connection to the battery is made only after the first application of VCC.

4

Pin Connections



12-Pin 600-mil DIP Module

PN-23

Pin Names

V_{OUT}	supply output
$\overline{RST}$	Reset output
THS	Threshold select input
$\overline{CE}$	Chip enable active low input
$\overline{CE}_{CON1}$, $\overline{CE}_{CON2}$	Conditioned chip enable outputs
A	Bank select input
NC	No connect
V_{CC}	+5 volt supply input

Functional Description

Two banks of CMOS static RAM can be battery-backed using the V_{OUT} and conditioned chip enable output pins from the bq2502. As the voltage input Vcc slews down during a power failure, the two conditioned chip enable outputs, $\overline{CE}_{CON1}$ and $\overline{CE}_{CON2}$, are forced inactive independent of the chip enable input $\overline{CE}$.

This activity unconditionally write-protects external SRAM as V_{CC} falls to an out-of-tolerance threshold V_{PFD}. V_{PFD} is selected by the threshold select input pin, THS. If THS is tied to V_{SS}, the power-fail detection occurs at 4.62V typical for 5% supply operation. If THS is tied to VOW, power-fail detection occurs at 4.37V typical for 10% supply operation. The THS pin must be tied to V_{SS} or V_{OUT} for proper operation.

If a memory access is in process to any of the two external banks of SRAM during power-fail detection, that memory cycle continues to completion before the memory is write-protected. If the memory cycle is not terminated within time t_{WPT} (150µs maximum), the two chip enable outputs are unconditionally driven high, write-protecting the controlled SRAMs.

As the supply continues to fall past V_{PFD}, an internal switching device forces V_{OUT} to the internal backup energy source. $\overline{CE}_{CON1}$ and $\overline{CE}_{CON2}$ are held high by the V_{OUT} energy source.

During power-up, V_{OUT} is switched back to the 5V supply as V_{CC} rises above the backup cell input voltage sourcing VOW. Outputs $\overline{CE}_{CON1}$ and $\overline{CE}_{CON2}$ are held inactive for time t_{CER} (120ms maximum) after the power supply has reached V_{PFD}, independent of the $\overline{CE}$ input, to allow for processor stabilization.

The reset output ($\overline{RST}$) goes active within t_R (150 µs maximum) after V_{PFD}, and remains active for a minimum of 40ms (120ms maximum) after power returns valid. The $\overline{RST}$ output can be used as the power-on reset for a microprocessor. Access to the external RAM may begin when $\overline{RST}$ returns inactive.

During power-valid operation, the $\overline{CE}$ input is passed through to one of the two $\overline{CE}_{CON}$ outputs with a propagation delay of less than 10 ns. The $\overline{CE}$ input is output on one of the two $\overline{CE}_{CON}$ output pins depending on the level of bank select input A, as shown in the Truth Table.

Bank select input A is usually tied to a high-order address pin so that a large nonvolatile memory can be designed using lower-density memory devices. Nonvolatility and decoding are achieved by hardware hookup aa shown in Figure 1.

The internal lithium cell is capable of supplying 3V on V_{OUT} for an extended period of time. The cumulative length of time that the external SRAMs retain data in the absence of power is a function of the data-retention current of the SRAMs used. The initial capacity of the internal lithium cell is 130mAh. Typically, if the data-retention currents for two external SRAMs are 1µA per SRAM at room temperature, nonvolatility is calculated to be for more than 7 years. If only one external SRAM is used, the data-retention time increases to more than 13 years.

The bq2502 battery life is a function of the time spent in battery-backed mode and the data-retention current of the external SRAM. For example, office equipment is generally powered on for 8 hours and powered off for 16 hours. Under these conditions, a single bq2502 provides SRAMs drawing 2µA total data-retention current with more than 10 years of nonvolatility.

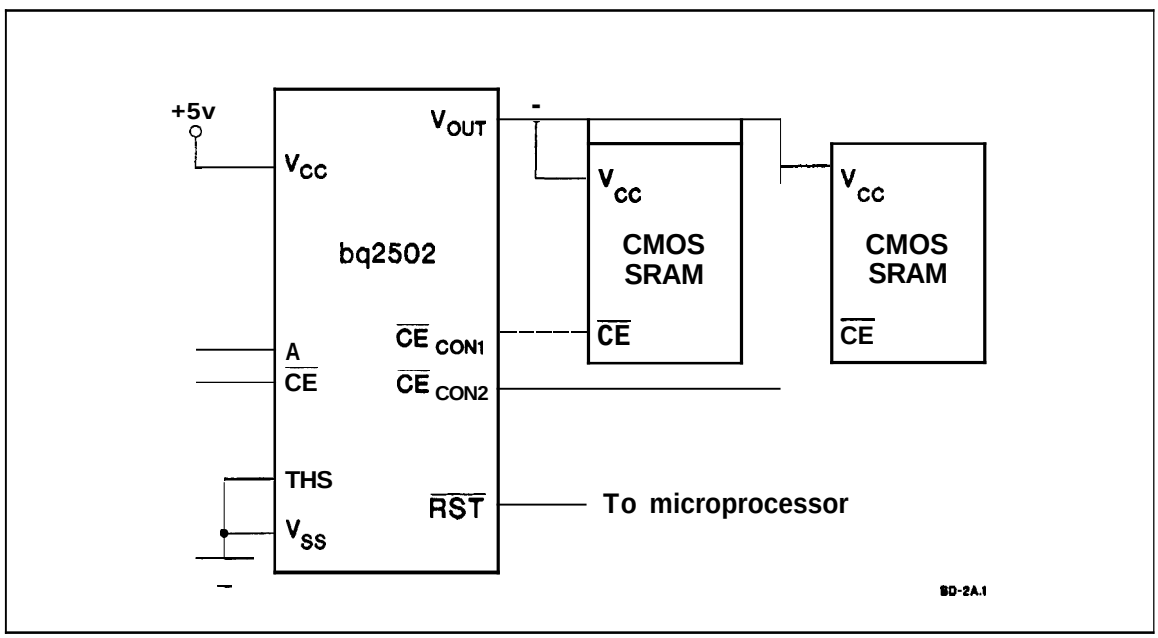


Figure 1. Hardware Hookup (5% Supply Operation)

As shipped from Benchmarq, the internal lithium—cell is electrically isolated from V_{OUT}, $\overline{CE}_{CON1}$, and $\overline{CE}_{CON2}$. Self-discharge in this condition is lees than .5% per year at 20°C.

Note: Following the first application of V_{CC}, this isolation is broken, and the backup cell provides power to V_{OUT}, $\overline{CE}_{CON1}$, and $\overline{CE}_{CON2}$ for the external SRAM.

Caution:

Take care to avoid inadvertent discharge through V_{OUT}, $\overline{CE}_{CON1}$, and $\overline{CE}_{CON2}$ after battery isolation has been broken.

This isolation can be reestablished by applying a valid isolation signal to the bq2502. This signal requires $\overline{CE}$ low as Vcc crosses both V_{PFD} and V_{SO} during a power-down. Between these two points in time, $\overline{CE}$ must be brought to (0.48 to 0.52) • Vcc and held for at least 700ns. The isolation signal is invalid if $\overline{CE}$ exceeds $0.54 \cdot V_{CC}$ at any point between Vcc crossing V_{PFD} and V_{SO}. See Figure 2.

The battery is connected to V_{OUT} immediately on subsequent application and removal of Vcc.

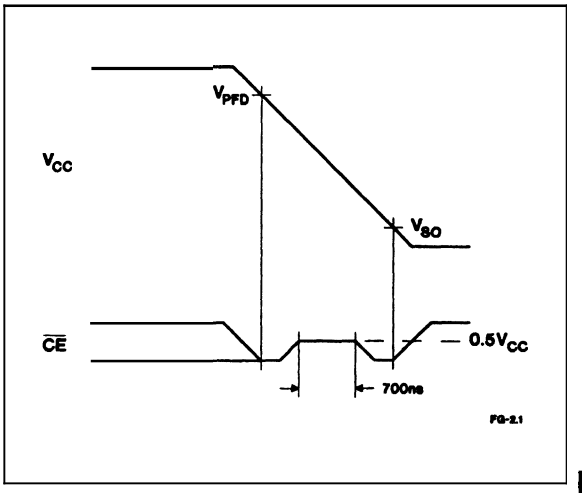


Figure 2. Battery Isolation Signal

4

Truth Table

Input		Output	
$\overline{CE}$	A	$\overline{CE}_{CON1}$	$\overline{CE}_{CON2}$
H	X	H	H
L	L	L	H
L	H	H	L

Absolute Maximum Ratings

Symbol	Parameter	Valve	Unit	Conditions
V_{CC}	DC voltage applied on Vcc relative to Vss	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding Vcc relative to Vss	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to 70	°C	
T_{STG}	Storage temperature	-40 to 70	°C	
T_{BIAS}	Temperature under bias	-10 to 70	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds
I_{OUT}	V_{OUT} current	200	mA	

Note: Permanent device damage may occur if **Absolute Maximum Ratings are** exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. **Exposure** to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbd	Parameter	Minimum	Typical	Maximum	Unit	Notes
Vcc	Supply voltage	4.75	5.0	5.5	V	THS = Vss
		4.50	5.0	5.5	V	THS = V_{OUT}
Vss	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3		0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	
THS	Threshold select	-0.3	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BAT}.

DC Electrical Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbd	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
C	Battery capacity		130		mAhr	Refer to graphs in Typical Battery Characteristics section.
I_{LI}	Input leakage current			± 1	µA	V_{IN} = V_{SS} to V_{CC}
V_{OH}	Output high voltage	2.4			V	I_{OH} = -2.0 mA
V_{OHB}	V_{OH}, backup supply	V_{BAT} - 0.3			V	V_{BAT} > V_{CC}, I_{OH} = -10µA
V_{OL}	Output low voltage			0.4	V	I_{OL} = 4.0 mA
V_{BAT}	Internal battery voltage		2.9		V	Refer to graphs in Typical Battery Characteristics section.
I_{CC}	Operating supply current		3	6	mA	No load on V_{OUT}, $\overline{CE}_{CON1}$, $\overline{CE}_{CON2}$, and $\overline{RST}$.
V_{PFD}	Power-fail detect voltage	4.55	4.62	4.75	V	THS = V_{SS}
		4.30	4.37	4.50	V	THS = V_{OUT}
V_{SO}	Supply switch-over voltage		2.9		V	
I_{CCDR}	Data-retention mode current from internal battery			100	nA	No load on V_{OUT}, $\overline{CE}_{CON1}$, $\overline{CE}_{CON2}$, and $\overline{RST}$.
V_{OUT1}	Vour voltage	vcc - 0.2			V	V_{CC} > V_{BAT}, I_{OUT} = 100mA
		Vcc - 0.3			V	V_{CC} > V_{BAT}, I_{OUT} = 160mA
V_{OUT2}	V_{OUT} voltage from internal battery	V_{BAT} - 0.2			V	V_{CC} < V_{BAT}, I_{OUT} = 100µA, from internal battery
I_{OUT1}	V_{OUT} current			160	mA	V_{OUT} ≥ V_{CC} - 0.3V

Note: Typical values indicate operation at T_A = 25°C, Vcc = 5V or V_{BAT}.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
C_{IN}	Input capacitance			8	pF	Input voltage = 0V
C_{OUT}	Output capacitance			10	pF	Output voltage = 0V

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0 V to 3.0 V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figure 3

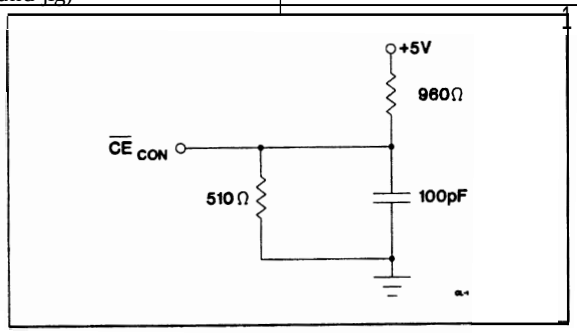


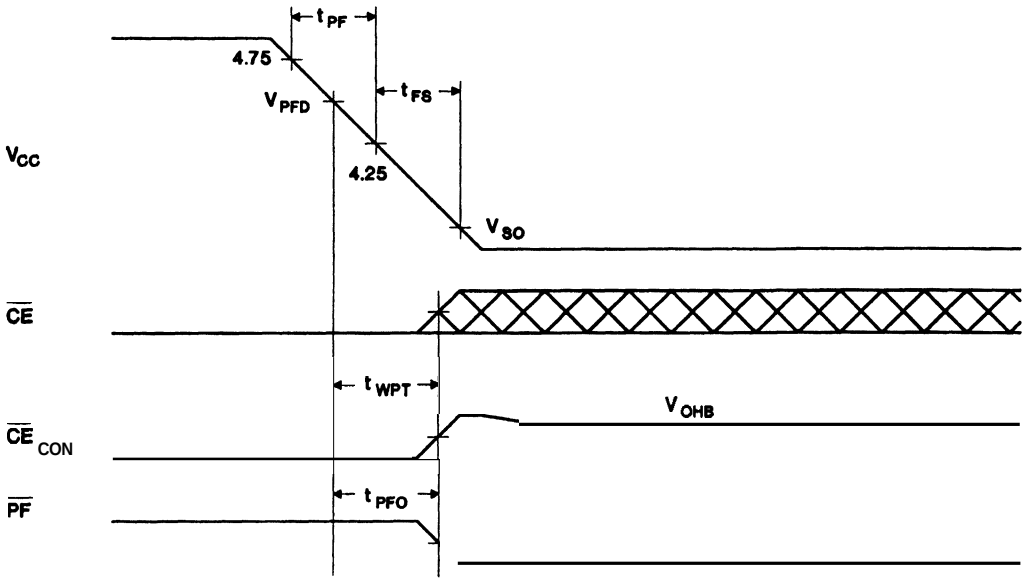
Figure 3. Output Load

Power-Fail Control (T_A = 0 to 70°C)

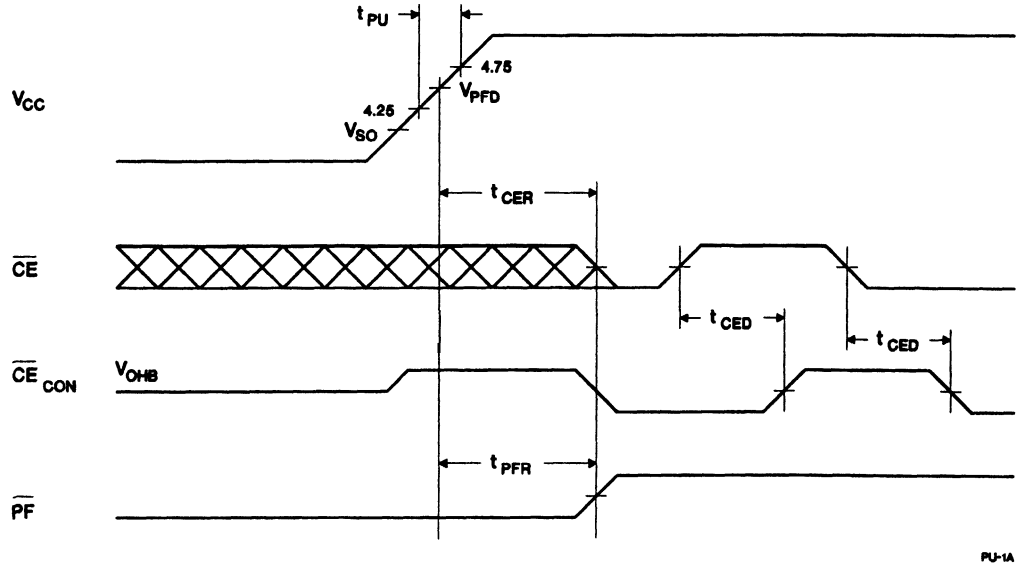
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{PF}	V_{CC} slew 4.75 to 4.25 V	300	-	-	µs	
t_{FS}	V_{CC} slew 4.25 V to V_{SO}	10	-	-	µs	
t_{PU}	V_{CC} slew 4.25 to 4.75 V	0		-	µs	
t_{CED}	Chip-enable propagation delay		7	10	ns	
t_{CER}	Chip-enable recovery time	t_{RR}	-	t_{RR}	ms	Time during which SRAM is write-protected after V_{CC} passes V_{PFD} on power-up
t_{RR}	V_{PFD} to $\overline{RST}$ inactive	40	80	120	ms	Time, after V_{CC} becomes valid, before $\overline{RST}$ is cleared
t_{AS}	Input A set up to $\overline{CE}$	0		-	ns	
t_{WPT}	Write-protect time	t_R	-	t_R	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected
t_R	V_{PFD} to $\overline{RST}$ active	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before $\overline{RST}$ is active

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.

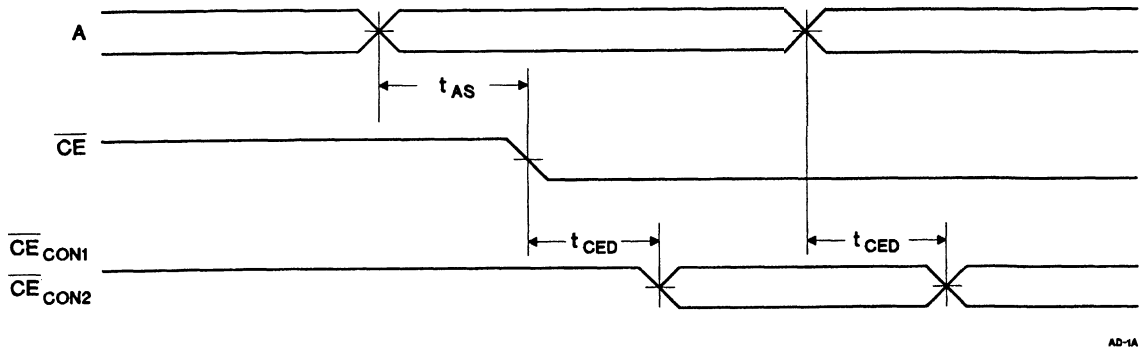
Power-Down Timing



Power-Up Timing

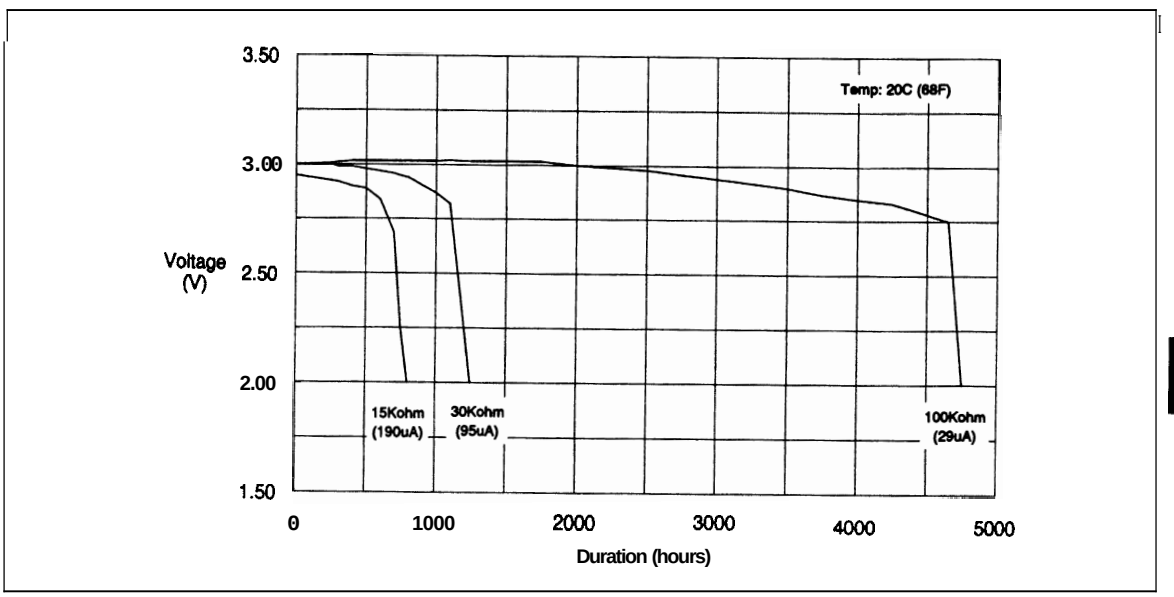


Address-Decode Timing

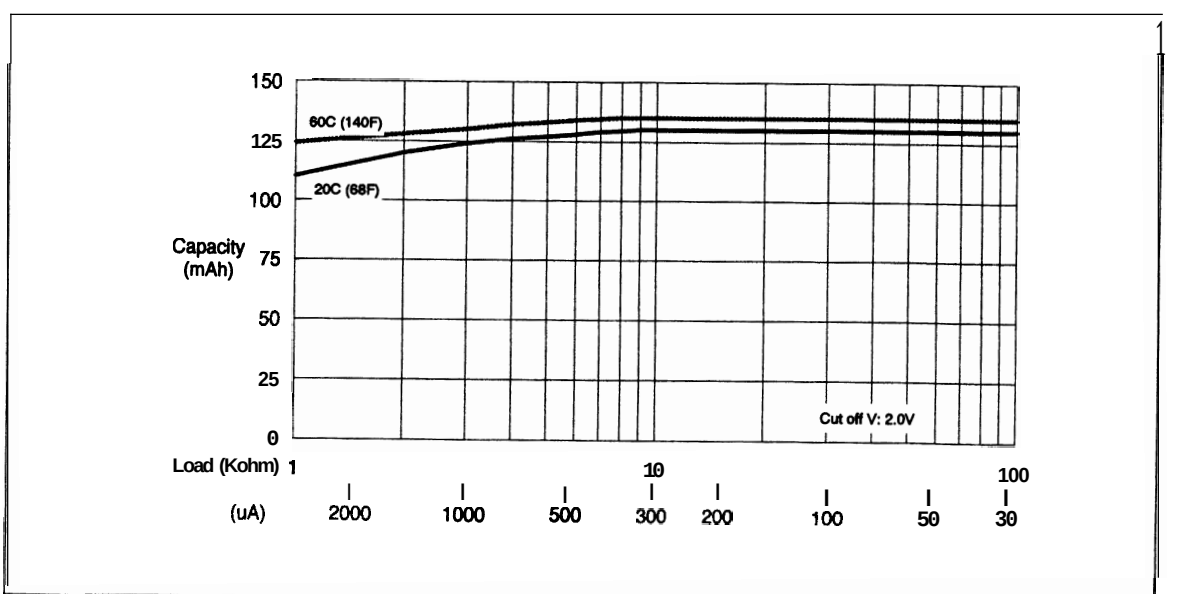


Typical Battery Characteristics (source = Panasonic)

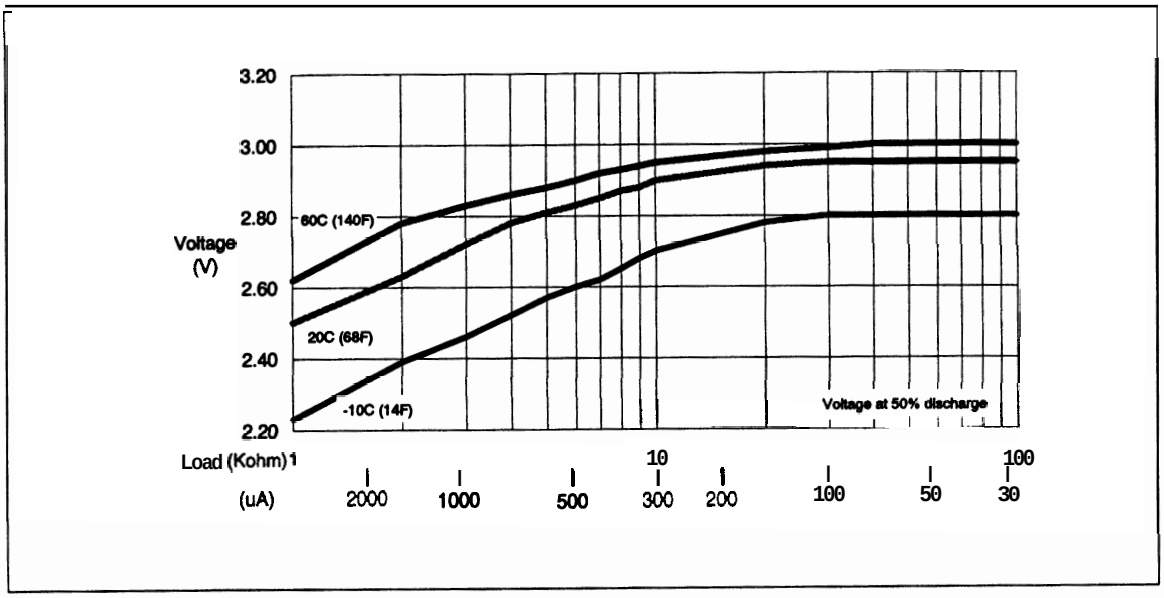
CR1632 Load Characteristics



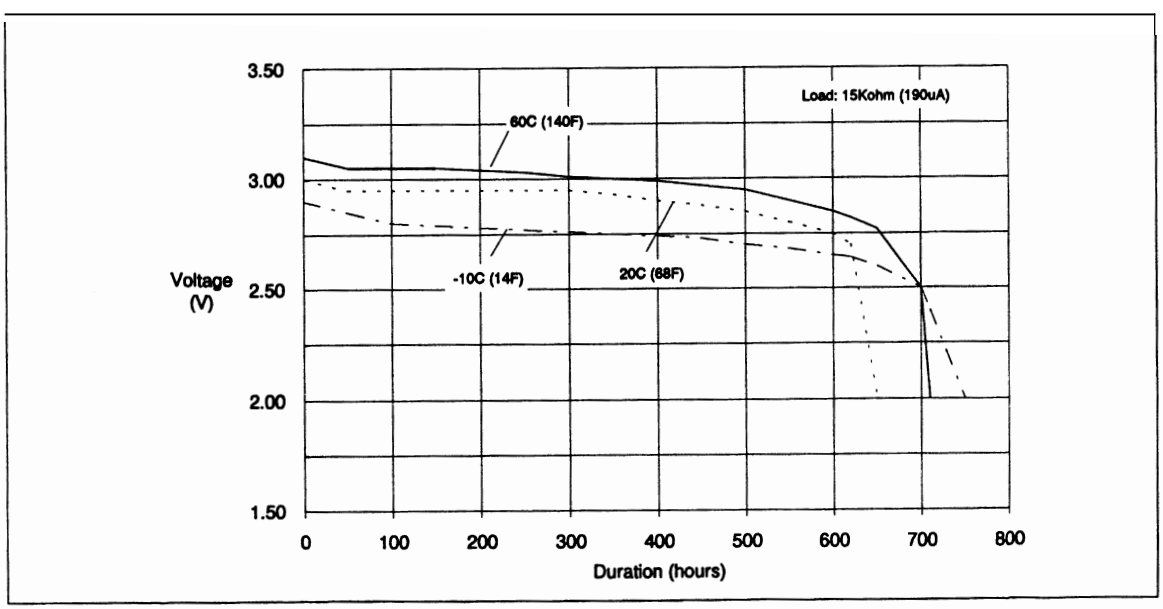
CR1632 Capacity vs. Load Resistance



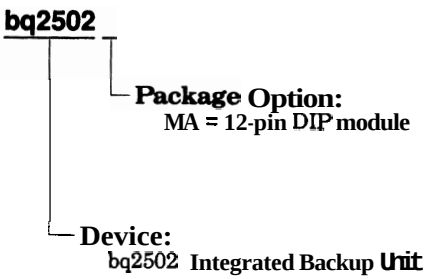
CR1632 Operating Voltage vs. Load Resistance



CR1632 Temperature Characteristics



Ordering Information



Notes

bq3285

Real-Time Clock (RTC)

Features

- Direct clock/calendar replacement for IBM® AT-compatiblecomputers and other applications
- Functionally compatible with the DS1285
  - Closely matches MC146818A pin configuration
- 114 bytes of general nonvolatile storage
- 160 ns cycle time allows fast bus operation

  Selectable Intel or Motorola bus timing
- Less than 0.5 µA load under battery operation
- 14 bytes for clock/calendar and control
- BCD or binary format for clock and calendar data

  Calendar in day of the week, day of the month, months, and years, with automatic leap-year adjustment
- Time of day in seconds, minutes, and hours
  - 12- or 24-hour Optional daylight saving adjuetment
- Programmable square wave output
- Three individually maskable interrupt event
  - Periodic rates from 122 µs to 500 ms
  - Time-of-day alarm once per second to once per day
  - End-of-clock update cycle
- 24-pin plastic DIP or SOIC and 28-pin PLCC

General Description

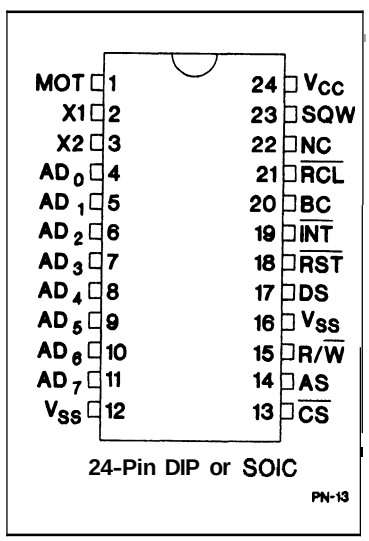
The CMOS bq3285 is a low-power microprocessor peripheral providing a timesf-day clock and 100-year calendar with alarm features and battery operation. Other features include three maskable interrupt sources, square wave output, and 114 bytes of general nonvolatile storage.

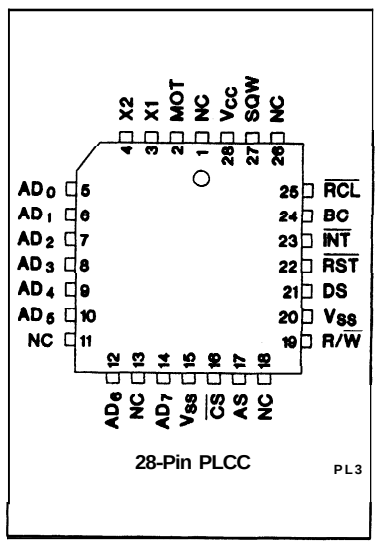
The bq3285 write-protects the clock, calendar, and storage registers during power failure. A backup battery then maintains data and operates the clock and calendar.

The bq3285 is a fully compatible real-time clock for IBM AT compatible computers and other applications. The only external components are a 32.768kHz crystal and a backup battery.

5

Pin Connections

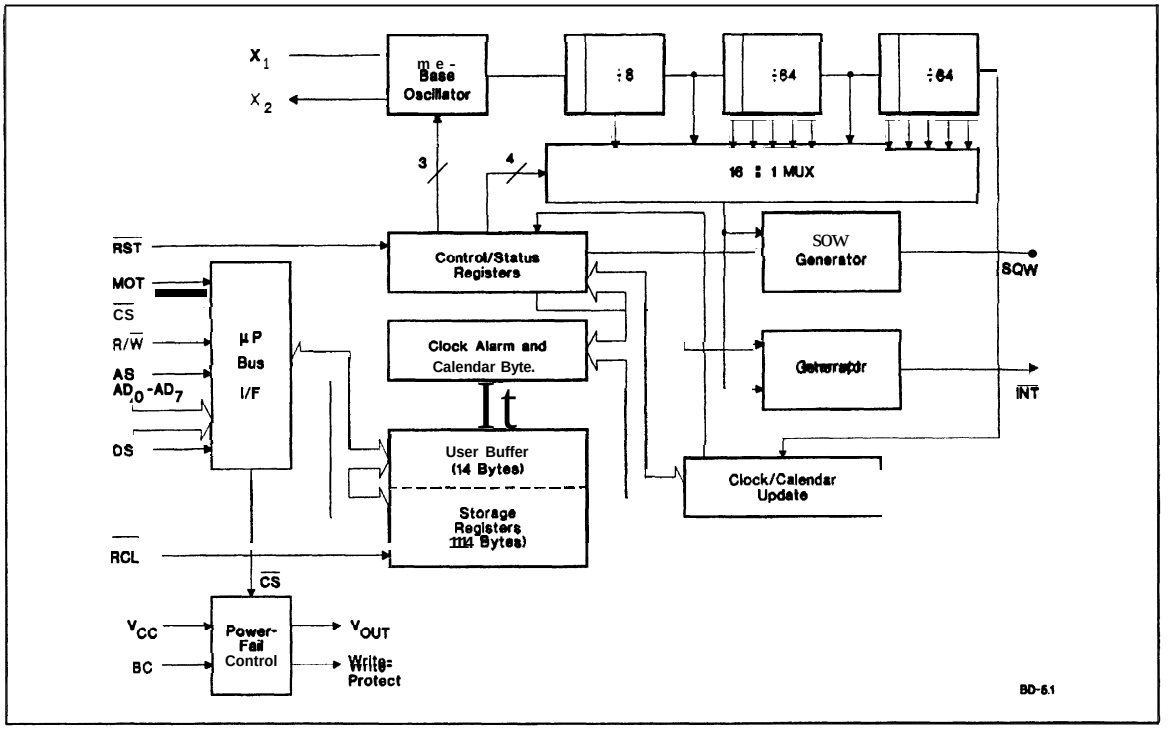




Pin Names

AD0-AD7	Multiplexed address/data input/output
MOT	Bus type select input
$\overline{CS}$	Chip select input
AS	Address strobe input
DS	Data strobe input
R/$\overline{W}$	Read/write input
$\overline{INT}$	Interrupt request output
$\overline{RST}$	Reset input
SQW	Square wave output
$\overline{RCL}$	RAM clear input
BC	3V backup cell input
X1, X2	Crystal inputs
NC	No connect
VCC	+5V supply
VSS	Ground

Block Diagram



Pin Descriptions

MOT **Bus** type select input

MOT selects bus timing for either Motorola or Intel architecture. **This** pin should be tied to Vcc for Motorola timing or to Vss for Intel timing (see Table 1). **The** setting should not be changed during system operation. MOT **is** internally pulled low by a 30KR resistor.

Table 1. Bus Setup

Bus Type	MOT Level	DS Equivalent	R/$\overline{W}$ Equivalent	AS Equivalent
Motorola	Vcc	DS, E, or Φ2	R/$\overline{W}$	AS
Intel	Vss	$\overline{RD}$, $\overline{MEMR}$, or $\overline{I/OR}$	$\overline{WR}$, $\overline{MEMW}$, or $\overline{I/OW}$	ALE

AD_0–AD_7 Multiplexed **address/data input/output**

The bq3285 bus cycle consists of two phases: the address phase and the data-transfer phase. The address phase precedes the data-transfer phase. During the address phase, an address placed on AD_0–AD_7 is latched **into** the bq3285 on the falling edge of the AS signal. During the data-transfer phase of the bus cycle, the **AD_0–AD_7** pins serve *as* a bidirectional data bus.

AS Address strobe input

AS serves **to** demultiplex the **address/data** bus. The falling edge of AS latches the address on AD_0–AD_7. This **demultiplexing** process **is** independent of the $\overline{CS}$ signal. For **DIP,** SOIC, and PLCC packages with MOT = Vcc, the **AS input is provided** a **signal similar** to ALE in an **Intel-based** system.–

DS — Data strobe input

When MOT = V_{CC}, DS controls data transfer during a bq3285 bus cycle. During a read cycle, the bq3285 drives the bus after the rising edge on DS. During a write cycle, the falling edge on DS is used to latch write data into the chip.

When MOT = V_{SS}, the DS input is provided a signal similar to $\overline{RD}$, $\overline{MEMR}$, or $\overline{I/OR}$ in an Intel-based system. The falling edge on DS is used to enable the outputs during a read cycle.

R/$\overline{W}$ — Read/write input

When MOT = V_{CC}, the level on R/$\overline{W}$ identifies the direction of data transfer. A high level on R/$\overline{W}$ indicates a read bus cycle, whereas a low on this pin indicates a write bus cycle.

When MOT = V_{SS}, R/$\overline{W}$ is provided a signal similar to $\overline{WR}$, $\overline{MEMW}$, or $\overline{I/OW}$ in an Intel-based system. The rising edge on R/$\overline{W}$ latches data into the bq3285.

$\overline{CS}$ — Chip select input

$\overline{CS}$ should be driven low and held stable during the data-transfer phase of a bus cycle accessing the bq3285.

$\overline{INT}$ — Interrupt request output

$\overline{INT}$ is an open-drain output. $\overline{INT}$ is asserted low when any event flag is set and the corresponding event enable bit is also set. $\overline{INT}$ becomes high-impedance whenever register C is read (see the Control/Status Registers section).

SQW — Square-wave output

SQW may output a programmable frequency square-wave signal during normal (V_{CC} valid) system operation. Any one of the 13 specific frequencies may be selected through register A. This pin is held low when the square-wave enable bit (SQWE) in register B is 0 (see the Control/Status Registers section).

$\overline{RCL}$ — RAM clear input

A low level on the $\overline{RCL}$ pin causes the contents of each of the 114 storage bytes to be set to FF(hex). The contents of the clock and control registers are unaffected. This pin should be used as a user-interface input (pushbutton to ground) and not connected to the output of any active component. $\overline{RCL}$ input is only recognized when held low for at least 125ms in the presence of V_{CC} when the oscillator is running. Using RAM clear does not affect the battery load. This pin is connected internally to a 30KΩ pull-up resistor.

BC — 3V backup cell input

BC should be connected to a 3V backup cell for RTC operation and storage register nonvolatility in the absence of power. When V_{CC} slews down past V_{BC} (3V typical), the integral control circuitry switches the power source to BC. When V_{CC} returns above V_{BC}, the power source is switched to V_{CC}.

Upon power-up, a voltage within the V_{BC} range must be present on the BC pin for the oscillator to start up.

$\overline{RST}$ — Reset input

The bq3285 is reset when $\overline{RST}$ is pulled low. When reset, $\overline{INT}$ becomes high-impedance, and the bq3285 is not accessible. Table 4 in the Control/Status Registers section lists the register bits that are cleared by a reset.

Reset may be disabled by connecting $\overline{RST}$ to V_{CC}. This allows the control bits to retain their states through power-down/power-up cycles.

X1, X2 — Crystal input

The X1, X2 inputs are provided for an external 32.768Khz quartz crystal, Daiwa DT-26 or equivalent, with 6pF load capacitance. A trimming capacitor may be necessary for extremely precise time-base generation.

In the absence of a crystal, an oscillated output of 32.768kHz can be fed into the X1 input.

Functional Description

Address Map

The bq3285 provides 14 bytes of clock and control/status registers and 114 bytes of general nonvolatile storage. Figure 1 illustrates the address map for the bq3285.

Update Period

The update period for the bq3285 is one second. The bq3285 updates the contents of the clock and calendar locations during the update cycle at the end of each update period (see Figure 2). The alarm flag bit may also be set during the update cycle.

The bq3285 copies the local register updates into the user buffer accessed by the host processor. When a 1 is written to the update transfer inhibit bit (UTI) in register B, the user copy of the clock and calendar bytes remains unchanged, while the local copy of the same bytes continua to be updated every second.

The update-in-progress bit (UIP) in register A is set t_{BUC} time before the beginning of an update cycle (see Figure 2). This bit is cleared and the update-complete flag (UF) is set at the end of the update cycle.

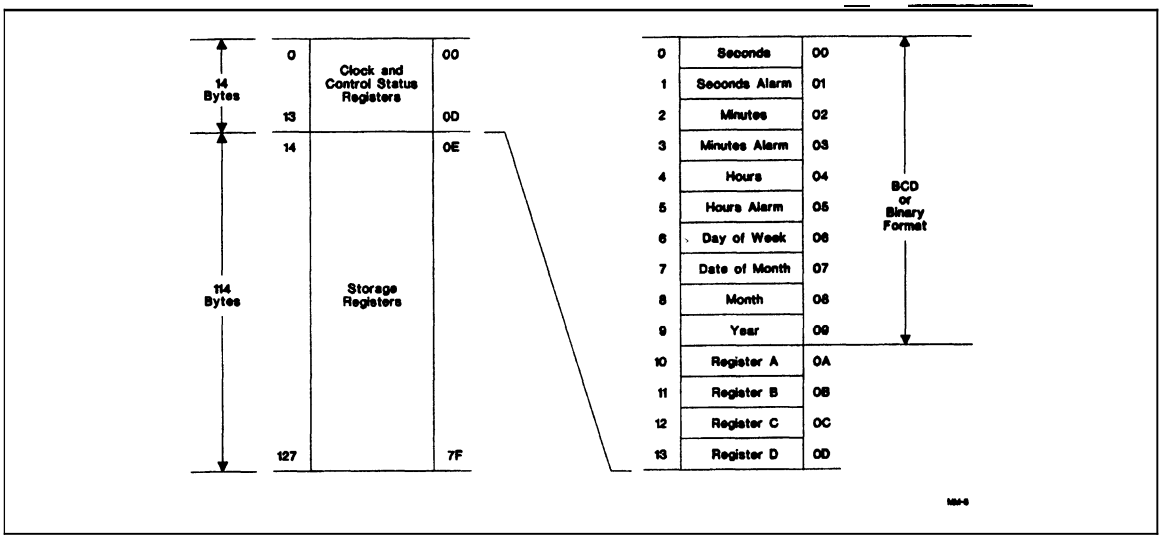


Figure 1. Address Map

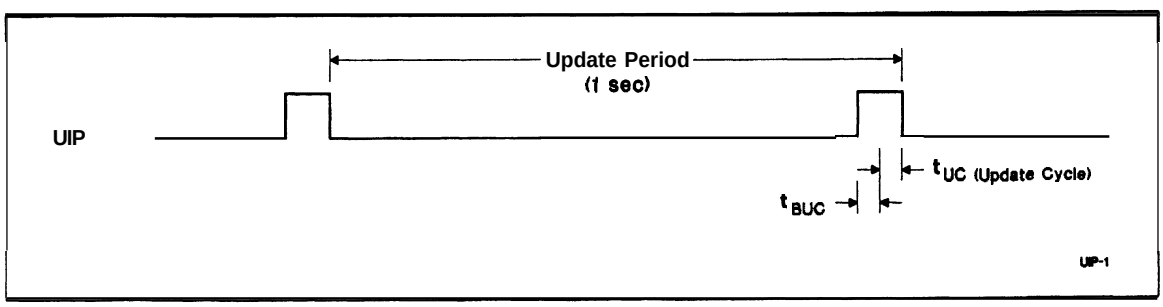


Figure 2. Update Period Timing and UIP

Programming the RTC

The time-of-day, alarm, and calendar bytes can be written in either the BCD or binary format (see Table 2).

These steps may be followed to program the time, alarm, and calendar:

1. Modify the contents of register B:
   a. Write a 1 to the UTI bit to prevent transfers between RTC bytes and user buffer.
   b. Write the appropriate value to the data format (DF) bit to select BCD or binary format for all time, alarm, and calendar bytes.
   c. Write the appropriate value to the hour format (HF) bit.
2. Write new values to all the time, alarm, and calendar locations.
3. Clear the UTI bit to allow update transfers.

On the next update cycle, the RTC updates all 10 bytes in the selected format.

Table 2. Time, Alarm, and Calendar Formats

Address	RTC Bytes	Range		
		Decimal	Binary	Binary-Coded Decimal
0	Seconds	0–59	00H–3BH	00H–59H
1	Seconds alarm	0-59	00H–3BH	00H–59H
2	Minutes	0 5 9	00H–3BH	00H–59H
3	Minutes alarm	0–59	00H–3BH	00H–59H
4	Hours, 12-hour format	1–12	01H–0CH AM; 81H–8CH PM	01H–12H AM; 81H–92H PM
	Hours, 24-hour format	0–23	00H–17H	00H–23H
5	Hours alarm, 12-hour format	1–12	01H–0CH AM; 81H–8CH PM	01H–12H AM; 81H–92H PM
	Hours alarm, 24-hour format	0–23	00H–17H	00H–23H
6	Day of week (1=Sunday)	1–7	01H–07H	01H–07H
7	Day of month	1–31	01H–1FH	01H–31H
8	Month	1–12	01H–0CH	01H–12H
9	Year	0-99	00H–63H	00H–99H

Square-Wave Output

The bq3285 divides the 32.768kHz oscillator frequency to produce the 1Hz update frequency for the clock and calendar. Thirteen taps from the frequency divider are fed to a 16:1 multiplexer circuit. The output of this mux is fed to the SQW output and periodic interrupt generation circuitry. The four least-significant bits of register A, RS0–RS3, select among the 13 taps (see Table 3). The square-wave output is enabled by writing a 1 to the square-wave enable bit (SQWE) in register B.

Interrupts

The bq3285 allows three individually selected interrupt events to generate an interrupt request. These three interrupt events are:

- The periodic interrupt, programmable to occur once every 122µs to 500ms
- The alarm interrupt, programmable to occur once per second to once per day
- The update-ended interrupt, which occurs at the end of each update cycle

Each of the three interrupt events is enabled by an individual interrupt-enable bit in register B. When an event occurs, its event flag bit in register C is set. If the corresponding event enable bit is also set, then an interrupt request is generated. The interrupt request flag bit (INTF) of register C is set with every interrupt request. Reading register C clears all flag bits, including INTF, and makes $\overline{INT}$ high-impedance.

Two methods can be used to process bq3285 interrupt events:

- Enable interrupt events and use the interrupt request output to invoke an interrupt service routine.
- Do not enable the interrupts and use a polling routine to periodically check the status of the flag bits.

The individual interrupt sources are described in detail in the following sections.

Table 3. Square-Wave Frequency/Periodic Interrupt Rate

Register A Bits				Square Wave		Periodic Interrupt	
RS3	RS2	RS1	RSO	Frequency	Units	Period	Units
0	0	0	0	None		None	
0	0	0	1	256	Hz	3.90625	ms
0	0	1	0	128	Hz	7.8125	ms
0	0	1	1	8.192	kHz	122.070	µs
0	1	0	0	4.096	kHz	244.141	µs
0	1	0	1	2.048	kHz	488.281	µs
0	1	1	0	1.024	kHz	976.5625	µs
0	1	1	1	512	Hz	1.953125	ms
1	0	0	0	256	Hz	3.90625	ms
1	0	0	1	128	Hz	7.8125	ms
1	0	1	0	64	Hz	15.625	ms
1	0	1	1	32	Hz	31.25	ms
1	1	0	0	16	Hz	62.5	ms
1	1	0	1	8	Hz	125	ms
1	1	1	0	4	Hz	250	ms
1	1	1	1	2	Hz	500	ms

Periodic Interrupt

The mux output used to drive the **SQW** output also drives the interrupt-generation circuitry. If the periodic interrupt event is enabled by writing a 1 to the periodic interrupt enable bit (PIE) in register C, an interrupt request is generated once every 122µs to 500ms. The period between interrupts is selected by the same bits in register A that select the square wave frequency (see Table 3).

Alarm Interrupt

During each update cycle, the RTC compares the hours, minutes, and seconds bytes with the three corresponding alarm bytes. If a match of all bytes is found, the alarm interrupt event flag bit, AF in register C, is set to 1. If the alarm event is enabled, an interrupt request is generated.

An alarm byte may be removed from the comparison by setting it to a 'don't care' state. An alarm byte is set to a 'don't care" state by writing a 1 to each of its two most-significant bits. A 'don't care' state may be used to select the frequency of alarm interrupt events as follows:

- If none of the three alarm bytes is 'don't care," the frequency is once per day, when hours, minutes, and seconds match.
- If only the hour alarm byte is 'don't care,' the frequency is once per hour, when minutes and seconds match.
- If only the hour and minute alarm bytes are 'don't care,' the frequency is once per minute, when seconds match.
- If the hour, minute, and second alarm bytes are 'don't care,' the frequency is once per second.

Update Cycle Interrupt

The update cycle ended flag bit (UF) in register C is set to a 1 at the end of an update cycle. If the update interrupt enable bit (UIE) of register B is 1, and the update transfer inhiiit bit (UTI) in register B is 0, then an interrupt request is generated at the end of each update cycle.

Accessing RTC bytes

Time and calendar bytes read during an update cycle may be in error. Three methods to access the time and calendar bytes without ambiguity are:

- Enable the update interrupt event to generate interrupt requests at the end of the update cycle. The interrupt handler has a maximum of 999ms to access the clock bytes before the next update cycle begins (see Figure 3).
- Poll the update-in-progrew bit (UIP) in register A. If UIP = 0, the polling routine has a minimum of t_{BUC} time to access the clock bytes (see Figure 3).
- Use the periodic interrupt went to generate interrupt requests every t_{PI} time, such that UIP = 1 always occurs between the periodic interrupts. The interrupt handler has a minimum of $t_{PI}/2 + t_{BUC}$ time to access the clock bytes (see Figure 3).

Oscillator Control

When power is first applied to the bq3285 and V_{CC} is above V_{PFD}, the internal oscillator and frequency divider are turned on by writing a 010 pattern to bits 4 through 6 of register A. A pattern of 11X turns the oscillator on, but keep the frequency divider disabled. Any other pattern to these bits keeps the oscillator off.

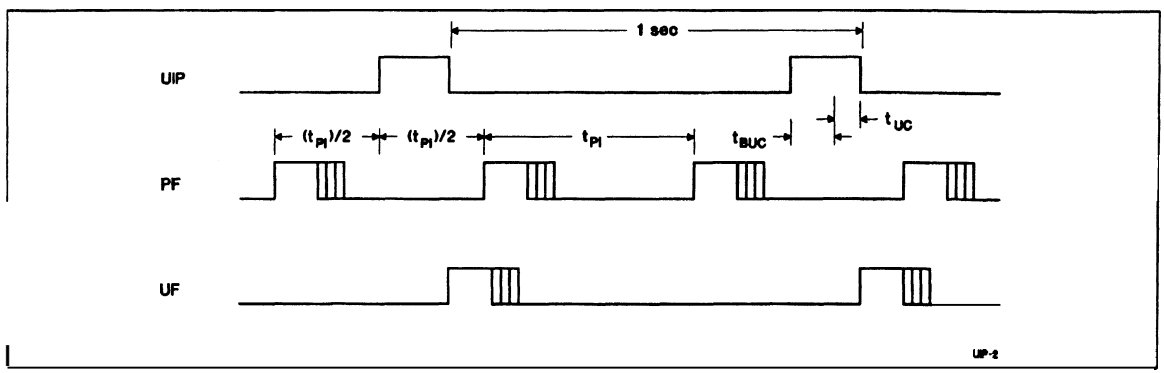


Figure 3. Update-Ended/Periodic Interrupt Relationship

Power-Down/Power-Up Cycle

The bq3285 continuously monitors V_{CC} for out-of-tolerance. During a power failure, when V_{CC} falls below V_{PFD} (4.17V typical), the bq3285 write-protects the clock and storage registers. When V_{CC} is below V_{BC} (3V typical), the power source is switched to BC. RTC operation and storage data are sustained by a valid backup energy source. When V_{CC} is above V_{BC}, the power source is Vcc. Write-protection continues for t_{CSR} time after V_{CC} rises above V_{PFD}.

Control/Status Registers

The four control/status registers of the bq3285 are accessible regardless of the status of the update cycle (see Table 4).

Register A

Register A Bits							
7	6	5	4	3	2	1	0
UIP	OS2	OS1	OS0	RS3	RS2	RS1	RS0

Register A programs:

- The frequency of the square-wave and the periodic event rate.
- Oscillator operation.

Register A provides:

- Status of the update cycle.

RS0–RS3 - Frequency Select

7	6	5	4	3	2	1	0
			-	RS3	RS2	RS1	RS0

These bits select one of the 13 frequencies for the SQW output and the periodic interrupt rate, as shown in Table 3.

OS0–OS2 - Oscillator Control

7	6	5	4	3	2	1	0
-	OS2	OS1	OS0	-	-	-	-

These three bits control the state of the oscillator and divider stages. A pattern of 010 enables RTC operation by turning on the oscillator and enabling the frequency divider. A pattern of 11X turns the oscillator on, but keeps the frequency divider disabled. When 010 is written, the RTC begins its first update after 500ms.

UIP - Update Cycle Status

7	6	5	4	3	2	1	0
UIP	-	-	-	-	-	-	-

This read-only bit is set prior to the update cycle. When UIP equals 1, an RTC update cycle may be in progress. UIP is cleared at the end of each update cycle. This bit is also cleared when the update transfer inhibit (UTI) bit in register B is 1.

Table 4. Control/Status Registers

Reg.	Loc. (Hex)	Read	Write	Bit Name and State on Reset															
				7 (MSB)		6		5		4		3		2		1		0 (LSB)	
A	0A	Yes	Yes[1]	UIP	na	0S2	na	OS1	na	OSO	na	RS3	na	RS2	na	RS1	na	RS0	na
B	CB	Yes	Yes	UTI	na	PIE	0	AIE	0	UIE	0	SQWE	0	DF	na	HF	na	DSE	na
C	0C	Yes	No	INTF	0	PF	0	AF	0	UF	0	-	0	-	0	-	0	-	0
D	0D	Yes	No	VRT	na	-	0	-	0	-	0	-	0	-	0	-	0	-	0

Notes: 1. Except bit 7.
2. na = not affected

Register B

Register B Bits							
7	6	5	4	3	2	1	0
UTI	PIE	AIE	UIE	SQWE	DF	HF	DSE

Register B enables:

- Update cycle transfer operation
- Square-waveoutput
- Interrupt events
- Daylight saving adjustment

Register B selects:

- Clock and calendar data formats

All bits of register B are read/write.

DSE - Daylight Saving Enable

7	6	5	4	3	2	1	0
				-		-	DSE

This bit enables daylight-saving time adjustments when written to 1:

- On the last Sunday in October, the first time the bq3285 increments past 1:59:59 AM, the time falls back to 1:00:00 AM.
- On the first Sunday in April, the time springs forward from 2:00:00 AM to 3:00:00 AM.

HF - Hour Format

7	6	5	4	3	2	1	0
-	-	-	-	-	-	HF	-

This bit selects the time-of-day and alarm hour format:

1 = 24-hour format

0 = 12-hour format

DF - Data Format

7	6	5	4	3	2	1	0
-	-	-	-	-	DF	-	-

This bit selects the numeric format in which the time, alarm, and calendar bytes are represented:

1 = Binary

0 = BCD

SQWE - Square-Wave Enable

7	6	5	4	3	2	1	0
-	-	-	-	SQWE	-	-	-

This bit enablea the square-wave output:

1 = Enabled

0 = Disabled and held low

UIE - Update Cycle Interrupt Enable

7	6	5	4	3	2	1	0
-	-	-	UIE	-	-	-	-

This bit enables an interrupt request due to an update ended interrupt event:

1 = Enabled

0 = Disabled

The UIE bit is automatically cleared when the UTI bit equals 1.

AIE - Alarm Interrupt Enable

7	6	5	4	3	2	1	0
-	-	AIE	-	-	-	-	-

This bit enables an interrupt request due to an alarm interrupt event:

1 = Enabled

0 = Disabled

PIE - Periodic Interrupt Enable

7	6	5	4	3	2	1	0
-	PIE	-	-	-	-	-	-

This bit enables an interrupt request due to a periodic interrupt event:

1 = Enabled

0 = Disabled

UTI - Update Transfer Inhibit

7	6	5	4	3	2	1	0
UTI	-	-	-	-	-	-	-

This bit inhibits the transfer of RTC bytes to the user buffer:

1 = Inhibits transfer and clears UIE

0 = Allows transfer

Register C

Reaister C Bits							
7	6	5	4	3	2	1	0
INTF	PF	AF	UF	0	0	0	0

Register C is the read-only event status register.

Bits 0–3 - Unused Bits

7	6	5	4	3	2	1	0
-	-	-	-	0	0	0	0

These bits are always set to 0.

UF - Update Event Flag

7	6	5	4	3	2	1	0
-	-	-	UF	-	-	-	-

This bit is set to a 1 at the end of the update cycle. Reading register C clears this bit.

AF - Alarm Event Flag

7	6	5	4	3	2	1	0
	-	AF	-	-	-		

This bit is set to a 1 when an alarm event occurs. Reading register C clears this bit.

PF - Periodic Event Flag

7	6	5	4	3	2	1	0
-	PF	-	-	-	-	-	-

This bit is set to a 1 every t_{PI} time, where t_{PI} is the time period selected by the settings of RS0–RS3 in register A. Reading register C clears this bit.

INTF - Interrupt Request Flag

7	6	5	4	3	2	1	0
INTF	-	-	-	-	-	-	-

This flag is set to a 1 when any of the following is true:

AIE = 1 and AF = 1

PIE = 1 and PF = 1

UIE = 1 and UF = 1

Reading register C clears this bit.

Register D

Rwister D Bits							
7	6	5	4	3	2	1	0
VRT	0	0	0	0	0	0	0

Register D is the read-only data integrity status register.

Bits 0–6 - Unused Bits

7	6	5	4	3	2	1	0
-	0	0	0	0	0	0	0

These bits are always set to 0.

VRT - Valid RAM and Time

7	6	5	4	3	2	1	0
VRT	-	-	-	-	-	-	-

1 = Valid backup energy source

0 = Backup energy source is depleted

When the backup energy source is depleted (VRT = 0), data integrity of the RTC and storage registers is not guaranteed.

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Condition8
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
T_{STG}	Storage temperature	-55 to +125	°C	
T_{BIAS}	Temperature under bias	-40 to +85	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this table. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IL}	Input low voltage	-0.3		0.8	V
V_{IH}	Input high voltage	2.2		V_{CC} + 0.3	V
V_{BC}	Backup cell voltage	2.5		4.0	V

Note: Typical values indicate operation at T_A = 25°C.

5

DC Electrical Characteristics (TA = TOPR, VCC = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current			±1	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LD}	Output leakage current			±1	µA	AD_0–AD_7, $\overline{INT}$, and SQW in high impedance, V_{OUT} = vss to V_{CC}
V_{OH}	Output high voltage	2.4			V	I_{OH} = -2.0 mA
V_{OL}	Output low voltage			0.4	V	I_{OL} = 4.0 mA
I_{CC}	Operating supply current		7	15	mA	Min. cycle, duty = 100%, I_{OH} = 0mA, I_{OL} = 0mA
V_{SO}	Supply switch-over voltage		V_{BC}		V	
I_{CCB}	Battery operation current		0.3	0.5	µA	V_{BC} = 3V, T_A = 25°C
V_{PFD}	Power-fail-detect voltage	4.0	4.17	4.35	V	
I_{RCL}	Input current when $\overline{RCL}$ = Vss.			185	µA	Internal 30K pull-up
I_{MOTH}	Input current when MOT = Vcc			-185	µA	Internal 30K pull-down

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC} = 3V.

Crystal Specifications (DT-26 or Equivalent)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
f_O	Oscillation frequency		32.768		kHz
C_L	Load capacitance		6		pF
T_P	Temperature turnover point	20	25	30	°C
k	Parabolic curvature constant			-0.042	ppm/°C
Q	Quality factor	40,000	70,000		
R_1	Series resistance			45	KΩ
C_O	Shunt capacitance		1.1	1.8	pF
C_O/C_1	Capacitance ratio		430	600	
D_L	Drive level			1	µW
$\Delta f/f_O$	Aging (first year at 25°C)		1		ppm

Capacitance (T_A = 25°C, F = 1MHz, VCC = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance			7	pF	V_{OUT} = 0V
C_{IN}	Input capacitance			5	pF	V_{IN} = 0V

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

Parameter	*Ted* Conditions
Input pulse levels	0 to 3.0 V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 4 and 5

5

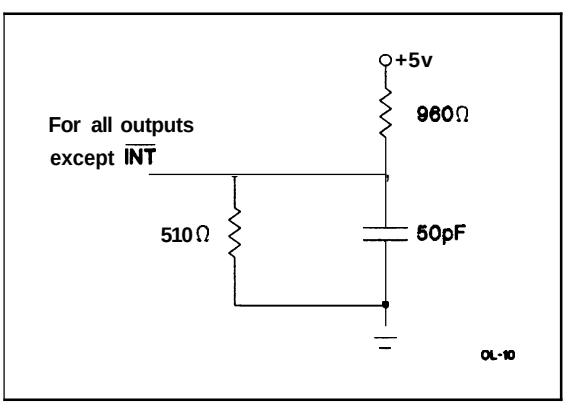


Figure 4. Output Load A

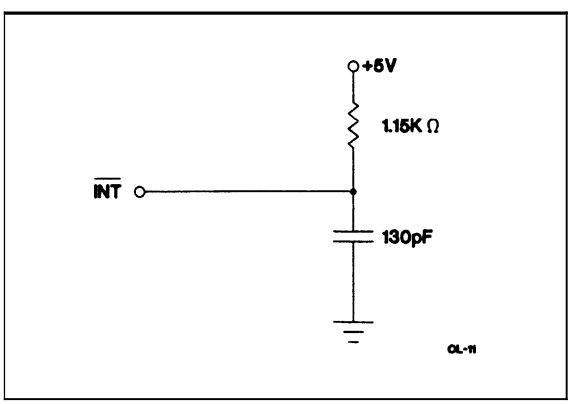
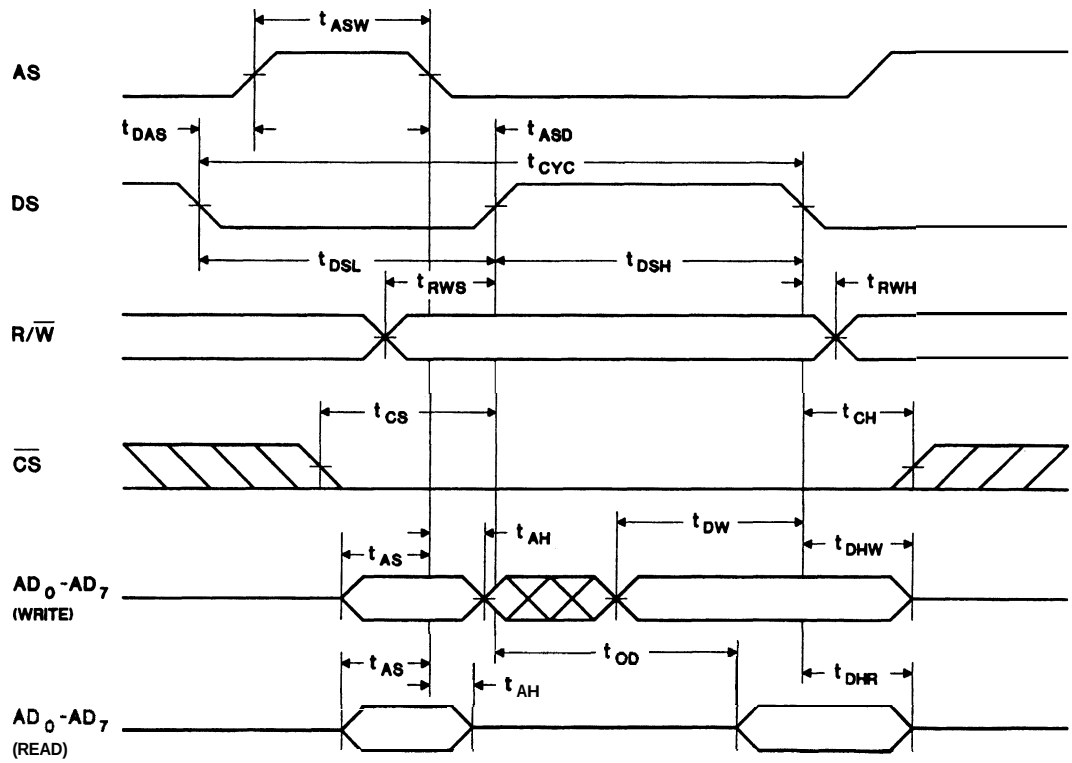


Figure 5. Output Load B

Read/Write Timing ($T_A = T_{OPR}$, $V_{CC} = 5V \pm 10\%$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYC}	Cycle time	160			ns	
t_{DSL}	DS low or $\overline{RD}/\overline{WR}$ high time	80			ns	
t_{DSH}	DS high or $\overline{RD}/\overline{WR}$ low time	55			ns	
t_{RWH}	R/$\overline{W}$ hold time	0			ns	
t_{RWS}	R/$\overline{W}$ setup time	10			ns	
t_{CS}	Chip select setup time	5			ns	
t_{CH}	Chip select hold time	0			ns	
t_{DHR}	Read data hold time	0		25	ns	
t_{DHW}	Write data hold time	0			ns	
t_{AS}	Address setup time	20			ns	
t_{AH}	Address hold time	5			ns	
t_{DAS}	Delay time, DS to AS rise	10			ns	
t_{ASW}	Pulse width, AS high	30			ns	
t_{ASD}	Delay time, AS to DS rise ($\overline{RD}/\overline{WR}$ fall)	35			ne	
t_{OD}	Output data delay time from DS rise ($\overline{RD}$ fall)			50	ns	
t_{DW}	Write data setup time	30			ns	
t_{BUC}	Delay time before update cycle		244		µs	
t_{PI}	Periodic interrupt time interval					See Table 3
t_{UC}	Time of update cycle		1		µs	

Motorola Bus Read/Write Timing



RC-4

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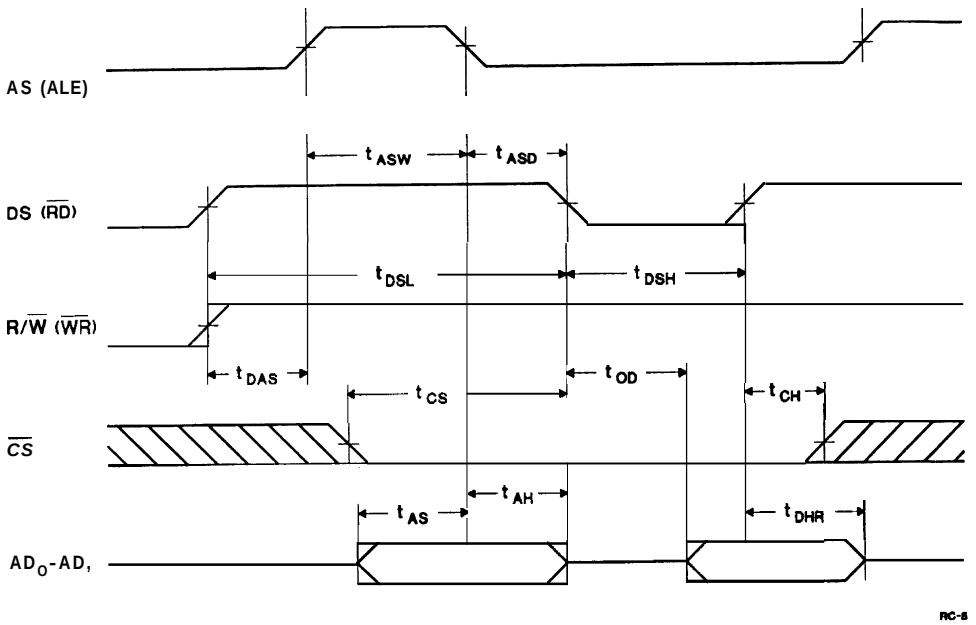
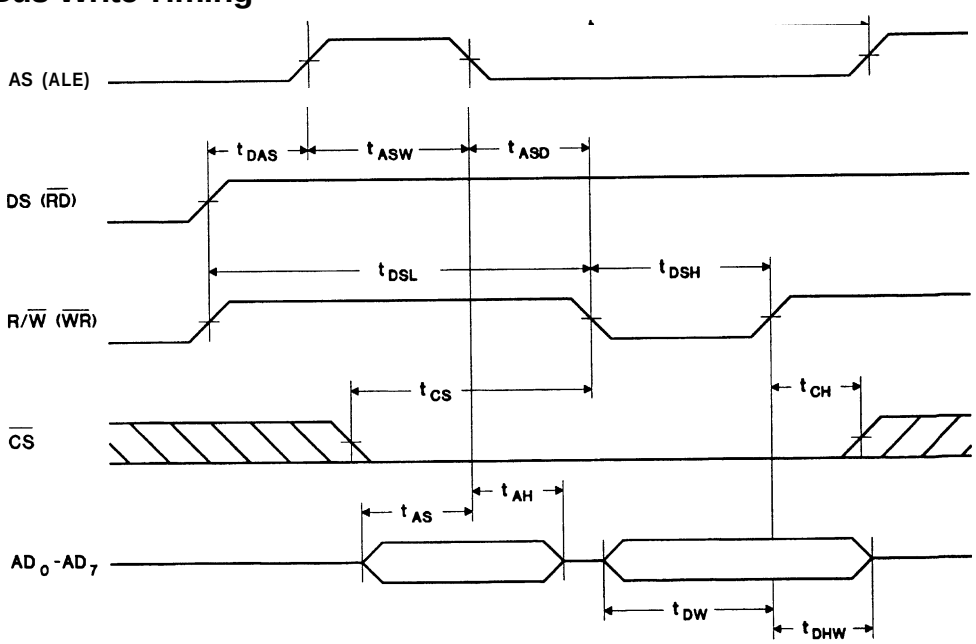
Intel Bus Read Timing



Intel Bus Write Timing

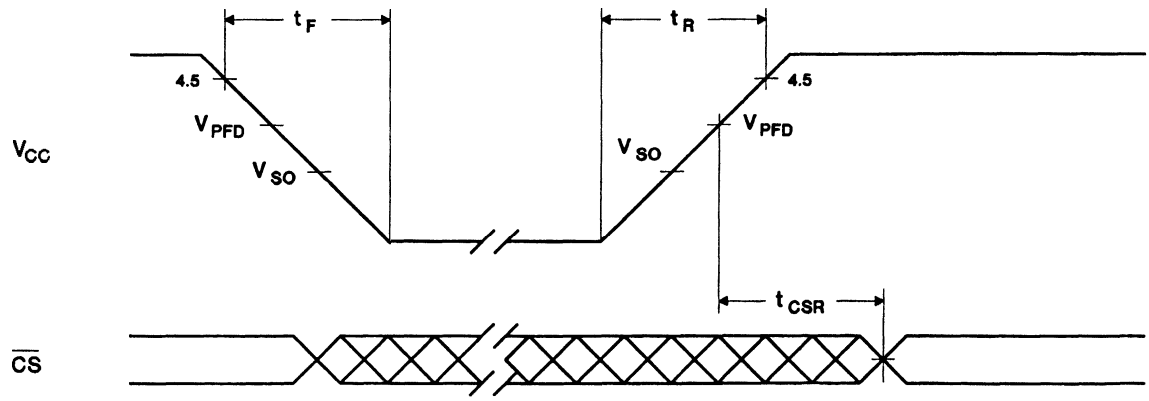


Power-Down/Power-Up Timing ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_F	V_{CC} slew from 4.5V to 0V	300			µs	
t_R	V_{CC} slew from 0V to 4.5V	100			µs	
t_{CSR}	$\overline{CS}$ at V_{IH} after power-up	20		200	ms	Internal write-protection period after V_{CC} passes V_{PFD} on power-up.

Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

Power-Down/Power-Up Timing

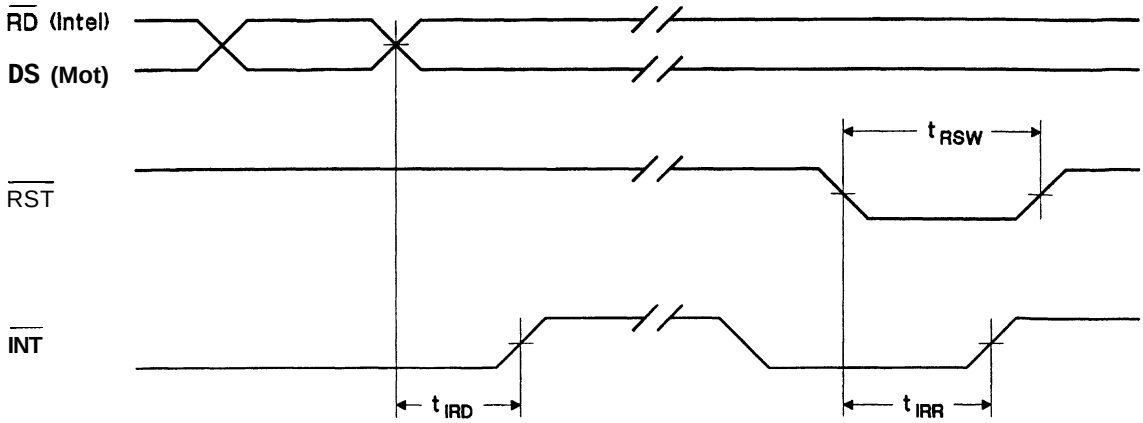


PD-4A

Interrupt Delay Timing ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
t_{RSW}	Reset pulse width	5	-	-	µs
t_{IRR}	$\overline{INT}$ release from $\overline{RST}$	-	-	2	µs
t_{IRD}	$\overline{INT}$ release from DS ($\overline{RD}$)			2	µs

Interrupt Delay Timing



INT-1

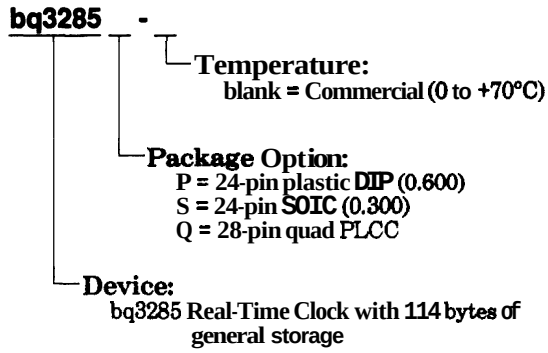
Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	2	Address strobe input	Clarification
1	11	Backup cell voltage V_{BC}	Was 2.0 min; is 2.6 min
1	12	Power-fail detect voltage V_{PFD}	Was 4.1 min, 4.26 max; is 4.0 min, 4.35 max
2	3, 12	Crystal type Daiwa DT-26 (not DT-26S)	Clarification
3	12	Changed value in first table	I_{RCL} max. was 275; is now 185
3	12	Changed value in first table	I_{MOTH} max. was -275; is now -185
3	12	Changed values for conditions of I_{RCL}, I_{MOTH}	Was 20K; is now 30K

Note: Change 1 = Nov. 1992 B changes from June 1991 A.
Change 2 = Nov. 1993 C changes from Nov. 1992 B.
Change 3 = Sept. 1996 D changes from Nov. 1993C.

5

Ordering Information



BENCHMARQ

bq3285E/L

Real-Time Clock (RTC)

Features

- Direct clock/calendar replacement for IBM® AT-compatible computers and other applications
- Functionally compatible with the DS1285
  - Closely matches MC146818A pin configuration
- 2.7–3.6V operation (bq3285L); 4.5–5.5V operation (bq3285E)
- ➤ 242 bytes of general nonvolatile storage
- 32.768KHz output for power management
- ➤ System wake-up capability—alarm interrupt output active in battery-backup mode
- Less than 0.5 µA load under battery operation
- ➤ Selectable Intel or Motorola bus timing
- ➤ 14 bytes for clock/calendar and control
- BCD or binary format for clock and calendar data
- Calendar in day of the week, day of the month, months, and years, with automatic leap-year adjustment
- ➤ Time of day in seconds, minutes, and hours
  - 12- or 24-hour format
  - Optional daylight saving adjustment
- ➤ Programmable square wave output
- Three individually maskable interrupt event flags:
  - Periodic rates from 122 µs to 500 ms
  - Time-of-day alarm once per second to once per day
  - End-of-clock update cycle
- 24-pin plastic DIP, SOIC, or SSOP and 28-pin PLCC

General Description

The CMOS bq3285E/L is a low-power microprocessor peripheral providing a time-of-day clock and 100-year calendar with alarm features and battery operation. The bq3285L supports 3V systems. Other bq3285E/L features include three maskable interrupt sources, square-wave output, and 242 bytes of general nonvolatile storage.

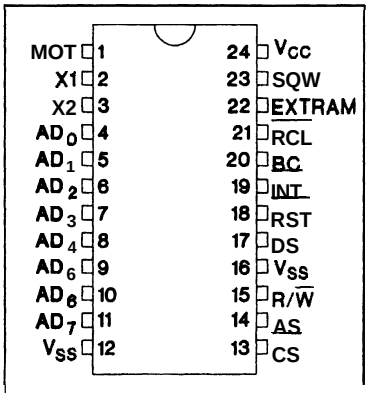
A 32.768KHz output is available for sustaining power-management activities. Wake-up capability is provided by an alarm interrupt, which is active in battery-backup mode.

The bq3285E/L write-protects the clock, calendar, and storage registers during power failure. A backup battery then maintains data and operates the clock and calendar.

The bq3285E/L is a fully compatible real-time clock for IBM AT-compatible computers and other applications. The only external components are a 32.768kHz crystal and a backup battery.

5

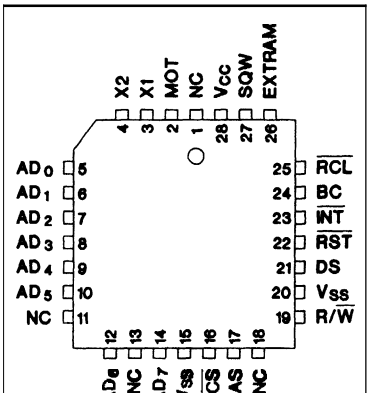
Pin Connections



24-Pin DIP or SOIC/SSOP

PN-41

Pin Names

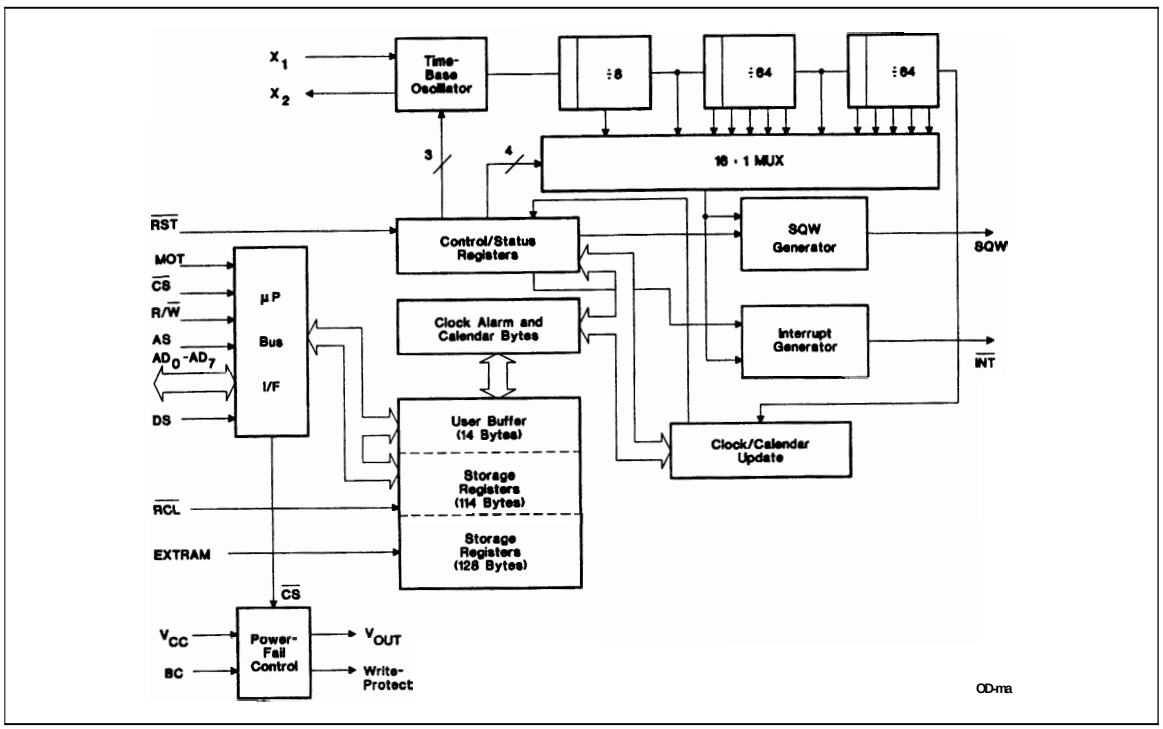


28-Pin PLCC

PL-10

AD0–AD7	Multiplexed address/data input/output
MOT	Bus type select input
$\overline{CS}$	Chip select input
AS	Address strobe input
DS	Data strobe input
R/$\overline{W}$	Read/write input
$\overline{INT}$	Interrupt request output
$\overline{RST}$	Reset input
SQW	Square wave output
EXTRAM	Extended RAM enable
$\overline{RCL}$	RAM clear *input*
BC	3V backup cell input
X1, X2	Crystal *inputs*
VCC	Power supply
VSS	Ground

Block Diagram



Pin Descriptions

MOT Bus type select input

MOT selects bus timing for either Motorola or Intel architecture. This pin should be tied to V_{CC} for Motorola timing or to Vss for Intel timing (see Table 1). The setting should not be changed during system operation. MOT is internally pulled low by a 30KR resistor.

Table 1. Bus Setup

Bus Type	MOT Level	DS Equivalent	R/W Equivalent	AS Equivalent
Motorola	V_{CC}	DS, E, or 0 2		AS
Intel	Vss	RD, MEMR, or I/OR	WR, MEMW, or VOW	ALE

AD_0-AD_7 Multiplexed address/data input/output

The bq3285E/L bus cycle consists of two phases: the address phase and the data-transfer phase. The address phase precedes the data-transfer phase. During the address phase, an address placed on AD_0–AD_7 and EXTRAM is latched into the bq3285E/L on the falling edge of the AS signal. During the data-transfer phase of the bus cycle, the AD_0–AD_7 pins serve as a bidirectional data bus.

AS Address strobe input

AS serves to demultiplex the address/data bus. The falling edge of AS latches the address on AD_0–AD_7 and EXTRAM. This demultiplexing process is independent of the CS signal. For DIP and SOIC packages with MOT = Vss, the AS input is provided a signal similar to ALE in an Intel-based system.

DS **Data strobe input**

When **MOT = V_{CC},** DS controls data transfer during a **bq3285E/L** bus cycle. During a read cycle, the **bq3285E/L** drives the bus after the rising edge on DS. During a write cycle, the falling edge on DS is used to latch write data into the chip.

When **MOT = V_{SS},** the DS input is used a signal similar to RD, MEMR, or **I/OR** in an Intel-bared system. The falling edge on DS is used to enable the outputs during a read cycle.

R/$\overline{W}$ **Read/write input**

When MOT = V_{CC}, the level on **R/$\overline{W}$** identifies the direction of data transfer. A high level on R/$\overline{W}$ indicates a read bus cycle, whereas a low on this pin indicates a write bus cycle.

When **MOT = V_{SS}, R/$\overline{W}$** is provided a signal similar to $\overline{WR}$, $\overline{MEMW}$, or **I/$\overline{OW}$** in an Intel-based system. The rising edge on **R/W** latches data into the **bq3285E/L.**

$\overline{CS}$ **Chip select input**

$\overline{CS}$ should be driven low and held stable during the data-transfer phase of a bus cycle accessing the **bq3285E/L.**

$\overline{INT}$ **Interrupt request output**

$\overline{INT}$ is open-drain output. This allows alarm INT to be valid in battery-backup mode. To use this feature, $\overline{INT}$ must be connected to a power supply other than V_{CC}. INT is asserted low when any event flag is set and the corresponding event enable bit is also set. $\overline{INT}$ becomes high-impedance whenever register C is read (see the Control/Status Registers section).

SQW **Square-wave output**

SQW may output a programmable frequency square-wave signal during normal (V_{CC} valid) system operation. Any one of the 13 specific frequencies may be selected through register A. This pin is held low when the square-wave enable bit (SQWE) in register B is 0 (see the Control/Status Registers section).

A 32.768kHz output is enabled by setting the SQWE bit in register B to 1 and the 32KE bit in register C to 1 after setting OSC2–OSC0 in register A to 011 (binary).

EXTRAM **Extended RAM enable**

Enables 128 bytes of additional nonvolatile SRAM. It is connected intemally to a 30KΩ pull-down resistor. To access the RTC registers, EXTRAM must be low.

$\overline{RCL}$ **RAM clear input**

A low level on the $\overline{RCL}$ pin causes the contents of each of the 242 storage bytes to be set to FF(hex). The contents of the clock and control registers are unaffected. This pin should be used as a user-interface input (pushbutton to ground) and not connected to the output of any active component. $\overline{RCL}$ input is only recognized when held low for at least 125ms in the presence of Vcc. Using RAM clear does not affect the battery load. This pin is connected internally to a 30KΩ pull-up resistor.

BC 3V **backup cell input**

BC should be connected to a 3V backup cell for RTC operation and storage register nonvolatility in the absence of system power. When V_{CC} slews down past V_{BC} (3V typical), the integral control circuitry switches the power source to BC. When V_{CC} returns above V_{BC}, the power source is switched to V_{CC}.

Upon power-up, a voltage within the V_{BC} range must be present on the BC pin for the oscillator to start up.

$\overline{RST}$ **Reset input**

The **bq3285E/L** is reset when $\overline{RST}$ is pulled low. When reset, $\overline{INT}$ becomes high impedance, and the **bq3285E/L** is not accessible. Table 4 in the Control/Status Registers section lists the register bite that are cleared by a reset.

Reset may be disabled by connecting $\overline{RST}$ to Vcc. This allows the control bits to retain their states through power-down/power-up cycles.

X1, X2 **Crystal input**

The **X1,** X2 inputs are provided for an external 32.768kHz quartz crystal, Daiwa DT-26 or equivalent, with 6pF load capacitance. A trimming capacitor may be necessary for extremely precise time-base generation.

In the absence of a crystal, a 32.768kHz waveform can be fed into the X1 input.

Functional Description

Address Map

The bq3285E/L provides 14 bytes of clock and control/status registers and 242 bytes of general nonvolatile storage. Figure 1 illustrates the address map for the bq3285E/L.

Update Period

The update period for the bq3285E/L is one second. The bq3285E/L updates the contents of the clock and calendar locations during the update cycle at the end of each update period (see Figure 2). The alarm flag bit may also be set during the update cycle.

The bq3285E/L copies the local register updates into the user buffer accessed by the host processor. When a 1 is written to the update transfer inhibit bit (UTI) in register B, the user copy of the clock and calendar bytes remains unchanged, while the local copy of the same bytes continues to be updated every second.

The update-in-progress bit (UIP) in register A is set t_{BUC} time before the beginning of an update cycle (see Figure 2). This bit is cleared and the update-complete flag (UF) is set at the end of the update cycle.

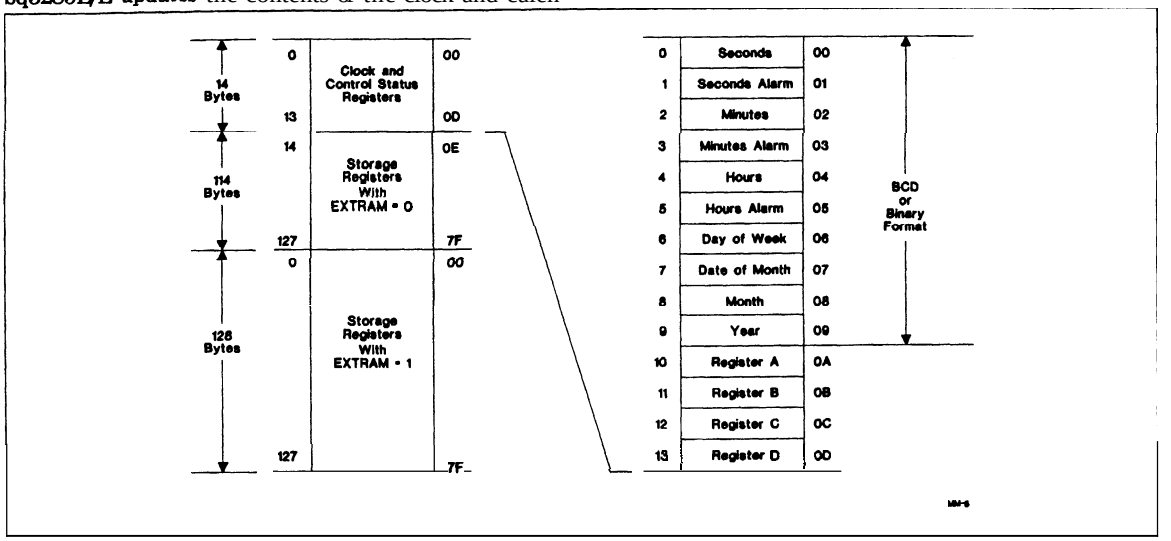


Figure 1. Address Map

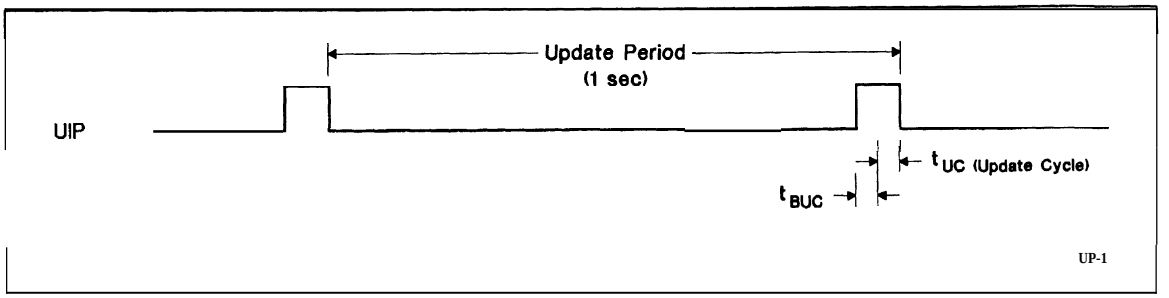


Figure 2. Update Period Timing and UIP

Programming the RTC

The time-of-day, alarm, and calendar bytes can be written in either the BCD or binary format (see Table 2).

These steps may be followed to program the time, alarm, and calendar:

1. Modify the contents of register B:
   a. Write a 1 to the UTI bit to prevent transfers between RTC bytes and user buffer.
   b. Write the appropriate value to the data format (DF) bit to select BCD or binary format for all time, alarm, and calendar bytes.
   c. Write the appropriate value to the hour format (HF) bit.
2. Write new values to all the time, alarm, and calendar locations.
3. Clear the UTI bit to allow update transfers.

On the next update cycle, the RTC updates all 10 bytes in the selected format.

Table 2. Time, Alarm, and Calendar Formats

Address	RTC Bytes	Range		
		Decimal	Binary	Binary-Coded Decimal
0	Seconds	0–59	00H–3BH	00H–59H
1	Seconds alarm	0–59	00H–3BH	00H–59H
2	Minutes	0-59	00H–3BH	00H–59H
3	Minutes alarm	0–59	OOH-3BH	00H–59H
4	Hours, 12-hour format	1–12	01H–OCH AM; 81H–8CH PM	01H–12H AM; 81H–92H PM
	Hours, 24-hour format	0–23	00H–17H	00H–23H
5	Hours alarm, 12-hour format	1–12	01H–OCH AM; 81H–8CH PM	01H–12H AM; 81H–92H PM
	Hours alarm, 24-hour format	0–23	OOH-17H	00H–23H
6	Day of week (1=Sunday)	1–7	01H–07H	01H–07H
7	Day of month	1-31	01H–1FH	01H–31H
8	Month	1–12	01H–0CH	01H–12H
9	Year	0–99	00H–63H	00H–99H

Square-Wave Output

The bq3285E/L divides the 32.768kHz oscillator frequency to produce the 1Hz update frequency for the clock and calendar. Thirteen taps from the frequency divider are fed to a 16:1 multiplexer circuit. The output of this mux is fed to the SQW output and periodic interrupt generation circuitry. The four least-significant bits of register A, RS0–RS3, select among the 13 taps (see Table 3). The square-wave output is enabled by writing a 1 to the square-wave enable bit (SQWE) in register B. A 32.768kHz output may be selected by setting OSC2–OSC0 in register A to 011 while SQWE = 1 and 32KE = 1.

Interrupts

The bq3285E/L allows three individually selected interrupt events to generate an interrupt request. These three interrupt events are:

- The periodic interrupt, programmable to occur once every 122µs to 500ms.
- The alarm interrupt, programmable to occur once per second to once per day, is active in battery-backup mode, providing a 'wake-up' feature.
- The update-ended interrupt, which occurs at the end of each update cycle.

Each of the three interrupt events is enabled by an individual interrupt-enable bit in register B. When an event occurs, its event flag bit in register C is set. If the corresponding event enable bit is also set, then an interrupt request is generated. The interrupt request flag bit (INTF) of register C is set with every interrupt request. Reading register C clears all flag bits, including INTF, and makes $\overline{INT}$ high-impedance.

Two methods can be used to process bq3285E/L interrupt events:

- Enable interrupt events and use the interrupt request output to invoke an interrupt service routine.
- Do not enable the interrupts and use a polling routine to periodically check the status of the flag bits.

The individual interrupt sources are described in detail in the following sections.

Table 3. Square-Wave Frequency/Periodic Interrupt Rate

Register A Bits							Square Wave		Periodic Interrupt	
OSC2	OSC1	OSC0	RS3	RS2	RS1	RS0	Frequency	Units	Period	Units
0	1	0	0	0	0	0	None		None	
0	1	0	0	0	0	1	256	Hz	3.90625	ms
0	1	0	0	0	1	0	128	Hz	7.8125	ms
0	1	0	0	0	1	1	8.192	kHz	122.070	µs
0	1	0	0	1	0	0	4.096	kHz	244.141	µs
0	1	0	0	1	0	1	2.048	kHz	488.281	µs
0	1	0	0	1	1	0	1.024	kHz	976.5625	µs
0	1	0	0	1	1	1	512	Hz	1.953125	ms
0	1	0	1	0	0	0	256	Hz	3.90625	ms
0	1	0	1	0	0	1	128	Hz	7.8125	ms
0	1	0	1	0	1	0	64	Hz	15.625	ms
0	1	0	1	0	1	1	32	Hz	31.25	ms
0	1	0	1	1	0	0	16	Hz	62.5	ms
0	1	0	1	1	0	1	8	Hz	125	ms
0	1	0	1	1	1	0	4	Hz	250	ms
0	1	0	1	1	1	1	2	Hz	500	ms
0	1	1	X	X	X	X	32.768	kHz	same as above defined by RS3–RS0	

Periodic Interrupt

The mux output used to drive the SQW output also drives the interrupt-generation circuitry. If the periodic interrupt event is enabled by writing a 1 to the periodic interrupt enable bit (PIE) in register C, an interrupt request is generated once every 122µs to 500ms. The period between interrupts is selected by the same bits in register A that select the square wave frequency (see Table 3). Setting OSC2–OSC0 in register A to 011 does not affect, the periodic interrupt timing.

Alarm Interrupt

The alarm interrupt is active in battery-backup mode, providing a 'wake-up' capability. During each update cycle, the RTC compares the hours, minutes, and seconds bytes with the three corresponding alarm bytes. If a match of all bytes is found, the alarm interrupt event flag bit, AF in register C, is set to 1. If the alarm event is enabled, an interrupt request is generated.

An alarm byte may be removed from the comparison by setting it to a 'don't care' state. An alarm byte is set to a 'don't care' state by writing a 1 to each of its two most-significant bite. A 'don't care* state may be used to select the frequency of alarm interrupt events as follows:

- If none of the three alarm bytes is 'don't care,' the frequency is once per day, when hours, minutes, and seconds match.
- If only the hour alarm byte is 'don't care.' the frequency is once per hour, when minutes and seconds match.
- If only the hour and minute alarm bytes are 'don't care," the frequency is once per minute, when seconds match.
- If the hour, minute, and second alarm bytes are 'don't care," the frequency is once per second.

Update Cycle Interrupt

The update cycle ended flag bit (UF) in register C is set to a 1 at the end of an update cycle. If the update interrupt enable bit (UIE) of register B is 1, and the update transfer inhibit bit (UTI) in register B is 0, then an interrupt request is generated at the end of each update cycle.

Accessing RTC bytes

The EXTRAM pin must be low to access the RTC registers. Time and calendar bytes read during an update cycle may be in error. Three methods to access the time and calendar bytes without ambiguity are:

- Enable the update interrupt event to generate interrupt requests at the end of the update cycle. The interrupt handler has a maximum of 999ms to access the clock bytes before the next update cycle begins (see Figure 3).
- Poll the update-in-progreaa bit (UIP) in register A. If UIP = 0, the polling routine has a minimum of t_{BUC} time to access the clock bytes (see Figure 3).
- Use the periodic interrupt event to generate interrupt requests every t_{PI} time, such that UIP = 1 always occurs between the periodic interrupts. The interrupt handler has a minimum of $t_{PI}/2 + t_{BUC}$ time to access the clock bytes (see Figure 3).

Oscillator Control

When power is first applied to the bq3285E/L and V_{CC} is above V_{PFD}, the internal oscillator and frequency divider are turned on by writing a 010 pattern to bits 4 through 6 of register A. A pattern of 011 behaves as 010 but additionally transforms register C into a read/write register. This allows the 32.768kHz output on the square wave pin to be turned on. A pattern of 11X turns the oscillator on, but keeps the frequency divider disabled. Any other pattern to these bits keeps the oscillator off.

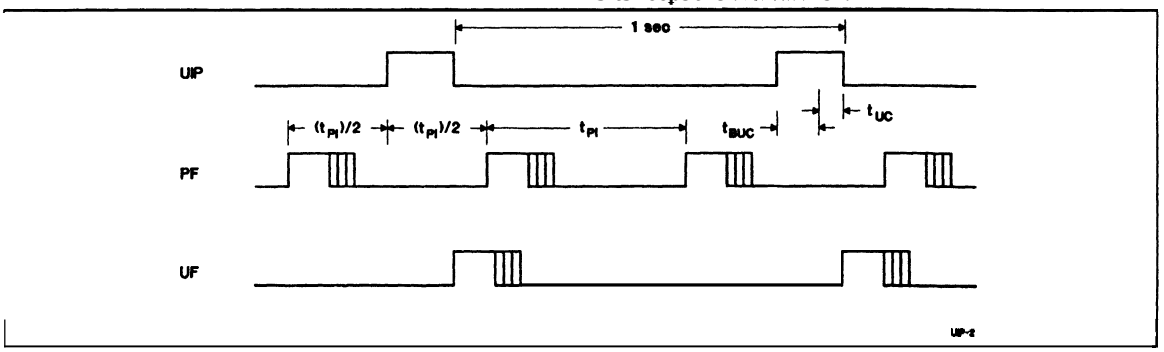


Figure 3. Update-Ended/Periodic Interrupt Relationship

Power-Down/Power-Up Cycle

The bq3285E and bq3285L power-up/power-down cycles are different. The bq3285L continuously monitors V_{CC} for out-of-tolerance. During a power failure, when V_{CC} falls below V_{PFD} (2.53V typical), the bq3285L write-protects the clock and storage registers. The power source is switched to BC when V_{CC} is less than V_{PFD} and BC is greater than V_{PFD}, or when V_{CC} is less than V_{BC} and V_{BC} is less than V_{PFD}. RTC operation and storage data are sustained by a valid backup energy source. When V_{CC} is above V_{PFD}, the power source is V_{CC}. Write-protection continues for t_{CSR} time after V_{CC} rises above V_{PFD}.

The bq3285E continuously monitors V_{CC} for out-of-tole——. During a power failure, when V_{CC} falls below V_{PFD} (4.17V typical), the bq3285E write-protects the clock and storage registers. When V_{CC} is below V_{BC} (3V typical), the power source is switched to BC. RTC operation and storage data are sustained by a valid backup energy source. When V_{CC} is above V_{BC}, the power murce is V_{CC}. Write-protecton continues for t_{CSR} time after V_{CC} rises above V_{PFD}.

Control/Status Registers

The four control/status registers of the bq3285E/L are accessible regardless of the status of the update cycle (see Table 4).

Register A

Register A Bits							
7	6	5	4	3	2	1	0
UIP	OS2	OS1	OS0	RS3	RS2	RS1	RS0

Register A programs:

- The frequency of the square-wave and the periodic event rate.
- Oscillator operation.

Register A provides:

- Statue of the update cycle.

RS0–RS3 - Frequency Select

7	6	5	4	3	2	1	0
-	-	-	-	RS3	RS2	RS1	RS0

These bite select one of the 13 frequencies for the SQW output and the periodic interrupt rate, as shown in Table 3.

OS0–OS2 - Oscillator Control

7	6	5	4	3	2	1	0
-	OS2	OS1	OS0	-	-	-	-

These three bite control the state of the oscillator and divider stages. A pattern of 010 enables RTC operation by turning on the oscillator and enabling the frequency divider. A pattern of 011 behaves as 010 but additionally transforma register C into a read/write register. This allows the 32.768kHz output on the square wave pin to be turned on. A pattern of 11X turns the oscillator on, but keeps the frequency divider disabled. When 010 is written, the RTC begins its first update after 500ms.

UIP - Update Cycle Status

7	6	5	4	3	2	1	0
UIP	-	-	-	-	-	-	-

This read-only bit is set prior to the update cycle. When UIP equals 1, an RTC update cycle may be in progress. UIP is cleared at the end of each update cycle. This bit is also cleared when the update transfer inhibit (UTI) bit in register B is 1.

Table 4. Control/Status Registers

Reg.	Loc. (Hex)	Read	Write	Bit Name and State on Reset															
				7 (MSB)		6		5		4		3		2		1		0 (LSB)	
A	0A	Yes	Yes[1]	UIP	na	OS2	na	OS1	na	OS0	na	RS3	na	RS2	na	RS1	na	RS0	na
B	0B	Yes	Yes	UTI	na	PIE	0	AIE	0	UIE	0	SQWE	0	DF	na	HF	na	DSE	na
C	0C	Yes	No[2]	INTF	0	PF	0	AF	0	UF	0	-	0	32KE	na	-	0	-	0
D	0D	Yes	No	VRT	na	-	0	-	0	-	0	-	0	-	0	-	0	-	0

Notes: na = not affected.

1. Except bit 7.
2. Read/write only when OSC2–OSC0 in register A is 011 (binary).

Register B

Register B Bits							
7	6	5	4	3	2	1	0
UTI	PIE	AIE	UIE	SQWE	DF	HF	DSE

Register B enables:

- Update cycle transfer operation
- Square-wave output
- Interrupt events
- Daylight saving adjustment

Register B selects:

- Clock and calendar data formats

All bits of register B are read/write.

DSE - Daylight Saving Enable

7	6	5	4	3	2	1	0
						-	DSE

This bit enables daylight-saving time adjustments when written to 1:

- On the last Sunday in October, the first time the bq3285E/L increments past 1:59:59 AM, the time falls back to 1:00:00 AM.
- On the first Sunday in April, the time springs forward from 2:00:00 AM to 3:00:00 AM.

HF - Hour Format

7	6	5	4	3	2	1	0
-	-	-	-	-	-	HF	-

This bit selects the time-of-day and alarm hour format:

1 = 24-hour format

0 = 12-hour format

DF - Data Format

7	6	5	4	3	2	1	0
-	-	-	-	-	DF	-	-

This bit selects the numeric format in which the time, alarm, and calendar bytes are represented:

1 = Binary

0 = BCD

SQWE - Square-Wave Enable

7	6	5	4	3	2	1	0
			-	SQWE	-	-	-

This bit enables the square-wave output:

1 = Enabled

0 = Disabled and held low

UIE - Update Cycle Interrupt Enable

7	6	5	4	3	2	1	0
-	-	-	UIE	-	-	-	-

This bit enables an interrupt request due to an update ended interrupt event:

1 = Enabled

0 = Disabled

The UIE bit is automatically cleared when the UTI bit equals 1.

AIE - Alarm Interrupt Enable

7	6	5	4	3	2	1	0
A					-	-	-

This bit enables an interrupt request due to an alarm interrupt event:

1 = Enabled

0 = Disabled

PIE - Periodic Interrupt Enable

7	6	5	4	3	2	1	0
-	PIE	-	-	-	-	-	-

This bit enables an interrupt request due to a periodic interrupt event:

1 = Enabled

0 = Disabled

UTI - Update Transfer Inhibit

7	6	5	4	3	2	1	0
UTI	-	-	-	-	-	-	-

This bit inhibits the transfer of RTC bytes to the user buffer:

1 = Inhibits transfer and clears UTE

0 = Allows transfer

Register C

Register C Bits							
7	6	5	4	3	2	1	0
INTF	PF	AF	UF	0	32KE	0	0

Register C is the read-only event status register.

Bits 0, 1, 3 - Unused Bits

7	6	5	4	3	2	1	0
				0	-	0	0

These bits are always set to 0.

32KE - 32kHz Enable Output

7	6	5	4	3	2	1	0
-	-	-	-	-	32KE	-	-

This bit may be set to a 1 only when the OSC2–OSC0 bits in register A are set to 011. Setting OSCWSCO to anything other than 011 clears this bit. If SQWE in register B and 32KE are set, a 32.768kHz waveform is output on the square wave pin.

UF - Update Event Flag

7	6	5	4	3	2	1	0
-	-	-	UF	-	-	-	-

This bit is set to a 1 at the end of the update cycle. Reading register C clears this bit.

AF - Alarm Event Flag

7	6	5	4	3	2	1	0
-	-	AF	-	-	-	-	-

This bit is set to a 1 when an alarm event occurs. Reading register C clears this bit.

PF - Periodic Event Flag

7	6	5	4	3	2	1	0
-	PF	-	-	-	-	-	-

This bit is set to a 1 every t_{PI} time, where t_{PI} is the time period selected by the settings of RS0–RS3 in register A. Reading register C clears this bit.

INTF - Interrupt Request Flag

7	6	5	4	3	2	1	0
INTF	-	-	-	-	-	-	-

This flag is set to a 1 when any of the following is true:

AIE = 1 and AF = 1

PIE = 1 and PF = 1

UIE = 1 and UF = 1

Reading register C clears this bit.

Register D

Register D Bits							
7	6	5	4	3	2	1	0
VRT	0	0	0	0	0	0	0

Register D is the read-only data integrity status register.

Bits 0–6 - Unused Bits

7	6	5	4	3	2	1	0
-	0	0	0	0	0	0	0

These bits are always set to 0.

VRT - Valid RAM and Time

7	6	5	4	3	2	1	0
VRT	-	-	-	-	-	-	

1 = Valid backup energy source

0 = Backup energy source is depleted

When the backup energy source is depleted (VRT = 0), data integrity of the RTC and storage registers is not guaranteed.

Absolute Maximum Ratings—bq3285E

Symbol	Parameter	Value	Unit	Condition8
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \le V_{CC} + 0.3$
T_{OPR}	Operating temperature	Oto +70	°C	Commercial
		-40 to +85	°C	Industrial
T_{STG}	Storage temperature	-55 to +125	°C	
T_{BIAS}	Temperature under bias	-40 to +85	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute** Maximum **Ratings are** exceeded. Functional operation **should** be limited to the Recommended DC Operating **Conditions** detailed in **this** data sheet. **Exposure** to conditions beyond the operational **limits** for extended periods of time may affect device reliability.

5

Absolute Maximum Ratings—bq3285L

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on Vcc relative to V_{SS}	-0.3 to 6.0	V	
VT	DC voltage applied on any pin **excluding** Vcc relative to V_{SS}	-0.3 to 6.0	V	$V_T \le V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
T_{STG}	Storage temperature	-55 to +125	"C	
T_{BIAS}	Temperature under bias	-40 to +85	°C	
T_{SOLDER}	Soldering temperature	260	"C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings are** exceeded. Functional operation should be limited to the Recommended DC **Operating Conditions** detailed in this data sheet. Exposure to conditions beyond the operational **limits** for extended periods of time may affect device reliability.

Recommended DC Operating Conditions—bq3285E ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IL}	Input low voltage	-0.3		0.8	V
V_{IH}	Input high voltage	2.2		V_{CC} + 0.3	V
V_{BC}	Backup cell voltage	2.5		4.0	V

Note: Typical values indicate operation at T_A = 25°C.

Recommended DC Operating Conditions—bq3285L ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{CC}	Supply voltage	2.7	3.15	3.6	V
V_{SS}	Supply voltage	0	0	0	V
V_{IL}	Input low voltage	-0.3		0.6	V
V_{IH}	Input high voltage	2.2		V_{CC} + 0.3	V
V_{BC}	Backup cell voltage	2.4		4.0	V

Note: Typical values indicate operation at T_A = 25°C.

Crystal Specifications—bq3285E/L (DT-26 or Equivalent)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
f_O	Oscillation frequency		32.768		kHz
C_L	Load capacitance		6		pF
T_P	Temperature turnover point	20	25	30	°C
k	Parabolic curvature constant			-0.042	ppm/°C
Q	Quality factor	40,000	70,000		
R_1	Series resistance			45	KΩ
C_O	Shunt capacitance		1.1	1.8	pF
C_O/C_1	Capacitance ratio		430	600	
D_L	Drive level			1	µW
$\Delta f/f_O$	Aging (first year at 25°C)	-	1	-	ppm

DC Electrical Characteristics—bq3285E ($T_A = T_{OPR}$, V_{CC} = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current			± 1	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current			± 1	µA	AD_0–AD_7, $\overline{INT}$, and SQW in high impedance, $V_{OUT} = V_{SS}$ to V_{CC}
V_{OH}	Output high voltage	2.4			V	I_{OH} = -2.0 mA
V_{OL}	Output low voltage			0.4	V	I_{OL} = 4.0 mA
I_{CC}	Operating supply current		7	15	mA	Mia cycle, duty = 100%, I_{OH} = 0mA, I_{OL} = 0mA
I_{CCSB}	Standby supply current		300		µA	V_{IN} = V_{SS} or V_{CC}, $\overline{CS} \geq V_{CC}$ - 0.2
V_{SO}	Supply switch-over voltage		V_{BC}		V	
I_{CCB}	Battery operation current		0.3	0.5	µA	V_{BC} = 3V, T_A = 25°C
V_{PFD}	Power-fail-detect voltage	4.0	4.17	4.35	V	
I_{RCL}	Input current when $\overline{RCL} = V_{SS}$.			185	µA	Internal 30K pull-up
I_{MOTH}	Input current when MOT = V_{CC}			-185	µA	Internal 30K pull-down
	Input current when MOT = V_{SS}			0	µA	Internal 30K pull-down
I_{XTRAM}	Input current when EXTRAM = V_{CC}			-185	µA	Internal 30K pull-down
	Input current when EXTRAM = V_{SS}			0	µA	Internal 30K pull-down

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC} = 3V.

DC Electrical Characteristics—bq3285L (T_A = TOPR, VCC = 3.15V ±0.45V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current			± 1	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output leakage current			± 1	µA	AD_0–AD_7 and $\overline{INT}$ in high impedance, V_{OUT} = V_{SS} to vcc
V_{OH}	Output high voltage	2.2			V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage			0.4	V	I_{OL} = 2.0 mA
I_{CC}	Operating supply current		5	9	mA	Min. cycle, duty = 100%, I_{OH} = 0mA, I_{OL} = 0mA
I_{CCSB}	Standby supply current		100		µA	V_{IN} = V_{SS} or V_{CC}, $\overline{CS}$ ≥ V_{CC} - 0.2
V_{SO}	Supply switch-over voltage		V_{PFD}		V	V_{BC} > V_{PFD}
			V_{BC}		V	V_{BC} < V_{PFD}
I_{CCB}	Battery operation current		0.3	0.5	µA	V_{BC} = 3V, T_A = 25°C, V_{CC} < V_{BC}
V_{PFD}	Power-fail-detect voltage	2.4	2.53	2.65	V	
I_{RCL}	Input current when $\overline{RCL}$ = Vss.			120	µA	Internal 30K pull-up
I_{MOTH}	Input current when MOT = V_{CC}			-120	µA	Internal 30K pull-down
	Input current when MOT = V_{SS}			0	µA	Internal 30K pull-down
I_{XTRAM}	Input current when EXTRAM = vcc			-120	µA	Internal 30K pull-down
	Input current when EXTRAM = V_{SS}			0	µA	Internal 30K pull-down

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 3V.

Capacitance—bq3285E/L (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance			7	pF	V_{OUT} = 0V
C_{IN}	Input capacitance			5	pF	V_{IN} = 0V

Note: This parameter is sampled and not 100% tested. It does not include the X1 or X2 pin.

. Test Conditions—bq3285E

Parameter	Test Conditions
Input pulse levels	0 to 3.0V
Input rise and fall times	5ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 4 and 5

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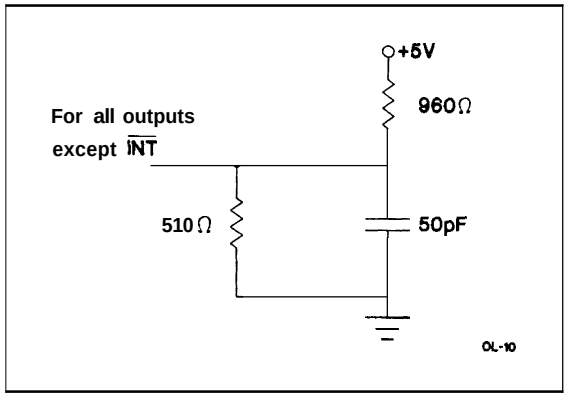

Figure 4. Output Load A—bq3285E

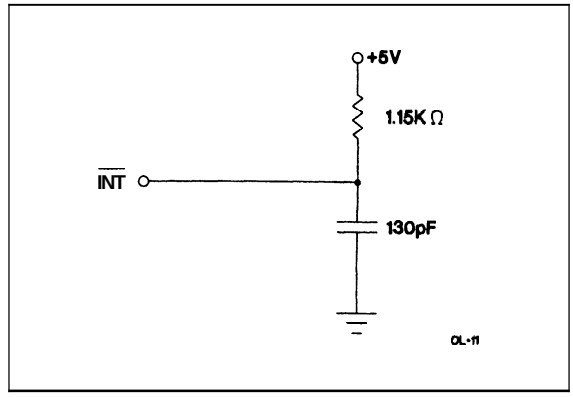

Figure 5. Output Load B—bq3285E

AC Test Conditions—bq3285L

Parametw	Test Conditions
Input pulse levels	0 to 2.3 V
Input rise and fall times	5 ns
Input and output timing reference levels	1.2 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 6 and 7

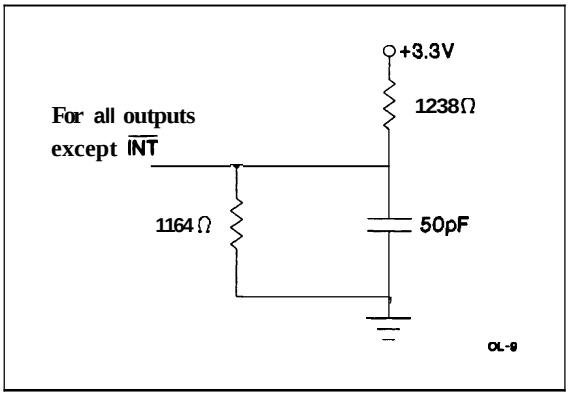

Figure 6. Output Load A—bq3285L

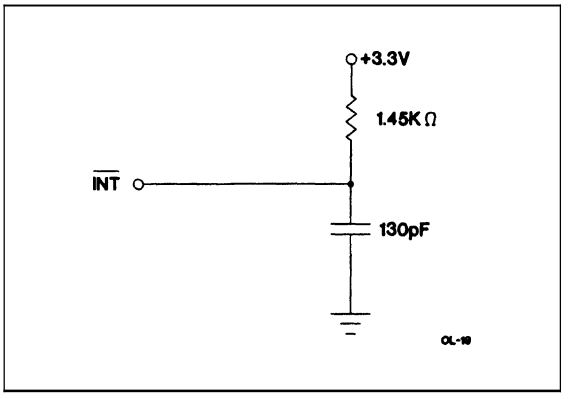

Figure 7. Output Load B—bq3285L

Read/Write Timing—bq3285E ($T_A = T_{OPR}$, V_{CC} = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYC}	Cycle time	160			ns	
t_{DSL}	DS low or $\overline{RD}/\overline{WR}$ high time	80			ns	
t_{DSH}	DS high or $\overline{RD}/\overline{WR}$ low time	55			ns	
t_{RWH}	R/$\overline{W}$ hold time	0			ns	
t_{RWS}	R/$\overline{W}$ setup time	10			ns	
t_{CS}	Chip select setup time	5			ns	
t_{CH}	Chip select hold time	0			ns	
t_{DHR}	Read data hold time	0		25	ne	
t_{DHW}	Write data hold time	0			ns	
t_{AS}	Address setup time	20			ns	
t_{AH}	Address hold time	5			ns	
t_{DAS}	Delay time, DS to AS rise	10			ns	
t_{ASW}	Pulse width, AS high	30			ne	
t_{ASD}	Delay time, AS to DS rise ($\overline{RD}/\overline{WR}$ fall)	35			ns	
t_{OD}	Output data delay time from DS rise ($\overline{RD}$ fall)			50	ns	
t_{DW}	Write data setup time	30			ns	
t_{BUC}	Delay time before update cycle		244		µs	
t_{PI}	Periodic interrupt time interval					See Table 3
t_{UC}	Time of update cycle		1		µs	

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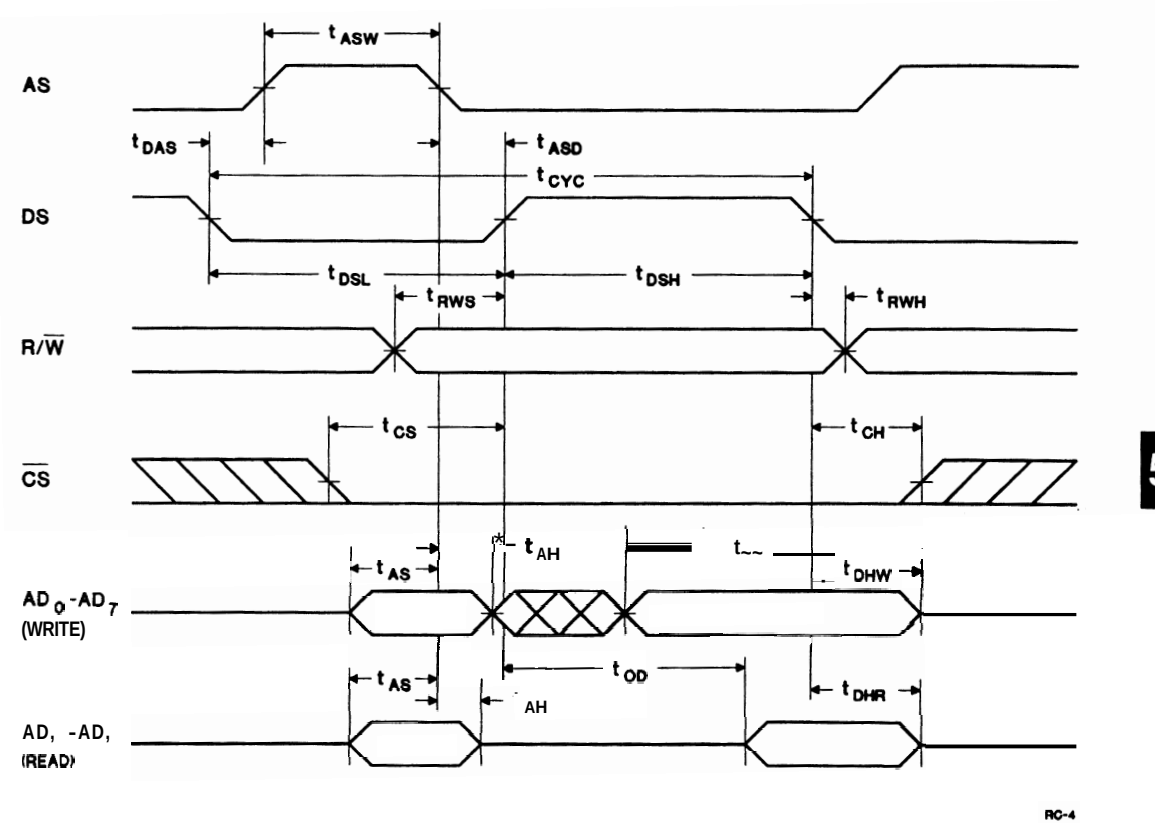
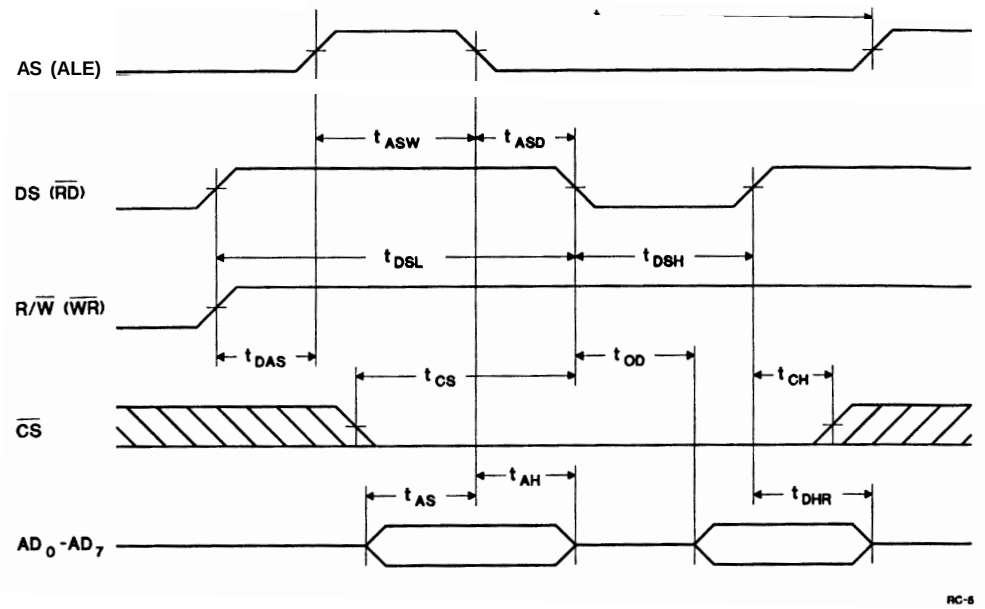
Read/Write Timing—bq3285L (T_A = T_{OPR}, V_{CC} = 3.15V ± 0.45V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYC}	Cycle time	270			ns	
t_{DSL}	DS low or $\overline{RD}/\overline{WR}$ high time	135			ns	
t_{DSH}	DS high or $\overline{RD}/\overline{WR}$ low time	90			ns	
t_{RWH}	R/$\overline{W}$ hold time	0			ns	
t_{RWS}	R/$\overline{W}$ setup time	15			ns	
t_{CS}	Chip select setup time	8			ns	
t_{CH}	Chip select hold time	0			ns	
t_{DHR}	Read data hold time	0		40	ns	
t_{DHW}	Write data hold time	0			ns	
t_{AS}	Address setup time	30			ns	
t_{AH}	Address hold time	15			ns	
t_{DAS}	Delay time, DS to AS rise	15			ns	
t_{ASW}	Pulse width, AS high	50			ns	
t_{ASD}	Delay time, AS to DS rise ($\overline{RD}/\overline{WR}$ fall)	55			ns	
t_{OD}	Output data delay time from DS rise ($\overline{RD}$ fall)			100	ns	
t_{DW}	Write data setup time	50			ns	
t_{BUC}	Delay time before update cycle		244		µs	
t_{PI}	Periodic interrupt time interval					See Table 3
t_{UC}	Time of update cycle		1		µs	

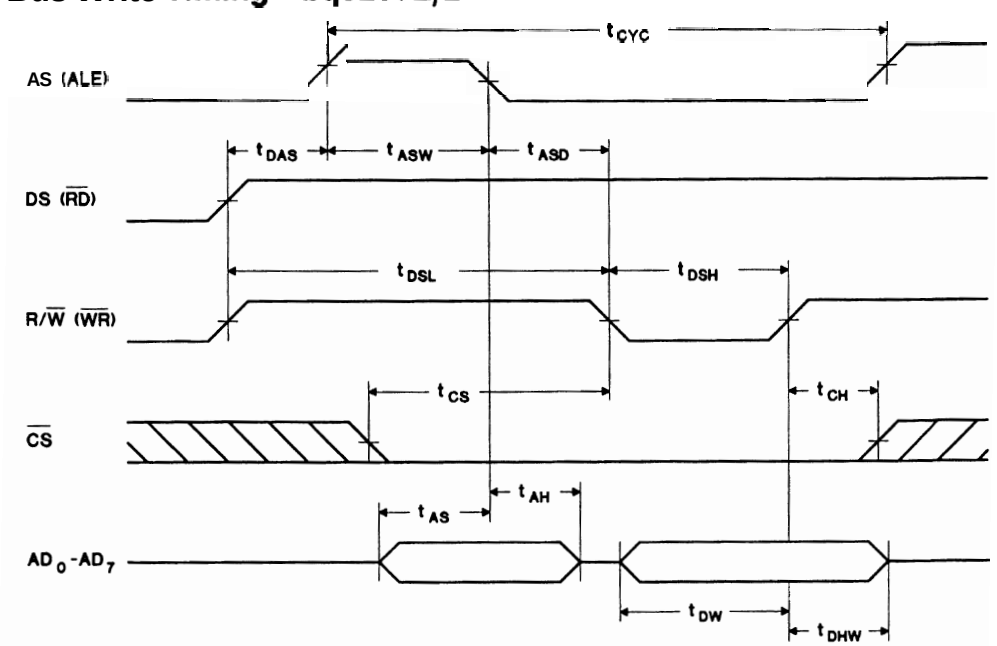
Motorola Bus Read/Write Timing—bq3285E/L



Intel Bus Read Timing—bq3285E/L



Intel Bus Write Timing—bq3285E/L

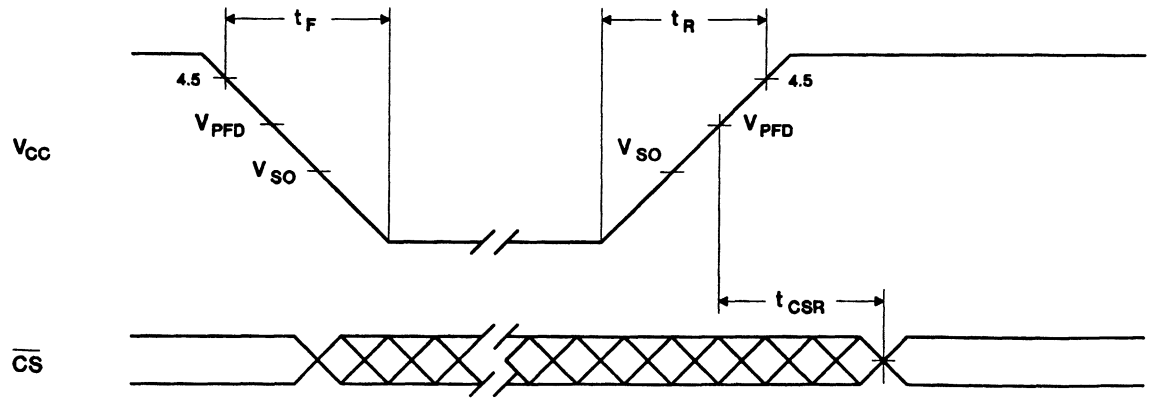


Power-Down/Power-Up Timing—bq3285E (TA = TOPR)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_F	V_{CC} slew from 4.5V to 0V	300			µs	
t_R	V_{CC} slew from 0V to 4.5V	100			µs	
t_{CSR}	$\overline{CS}$ at V_{IH} after power-up	20	-	200	ms	Internal write-protection period after V_{CC} passes V_{PFD} on power-up.

Caution. Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

Power-Down/Power-Up Timing—bq3285E



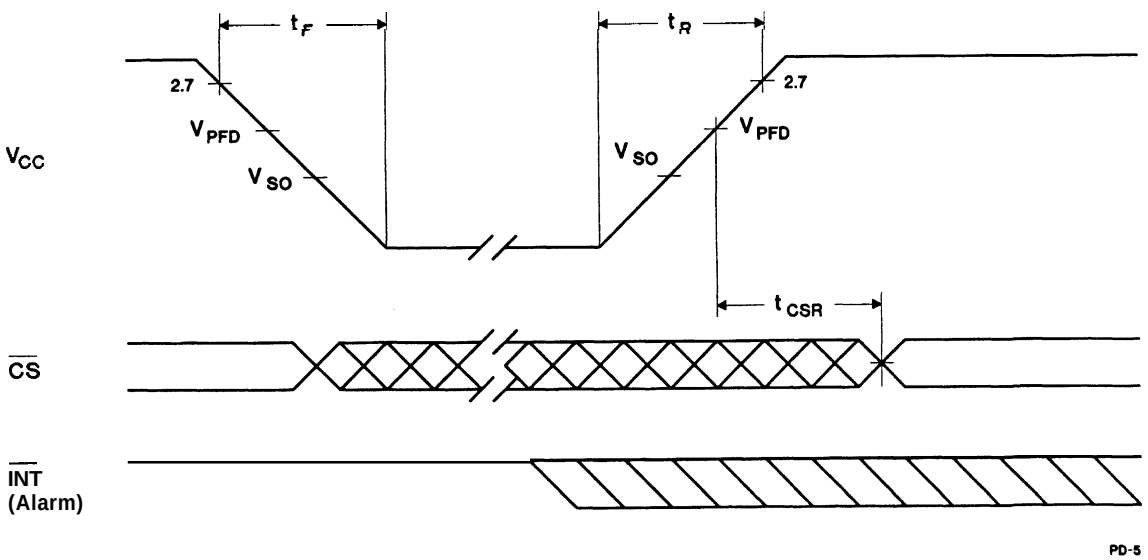
PD-4A

Power-Down/Power-Up Timing—bq3285L (TA = TOPR)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_F	V_{CC} slew from 2.*W* to 0*V*	300			µs	
t_R	V_{CC} slew from 0V to 2.*W*	100			µs	
t_{CSR}	$\overline{CS}$ at V_{IH} after power-up	20		200	ms	Internal write-protection period after V_{CC} passes V_{PFD} on power-up.

Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

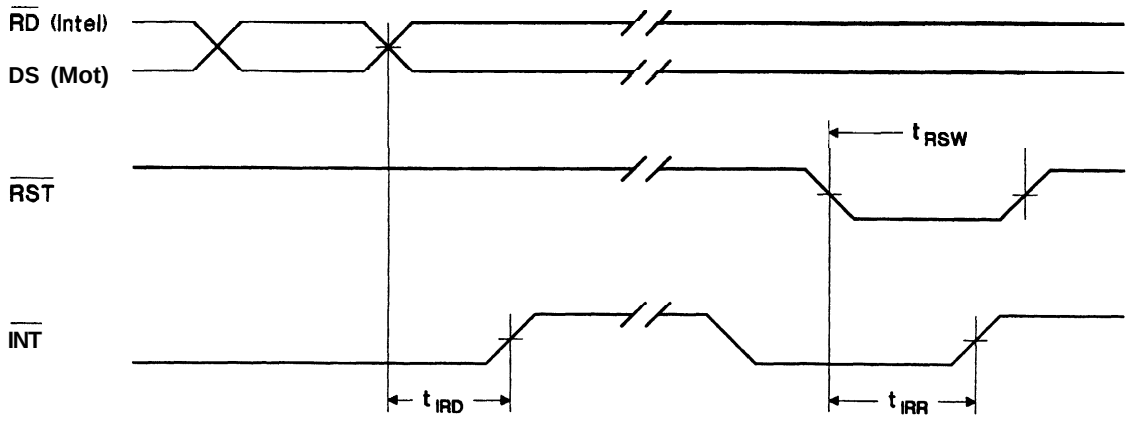
Power-Down/Power-Up Timing—bq3285L



Interrupt Delay Timing—bq3285E/L ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
t_{RSW}	Reset pulse width	5			µs
t_{IRR}	$\overline{INT}$ release from $\overline{RST}$			2	µs
t_{IRD}	$\overline{INT}$ release from DS	-	-	2	µs

Interrupt Delay Timing—bq3285E/L



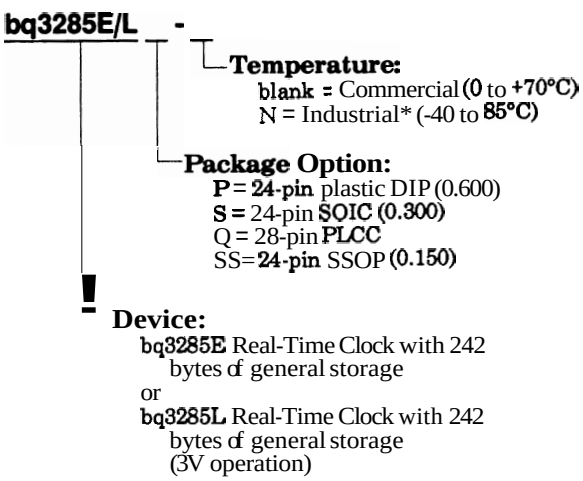
INT-1

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	8	Register C, bit 2	Was 0; is na (not affected)
1	~~18~~	~~Output data delay time tOD~~	Was ~~80~~ ns max; is ~~100~~ ns max

Note: Change 1 = Jan. 1995 B 'Final' changes from Dec. 1993 A "Preliminary."

Ordering Information



*bq3285E Q package only

BENCHMARQ

bq3285EC/LC

Real-Time Clock (RTC)

Features

- Direct clock/calendar replacement for IBM® AT-compatible computers and other applications
- 2.7–5.5V operation (bq3285LC); 4.5–5.5V operation (bq3285EC)
- 242 bytes of general nonvolatile storage
- Dedicated 32.768kHz output pin
- System wake-up capability—alarm interrupt output active in battery-backup mode
- Less than 0.5µA load under battery operation
- Selectable Intel or Motorola bus timing
- 24-pin plastic SOIC or SSOP

General Description

The CMOS bq3285EC/LC is a low-power microprocessor peripheral providing a time-of-day clock and 100-year calendar with alarm features and battery operation. The architecture ia based on the bq3285/7 RTC with added features: low-voltage operation, 32.768kHz output, and an extra 128 bytes of CMOS.

A 32.768kHz output is available for sustaining power-management activities. The bq3285EC 32kHz output is always on whenever Vcc is valid. For the bq3285LC, the output is on when the oscillator is turned on. In Vcc standby mode, the 32kHz is active, and the bq3285LC typically draws 100µA while the bq3285EC typically draws 300µA. Wake-up capability is provided by an alarm interrupt, which is active in battery-backup mode. In battery backup mode, current drain is less than 500nA.

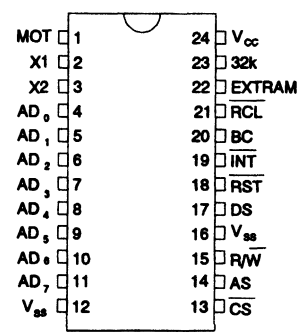
The bq3285EC/LC write-protects the clock, calendar, and storage registers during power failure. A backup battery then maintains data and operates the clock and calendar.

The bq3285EC/LC is a fully compatible real-time clock for IBM AT-compatible computers and other applications. The only external components are a 32.768kHz crystal and a backup battery.

The bq3285EC is intended for use in 5V systems. The bq3285LC is intended for use in 3V system; the bq3285LC, however, may also operate at 5V and then go into a 3V power-down state, write-protecting as if in a 3V system.

5

Pin Connections



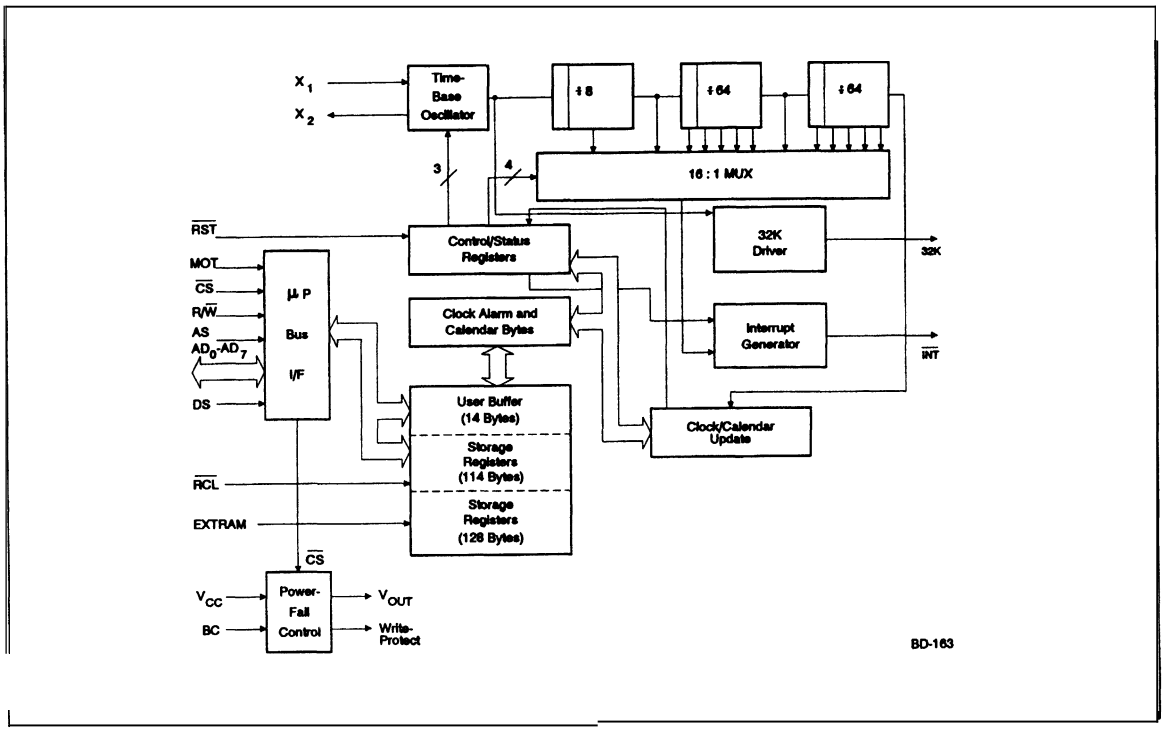
24-Pin SOIC or SSOP

PN-115

Pin Names

AD0–AD7	Multiplexed address/data input/output
MOT	Bus type select input
$\overline{CS}$	Chip select input
AS	Address strobe input
DS	Data strobe input
R/$\overline{W}$	Read/write input
$\overline{INT}$	Interrupt request output
RST	Reset input
32K	32.768kHz output
EXTRAM	Extended RAM enable
RCL	RAM clear input
BC	3V backup cell input
X1, X2	Crystal inputs
Vcc	Power supply
Vss	Ground

Block Diagram



Pin Descriptions

MOT — Bus type select input

MOT selects bus timing for either Motorola or Intel architecture. This pin should be tied to V_{CC} for Motorola timing or to V_{SS} for Intel timing (see Table 1). The setting should not be changed during system operation. MOT is internally pulled low by a 30KR resistor.

Table 1. Bus Setup

Bus Type	MOT Level	DS Equivalent	R/$\overline{W}$ Equivalent	AS Equivalent
Motorola	V_{CC}	DS, E, or Φ2	R/$\overline{W}$	AS
Intel	V_{SS}	$\overline{RD}$, $\overline{MEMR}$, or $\overline{I/OR}$	$\overline{WR}$, $\overline{MEMW}$, or $\overline{I/OW}$	ALE

AD_0–AD_7 — Multiplexed address/data input/output

The bq3285EC/LC bus cycle consists of two phases: the address phase and the data-transfer phase. The address phase precedes the data-transfer phase. During the address phase, an address placed on AD_0–AD_7 and EXTRAM is latched into the bq3285EC/LC on the falling edge of the AS signal. During the data-transfer phase of the bus cycle, the AD_0–AD_7 pins serve as a bidirectional data bus.

AS — Address strobe input

AS serves to demultiplex the address/data bus. The falling edge of AS latches the address on AD_0–AD_7 and EXTRAM. This demultiplexing process is independent of the CS signal. For DIP and SOIC packages with MOT = V_{SS}, the AS input is provided a signal similar to ALE in an Intel-based system.

DS **Data strobe input**

When MOT = Vcc, DS controls data transfer during a bq3285EC/LC bus cycle. During a read cycle, the bq3285EC/LC drives the bus after the rising edge on DS. During a write cycle, the falling edge on DS is used to latch write data into the chip.

When MOT = Vss, the DS input is provided a signal similar to $\overline{RD}$, $\overline{MEMR}$, or $\overline{I/OR}$ in an Intel-based system. The falling edge on DS is used to enable the outputs during a read cycle.

R/$\overline{W}$ **Read/write input**

When MOT = Vcc, the level on R/$\overline{W}$ identifies the direction of data transfer. A high level on R/$\overline{W}$ indicates a read bus cycle, whereas a low on this pin indicates a write bus cycle.

When MOT = Vss, R/$\overline{W}$ is provided a signal similar to $\overline{WR}$, $\overline{MEMW}$, or $\overline{I/OW}$ in an Intel-based system. The rising edge on R/$\overline{W}$ latches data into the bq3285EC/LC.

$\overline{CS}$ **Chip select input**

$\overline{CS}$ should be driven low and held stable during the data-transfer phase of a bus cycle accessing the bq3285EC/LC.

$\overline{INT}$ **Interrupt request output**

$\overline{INT}$ is an open-drain output This allows alarm $\overline{INT}$ to be valid in battery-backup mode. To use this feature, connect $\overline{INT}$ through a resistor to a power supply other than Vcc. $\overline{INT}$ is asserted low when any event flag is set and the corresponding event enable bit is also set. $\overline{INT}$ becomes high-impedance whenever register C is read (see the Control/Status Registers section).

32K **32.768 kHz output**

32K provides a buffered 32.768 kHz output. The frequency remains on and fixed at 32.768kHz as long as Vcc is valid.

EXTRAM **Extended RAM enable**

Enables 128 bytes of additional nonvolatile SRAM. It is connected internally to a 30kΩ pull-down resistor. To access the RTC registers, EXTRAM must be low.

$\overline{RCL}$ **RAM clear input**

A low level on the $\overline{RCL}$ pin causes the contents of each of the 242 storage bytes to be set to FF(hex). The contents of the clock and control registers are unaffected. This pin should be used as a user-interlace input (pushbutton to ground) and not connected to the output of any active component. $\overline{RCL}$ input is only recognized when held low for at least 125ms in the presence of Vcc. Using RAM clear does not *affect* the battery load. This pin is connected internally to a 30kΩ pull-up resistor.

BC **3V backup cell input**

BC should be connected to a 3V backup cell for RTC operation and storage register nonvolatility in the absence of system power. When Vcc slews down past V_{BC} (3V typical), the integral control circuitry switches the power source to BC. When Vcc returns above V_{BC}, the power source is switched to Vcc.

Upon power-up, a voltage within the V_{BC} range must be present on the BC pin for the oscillator to start up.

$\overline{RST}$ **Reset input**

The bq3285EC/LC is reset when $\overline{RST}$ is pulled low. When reset, $\overline{INT}$ becomes high impedance, and the bq3285EC/LC is not accessible. Table 4 in the Control/Status Registers section lists the register bits that are cleared by a reset.

Reset may be disabled by connecting $\overline{RST}$ to Vcc. This allows the control bite to retain their states through power-down/power-up cycles.

X1, X2 **Crystal input**

The X1, X2 inputs are provided for an external 32.768kHz quartz crystal, Daiwa DT-26 or equivalent, with 6pF load capacitance. A trimming capacitor may be necessary for extremely precise time-base generation.

In the absence of a crystal, a 32.768kHz waveform can be fed into the X1 input.

5

Functional Description

Address Map

The bq3285EC/LC provides 14 bytes of clock and control/status registers and 242 bytes of general nonvolatile storage. Figure 1 illustrates the address map for the bq3285EC/LC.

Update Period

The update period for the bq3285EC/LC is one second. The bq3285EC/LC updates the contents of the clock and calendar locations during the update cycle at the end of each update period (see Figure 2). The alarm flag bit may also be set during the update cycle.

The bq3285EC/LC copies the local register updates into the user buffer accessed by the host processor. When a 1 is written to the update transfer inhibit bit (UTI) in register B, the *user* copy of the clock and calendar bytes remains unchanged, while the local copy of the same bytes continues to be updated every second.

The update-in-progress bit (UIP) in register A is set t_{BUC} time before the beginning of an update cycle (see Figure 2). This bit is cleared and the update-complete flag (UF) is set at the end of the update cycle.

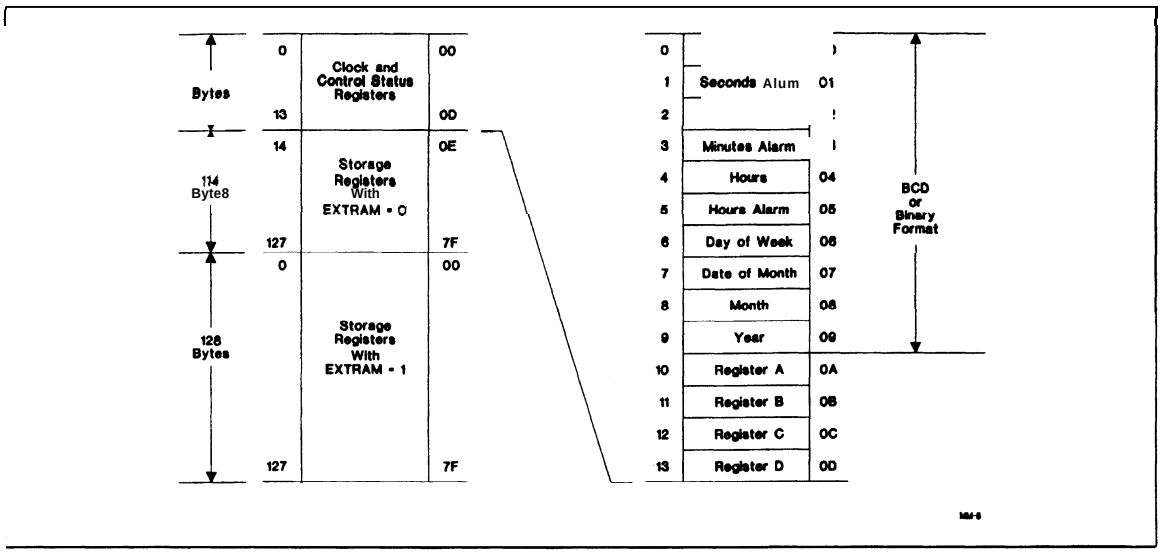


Figure 1. Address Map

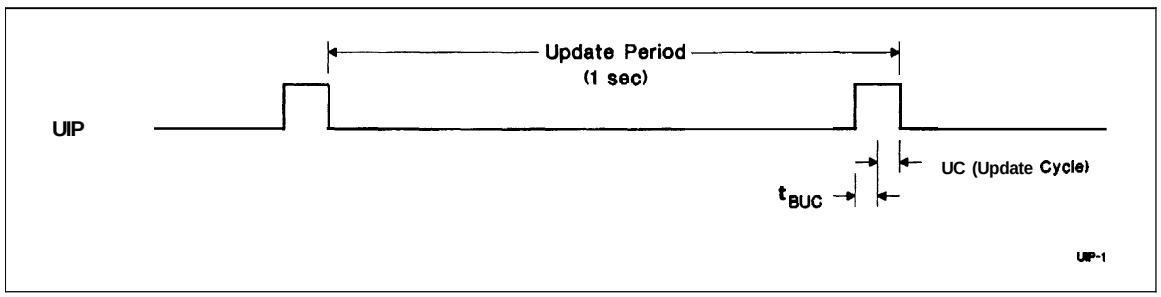


Figure 2. Update Period Timing and UIP

Programming the RTC

The time-of-day, alarm, and calendar bytes can be written in either the BCD or binary format (see Table 2).

These steps may be followed to program the time, alarm, and calendar:

1. Modify the contents of register B:
   a. Write a 1 to the UTI bit to prevent transfers between RTC bytes and user buffer.
   b. Write the appropriate value to the data format (DF) bit to select BCD or binary format for all time, alarm, and calendar bytes.
   c. Write the appropriate value to the hour format (HF) bit
2. Write new values to all the time, alarm, and calendar locations.
3. Clear the UTI bit to allow update transfers.

On the next update cycle, the RTC updates all 10 bytes in the selected format

Table 2. Time, Alarm, and Calendar Formats

Address	RTC Bytes	Range		
		Decimal	Binary	Binary-Coded Decimal
0	Seconds	0–59	00H–3BH	00H–59H
1	Seconds alarm	0–59	00H–3BH	00H–59H
2	Minutes	0-59	00H–3BH	00H–59H
3	Minutes alarm	0–59	00H–3BH	00H–59H
4	Hours, 12-hour format	1–12	01H–0CH AM; 81H–8CH PM	01H–12H AM; 81H–92H PM
	Hours, 24-hour format	0–23	00H–17H	00H–23H
5	Hours alarm, 12-hour format	1–12	01H–0CH AM, 81H–8CH PM	01H–12H AM; 81H–92H PM
	Hours alarm, 24-hour format	0–23	00H–17H	00H–23H
6	Day of week (1=Sunday)	1–7	01H–07H	01H–07H
7	Day of month	1-31	01H–1FH	01H–31H
8	Month	1–12	01H–0CH	01H–12H
9	Year	0–99	00H–63H	00H–99H

32kHz Output

The bq3285EC/LC provides for a 32.768 kHz output. For the bq3285EC, the output is always active whenever Vcc is valid (V_{PFD} + t_{CSR}). The bq3285EC output is not affected by the bit settings in Register A. Time-keeping aspects, however, still require setting OS0-OS2. The bq3285LC output is active when the oscillator is turned on by setting the OSCO-OSC2 bits in Register A.

Interrupts

The bq3285EC/LC allows three individually selected interrupt events to generate an interrupt request. These three interrupt events are:

- The periodic interrupt, programmable to occur once every 122µs to 500ms.
- The alarm interrupt, programmable to occur once per second to once per day, is active in battery-backup mode, providing a 'wake-up' feature.
- The update-ended interrupt, which occurs at the end of each update cycle.

Each of the three interrupt events is enabled by an individual interrupt-enable bit in register B. When an event occurs, its event flag bit in register C is set. If the corresponding event enable bit is also set, then an interrupt request is generated. The interrupt request flag bit (INTF) of register C is set with every interrupt request. Reading register C clears all flag bits, including INTF, and makes $\overline{INT}$ high-impedance.

Two methods can be used to process bq3285EC/LC interrupt events:

- Enable interrupt events and use the interrupt request output to invoke an interrupt service routine.
- Do not enable the interrupts and use a polling routine to periodically check the status of the flag bits.

The individual interrupt sources are described in detail in the following sections.

Table 3. Periodic Interrupt Rate

Register A Bits							Periodic Interrupt	
OSC2	OSC1	OSCO	RS3	RS2	RS1	RSO	Period	Units
0	1	0	0	0	0	0	None	
0	1	0	0	0	0	1	3.90625	ms
0	1	0	0	0	1	0	7.8125	ms
0	1	0	0	0	1	1	122.070	µs
0	1	0	0	1	0	0	244.141	µs
0	1	0	0	1	0	1	488.281	µs
0	1	0	0	1	1	0	976.5625	µs
0	1	0	0	1	1	1	1.953125	ms
0	1	0	1	0	0	0	3.90625	ms
0	1	0	1	0	0	1	7.8125	ms
0	1	0	1	0	1	0	15.625	ms
0	1	0	1	0	1	1	31.25	ms
0	1	0	1	1	0	0	62.5	ms
0	1	0	1	1	0	1	125	ms
0	1	0	1	1	1	0	250	ms
0	1	0	1	1	1	1	500	ms
0	1	1	X	X	X	X	same as above defined by RS3–RS0	

Periodic Interrupt

If the periodic interrupt event is enabled by writing a 1 to the periodic interrupt enable bit (PIE) in register C, an interrupt request is generated once every 122µs to 500ms. The period between interrupts is selected with bits RS3-RS0 in register A (see Table 3).

Alarm Interrupt

The alarm interrupt is active in battery-backup mode, providing a "wake-up" capability. During each update cycle, the RTC compares the hours, minutes, and seconds bytes with the three corresponding alarm bytes. If a match of all bytes is found, the alarm interrupt event flag bit, AF in register C, is set to 1. If the alarm event is enabled, an interrupt request is generated.

An alarm byte may be removed from the comparison by setting it to a 'don't *care*" state. An alarm byte is set to a 'don't care' state by writing a 1 to each of its two most-significant bits. A 'don't care' state may be used to select the frequency of alarm interrupt events as follows:

- If none of the three alarm bytes is 'don't care,' the frequency is once per day, when hours, minutes, and seconds match.
- If only the hour alarm byte is "don't care," the frequency is once per hour, when minutes and seconds match.
- If only the hour and minute alarm bytes are 'don't *care,"* the frequency is once per minute, when seconds match.
- If the hour, minute, and second alarm bytes are 'don't care,' the frequency is once per second.

Update Cycle Interrupt

The update cycle ended flag bit (UF) in register C is set to a 1 at the end of an update cycle. If the update interrupt enable bit (UIE) of register B is 1, and the update transfer inhibit bit (UTI) in register B is 0, then an interrupt request is generated at the end of each update cycle.

Accessing RTC bytes

The EXTRAM pin must be low to access the RTC registers. Time and calendar bytes read during an update cycle may be in error. Three methods to access the time and calendar bytes without ambiguity are:

- Enable the update interrupt event to generate interrupt requests at the end of the update cycle. The interrupt handler has a maximum of 999ms to access the clock bytes before the next update cycle begins (see Figure 3).
- Poll the update-in-progress bit (UIP) in register A. If UIP = 0, the polling routine has a minimum of t_{BUC} time to access the clock bytes (see Figure 3).
- Use the periodic interrupt event to generate interrupt requests every t_{PI} time, such that UIP = 1 always occurs between the periodic interrupts. The interrupt handler has a minimum of $t_{PI}/2 + t_{BUC}$ time to access the clock bytes (see Figure 3).

Oscillator Control

When power is first applied to the bq3285LC and V_{CC} is above V_{PFD}, the internal oscillator and frequency divider are turned on by writing a 010 pattern to bits 4 through 6 of register A. A pattern of 11X turns the oscillator on but keeps the frequency divider disabled. Any other pattern to these bits keeps the oscillator off, A pattern of 010 must be set for the bq3285EC/LC to keep time in battery backup mode.

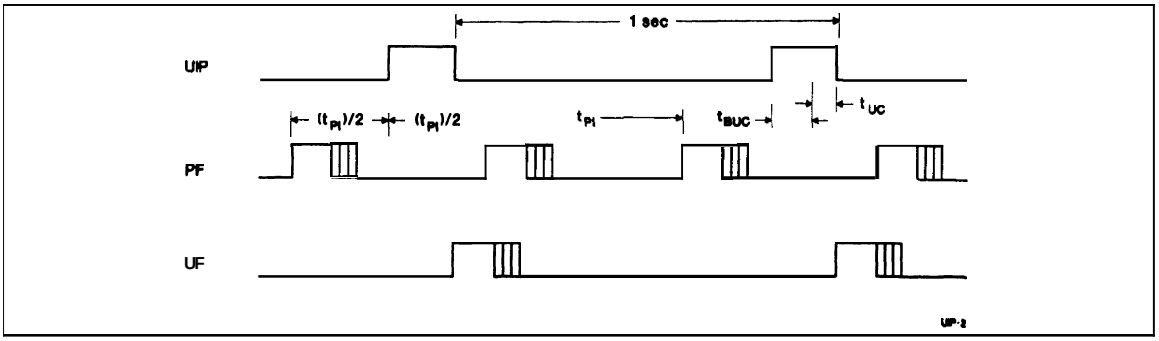


Figure 3. Update-Ended/Periodic Interrupt Relationship

Power-Down/Power-Up Cycle

The bq3285EC and bq3285LC power-up/power-down cycles are different. The bq3285LC continuously monitors V_{CC} for out-of-tolerance. During a power failure, when V_{CC} falls below V_{PFD} (2.53V typical), the bq3285LC write protects the clock and storage registers. The power source is switched to BC when V_{CC} is less than V_{PFD} and BC is greater than V_{PFD}, or when V_{CC} is less than V_{BC} and V_{BC} is less than V_{PFD}. RTC operation and storage data are sustained by a valid backup energy source. When V_{CC} is above V_{PFD}, the power source is V_{CC}. Write-protection continues for t_{CSR} time after V_{CC} rises above V_{PFD}.

The bq3285EC continuously monitors V_{CC} for out-of-tolerance. During a power failure, when V_{CC} falls below V_{PFD} (4.17V typical), the bq3285EC write-protects the clock and storage registers. When V_{CC} is below V_{BC} (3V typical), the power source is switched to BC. RTC operation and storage data are sustained by a valid backup energy source. When V_{CC} is above V_{BC}, the power source is V_{CC}. Write-protection continues for t_{CSR} time after V_{CC} rises above V_{PFD}.

Control/Status Registers

The four control/status registers of the bq3285EC/LC are accessible regardless of the status of the update cycle (see Table 4).

Register A

Register A Bits							
7	6	5	4	3	2	1	0
UIP	OS2	OS1	OS0	RS3	RS2	RS1	RS0

Register A programs:

- The frequency of the periodic event rate.
- Oscillator operation.
- Time-keeping

Register A provides:

- Status of the update cycle.

RS0–RS3 - Frequency Select

7	6	5	4	3	2	1	0
-	-	-	-	RS3	RS2	RS1	RS0

These bits select the periodic interrupt rate, as shown in Table 3.

OS0–OS2 - Oscillator Control

7	6	5	4	3	2	1	0
-	OS2	OS1	OS0	-	-	-	-

These three bits control the state of the oscillator and divider stages. A pattern of 010 or 011 enables RTC operation by turning on the oscillator and enabling the frequency divider. This pattern must be set to turn the oscillator on for the bq3285LC and to ensure that the bq3285EC/LC will keep time in battery-backup mode. A pattern of 11X turns the oscillator on, but keeps the frequency divider disabled. When 010 is written, the begins its first update after 500ms.

UIP - Update Cyck Status

7	6	5	4	3	2	1	0
UIP	-	-	-	-	-	-	-

This read-only bit is set prior to the update cycle. When UIP equals 1, an RTC update cycle may be in progress. UIP is cleared at the end of each update cycle. This bit is also cleared when the update transfer inhibit (UTI) bit in register B is 1.

Table 4. Control/Status Registers

Reg.	Loc. (Hex)	Read	Write	Bit Name and State on Reset													
				7 (MSB)		6		5		4		3		2		1	0 (LSB)
A	0A	Yes	Yes[1]	UIP	na	OS2	na	OS1	na	OS0	na	RS3	na	RS2	na	RS1	na	RS0	na
B	0B	Yes	Yes	UTI	na	PIE	0	AIE	0	UIE	0	-	0	DF	na	HF	na	DSE	na
C	0C	Yes	No	INTF	0	PF	0	AF	0	UF	0	-	0	-	na	-	0	-	0
D	0D	Yes	No	VRT	na	-	0	-	0	-	0	-	0	-	0	-	0	-	0

Notes: na = not affected.

1. Except bit 7.

Register B

Register B Bits							
7	6	5	4	3	2	1	0
UTI	PIE	AIE	UIE	-	DF	HF	DSE

Register B enables:

- Update cycle transfer operation
- Interrupt events
- Daylight saving adjustment

Register B selects:

- Clock and calendar data formats

All bits of register B are **read/write.**

Bit 3 - **Unused Bit.**

DSE - Daylight Saving Enable

7	6	5	4	3	2	1	0
						-	DSE

This bit enables daylight-saving time adjustments when written to 1:

- On the last Sunday in October, the first time the bq3285EC/LC increments past 1:59:59 AM, the time falls back to 1:00:00 AM.
- On the first Sunday in April, the time springs forward from 2:00:00 AM to 3:00:00 AM.

HF - Hour Format

7	6	5	4	3	2	1	0
					-	HF	-

This bit selects the time-of-day and alarm hour format:

1 = 24-hour format

0 = 12-hour format

DF - Data Format

7	6	5	4	3	2	1	0
				-	DF	-	-

This bit selects the numeric format in which the time, alarm, and calendar bytes are represented:

1 = Binary

0 = BCD

UIE - Update Cycle Interrupt Enable

7	6	5	4	3	2	1	0
-	-	-	UIE	-	-	-	-

This bit enables an interrupt request due to an update ended interrupt event:

1 = Enabled

0 = Disabled

The UIE bit is automatically cleared when the UTI bit equals 1.

AIE - Alarm Interrupt Enable

7	6	5	4	3	2	1	0
-	-	AIE	-	-	-	-	-

This bit enables an interrupt request due to an alarm interrupt event:

1 = Enabled

0 = Disabled

PIE - Periodic Interrupt Enable

7	6	5	4	3	2	1	0
-	PIE	-	-	-	-	-	-

This bit enables an interrupt request due to a periodic interrupt event:

1 = Enabled

0 = Disabled

UTI - Update Transfer Inhibit

7	6	5	4	3	2	1	0
UTI	-	-	-	-	-	-	-

This bit inhibits the transfer of RTC bytes to the user buffer:

1 = Inhibits transfer and clears UIE

0 = Allows transfer

5

Register C

Register C Bits							
7	6	5	4	3	2	1	0
INTF	PF	AF	UF	0	-	0	0

Register C is the read-only event status register.

Bits 0, 1, 2, 3 - Unused Bits

7	6	5	4	3	2	1	0
-	-	-	-	0	-	0	0

These bits are always set to 0.

UF - Update Event Flag

7	6	5	4	3	2	1	0
-	-	-	UF	-	-	-	-

This bit is set to a 1 at the end of the update cycle. Reading register C clears this bit.

AF - Alarm Event Flag

7	6	5	4	3	2	1	0
-	-	AF	-	-	-	-	-

This bit is set to a 1 when an alarm event occurs. Reading register C clears this bit.

PF - Periodic Event Flag

7	6	5	4	3	2	1	0
-	PF	-	-	-	-	-	-

This bit is set to a 1 every t_{PI} time, where t_{PI} is the time period selected by the settings of RS0–RS3 in register A. Reading register C clears this bit.

INTF - interrupt Request Flag

7	6	5	4	3	2	1	0
INTF	-	-	-	-	-	-	-

This flag is set to a 1 when any of the following is true:

AIE = 1 and AF = 1

PIE = 1 and PF = 1

UIE = 1 and UF = 1

Reading register C clears this bit.

Register D

Register D Bits							
7	6	5	4	3	2	1	0
VRT	0	0	0	0	0	0	0

Register D is the read-only data integrity status register.

Bits 0–6 - Unuwd Bits

7	6	5	4	3	2	1	0
-	0	0	0	0	0	0	0

These bits are always set to 0.

VRT - Valid RAM and Time

7	6	5	4	3	2	1	0
VRT	-	-	-	-	-	-	-

1 = Valid backup energy source

0 = Backup energy source is depleted

When the backup energy source is depleted (VRT = 0), data integrity of the RTC and storage registers is not guaranteed.

Absolute Maximum Ratings—bq3285EC

Symbol	Parameter	Value	Unit	Conditions
Vcc	DC voltage applied on Vcc relative to Vss	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding Vcc relative to Vss	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
T_{STG}	Storage temperature	-55 to +125	°C	
T_{BIAS}	Temperature under bias	-40 to +85	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may *affect* device reliability.

5

Absolute Maximum Ratings—bq3285LC

Symbol	Parameter	Value	Unit	Conditions
Vcc	DC voltage applied on Vcc relative to Vss	-0.3 to 7.0	V	
VT	DC voltage applied on any pin excluding Vcc relative to Vss	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
T_{STG}	Storage temperature	-55 to +125	°C	
T_{BIAS}	Temperature under bias	-40 to +85	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may *affect* device reliability.

Recommended DC Operating Conditions—bq3285EC ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IL}	Input low voltage	-0.3		0.8	V
V_{IH}	Input high voltage	2.2		V_{CC} + 0.3	V
V_{BC}	Backup cell voltage	2.4		4.0	V

Note: Typical values indicate operation at T_A = 25°C.

Recommended DC Operating Conditions—bq3285LC ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{CC}	Supply voltage	2.7	3.0	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IL}	Input low voltage	-0.3		0.6	V
V_{IH}	Input high voltage	2.2		V_{CC} + 0.3	V
V_{BC}	Backup cell voltage	2.4		4.0	V

Note: Typical values indicate operation at T_A = 25°C.

Crystal Specifications—bq3285EC/LC (DT-26 or Equivalent)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
f_O	Oscillation frequency		32.768		kHz
C_L	Load capacitance		6		pF
T_P	Temperature turnover point	20	25	30	°C
k	Parabolic curvature constant			-0.042	ppm/°C
Q	Quality factor	40,000	70,000		
R_1	Series resistance			45	KΩ
C_0	Shunt capacitance		1.1	1.8	pF
C_0/C_1	Capacitance ratio		430	600	
D_L	Drive level			1	µW
$\Delta f/f_O$	Aging (first year at 25°C)		1		ppm

DC Electrical Characteristics—bq3285EC ($T_A = T_{OPR}$, V_{CC} = 5V +-0H HÇæ 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current			± 1	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current			± 1	µA	AD_0–AD_7 and $\overline{INT}$ in high impedance, $V_{OUT} = V_{SS}$ to V_{CC}
V_{OH}	Output high voltage	2.4			V	I_{OH} = -2.0mA
V_{OL}	Output low voltage			0.4	V	I_{OL} = 4.0 mA
I_{CC}	Operating supply current		7	15	mA	Min. cycle, duty = 100%, I_{OH} = 0mA, I_{OL} = 0mA
I_{CCSB}	Standby supply current		300		µA	$\overline{V_{IN}} = V_{SS}$ or V_{CC}, $\overline{CS} \geq V_{CC}$ - 0.2
V_{SO}	Supply switch-over voltage		V_{BC}		V	
I_{CCB}	Battery operation current		0.3	0.5	µA	V_{BC} = 3V, T_A = 25°C
V_{PFD}	Power-fail-detect voltage	4.0	4.17	4.35	V	
I_{RCL}	Input current when $\overline{RCL} = V_{SS}$.			185	µA	Internal 30K pull-up
I_{MOTH}	Input current when MOT = V_{CC}			-185	µA	Internal 30K pull-down
	Input current when MOT = V_{SS}			0	µA	Internal 30K pull-down
I_{XTRAM}	Input current when EXTRAM = V_{CC}			-185	µA	Internal 30K pull-down
	Input current when EXTRAM = V_{SS}			0	µA	Internal 30K pull-down

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC} = 3V.

5

DC Electrical Characteristics—bq3285LC ($T_A = T_{OPR}$, V_{CC} = 3V)

Symbol	Parameter	Minimum	Typical[1]	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current			±1	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current			±1	µA	AD_0–AD_7 and $\overline{INT}$ in high impedance, $V_{OUT} = V_{SS}$ to V_{CC}
V_{OH}	Output high voltage	2.2			V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage			0.4	V	I_{OL} = 2.0 mA
I_{CC}	Operating supply current		5[2]	9	mA	Min. cycle, duty = 100%, I_{OH} = 0mA, I_{OL} = 0mA
I_{CCSB}	Standby supply current	-	100[3]	-	µA	$\overline{CS} \geq V_{SS}$ -0.2V_{CC},
V_{SO}	Supply switch-over voltage		V_{PFD}		V	$V_{BC} > V_{PFD}$
			V_{BC}		V	$V_{BC} < V_{PFD}$
I_{CCB}	Battery operation current	-	0.3	0.5	µA	V_{BC} = 3V, T_A = 25°C, $V_{CC} < V_{BC}$
V_{PFD}	Power-fail-detect voltage	2.4	2.53	2.65	V	
I_{RCL}	Input current when $\overline{RCL}$ = Vss.			120	µA	Internal 30K pull-up
I_{MOTH}	Input current when MOT = Vcc			-120	µA	Internal 30K pull-down
	Input current when MOT = V_{SS}	-	-	0	µA	Internal 30K pull-down
I_{XTRAM}	Input current when EXTRAM = V_{CC}	-	-	-120	µA	Internal 30K pull-down
	Input current when EXTRAM = V_{SS}			0	µA	Internal 30K pull-down

Note: 1. Typical values indicate operation at T_A = 25°C, V_{CC} = 3V.

2. 7mA at Vcc = 5V

3. 300µA at Vcc = 5V

Capacitance—bq3285EC/LC (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance			7	pF	V_{OUT} = 0V
C_{IN}	Input capacitance			5	pF	V_{IN} = 0V

Note: This parameter is sampled and not 100% tested. It does not include the X1 or X2 pin.

AC Test Conditions—bq3285EC

Parameter	Test Conditions
Input pulse levels	0 to 3.0 V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 4 and 5

5

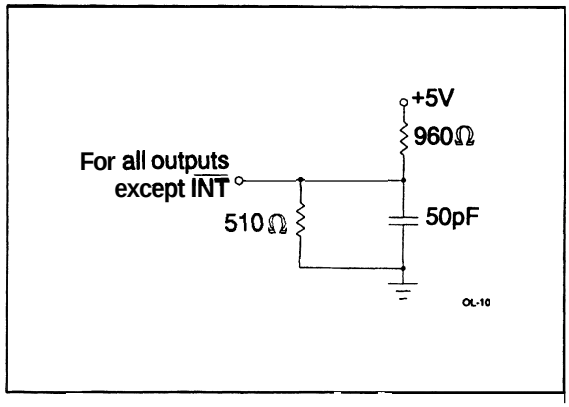


Figure 4. Output Load--bq3285EC

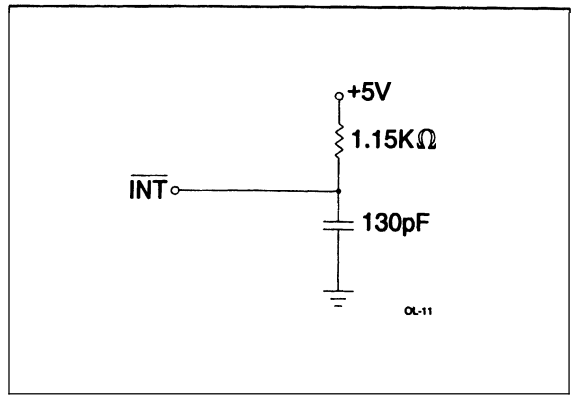


Figure 5. Output Load--bq3285EC

AC Test Conditions—bq3285LC

Parameter	Test Conditions
Input pulse levels	0 to 2.3 V, V_{CC} = 3V[1]
Input rise and fall times	5 ns
Input and output timing reference levels	1.2 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 6 and 7

Note: 1. For 5V timing, please refer to bq3285EC.

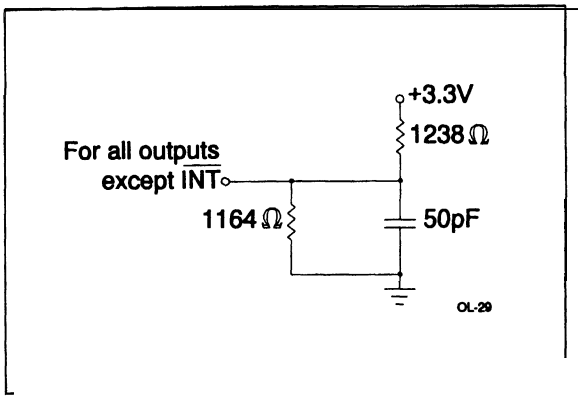


Figure 6. Output Load--bq3285LC

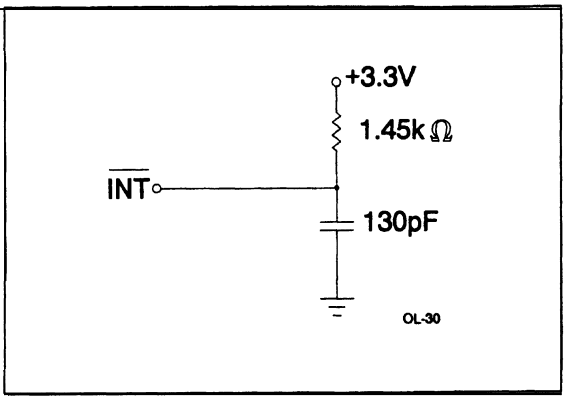


Figure 7. Output Load B--bq3285LC

Read/Write Timing—bq3285EC ($T_A = T_{OPR}$, $V_{CC} = 5V \pm 10\%$)

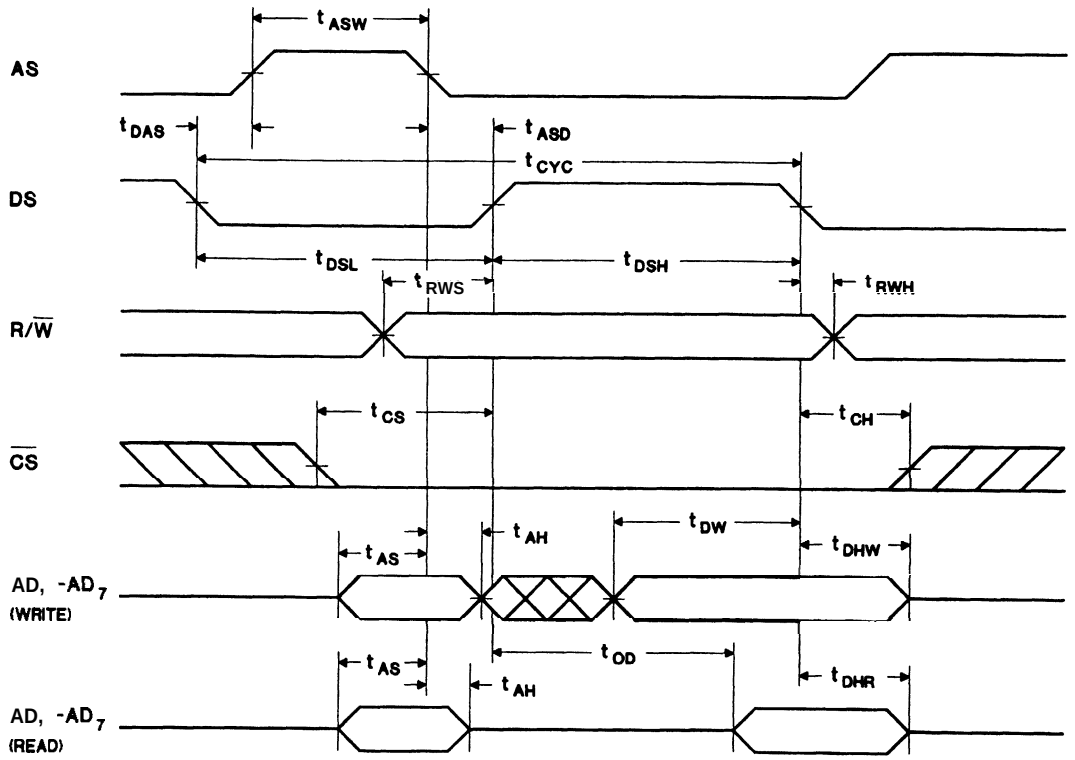
Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYC}	Cycle time	160			ns	
t_{DSL}	DS low or $\overline{RD}/\overline{WR}$ high time	80			ns	
t_{DSH}	DS high or $\overline{RD}/\overline{WR}$ low time	55			ns	
t_{RWH}	R/$\overline{W}$ hold time	0			ns	
t_{RWS}	R/$\overline{W}$ setup time	10			ns	
t_{CS}	Chip select setup time	5			ns	
t_{CH}	Chip select hold time	0			ns	
t_{DHR}	Read data hold time	0		25	ns	
t_{DHW}	Write data hold time	0			ns	
t_{AS}	Address setup time	20			ns	
t_{AH}	Address hold time	5			ns	
t_{DAS}	Delay time, DS to AS rise	10			ns	
t_{ASW}	Pulse width, AS high	30			ns	
t_{ASD}	Delay time, AS to DS rise	35			ns	
	Output data delay time from DS rise ($\overline{RD}$ fall)			50	ns	
t_{DW}	Write data setup time	30			ns	
t_{BUC}	Delay time before update cycle		244		µs	
t_{PI}	Periodic interrupt time interval					See Table 3
t_{UC}	Time of update cycle	-	1	-	µs	

5

Read/Write Timing—bq3285LC (T_A = TOPR, VCC = 3V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYC}	Cycle time	270			ns	
t_{DSL}	DS low or $\overline{RD}/\overline{WR}$ high time	135			ns	
t_{DSH}	DS high or $\overline{RD}/\overline{WR}$ low time	90			ns	
t_{RWH}	R/$\overline{W}$ hold time	0			ne	
t_{RWS}	R/$\overline{W}$ setup time	15			ne	
t_{CS}	Chip select setup time	8			ns	
t_{CH}	Chip select hold time	0			ns	
t_{DHR}	Read data hold time	0		40	ns	
t_{DHW}	Write data hold time	0			ne	
t_{AS}	Address setup time	30			ns	
t_{AH}	Address hold t i e	15			ne	
t_{DAS}	Delay time, DS to AS rise	15			ns	
t_{ASW}	Pulse width, AS high	50			ns	
t_{ASD}	Delay time, AS to DS rise ($\overline{RD}/\overline{WR}$ fall)	55			ne	
t_{OD}	Output data delay time from DS rise ($\overline{RD}$ fall)			100	ns	
t_{DW}	Write data setup t i e	50			ns	
t_{BUC}	Delay time before update cycle		244		µs	
t_{PI}	Periodic interrupt time interval					See Table 3
t_{UC}	Time of update cycle		1		µs	

Motorola Bus **Read/Write** Timing bq3285EC/LC



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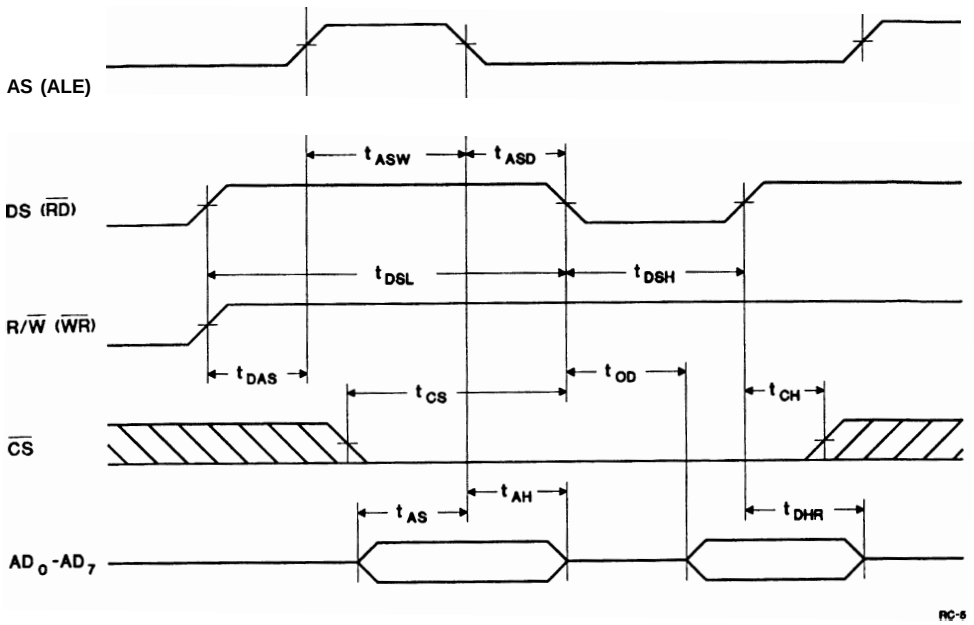
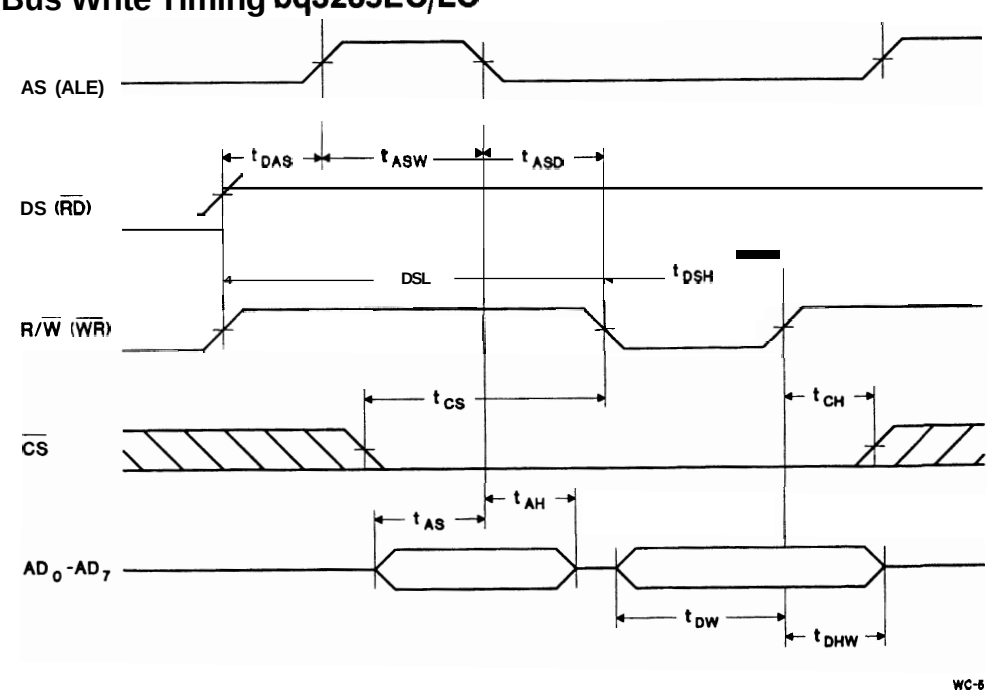
Intel Bus Read Timing bq3285EC/LC



Intel Bus Write Timing bq3285EC/LC

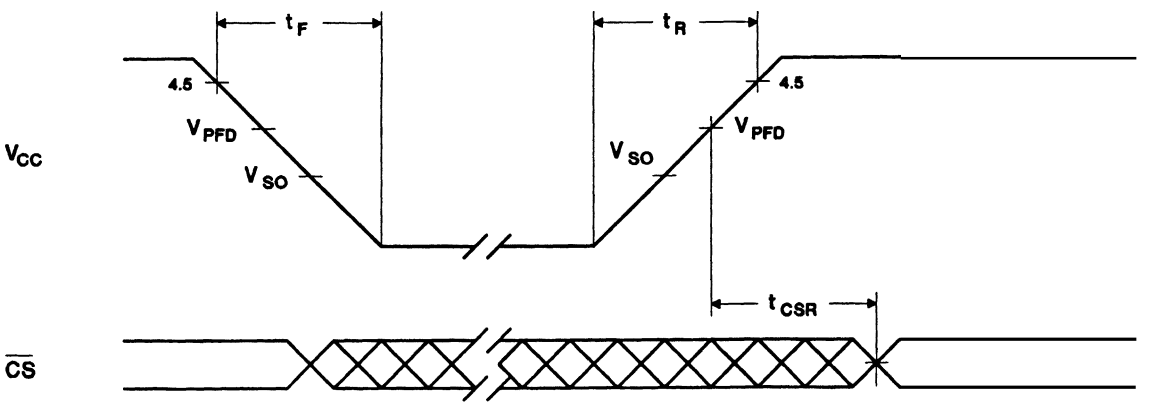


Power-Down/Power-Up Timing—bq3285EC ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_F	V_{CC} slew from 4.5V to 0V	300			µs	
t_R	V_{CC} slew from 0V to 4.5V	100			µs	
t_{CSR}	$\overline{CS}$ at V_{IH} after power-up	20		200	ms	Internal write-protection period after V_{CC} passes V_{PFD} on power-up.

Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

Power-Down/Power-Up Timing bq3285EC



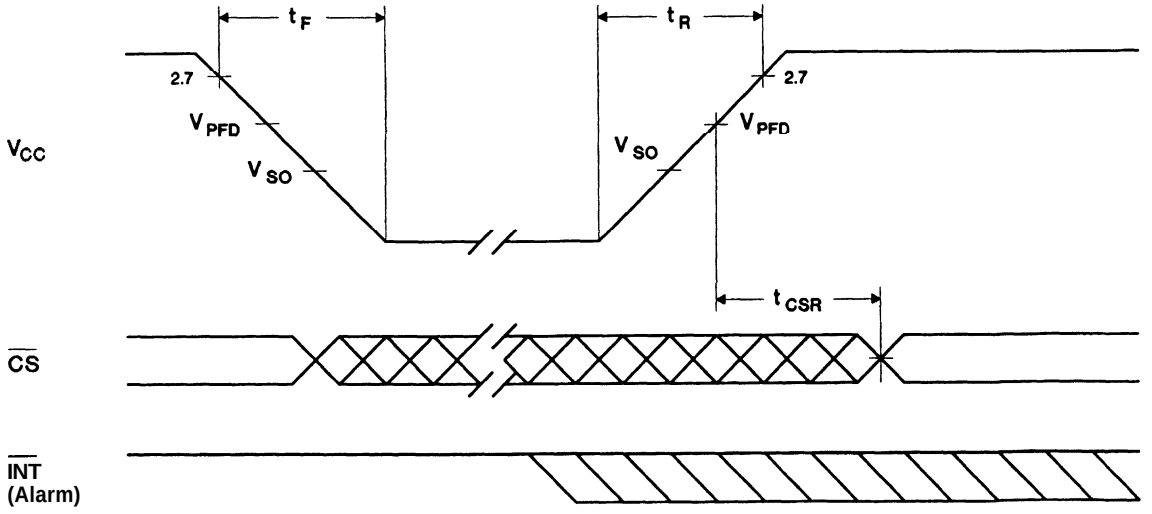
PD-4A

Power-Down/Power-Up Timing—bq3285LC (TA = TOPR)

Symbd	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_F	V_{CC} slew from 2.W to 0V	300			µs	
t_R	V_{CC} slew from 0V to 2.W	100			µs	
t_{CSR}	$\overline{CS}$ at V_{IH} after power-up	20		200	ms	Internal write-protection period after VCC passes V_{PFD} on power-up.

Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

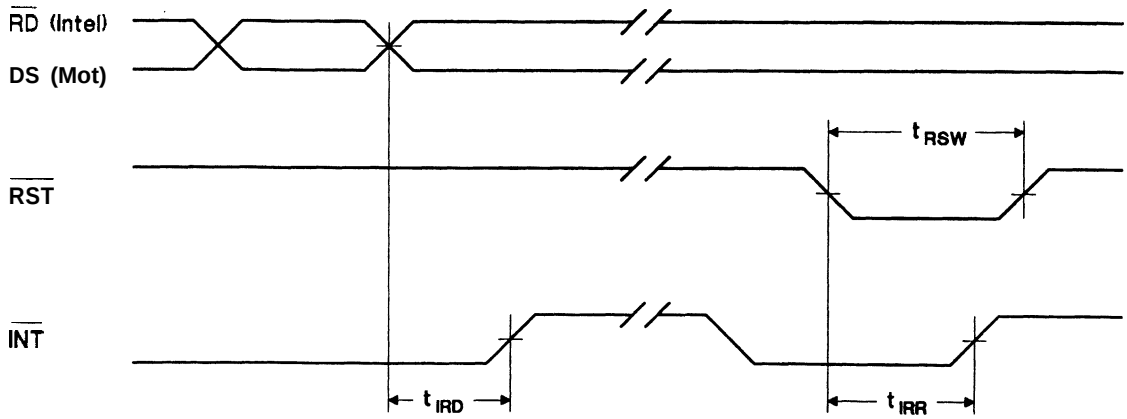
Power-Down/Power-Up Timing bq3285LC



Interrupt Delay Timing—bq3285EC/LC ($T_A = T_{OPR}$)

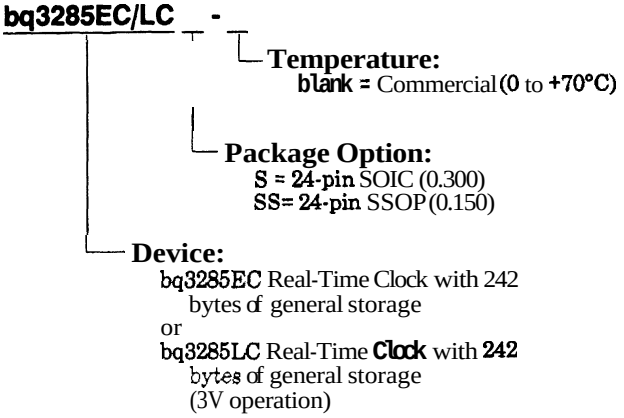
Symbol	Parameter	Minimum	Typical	Maximum	Unit
t_{RSW}	Reset pulse width	5			µs
t_{IRR}	$\overline{INT}$ release from $\overline{RST}$			2	µs
t_{IRD}	$\overline{INT}$ release from DS			2	µs

Interrupt Delay Timing bq3285EC/LC



INT-1

Ordering Information



bq3287/bq3287A

Real-Time Clock (RTC) Module

Features

- Direct clock/calendar replacement for IBM® AT-compatible computers and other applications
- Functionally compatible with the DS1287/DS1287A and MC146818A
- 114 bytes of general nonvolatile storage
- ➤ Integral lithium cell and crystal
- ➤ 160 ns cycle time allows fast bus operation
- ➤ Selectable Intel or Motorola bus timing
- ➤ 14 bytes for clock/calendar and control
- BCD or binary format for clock and calendar data
- Time of day in seconds, minutes, and hours
  - 12- or 24-hour format
  - Optional daylight saving adjustment
- ➤ Calendar in day of the week, day of the month, months, and years with automatic leap-year adjustment
- Programmable square wave output
- Three individually maskable interrupt event flags:
  - Periodic rates from 122 µs to 500 ms
  - Time-of-day alarm once per second to once per day
  - End-of-clock update cycle
- Better than one minute per month clock accuracy

General Description

The CMOS bq3287/bq3287A is a low-power microprocessor peripheral providing a time-of-day clock and 100-year calendar with alarm features and battery operation. Other features include three maskable interrupt sources, square-wave output, and 114 bytes of general nonvolatile storage. The bq3287A version is identical to the bq3287, with the addition of the RAM clear input.

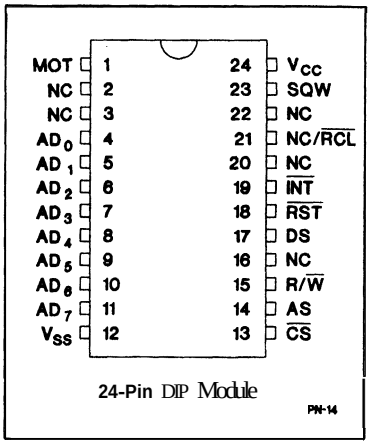
The bq3287 is a fully compatible real-time clock for IBM AT-compatible computers and other applications. The bq3287 write-protects the clock, calendar, and storage registers during power failure. The integral backup energy source then maintains data and operates the clock and calendar.

As shipped from Benchmarq, the real time clock is turned off to maximize battery capacity for in-system operation.

The bq3287 is functionally equivalent to the bq3285, except that the battery (16, 20) and crystal (2, 3) pins are not accessible. These pins are connected internally to a coin cell and quartz crystal. The coin cell is sized to provide 10 years of data retention and clock operation in the absence of power. For a complete description of features, operating conditions, electrical characteristics, bus timing, and pin descriptions, see the bq3285 data sheet.

5

Pin Connections



24-Pin DIP Module

PN-14

Pin Names

AD0-AD7	Multiplexed address/data input/output
MOT	Bus type select input
$\overline{CS}$	Chip select input
AS	Address strobe input
DS	Data strobe input
R/$\overline{W}$	Read/write input
$\overline{INT}$	Interrupt request output
$\overline{RST}$	Reset input
SQW	Square wave output
NC	No connect
$\overline{RCL}$	RAM clear input (bq3287A only)
Vcc	+5V supply
Vss	Ground

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on Vcc relative to Vss	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding Vcc relative to Vss	-0.3 to 7.0	V	$V_T \le V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
		-20 to +70	°C	Extended "I"
T_{STG}	Storage temperature	-40 to +70	°C	Commercial
		40 to +70	°C	Extended "I"
T_{BIAS}	Temperature under bias	-10 to +70	°C	Commercial
		-20 to +70	°C	Extended T
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings are** exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions (T_A = TOPR)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
Vcc	Supply voltage	4.5	5.0	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IL}	Input low voltage	-0.3		0.8	V
V_{IH}	Input high voltage	2.2		Vcc + 0.3	V

Note: Typical values indicate operation at T_A = 25°C.

DC Electrical Characteristics (T_A = TOPR, VCC = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current			± 1	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current			± 1	µA	AD_0–AD_7, $\overline{INT}$ and SQW in high impedance
V_{OH}	Output high voltage	2.4			V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage			0.4	V	I_{OL} = 4.0 mA
I_{CC}	Operating supply current		7	15	mA	Min. cycle, duty = 100%, I_{OH} = 0mA, I_{OL} = 0mA
V_{SO}	Supply switch-over voltage		3.0		V	
V_{PFD}	Power-fail-detect voltage	4.0	4.17	4.35	V	
I_{RCL}	Input current when $\overline{RCL}$ = V_{SS}			185	µA	Internal 30K pull-up (bq3287A only)
I_{MOTH}	Input current when MOT = V_{CC}			-185	µA	Internal 30K pull-down

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.

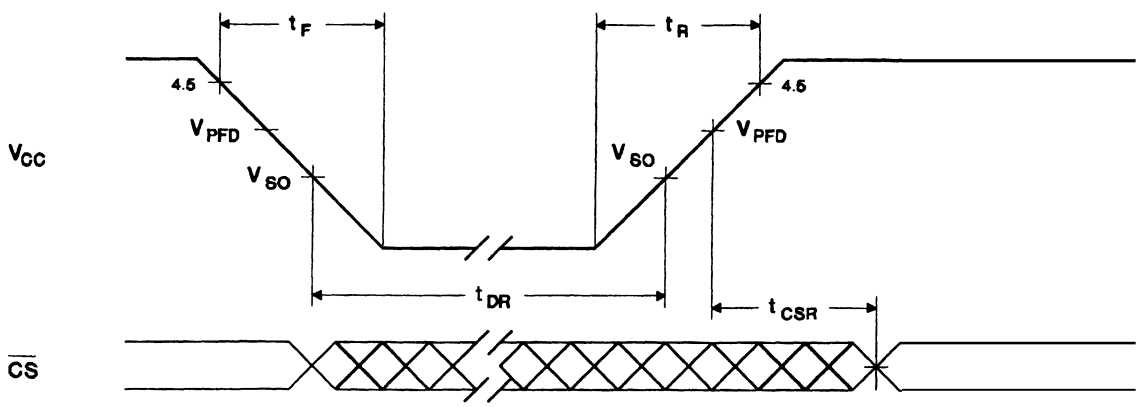
Power-Down/Power-Up Timing ($T_A = T_{OPR}$)

Symbd	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_F	V_{CC} slew from 4.5V to 0V	300			µs	
t_R	V_{CC} slew from 0V to 4.5V	100			µs	
t_{CSR}	$\overline{CS}$ at V_{IH} after power-UP	20		200	ms	Internal write-protection period after V_{CC} passes V_{PFD} on power-up.
t_{DR}	Data-retention and timekeeping time	10			years	T_A = 25°C.

Note: Clock accuracy is better than ± 1 minute per month at 25°C for the period of t_{DR}.

Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

Power-Down/Power-Up Timing



PD-4

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	1	Address strobe input	Clarification
1	2	Power-fail detect voltage V_{PFD}	Was 4.1 min, 4.25 max; is 4.0 min, 4.35 max
2	1	Was : "As shipped from Benchmarq, the backup cell is electrically isolated from the memory." Is: "As shipped from Benchmarq, the backup cell is electrically isolated from the active circuitry."	Clarification
2	2, 4	Changed temperature from N (industrial, -40 to +85°C) to I (extended, -20 to +70°C)	Specification change
3	2	I_{RCL} max. was 275; is now 185. Pull-up = 30K I_{MOTH} max. was -275; is now -185. Pull-down = 30K	Changed values

Note: Change 1 = Nov. 1992 B changes from June 1991 A.
Change 2 = Nov. 1995 C changes from Nov. 1992 B.
Change 3 = Sept. 1996 D changes from Nov. 1995 C

Ordering Information

bq3287 MT -

'Temperature:
blank = Commercial (0 to +70°C)
I = Extended* (-20 to +70°C)

Package Option:
MT = T-type module

RAM Clear Option:
A = RAM clear on pin 21
no mark = No connect on pin 21

Device:
bq3287 Real-Time Clock Module

'Contact factory for availability.

bq3287E/bq3287EA

Real-Time Clock (RTC) Module

Features

- Direct clock/calendar replacement for IBM® AT-compatible computers and other applications
- Functionally compatible with the DS1287/DS1287A and MC146818A/MC146818B
- 242 bytes of general nonvolatile storage
- Provides a 32.768kHz output for power management
- System wake-up capability—alarm interrupt active in battery-backup mode
- Integral lithium cell and crystal
- 160 ns cycle time allows fast bus operation
- 14 bytes for clock/calendar and control
- Time of day in seconds, minutes, and hours
  - 12- or 24-hour format
  - Optional daylight saving adjustment
- Calendar in day of the week, day of the month, months, and years with automatic leap-year adjustment
- Programmable square wave output
- Three individually maskable interrupt event flags:
  - Periodic rates from 122 µs to 500 ms
  - Time-of-day alarm once per second to once per day
  - End-of-clock update cycle
- Better than one minute per month clock accuracy

General Description

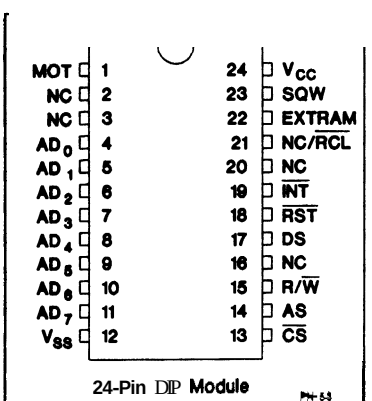
The CMOS bq3287E/bq3287EA is a low-power microprocessor peripheral providing a time-of-day clock and 100-year calendar with alarm features and battery operation. Other features include three maskable interrupt sources, square-wave output, and 242 bytes of general nonvolatile storage. A 32.768kHz output is available for sustaining power-management activities. Wake-up capability is provided by an alarm interrupt, which is active in battery-backup mode. The bq3287EA version is identical to the bq3287E, with the addition of the RAM clear input.

The bq3287E is a fully compatible real-time clock for IBM AT-compatible computers and other applications. The bq3287E write-protects the clock, calendar, and storage registers during power failure. The integral backup energy source then maintains data and operates the clock and calendar.

As shipped from Benchmarq, the real time clock is turned off to maximize battery capacity for in-system operation.

The bq3287E is functionally equivalent to the bq3285E, except the battery (16,20) and @ pins (2,3) are not accessible. These pine are connected internally to a coin cell and quartz *crystal.* The coin cell is sized to provide 10 years of data retention and clock operation in the absence of power. For a complete description of features, operating conditions, electrical characteristics, bus timing, and pin descriptions, see the bq3285E data sheet.

Pin Connections



24-Pin DIP Module PN-53

Pin Names

AD0-AD7	Multiplex address/data input/output
MOT	
CS	Chip select input
AS	Address strobe input
DS	Data strobe input
R/W	Read/write input
INT	Interrupt request output
RST	Reset input
SQW	Square wave output
EXTRAM	Extended RAM enable
NC	No connect
RCL	RAM clear input (bq3287EA only)
Vcc	+5V supply
Vss	Ground

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on Vcc relative to Vss	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding Vcc relative to Vss	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
T_{STG}	Storage temperature	-40 to +70	°C	Commercial
T_{BIAS}	Temperature under bias	-10 to +70	°C	Commercial
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IL}	Input low voltage	-0.3		0.8	V
V_{IH}	Input high voltage	2.2		Vcc + 0.3	V

Note: Typical values indicate operation at $T_A = 25°C$.

DC Electrical Characteristics (T_A = TOPR, VCC = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current			± 1	µA	V_{IN} = Vss to Vcc
I_{LO}	Output leakage current			± 1	µA	AD_0–AD_7, $\overline{INT}$ and SQW in high impedance
V_{OH}	Output high voltage	2.4			V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage			0.4	V	I_{OL} = 4.0 mA
I_{CC}	Operating supply current		7	15	mA	Min. cycle, duty = 100%, I_{OH} = 0mA, I_{OL} = 0mA
Vso	Supply switch-over voltage		3.0		V	
V_{PFD}	Power-fail-detect voltage	4.0	4.17	4.35	V	
I_{RCL}	Input current when $\overline{RCL}$ = V_{SS}			185	µA	Internal 30K pull-up (bq3287EA only)
I_{MOTH}	Input current when MOT = V_{CC}			-185	µA	Internal 30K pull-down
I_{XTRAM}	Input current when EXTRAM = Vcc			-185	µA	Internal 30K pull-down

Note: Typical values indicate operation at $T_A = 25°C$, V_{CC} = 5V.

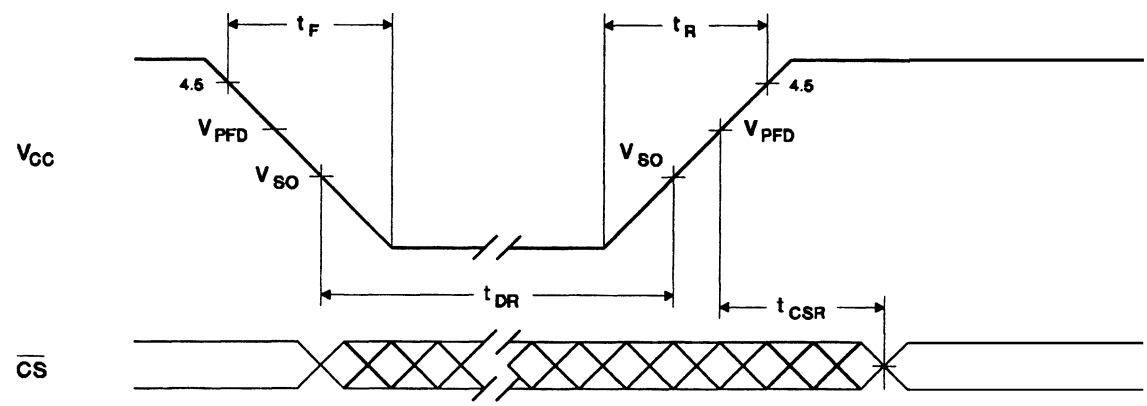
Power-Down/Power-Up Timing (T_A = T_{OPR})

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_F	V_{CC} slew from 4.5V to 0V	300			µs	
t_R	V_{CC} slew from 0V to 4.5V	100			µs	
t_{CSR}	$\overline{CS}$ at V_{IH} after power-up	20	-	200	ms	Internal write-protection period after V_{CC} passes V_{PFD} on power-up.
t_{DR}	Data-retention and timekeeping time	10			years	T_A = 25°C.

Note: Clock accuracy is better than ± 1 minute per month at 25°C for the period of t_{DR}.

Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

Power-Down/Power-Up Timing



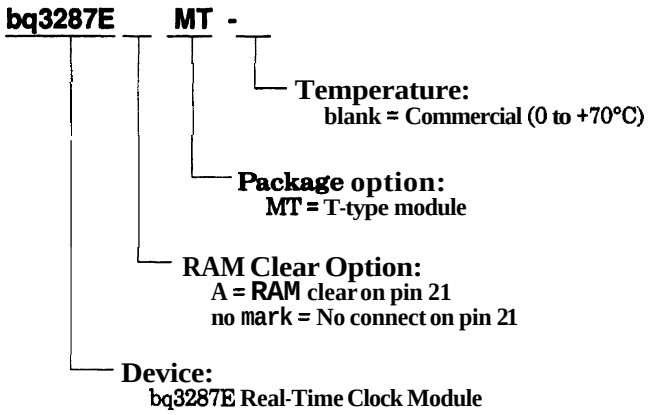
PD-4

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	8	Register C, bit 2	Was 0; is na (not affected)
2	2	I_{RCL} max. was 275; is now 185. Pull-down= 30K.	Value change
2	2	I_{XTRAM} max. was -75; is now -185.	Value change

Note: Change 1 = Apr. 1994 B "Final" changes from Dec. 1993 A "Preliminary."
Change 2 = Sept. 1996 C changes from April 1994 B.

Ordering Information



Real-Time Clock (RTC) With NVRAM Control

Features

- Direct clock/calendar replacement for IBM® AT-compatible computers and other applications
- Functionally compatible with the DS1285
  - Closely matches MC146818A pin configuration
- 114 bytes of general nonvolatile storage
- ➤ Automatic backup and write-protect control to external SRAM
- 160 ns cycle time allows fast bus operation
- Selectable Intel or Motorola bus timing (PLCC), Intel bus timing (DIP and SOIC)
- Less than 0.5 µA load under battery operation
- 14 bytes for clock/calendar and control
- Calendar in day of the week, day of the month, months, and years, with automatic leap-year adjustment
- Time of day in seconds, minutes, and hours
  - 12- or 24-hour format
  - Optional daylight saving adjustment
- BCD or binary format for clock and calendar data
- ➤ Programmable square wave output
- Three individually maskable interrupt event flags:
  - Periodic rates from 122 µs to 500 ms
  - Time-of-day alarm once per second to once per day
  - End-of-clock update cycle
- ➤ 24-pin plastic DIP or SOIC and 28-pin PLCC

General Description

The CMOS bq4285 is a low-power microprocessor peripheral providing a time-of-day clock and 100-year calendar with alarm features and battery operation. Other features include three maskable interrupt sources, square wave output, and 114 bytes of general nonvolatile storage.

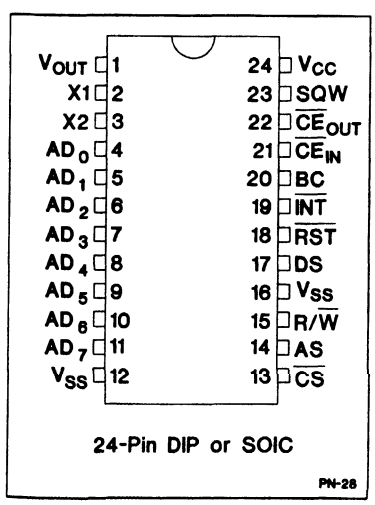
The bq4285 write-protects the clock, calendar, and storage registers during power failure. A backup battery then maintains data and operates the clock and calendar.

The bq4285 is a fully compatible real-time clock for IBM AT-compatible computers and other applications. The only external components are a 32.768kHz crystal and a backup battery.

The bq4285 integrates a battery-backup controller to make a standard CMOS SRAM nonvolatile during power-fail conditions. During power-fail, the bq4285 automatically write-protects the external SRAM and provides a V_{CC} output sourced from the clock backup battery.

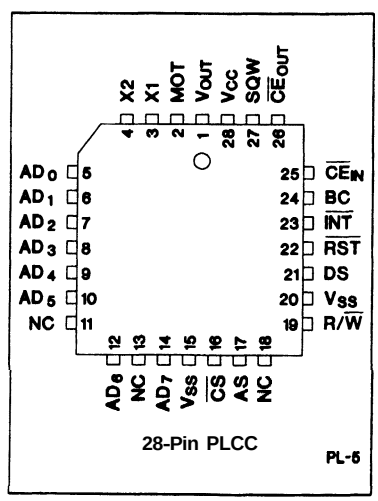
5

Pin Connections



24-Pin DIP or SOIC

PN-28

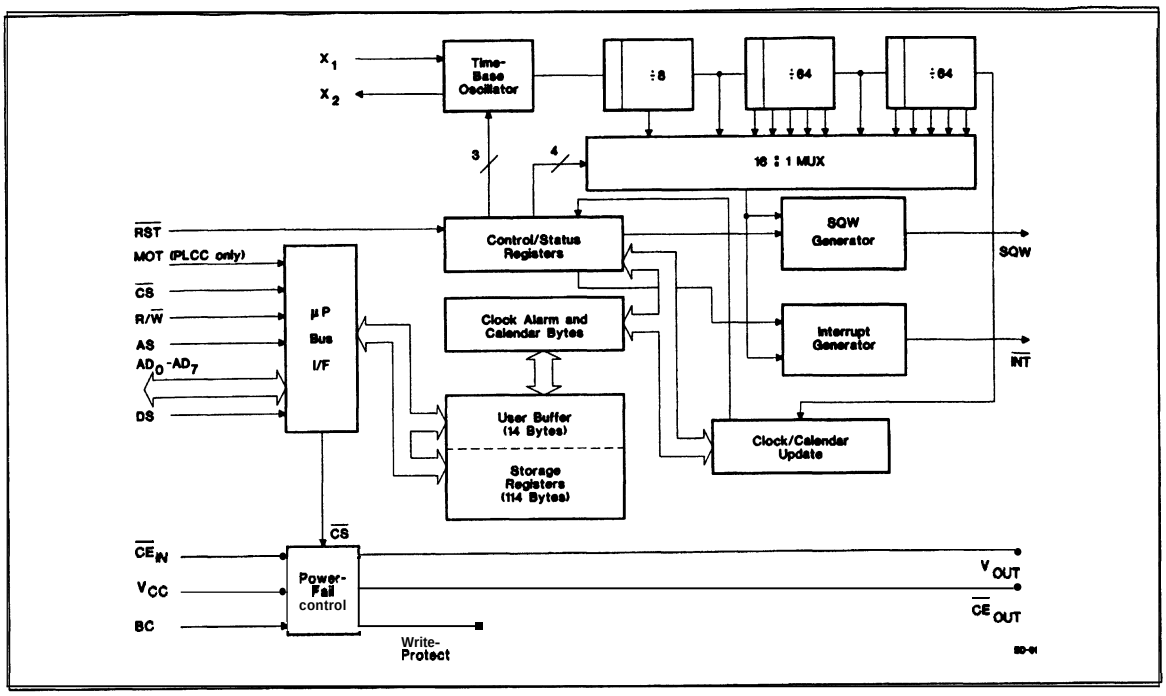


28-Pin PLCC

PL-5

Pin Names

AD0-AD7	Multiplexed address/data input/output
MOT	Bus type select input (PLCC only)
$\overline{CS}$	Chip select input
AS	Address strobe input
DS	Data strobe input
R/$\overline{W}$	Read/write input
$\overline{INT}$	Interrupt request output
RST	Reset input
SQW	Square wave output
BC	3V backup cell input
X1, X2	Crystal inputs
NC	No connect
$\overline{CE}_{IN}$	RAM chip enable input
$\overline{CE}_{OUT}$	RAM chip enable output
V_{OUT}	Supply output
V_{CC}	+5V supply
V_{SS}	Ground



Block Diagram

Pin Descriptions

AD_0–AD_7 Multiplexed address/data input/output

The bq4285 bus cycle consists of two phases: the address phase and the data-transfer phase. The address phase precedes the data-transfer phase. During the address phase, an address placed on AD_0–AD_7 is latched into the bq4285 on the falling edge of the AS signal. During the data-transfer phase of the bus cycle, the AD_0–AD_7 pins serve as a bidirectional data bus.

MOT Bus type select input (PLCC package only)

MOT selects bus timing for either Motorola or Intel architecture. This pin should be tied to V_{CC} for Motorola timing or to V_{SS} for Intel timing (see Table 1). The setting should not be changed during system operation. MOT is internally pulled low by a 20KR resistor. For the DIP and SOIC packages, this pin is internally connected to V_{SS}, enabling the bus timing for the Intel architecture.

$\overline{CS}$ Chip select input

$\overline{CS}$ should be driven low and held stable during the data-transfer phase of a bus cycle accessing the bq4285.

Table 1. Bus Setup

Bus Type	MOT Level	DS Equivalent	R/$\overline{W}$ Equivalent	AS Equivalent
Motorola	V_{CC}	DS, E, or Φ2	R/$\overline{W}$	AS
Intel	V_{SS}	$\overline{RD}$, $\overline{MEMR}$, or $\overline{I/OR}$	$\overline{WR}$, $\overline{MEMW}$, or $\overline{I/OW}$	ALE

AS — Address strobe input

AS serves to demultiplex the address/data bus. The falling edge of AS latches the address on AD0–AD7. This demultiplexing process is independent of the $\overline{CS}$ signal. For DIP, SOIC, and PLCC packaged with MOT = Vcc, the AS input is provided a signal similar to ALE in an Intel-based system.

DS — Data strobe input

For DIP, SOIC, and PLCC packages with MOT = Vss, the DS input is provided a signal similar to RD, MEMR, or $\overline{IOR}$ in an Intel-based system. The falling edge on DS is used to enable the outputs during a read cycle.

For the PLCC package, when MOT = Vcc, DS controls data transfer during a bq4285 bus cycle. During a read cycle, the bq4285 drives the bus after the rising edge on DS. During a write cycle, the falling edge on DS is used to latch write data into the chip.

R/$\overline{W}$ — Read/write input

For DIP, SOIC, and PLCC packages with MOT = Vss, R/$\overline{W}$ is provided a signal similar to $\overline{WR}$, $\overline{MEMW}$, or $\overline{IOW}$ in an Intel-based system. The rising edge on R/$\overline{W}$ latches data into the bq4285.

For the PLCC package, when MOT = Vcc, the level on R/$\overline{W}$ identifies the direction of data transfer. A high level on R/$\overline{W}$ indicates a read bua cycle, whereas a low on this pin indicates a write bus cycle.

$\overline{INT}$ — Interrupt request output

$\overline{INT}$ is an open-drain output. $\overline{INT}$ is asserted low when any event flag is set and the corresponding event enable bit is also set. $\overline{INT}$ becomes high-impedance whenever register C is read (see the Control/Status Registers section).

$\overline{RST}$ — Reset input

The bq4285 is reset when $\overline{RST}$ is pulled low. When reset, $\overline{INT}$ becomes high-impedance, and the bq4285 is not accessible. Table 4 in the Control/Status Registers section lists the register bits that are cleared by a reset.

Reset may be disabled by connecting $\overline{RST}$ to Vcc. This allows the control bite to retain their states through power-down/power-up cycles.

SQW — Square-wave output

SQW may output a programmable frequency square-wave signal during normal (Vcc valid) system operation. Any one of the 13 specific frequencies may be selected through register A. This pin is held low when the square-wave enable bit (SQWE) in register B is 0 (see the Control/Status Registers section).

BC — 3V backup cell input

BC should be connected to a 3V backup cell for RTC operation and storage register nonvolatility in the absence of power. When Vcc slews down past VBC (3V typical), the integral control circuitry switches the power source to BC. When Vcc returns above VBC, the power source is switched to Vcc.

Upon power-up, a voltage within the VBC range must be present on the BC pin for the oscillator to start up.

X1, X2 — Crystal input

The X1, X2 inputs are provided for an external 32.768Khz quartz crystal, Daiwa DT-26 or equivalent, with 6pF load capacitance. A trimming capacitor may be necessary for extremely precise time-base generation.

$\overline{CE}$IN — External RAM chip enable input, active low

$\overline{CE}_{IN}$ should be driven low to enable the controlled external RAM. $\overline{CE}_{IN}$ is internally pulled up with a 50KΩ resistor.

$\overline{CE}_{OUT}$ — External RAM chip enable output, active low

When power is valid, $\overline{CE}_{OUT}$ reflects $\overline{CE}_{IN}$.

VOUT — Supply output

VOUT provides the higher of Vcc or VBC, switched internally, to supply external RAM.

Vcc — +5V supply

Vss — Ground

5

Functional Description

Address Map

The bq4285 provides 14 bytes of clock and control/status registers and 114 bytes of general nonvolatile storage. Figure 1 illustrates the address map for the bq4285.

Update Period

The update period for the bq4285 is one second. The bq4285 updates the contents of the clock and calendar locations during the update cycle at the end of each update period (see Figure 2). The alarm flag bit may also be set during the update cycle.

The bq4285 copies the local register updates into the user buffer accessed by the host processor. When a 1 is written to the update transfer inhibit bit (UTI) in register B, the user copy of the clock and calendar bytes remains unchanged, while the local mpy of the same bytes continua to be updated every second.

The update-in-progress bit (UIP) in register A is set t_{BUC} time before the beginning of an update cycle (see Figure 2). This bit is cleared and the update-complete flag (UF) is set at the end of the update cycle.

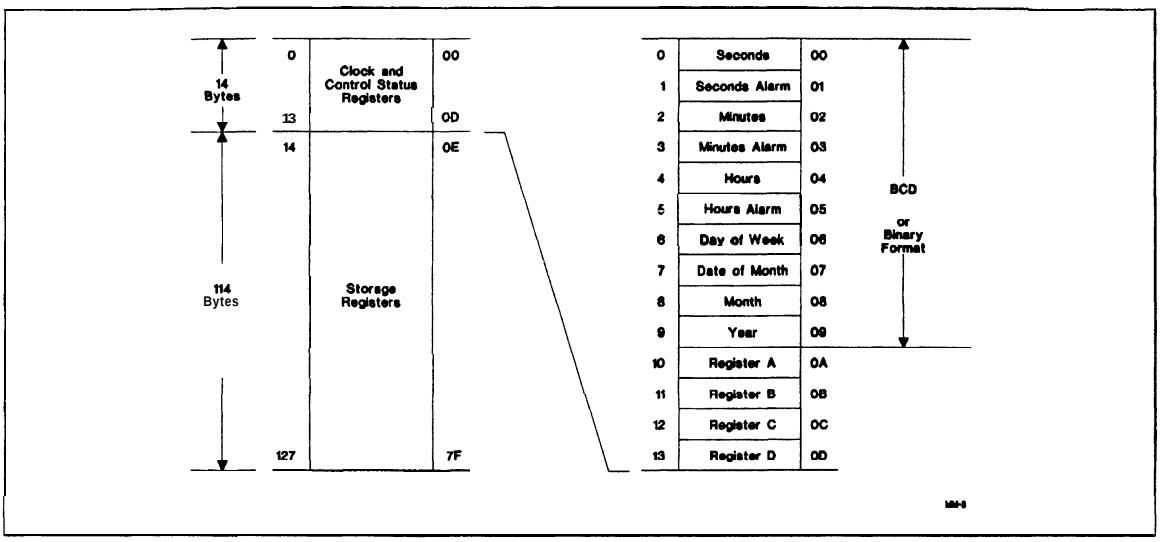


Figure 1. Address Map

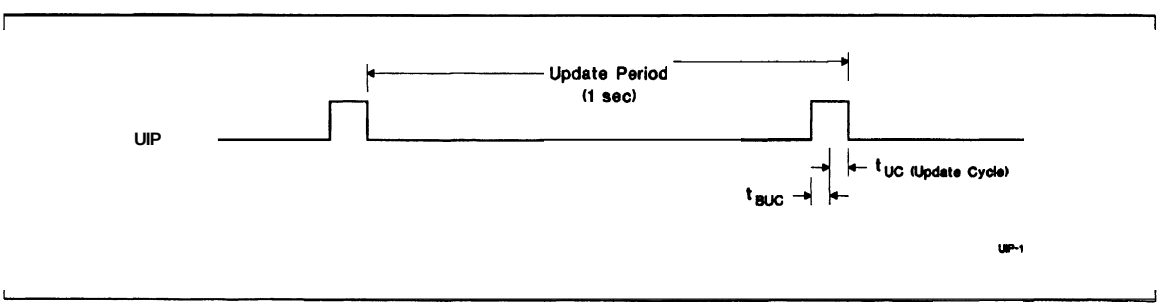


Figure 2. Update Period Timing and UIP

Programming the RTC

The time-of-day, alarm, and calendar bytes can be written in either the BCD or binary format (see Table 2).

These steps may be followed to program the time, alarm, and calendar:

1. Modify the contents of register B:
   a. Write a 1 to the UTI bit to prevent transfers between RTC bytes and user buffer.
   b. Write the appropriate value to the data format (DF) bit to select BCD or binary format for all time, alarm, and calendar bytes.
   c. Write the appropriate value to the hour format (HF) bit.
2. Write new values to all the time, alarm, and calendar locations.
3. Clear the UTI bit to allow update transfers.

On the next update cycle, the RTC updates all 10 bytes in the selected format.

Table 2. Time, Alarm, and Calendar Formats

Address	RTC Bytes	Range		
		Decimal	Binary	Binary-Coded Decimal
0	Seconds	0–59	00H–3BH	00H–59H
1	Seconds alarm	0–59	00H–3BH	00H–59H
2	Minutes	0–59	00H–3BH	00H–59H
3	Minutes alarm	0–59	00H–3BH	00H–59H
4	Hours, 12-hour format	1–12	01H–0CH AM; 81H–8CH PM	01H–12H AM; 81H–92H PM
	Hours, 24-hour format	0–23	00H–17H	00H–23H
5	Hours alarm, 12-hour format	1–12	01H–0CH AM; 81H–8CH PM	01H–12H AM; 81H–92H PM
	Hours alarm, 24-hour format	0–23	00H–17H	00H–23H
6	Day of week (1=Sunday)	1–7	01H–07H	01H–07H
7	Day of month	1-31	01H–1FH	01H–31H
8	Month	1–12	01H–0CH	01H–12H
9	Year	0–99	00H–63H	00H–99H

but keeps the frequency divider disabled. Any other pattern to these bite keeps the oscillator off.

Power-Down/Power-Up Cycle

The bq4285 continuously monitors V_{CC} for out-of-tolerance. During a power failure, when Vcc falls below V_{PFD} (4.17V typical), the bq4285 write-protects the clock and storage registers. When V_{CC} is below V_{BC} (3V typical), the power source is switched to BC. RTC operation and storage data are sustained by a valid backup energy source. When V_{CC} is above V_{BC}, the power source is V_{CC}. Write-protection continues for t_{CSR} time after V_{CC} rises above V_{PFD}.

An external CMOS static RAM is battery-backed using the V_{OUT} and chip enable output pins from the bq4285. As the voltage input V_{CC} slows down during a power failure, the chip enable output, $\overline{CE}_{OUT}$, is forced inactive independent of the chip enable input $\overline{CE}_{IN}$.

This activity unconditionally write-protects the external SRAM as V_{CC} falls below V_{PFD}. If a memory access is in process to the external SRAM during power-fail detection, that memory cycle continues to completion before the memory is write-protected. If the memory cycle is not terminated within time t_{WPT} (30µs maximum), the chip enable output is unconditionally driven high, write-protecting the controlled SRAM.

As the supply continues to fall past V_{PFD}, an internal switching device forces Vow to the external backup energy source. $\overline{CE}_{OUT}$ is held high by the V_{OUT} energy source.

During power-up, Vow is switched back to the 5V supply as V_{CC} rises above the backup cell input voltage sourcing V_{OUT}. $\overline{CE}_{OUT}$ is held inactive for time t_{CER} (200ms maximum) after the power supply has reached V_{PFD}, independent of the $\overline{CE}_{IN}$ input, to allow for processor stabilization.

During power-valid operation, the $\overline{CE}_{IN}$ input is passed through to the $\overline{CE}_{OUT}$ output with a propagation delay of less than 10ns.

Figure 4 shows the hardware hookup for the external RAM.

A primary backup energy source input is provided on the bq4285. The BC input accepts a 3V primary battery, typically some type of lithium chemistry. To prevent battery drain when there is no valid data to retain, V_{OUT} and $\overline{CE}_{OUT}$ are internally isolated from BC by the initial connection of a battery. Following the first application of Vcc above V_{PFD}, this isolation is broken, and the backup cell provides power to Vow and $\overline{CE}_{OUT}$ for the external SRAM.

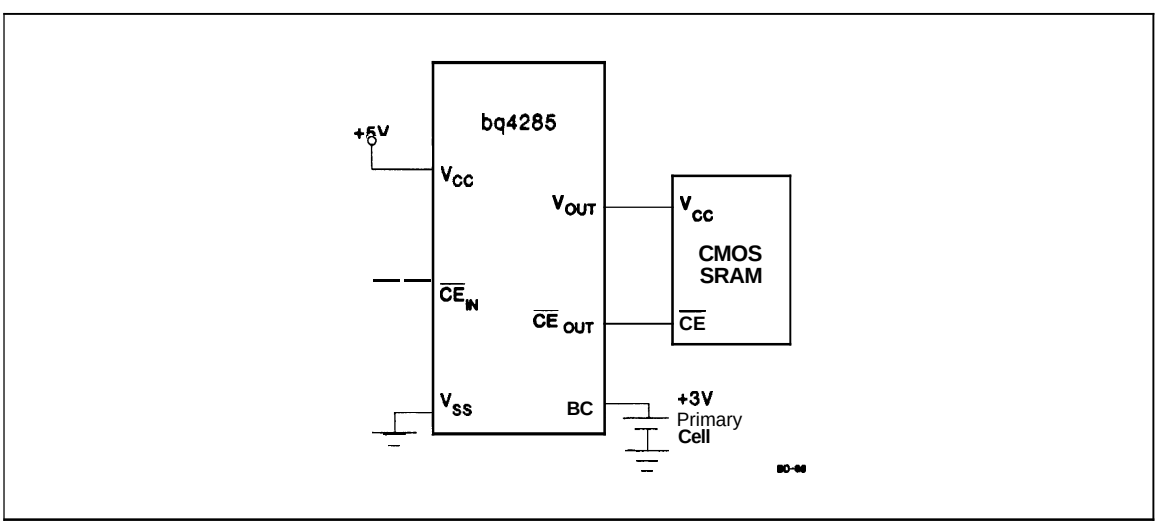


Figure 4. External RAM Hookup to the bq4285 RTC

Control/Status Registers

The four control/status registers of the bq4285 are accessible regardless of the status of the update cycle (see Table 4).

Register A

Register A Bits							
7	6	5	4	3	2	1	0
UIP	OS2	OS1	OS0	RS3	RS2	RS1	RS0

Register A programs:

- The frequency of the square-wave and the periodic event rate.
- Oscillator operation.

Register A provides:

- Status of the update cycle.

RS0–RS3 - Frequency Select

7	6	5	4	3	2	1	0
			-	RS3	RS2	RS1	RS0

These bits select one of the 13 frequencies for the SQW output and the periodic interrupt rate, as shown in Table 3.

OS0–OS2 - Oscillator Control

7	6	5	4	3	2	1	0
-	OS2	OS1	OS0	-	-	-	-

These three bits control the state of the oscillator and divider stages. A pattern of 010 enables RTC operation by turning on the oscillator and enabling the frequency divider. A pattern of 11X turns the oscillator on, but keeps the frequency divider disabled. When 010 is written, the RTC begins its first update after 500ms.

UIP - Update Cycle Status

7	6	5	4	3	2	1	0
UIP	-	-	-	-	-	-	-

This read-only bit is set prior to the update cycle. When UIP equals 1, an RTC update cycle may be in progress. UIP is cleared at the end of each update cycle. This bit is also cleared when the update transfer inhiiit (UTI) bit in register B is 1.

Register B

Register B Bit8							
7	6	5	4	3	2	1	0
UTI	PIE	AIE	UIE	SQWE	DF	HF	DSE

Register B enables:

- a Update cycle transfer operation
- a Square-waveoutput
- Interrupt events
- a Daylight saving adjustment

Register B selects:

- Clock and calendar data formats

All bits of register B are read/write.

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Table 4. Control/Status Registers

Reg.	Loc. (Hex)	Read	Write	Bit Name and State on Reset															
				7 (MSB)		6		5		4		3		2		1		0 (LSB)	
A	0A	Yes	Yes[1]	UIP	na	OS2	na	OS1	na	OS0	na	RS3	na	RS2	na	RS1	na	RS0	na
B	0B	Yes	Yes	UTI	na	PIE	0	AIE	0	UIE	0	SQWE	0	DF	na	HF	na	DSE	na
C	0C	Yes	No	INTF	0	PF	0	AF	0	UF	0	-	0	-	0	-	0	-	0
D	0D	Yes	No	VRT	na	-	0	-	0	-	0	-	0	-	0	-	0	-	0

Notes: na = not affected.

1. Except bit 7.

DSE - Daylight Saving Enable

7	6	5	4	3	2	1	0
						-	DSE

This bit enables daylight-saving time adjustments when written to 1:

- On the last Sunday in October, the first time the bq4285 increments past 1:59:59 AM, the time falls back to 1:00:00 AM.
- On the first Sunday in April, the time springs forward from 2:00:00 AM to 3:00:00 AM.

HF - Hour Format

7	6	5	4	3	2	1	0
-	-	-	-	-	-	HF	-

This bit selects the time-of-day and alarm hour format:

1 = 24-hour format

0 = 12-hour format

DF - Data Format

7	6	5	4	3	2	1	0
				-	DF	-	-

This bit selects the numeric format in which the time, alarm, and calendar bytes are represented:

1 = Binary

0 = BCD

SQWE - Square-Wave Enable

7	6	5	4	3	2	1	0
-	-	-	-	SQWE	-	-	-

This bit enables the square-wave output:

1 = Enabled

0 = Disabled and held low

UIE - Update Cyck Interrupt Enable

7	6	5	4	3	2	1	0
-	-	-	UIE	-	-	-	-

This bit enables an interrupt request due to an update ended interrupt event:

1 =Enabled

0 = Disabled

The UIE bit is automatically cleared when the UTI bit equals 1.

AIE - Alarm interrupt Enable

7	6	5	4	3	2	1	0
-	-	AIE	-	-	-	-	-

This bit enables an interrupt request due to an alarm interrupt event:

1 = Enabled

0 = Disabled

PIE - Periodic Interrupt Enable

7	6	5	4	3	2	1	0
-	PIE	-	-	-	-	-	-

This bit enables an interrupt request due to a periodic interrupt event:

1 = Enabled

0 = Disabled

UTI - Update Transfer inhibit

7	6	5	4	3	2	1	0
UTI	-	-	-	-	-	-	-

This bit inhibits the transfer of RTC bytes to the user buffer:

1 = Inhibits transfer and clears UIE

0 = Allows transfer

Register C

Reaister C Bits							
7	6	5	4	3	2	1	0
INTF	PF	AF	UF	0	0	0	0

Register C is the read-only event status register.

Bits 0-3 - Unuwd Bits

7	6	5	4	3	2	1	0
-	-	-	-	0	0	0	0

These bits are always set to 0.

UF - Update-Event Flag

7	6	5	4	3	2	1	0
-	-	-	UF	-	-	-	-

This bit is set to a 1 at the end of the update cycle. Reading register C clears this bit.

AF - Alarm Event Flag

7	6	5	4	3	2	1	0
-	-	AF	-	-	-	-	-

This bit is set to a 1 when an alarm event occurs. Reading register C clears this bit.

PF - Periodic Event Flag

7	6	5	4	3	2	1	0
-	PF	-	-	-	-	-	-

This bit is set to a 1 every t_{PI} time, where t_{PI} is the time period selected by the settings of RS0-RS3 in register A. Reading register C clears this bit.

INTF - interrupt Request Flag

7	6	5	4	3	2	1	0
INTF	-	-	-	-	-	-	-

This flag is set to a 1 when any of the following is true:

AIE = 1 and AF = 1

PIE = 1 and PF = 1

UIE = 1 and UF = 1

Reading register C clears this bit.

Register D

Register D Bits							
7	6	5	4	3	2	1	0
VRT	0	0	0	0	0	0	0

Register D is the read-only data integrity status register.

Bits 0-6 - Unused Bits

These bits are always set to 0.

7	6	5	4	3	2	1	0
-	0	0	0	0	0	0	0

VRT - Valid RAM and Time

1 = Valid backup energy source

7	6	5	4	3	2	1	0
VRT	-	-	-	-	-	-	-

0 = Backup energy source is depleted

When the backup energy source is depleted (VRT = 0), data integrity of the RTC and storage registers is not guaranteed.

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Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on Vcc relative to Vss	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding Vcc relative to V_{SS}	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
T_{STG}	Storage temperature	-55 to +125	°C	
T_{BIAS}	Temperature under bias	-40 to +85	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IL}	Input low voltage	-0.3		0.8	V
V_{IH}	Input high voltage	2.2		Vcc + 0.3	V
V_{BC}	Backup cell voltage	2.5		4.0	V

Note: Typical values indicate operation at T_A = 25°C.

DC Electrical Characteristics ($T_A = T_{OPR}$, V_{CC} = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current			±1	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current			±1	µA	AD_0–AD_7, $\overline{INT}$, and SQW in high impedance, $V_{OUT} = V_{SS}$ to V_{CC}
V_{OH}	Output high voltage	2.4			V	I_{OH} = -2.0mA
V_{OL}	Output low voltage			0.4	V	I_{OL} = 4.0 mA
I_{CC}	Operating supply current		7	15	mA	Min. cycle, duty = 100%, I_{OH} = 0mA, I_{OL} = 0mA
V_{SO}	Supply switch-over voltage		V_{BC}		V	
I_{CCB}	Battery operation current		0.3	0.5	µA	V_{BC} = 3V, T_A = 25°C, no load on V_{OUT} or $\overline{CE}_{OUT}$
V_{PFD}	Power-fail-detact voltage	4.0	4.17	4.35	V	
V_{OUT1}	V_{OUT} voltage	Vcc - 0.3V	-		V	I_{OUT} = 100mA, $V_{CC} > V_{BC}$
V_{OUT2}	V_{OUT} voltage	V_{BC} - 0.3V				I_{OUT} = 100µA, $V_{CC} < V_{BC}$
I_{MOTH}	Input current when MOT = Vcc			-275	*pi*	Internal 20K pull-down
$I_{\overline{CE}}$	Chip enable input current			100	*pi*	Internal 50K pull-up

Note: Typical values indicate operation at T_A = 25°C, Vcc = 5V or V_{BC} = 3V.

Crystal Specifications (DT-26 or Equivalent)

Symbd	Parameter	Minimum	Typical	Maximum	Unit
f_O	Oscillation frequency		32.768		kHz
C_L	Load capacitance		6		pF
T_P	Temperature turnover point	20	25	30	°C
k	Parabolic curvature constant			-0.042	ppm/°C
Q	Quality factor	40,000	70,000		
R_1	Series resistance			45	KΩ
C_0	Shunt capacitance		1.1	1.8	pF
C_0/C_1	Capacitance ratio		430	600	
DL	Drive level			1	µW
$\Delta f/f_O$	Aging (first year at 25°C)		1		ppm

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbd	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance			7	pF	V_{OUT} = 0V
C_{IN}	Input capacitance			5	pF	V_{IN} = 0V

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0 to 3.0 V
Input rise and fall times	5ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 5 and 6

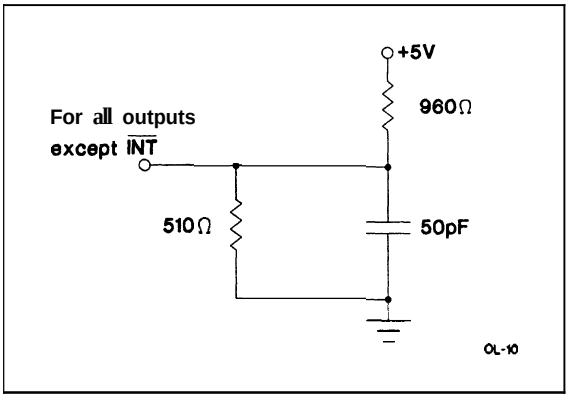

Figure 5. Output Load A

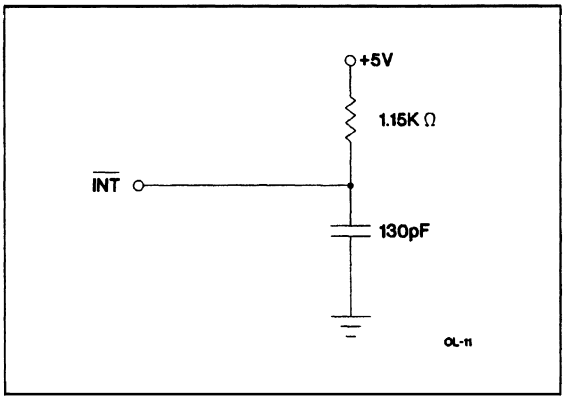

Figure 6. Output Load B

Read/Write Timing ($T_A = T_{OPR}$, $V_{CC} = 5V \pm 10\%$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYC}	Cycle time	160			ns	
t_{DSL}	DS low or $\overline{RD}/\overline{WR}$ high time	80	-	-	ns	
t_{DSH}	DS high or $\overline{RD}/\overline{WR}$ low time	55	-	-	ns	
t_{RWH}	R/$\overline{W}$ hold time	10	-	-	ns	
t_{RWS}	R/$\overline{W}$ setup time	10			ns	
t_{CS}	Chip select setup time	5			ns	
t_{CH}	Chip select hold time	0			ns	
t_{DHR}	Read data hold time	0	-	25	ns	
t_{DHW}	Write data hold time	0			ns	
t_{AS}	Address setup time	20	-	-	ns	
t_{AH}	Address hold time	5			ns	
t_{DAS}	Delay time, DS to AS rise	10			ns	
t_{ASW}	Pulse width, AS high	30			ns	
t_{ASD}	Delay time, AS to DS rise ($\overline{RD}/\overline{WR}$ fall)	35	-	-	ns	
t_{OD}	Output data delay time from DS rise ($\overline{RD}$ fall)	-	-	50	ns	
t_{DW}	Write data setup time	30	-	-	ns	
t_{BUC}	Delay time before update		244		µs	
t_{PI}	Periodic interrupt time interval					See Table 3
t_{UC}	Time of update cycle		1		µs	

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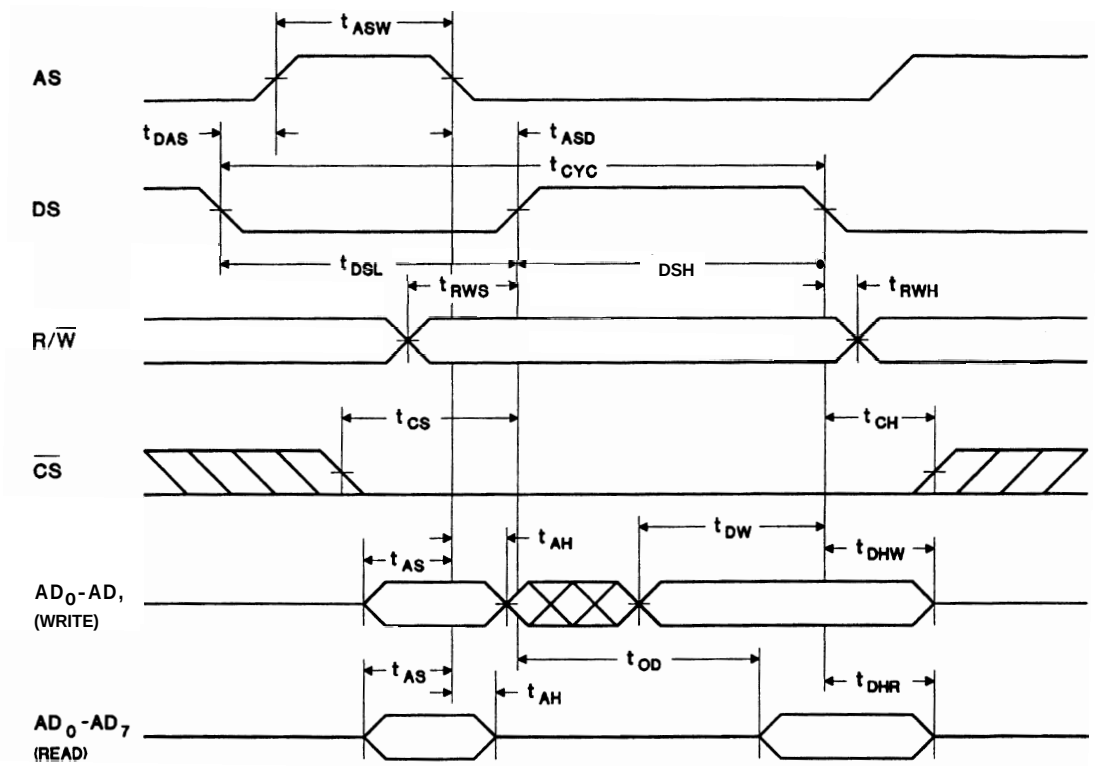
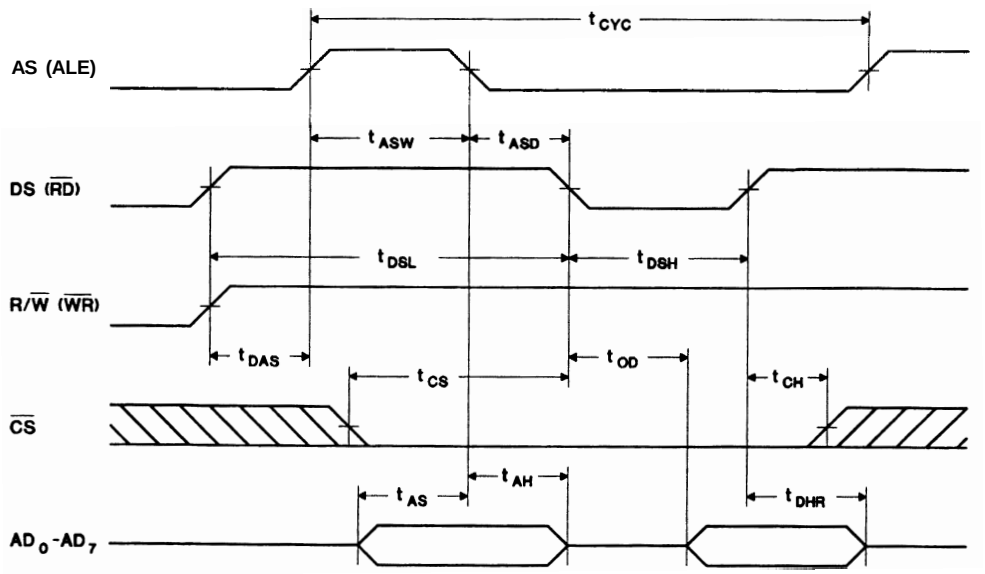
Motorola Bus Read/Write Timing (PLCC Package Only)



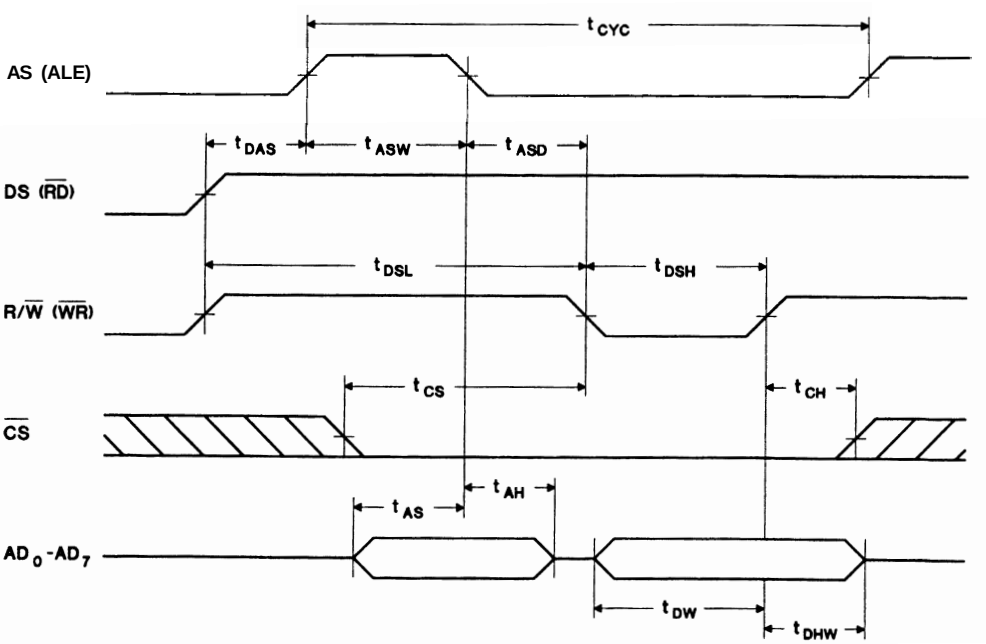
RC-4

Intel Bus Read Timing



RC-5

Intel Bus Write Timing



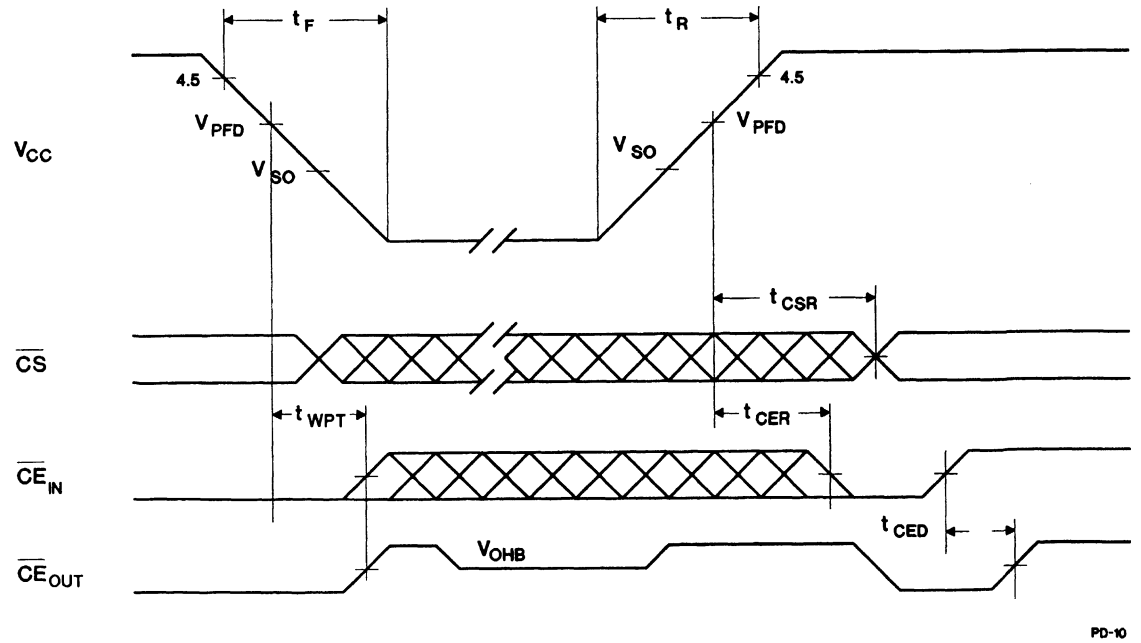
WC-5

Power-Down/Power-Up Timing ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_F	V_{CC} slew from 4.5V to 0V	300			µs	
t_R	V_{CC} slew from 0V to 4.5V	100			µs	
t_{CSR}	$\overline{CS}$ at V_{IH} after power-up	20		200	ms	Internal write-protection period after V_{CC} passes V_{PFD} on power-up.
t_{WPT}	Write-protect time for external RAM	10	16	30	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.
t_{CER}	Chip enable recovery time	t_{CSR}		t_{CSR}	ms	Time during which external SRAM is write-protected after V_{CC} passes V_{PFD} on power-up.
t_{CED}	Chip enable propagation delay to external SRAM		7	10	ns	

Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup *mode* may affect data integrity.

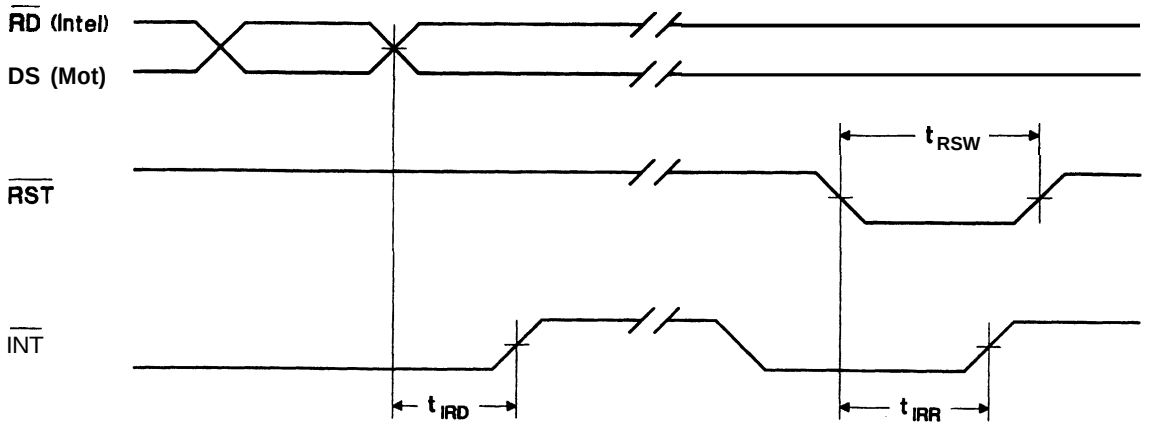
Power-Down/Power-Up Timing



Interrupt Delay Timing ($T_A = T_{OPR}$)

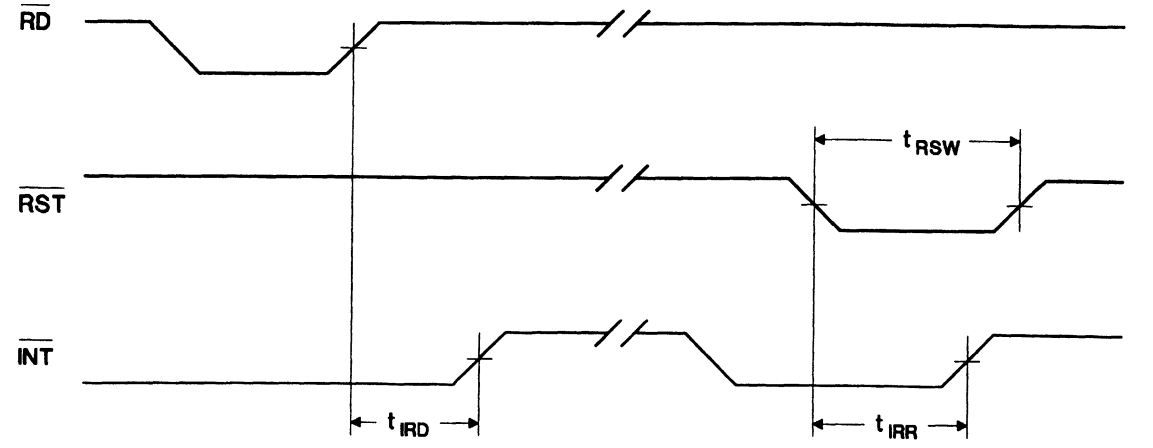
Symbol	Parameter	Minimum	Typical	Maximum	Unit
t_{RSW}	Reset pulse width	5			µs
t_{IRR}	$\overline{INT}$ release from			2	µs
t_{IRD}	$\overline{INT}$ release from DS ($\overline{RD}$)			2	µs

Interrupt Delay Timing (PLCC Package Only)



INT-1

Interrupt Delay Timing (SOIC, DIP Packages)



INT-4

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	3	Address strobe input	Clarification
1	12	Backup cell voltage V_{BC}	Was 2.0 min; is 2.5 min
1	13	Power-fail detect voltage V_{PFD}	Was 4.1 min, 4.25 max; is 4.0 min, 4.35 max
1	13	Chip enable input current	Additional specification
2	3, 13	Crystal type Daiwa DT-26 (not DT-26S)	Clarification

Note: Change 1 = Nov. 1992 B changes from June 1991 A.
Change 2 = Nov. 1993 C changes from Nov. 1992 B.

Ordering Information

bq4285 - _ _

Temperature:
blank = Commercial (0 to +70°C)

Package Option:
P = 24-pin plastic DIP (0.600)
S = 24-pin SOIC (0.300)
Q = 28-pin quad PLCC

Device:
bq4285 Real-Time Clock With NVRAM Control

bq4285E/bq4285L

Enhanced RTC With NVRAM Control

Features

- Direct clock/calendar replacement for IBM® AT-compatible computers and other applications
- ➤ 114 bytes of general nonvolatile storage
- ➤ Enhanced features include:
  - System wake-up capability—alarm interrupt output active in battery-backup mode
  - 2.7–3.6V operation (bq4285L); 4.5–5.5V operation (bq4285E)
  - 32KHz output for power management
- Automatic backup and write-protect control to external SRAM
- ➤ Functionally compatible with the DS1285
- Less than 0.5 µA load under battery operation
- Selectable Intel or Motorola bus timing (PLCC), Intel bus timing (DIP and SOIC)
- 14 bytes for clock/calendar and control
- BCD or binary format for clock and calendar data
- Calendar in day of the week, day of the month, months, and years, with automatic leap-year adjustment
- Time of day in seconds, minutes, and hours
  - 12- or 24-hour format
  - Optional daylight saving adjustment
- Programmable square wave output
- ➤ Three individually maskable interrupt event flags:
  - Periodic rates from 122 µs to 500 ms
  - Time-of-day alarm once per second to once per day
  - End-of-clock update cycle
- 24-pin plastic DIP or SOIC and 28-pin PLCC

General Description

The CMOS bq4285E/bq4285L is a low-power microprocessor peripheral providing a time-of-day clock and 100-year calendar with alarm features and battery operation. Other features include three maskable interrupt sources, square wave output, and 114 bytes of general nonvolatile storage.

A 32.768kHz output is available for sustaining power-management activities. Wake-up capability is provided by an alarm interrupt, which is active in battery-backup mode.

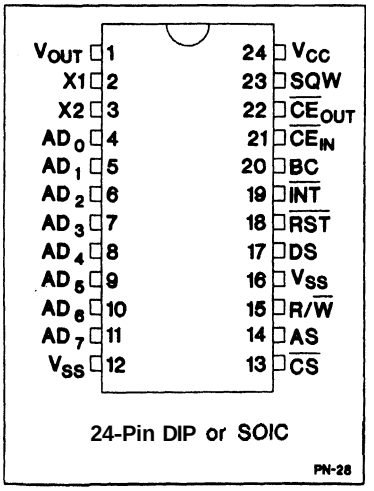
The bq4285E/bq4285L write-protects the clock, calendar, and storage registers during power failure. A backup battery then maintains data and operates the clock and calendar.

The bq4285E/bq4285L is a fully compatible real-time clock for IBM AT-compatible computers and other applications. The only external components are a 32.768kHz crystal and a backup battery.

The bq4285E/bq4285L integrates a battery-backup controller to make a

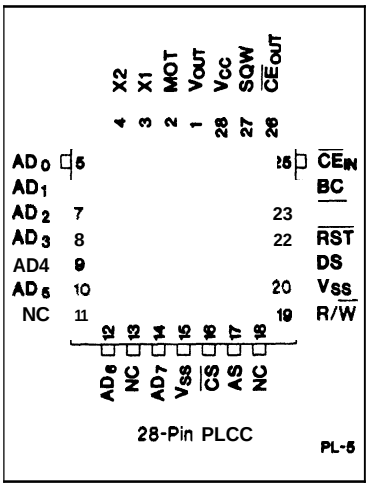
5

Pin Connections



24-Pin DIP or SOIC

PN-28



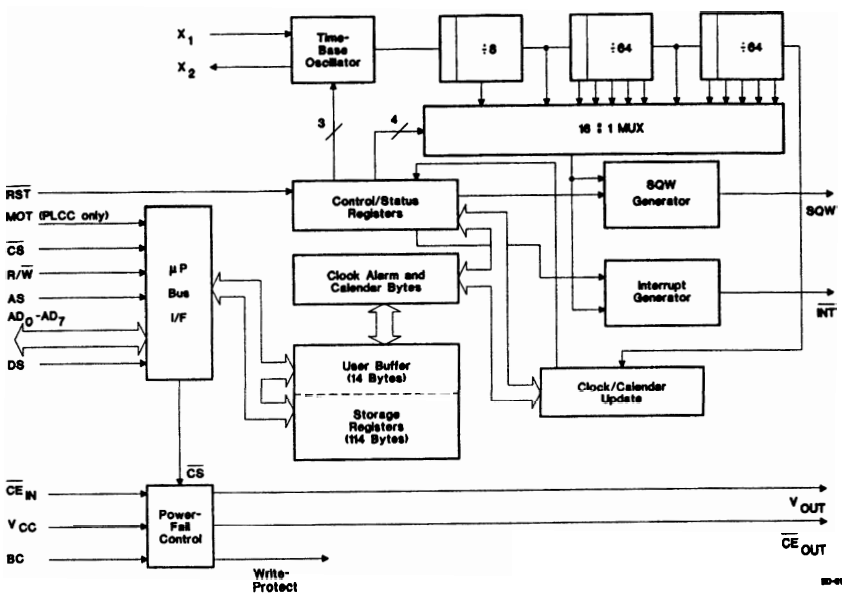
28-Pin PLCC

PL-5

Pin Names

AD0–AD7	Multiplexed address/data input/output
MOT	Bus type select input (PLCC only)
$\overline{CS}$	Chip select input
AS	Address strobe input
DS	Data strobe input
R/$\overline{W}$	Read/write input
$\overline{INT}$	Interrupt request output
$\overline{RST}$	Reset input
SQW	Square wave output
BC	3V backup cell *input*
X1, X2	Crystal *inputs*
NC	No connect
$\overline{CE}_{IN}$	RAM chip enable input
$\overline{CE}_{OUT}$	RAM chip enable output
VOUT	Supply output
Vcc	+5vsupply
Vss	Ground

Block Diagram



standard CMOS SRAM nonvolatile during power-fail conditions. During power-fail, the bq4285E/bq4285L automatically write-protects the external SRAM and provides a Vcc output sourced from the clock backup battery.

Pin Descriptions

AD_0–AD_7 Multiplexed address/data input/output

The bq4285E/bq4285L bus cycle consists of two phases: the address phase and the data-transfer phase. The address phase precedes the data-transfer phase. During the address phase, an address placed on AD_0–AD_7 is latched into the bq4285E/bq4285L on the falling edge of the AS signal. During the data-transfer phase of the bus cycle, the AD_0–AD_7 pins serve as a bidirectional data bus.

MOT Bus type select input (PLCC package only)

MOT selects bus timing for either Motorola or Intel architecture. This pin should be tied to Vcc for Motorola timing or to Vss for Intel timing (see Table 1). The setting should not be changed during system operation. MOT is internally pulled low by a 20KR resistor. For the DIP and SOIC packages, this pin is internally connected to Vss, enabling the bus timing for the Intel architecture.

$\overline{CS}$ Chip select input

$\overline{CS}$ should be driven low and held stable during the data-transfer phase of a bus cycle accessing the bq4285E/bq4285L.

Table 1. Bus Setup

Bus Type	MOT Level	DS Equivalent	R/$\overline{W}$ Equivalent	AS Equivalent
Motorola	Vcc	$\overline{DS}$, E, or $\Phi 2$	R/$\overline{W}$	AS
Intel	Vss	$\overline{RD}$, $\overline{MEMR}$, or $\overline{I/OR}$	$\overline{WR}$, $\overline{MEMW}$, or $\overline{I/OW}$	ALE

AS — Address strobe input

AS serves to demultiplex the address/data bus. The falling edge of AS latches the address on AD0–AD7. This demultiplexing process is independent of the $\overline{CS}$ signal. For DIP, SOIC, and PLCC packages with MOT = VCC, the AS input is provided a signal similar to ALE in an Intel-based system.

DS — Data strobe input

For DIP, SOIC, and PLCC packages with MOT = VSS, the DS input is provided a signal similar to $\overline{RD}$, MEMR, or $\overline{IOR}$ in an Intel-based system. The falling edge on DS is used to enable the outputs during a read cycle.

For the PLCC package, when MOT = VCC, DS controls data transfer during a bq4285E/bq4285L bus cycle. During a read cycle, the bq4285E/bq4285L drives the bus after the rising edge on DS. During a write cycle, the falling edge on DS is used to latch write data into the chip.

R/$\overline{W}$ — Read/write input

For DIP, SOIC, and PJXC packages with MOT = VSS, R/$\overline{W}$ is provided a signal similar to $\overline{WR}$, MEMW, or $\overline{IOW}$ in an Intel-based system. The rising edge on R/W latches data into the bq4285E/bq4285L.

For the PLCC package, when MOT = VCC, the level on R/$\overline{W}$ identifies the direction of data transfer. A high level on R/$\overline{W}$ indicates a read bus cycle, whereas a low on this pin indicates a write bus cycle.

$\overline{INT}$ — Interrupt request output

$\overline{INT}$ is an open-drain output. This allows $\overline{INT}$ to be valid in battery-backup mode for the alarm interrupt. To use this feature, $\overline{INT}$ must be connected to a power supply other than VCC. $\overline{INT}$ is asserted low when any event flag is set and the corresponding event enable bit is also set. $\overline{INT}$ becomes high-impedance whenever register C is read (see the Control/Status Registers section).

$\overline{RST}$ — Reset input

The bq4285E/bq4285L is reset when $\overline{RST}$ is pulled low. When reset, $\overline{INT}$ becomes high-impedance, and the bq4285E/bq4285L is not accessible. Table 4 in the Control/Status Registers section lists the register bits that are cleared by a reset.

Reset may be disabled by connecting $\overline{RST}$ to VCC. This allows the control bits to retain their states through power-down/power-up cycles.

SQW — Square-wave output

SQW may output a programmable frequency square-wave signal during normal (VCC valid) system operation. Any one of the 13 specific frequencies may be selected through register A This pin is held low when the square-wave enable bit (SQWE) in register B is 0 (see the Control/Status Registers section).

A 32.768kHz output is enabled by setting the SQWE bit in register B to 1 and the 32KE bit in register C to 1 after setting OSC2–OSC0 in register A to 011(binary).

BC — 3V backup cell input

BC should be connected to a 3V backup cell for RTC operation and storage register nonvolatility in the absence of power. When VCC slews down past VBC (3V typical), the integral control circuitry switches the power source to BC. When VCC returns above VBC, the power source is switched to VCC.

Upon power-up, a voltage within the VBC range must be present on the BC pin for the oscillator to start up.

X1, X2 — Crystal input

The X1, X2 inputs are provided for an external 32.768Khz quartz crystal, Daiwa DT-26 or equivalent, with 6pF load capacitance. A trimming capacitor may be necessary for extremely precise time-base generation.

$\overline{CE}_{IN}$ — External RAM chip enable input, active low

$\overline{CE}_{IN}$ should be driven low to enable the controlled external RAM. $\overline{CE}_{IN}$ is internally pulled up with a 50KΩ resistor.

$\overline{CE}_{OUT}$ — External RAM chip enable output, active low

When power is valid, $\overline{CE}_{OUT}$ reflects $\overline{CE}_{IN}$.

VOUT — Supply output

VOUT provides the higher of VCC or VBC, switched internally, to supply external RAM.

VCC — Positive power supply

VSS — Ground

5

Functional Description

Address Map

The bq4285E/bq4285L provides 14 bytes of clock and control/status registers and 114 byte. of general nonvolatile 1 illustrates the address map for the bq4285L.

Update Period

The update period for the bq4285E/bq4285L is one second. The bq4285E/bq4285L updates the contents of the clock and calendar locations during the update cycle at the end of each update period (see Figure 2). The alarm flag bit may also be set during the update cycle.

The bq4285E/bq4285L copies the local register updates into the user buffer acceesed by the host processor. When a 1 is written to the update transfer inhibit bit (UTI) in register B, the user copy of the clock and dendar bytes remains unchanged, while the local copy of the same bytes continues to be updated every second.

The update-in-progress bit (UIP) in register A is set t_{BUC} time before. the beginning of an update cycle (see Figure 2). This bit is cleared and the update-complete flag (UF) is set at the end of the update cycle.

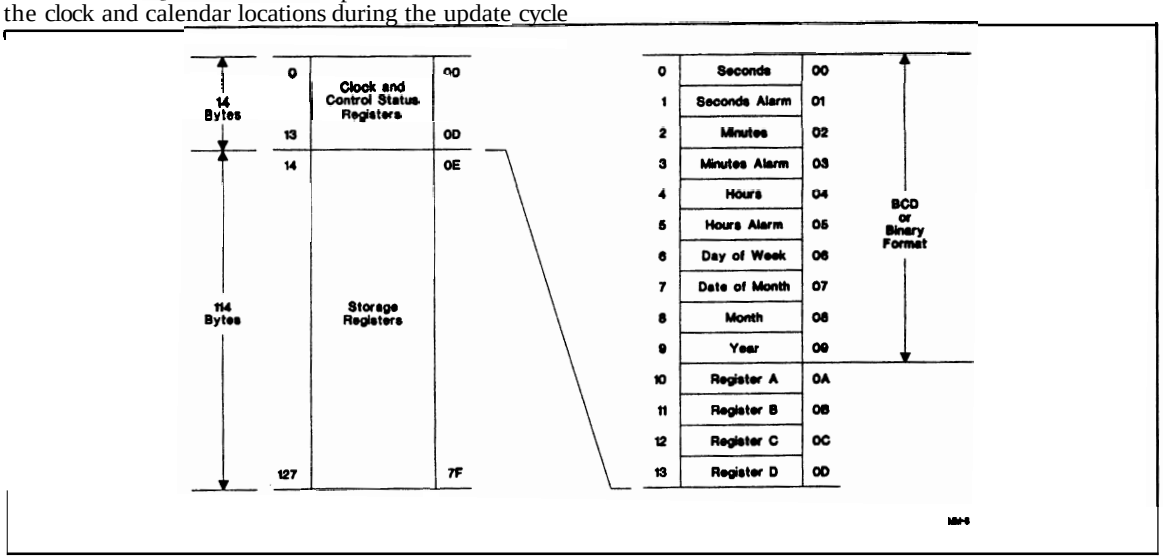


Figure 1. Address Map

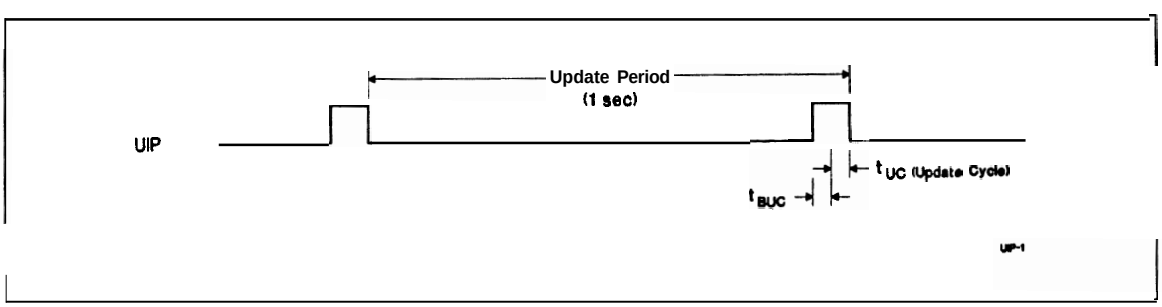


Figure 2. Update Period Timing and UIP

Programming the RTC

The time-of-day, alarm, and calendar bytes can be written in either the BCD or binary format (see Table 2).

These steps may be followed to program the time, alarm, and calendar:

1. Modify the contents of register B:
   a. Write a 1 to the UTI bit to prevent transfers between RTC bytes and user buffer.
   b. Write the appropriate value to the data format (DF) bit to select BCD or binary format for all time, alarm, and calendar bytes.
   c. Write the appropriate value to the hour format (HF) bit.
2. Write new values to all the time, alarm, and calendar locations.
3. Clear the UTI bit to allow update transfers.

On the next update cycle, the RTC updates all 10 bytes in the selected format.

Table 2. Time, Alarm, and Calendar Formats

Address	RTC Bytes	Range		
		Decimal	Binary	Binary-Coded Decimal
0	Seconds	0–59	00H–3BH	00H–59H
1	Seconds alarm	0–59	00H–3BH	00H–59H
2	Minutes	0–59	00H–3BH	00H–59H
3	Minutes alarm	0–59	00H–3BH	00H–59H
4	Hours, 12-hour format	1–12	01H–0CH AM; 81H–8CH PM	01H–12H AM; 81H–92H PM
	Hours, 24-hour format	0–23	00H–17H	00H–23H
5	Hours alarm, 12-hour format	1–12	01H–0CH AM; 81H–8CH PM	01H–12H AM; 81H–92H PM
	Hours alarm, 24-hour format	0–23	00H–17H	00H–23H
6	Day of week (1=Sunday)	1–7	01H–07H	01H–07H
7	Day of month	1–31	01H–1FH	01H–31H
8	Month	1–12	01H–0CH	01H–12H
9	Year	0–99	00H–63H	00H–99H

Square Wave Output

The bq4285E/bq4285L divides the 32.768kHz oscillator frequency to produce the 1 Hz update frequency for the clock and calendar. Thirteen taps from the frequency divider are fed to a 16:1 multiplexer circuit. The output of this mux is fed to the SQW output and periodic interrupt generation circuitry. The four least-significant bite of register A, RS0–RS3, select among the 13 taps (see Table 3). The square-wave output is enabled by writing a 1 to the square-wave enable bit (SQWE) in register B. A 32.768kHz output may be selected by setting OSC2–OSC0 in register A to 011 while SQWE = 1 and 32KE = 1.

Interrupts

The bq4285E/bq4285L allows three individually selected interrupt events to generate an interrupt request. These three interrupt events are:

- The periodic interrupt, programmable to occur once every 122 us to 500 ms.
- The alarm interrupt, programmable to occur once per second to once per day, is active in battery-backup mode, providing a "wake-up" feature.
- The update-ended interrupt, which occurs at the end of each update cycle.

Each of the three interrupt events is enabled by an individual interrupt-enable bit in register B. When an event occurs, its event flag bit in register C is set. If the corresponding event enable bit is also set, then an interrupt request is generated. The interrupt request flag bit (INTF) of register C is set with every interrupt request. Reading register C clears all flag bits, including INTF, and makes $\overline{INT}$ high-impedance.

Two methods can be used to process bq4285E/bq4285L interrupt events:

- Enable interrupt events and use the interrupt request output to invoke an interrupt service routine.
- Do not enable the interrupts and use a polling routine to periodically check the status of the flag bits.

The individual interrupt sources are described in detail in the following sections.

Table 3. Square-Wave Frequency/Periodic Interrupt Rate

Register A Bits							Square Wave		Periodic Interrupt	
OSC2	OSC1	OSC0	RS3	RS2	RS1	RS0	Frequency	Units	Period	Units
0	1	0	0	0	0	0	None		None	
0	1	0	0	0	0	1	256	Hz	3.90625	ms
0	1	0	0	0	1	0	128	Hz	7.8125	ms
0	1	0	0	0	1	1	8.192	kHz	122.070	µs
0	1	0	0	1	0	0	4.096	kHz	244.141	µs
0	1	0	0	1	0	1	2.048	kHz	488.281	µs
0	1	0	0	1	1	0	1.024	kHz	976.5625	µs
0	1	0	0	1	1	1	512	Hz	1.953125	ms
0	1	0	1	0	0	0	256	Hz	3.90625	ms
0	1	0	1	0	0	1	128	Hz	7.8125	ms
0	1	0	1	0	1	0	64	Hz	15.625	ms
0	1	0	1	0	1	1	32	Hz	31.25	ms
0	1	0	1	1	0	0	16	Hz	62.5	ms
0	1	0	1	1	0	1	8	Hz	125	ms
0	1	0	1	1	1	0	4	Hz	250	ms
0	1	0	1	1	1	1	2	Hz	500	ms
0	1	1	X	X	X	X	32.768	kHz	same as above defined by RS3–RS0	

Periodic Interrupt

The mux output used to drive the SQW output also drives the interrupt-generation circuitry. If the periodic interrupt event is enabled by writing a 1 to the periodic interrupt enable bit (PIE) in register C, an interrupt request is generated once every 122µs to 500ms. The period between interrupts is selected by the same bits in register A that select the square wave frequency (see Table 3). Setting OSC2–OSC0 in register A to 011 does not affect the periodic interrupt timing.

Alarm Interrupt

The alarm interrupt request is valid in battery-backup mode, providing a 'wake-up' capability. During each update cycle, the RTC compares the hours, minutes, and seconds bytes with the three corresponding alarm bytes. If a match of all bytes is found, the alarm interrupt event flag bit, A F in register C, is set to 1. If the alarm event is enabled, an interrupt request is generated.

An alarm byte may be removed from the comparison by setting it to a 'don't care" state. An alarm byte is set to a "don't care' state by writing a 1 to each of its two most-significant bits. A 'don't care" state may be used to select the frequency of alarm interrupt events as follows:

- If none of the three alarm bytes is 'don't care,' the frequency is once per day, when hours, minutes, and seconds match.
- If only the hour alarm byte is 'don't care,' the frequency is once per hour, when minutes and seconds match.
- If only the hour and minute alarm bytes are "don't care,' the frequency is once per minute, when seconds match.
- If the hour, minute, and second alarm bytes are 'don't care,' the frequency is once per second.

Update Cycle Interrupt

The update cycle ended flag bit (UF) in register C is set to a 1 at the end of an update cycle. If the update interrupt enable bit (UIE) of register B is 1, and the update transfer inhibit bit (UTI) in register B is 0, then an interrupt request is generated at the end of each update cycle.

Accessing RTC bytes

Time and calendar bytes read during an update cycle may be in error. Three methods to access the time and calendar bytes without ambiguity are:

- Enable the update interrupt event to generate interrupt requests at the end of the update cycle. The interrupt handler has a maximum of 999ms to access the clock bytes before the next update cycle begins (see Figure 3).
- Poll the update-in-progress bit (UIP) in register A. If UIP = 0, the polling routine has a minimum of t_{BUC} time to access the clock bytes (see Figure 3).
- Use the periodic interrupt event to generate interrupt requests every t_{PI} time, such that UIP = 1 always occurs between the periodic interrupts. The interrupt handler will have a minimum of $t_{PI}/2 + t_{BUC}$ time to access the clock bytes (see Figure 3).

Oscillator Control

When power is first applied to the bq4285E/bq4285L and V_{CC} is above V_{PFD}, the internal oscillator and frequency divider are turned on by writing a 010 pattern to bits 4 through 6 of register A. A pattern of 011 behaves as 010 but additionally transforms register C into a read/write register. This allows the 32,768kHz output on the square

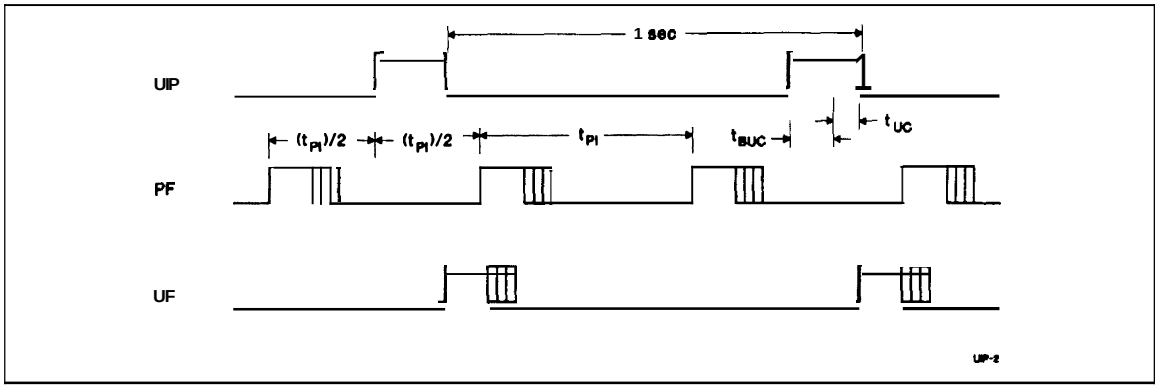


Figure 3. Update-Ended/Periodic Interrupt Relationship

wave pin to be turned on. A pattern of 11X turns the oscillator on, but keeps the frequency divider disabled. Any other pattern to these bits keeps the oscillator off.

Power-Down/Power-Up Cycle

The bq4285E/bq4285L power-up/power-down cycles are different. The bq4285L continuously monitors V_{CC} for out-of-tolerance. During a power failure, when Vcc falls below V_{PFD} (2.53V typical), the bq4285L write-protects the clock and storage registers. The power source is switched to BC when V_{CC} is less than V_{PFD} and BC is greater than V_{PFD}, or when V_{CC} is less than V_{BC} and V_{BC} is less than V_{PFD}. RTC operation and storage data are sustained by a valid backup energy source. When V_{CC} is above V_{PFD}, the power source is V_{CC}. Write-protection continues for t_{CSR} time after Vcc rises above V_{PFD}.

The bq4285E continuously monitors V_{CC} for out-of-tolerance. During a power failure, when V_{CC} falls below V_{PFD} (4.17V typical), the bq4285E write-protects the clock and storage registers. When V_{CC} is below V_{BC} (3V typical), the power source is switched to BC. RTC operation and storage data are sustained by a valid backup energy source. When V_{CC} is above V_{BC}, the power source is Vcc. Write-protection continues for t_{CSR} time after Vcc rises above V_{PFD}.

An external CMOS static RAM is battery-backed using the V_{OUT} and chip enable output pins from the bq4285E/bq4285L. As the voltage input Vcc slows down during a power failure, the chip enable output, $\overline{CE}_{OUT}$, is forced inactive independent of the chip enable input $\overline{CE}_{IN}$.

This activity unconditionally write-protects the external SRAM as V_{CC} falls below V_{PFD}. If a memory access is in process to the external SRAM during power-fail detection, that memory cycle continues to completion before the memory is write-protected. If the memory cycle is not terminated within time t_{WPT} (30µs maximum), the chip enable output is unconditionally driven high, write-protecting the controlled SRAM.

As the supply continues to fall past V_{PFD}, an internal switching device forces Vow to the external backup energy source. $\overline{CE}_{OUT}$ is held high by the Vow energy source.

During power-up, V_{OUT} is switched back to the main supply as V_{CC} rises above the backup cell input voltage sourcing V_{OUT}. If V_{PFD} < V_{BC} on the bq4285L, the switch to the main supply occurs at V_{PFD}. $\overline{CE}_{OUT}$ is held inactive for time t_{CER} (200ms maximum) after the power supply has reached V_{PFD}, independent of the $\overline{CE}_{IN}$ input, to allow for processor stabilization.

During power-valid operation, the $\overline{CE}_{IN}$ input is passed through to the $\overline{CE}_{OUT}$ output with a propagation delay of less than 10ns.

Figure 4 shows the hardware hookup for the external RAM.

A primary backup energy source input is provided on the bq4285E/bq4285L. The BC input accepts a 3V primary battery, typically some type of lithium chemistry. To prevent battery drain when there is no valid data to retain, Vow and $\overline{CE}_{OUT}$ are internally isolated from BC by the initial connection of a battery. Following the first application of V_{CC} above V_{PFD}, this isolation is broken, and the backup cell provides power to V_{OUT} and $\overline{CE}_{OUT}$ for the external SRAM.

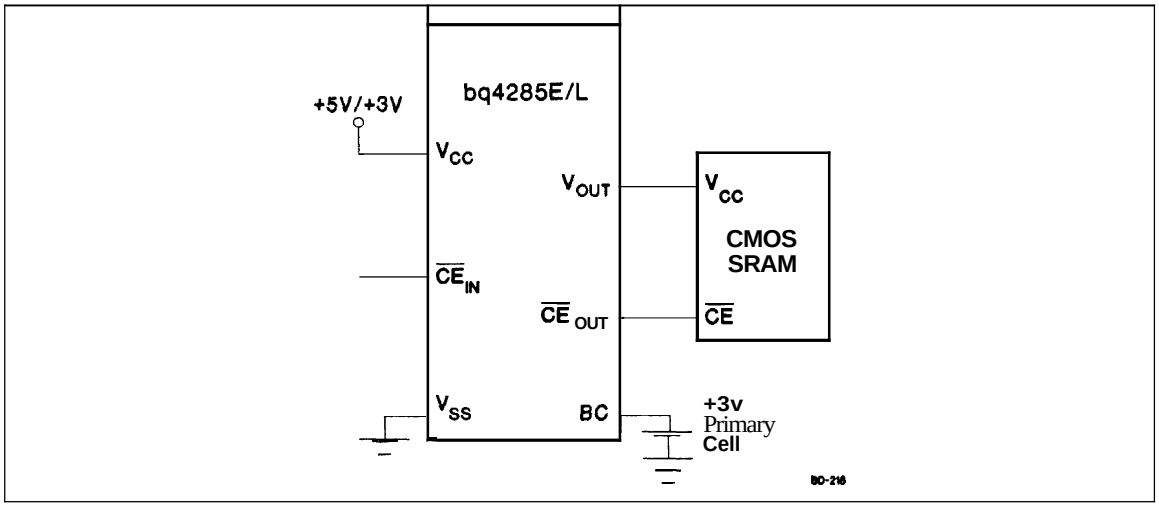


Figure 4. External RAM Hookup to the bq4285E/bq4285L RTC

Control/Status Registers

The four control/status registers of the bq4285E/bq4285L are accessible regardless of the status of the update cycle (see Table 4).

Register A

Register A Bits							
7	6	5	4	3	2	1	0
UIP	OS2	OS1	OS0	RS3	RS2	RS1	RS0

Register A programs:

- The frequency of the square-wave and the periodic event rate.
- Oscillator operation.

Register A provides:

- Status of the update cycle.

RS0–RS3 - Frequency Select

7	6	5	4	3	2	1	0
-	-	-	-	RS3	RS2	RS1	RS0

These bits select one of the 13 frequencies for the SQW output and the periodic interrupt rate, as shown in Table 3.

OS0–OS2 - Oscillator Control

7	6	5	4	3	2	1	0
-	OS2	OS1	OS0	-	-	-	-

These three bits control the state of the oscillator and divider stages. A pattern of 010 enables RTC operation by turning on the oscillator and enabling the frequency divider. A pattern of 011 behaves as 010 but additionally transforms register C into a read/write register. This allows the 32.768kHz output on the square wave pin to be turned on. A pattern of 11X turns the oscillator on, but keeps the frequency divider disabled. When 010 is written, the RTC begins its first update after 500ms.

UIP - Update Cycle Status

7	6	5	4	3	2	1	0
UIP	-	-	-	-	-	-	-

This read-only bit is set prior to the update cycle. When UIP equals 1, an RTC update cycle may be in progress. UIP is cleared at the end of each update cycle. This bit is also cleared when the update transfer inhibit (UTI) bit in register B is 1.

Register B

Register B Bits							
7	6	5	4	3	2	1	0
UTI	PIE	AIE	UIE	SQWE	DF	HF	DSE

Register B enables:

- Update cycle transfer operation
- Square-wave output
- Interrupt events
- Daylight saving adjustment

Register B selects:

- Clock and calendar data formats

All bits of register B are read/write.

5

Table 4. Control/Status Registers

Reg.	Loc. (Hex)	Read	Write	Bit Name and State on Reset													
				7 (MSB)		6		5		4		3		2		1	0 (LSB)
A	0A	Yes	Yes[1]	UIP	na	OS2	na	OS1	na	OS0	na	RS3	na	RS2	na	RS1	na	RS0	na
B	0B	Yes	Yes	UTI	na	PIE	0	AIE	0	UIE	0	SQWE	0	DF	na	HF	na	DSE	na
C	0C	Yes	No[2]	INTF	0	PF	0	AF	0	UF	0	-	0	32KE	na	-	0	-	0
D	0D	Yes	No	VRT	na	-	0	-	0	-	0	-	0	-	0	-	0	-	0

Notes: na = not affected.

1. Except bit 7.
2. Read/write only when OSC2–OSC0 in register A is 011 (binary).

DSE - Daylight Saving Enable

7	6	5	4	3	2	1	0
						-	DSE

This bit enables daylight-saving time adjustments when written to 1:

- On the last Sunday in October, the first time the bq4285E/bq4285L increments past 1:59:59 AM, the time falls back to 1:00:00 AM.
- On the first Sunday in April, the time springs forward from 2:00:00 AM to 3:00:00 AM.

HF - Hour Format

7	6	5	4	3	2	1	0
-	-	-	-	-	-	HF	-

This bit selects the time-of-day and alarm hour format:

1 = 24-hour format

0 = 12-hour format

DF - Data Format

7	6	5	4	3	2	1	0
-	-	-	-	-	DF	-	-

This bit selects the numeric format in which the time, alarm, and calendar bytes are represented:

1 = Binary

0 = BCD

SQWE - Square-Wave Enable

7	6	5	4	3	2	1	0
			-	SQWE	-	-	-

This bit enables the square-wave output:

1 = Enabled

0 = Disabled and held low

UIE - Update Cycle Interrupt Enable

7	6	5	4	3	2	1	0
-	-	-	UIE	-	-	-	-

This bit enables an interrupt request due to an update ended interrupt event:

1 = Enabled

0 = Disabled

The UIE bit is automatically cleared when the UTI bit equals 1.

AIE - Alarm Interrupt Enable

7	6	5	4	3	2	1	0
-	-	AIE	-	-	-	-	-

This bit enables an interrupt request due to an alarm interrupt event:

1 = Enabled

0 = Disabled

PIE - Periodic Interrupt Enable

7	6	5	4	3	2	1	0
-	PIE	-	-	-	-	-	-

This bit enables an interrupt request due to a periodic interrupt event:

1 = Enabled

0 = Disabled

UTI - Update Transfer Inhibit

7	6	5	4	3	2	1	0
UTI	-	-	-	-	-	-	-

This bit inhibits the transfer of RTC bytes to the user buffer:

1 = Inhibits transfer and clears UIE

0 = Allows transfer

Register C

Register C Bits							
7	6	5	4	3	2	1	0
INTF	PF	AF	UF	0	32KE	0	0

Register C is the read-only event status register.

Bits 0–3 - Unused Bits

7	6	5	4	3	2	1	0
		I	-	(	0	1	-	1	0	1	0

These bits are always set to 0.

32KE–32KHz Enable Output

7	6	5	4	3	2	1	0
-	-	-	-	-	32KE	-	-

This bit may be set to a 1 only when the OSC2–OSC0 bits in register A are set to 011. Setting OSC2–OSC0 to anything other than 011 clears this bit. If SQWE in register B and 32KE are set, a 32.768KHz waveform is output on the square wave pin.

UF - Update-Event Flag

7	6	5	4	3	2	1	0
-	-	-	UF	-	-	-	-

This bit is set to a 1 at the end of the update cycle. Reading register C clears this bit.

AF - Alarm Event Flag

7	6	5	4	3	2	1	0
	-	AF	-	-	-	-	-

This bit is set to a 1 when an alarm event occurs. Reading register C clears this bit.

PF - Periodic Event Flag

7	6	5	4	3	2	1	0
-	PF	-	-	-	-	-	-

This bit is set to a 1 every t_{PI} time, where t_{PI} is the time period selected by the settings of RS0–RS3 in register A. Reading register C clears this bit.

INTF - interrupt Request Flag

7	6	5	4	3	2	1	0
INTF	-	-	-	-	-	-	-

This flag is set to a 1 when any of the following is true:

AIE = 1 and AF = 1

PIE = 1 and PF = 1

UIE = 1 and UF = 1

Reading register C clears this bit.

Register D

Reaister D Bits							
7	6	5	4	3	2	1	0
VRT	0	0	0	0	0	0	0

Register D is the read-only data integrity status register.

Bits 0–6 - Unused Bits

7	6	5	4	3	2	1	0
-	0	0	0	0	0	0	0

These bits are always set to 0.

VRT - Valid RAM and Time

7	6	5	4	3	2	1	0
VRT	-	-	-	-	-	-	-

1 = Valid backup energy source

0 = Backup energy source is depleted

When the backup energy source is depleted (VRT = 0), data integrity of the RTC and storage registers is not guaranteed.

5

Absolute Maximum Ratings—bq4285E

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on Vcc relative to Vss	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding Vcc relative to Vss	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
		-40 to +85	°C	Industrial "N"
T_{STG}	Storage temperature	-55 to +125	°C	
T_{BIAS}	Temperature under bias	-40 to +85	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Absolute Maximum Ratings—bq4285L

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on Vcc relative to Vss	-0.3 to 6.0	V	
V_T	DC voltage applied on any pin excluding Vcc relative to Vss	-0.3 to 6.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
T_{STG}	Storage temperature	-55 to +125	°C	
T_{BIAS}	Temperature under bias	-40 to +85	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions—bq4285E (T_A = T_{OPR})

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IL}	Input low voltage	-0.3		0.8	V
V_{IH}	Input high voltage	2.2		V_{CC} + 0.3	V
V_{BC}	Backup cell voltage	2.6		4.0	V

Notes: Typical values indicate operation at T_A = 25°C.
Potentials are relative to V_{SS}.

Recommended DC Operating Conditions—bq4285L (T_A = T_{OPR})

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{CC}	Supply voltage	2.7	3.15	3.6	V
V_{IL}	Input low voltage	-0.3		0.6	V
V_{IH}	Input high voltage	2.2		V_{CC} + 0.3	V
V_{BC}	Backup cell voltage	2.4		4.0	V

Notes: Typical values indicate operation at T_A = 25°C.
Potentials are relative to V_{SS}.

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Crystal Specifications—bq4285E/bq4285L (DT-26 or Equivalent)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
f_O	Oscillation frequency		32.768		kHz
C_L	Load capacitance		6		pF
T_P	Temperature turnover point	20	25	30	°C
k	Parabolic curvature constant			-0.042	ppm/°C
Q	Quality factor	40,000	70,000		
R_1	Series resistance			45	KR
C_0	Shunt capacitance		1.1	1.8	pF
C_0/C_1	Capacitance ratio		430	600	
D_L	Drive level			1	µW
$\Delta f/f_O$	Aging (first year at 25°C)		1		ppm

DC Electrical Characteristics—bq4285E ($T_A = T_{OPR}$, VCC = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current			± 1	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current			± 1	µA	AD_0–AD_7, $\overline{INT}$, and SQW in high impedance, $V_{OUT} = V_{SS}$ to V_{CC}
V_{OH}	Output high voltage	2.4			V	I_{OH} = -2.0 mA
V_{OL}	Output low voltage			0.4	V	I_{OL} = 4.0 mA
I_{CC}	Operating supply current		7	15	mA	Min. cycle, duty = 100%, I_{OH} = 0mA, I_{OL} = 0mA
V_{SO}	Supply switch-over voltage		V_{BC}		V	
I_{CCB}	Battery operation current		0.3	0.5	µA	V_{BC} = 3V, T_A = 25°C, no load on V_{OUT} or $\overline{CE}_{OUT}$
I_{CCSB}	Standby supply current		300		µA	V_{IN} = Vcc or V_{SS}, $\overline{CS} \geq V_{CC}$ - 0.2, no load on V_{OUT}
V_{PFD}	Power-fail-detect voltage	4.0	4.17	4.35	V	
V_{OUT1}	Vow voltage	Vcc - 0.3V	-		V	I_{OUT} = 100mA, $V_{CC} > V_{BC}$
V_{OUT2}	V_{OUT} voltage	V_{BC} - 0.3V				I_{OUT} = 100µA, Vcc < V_{BC}
I_{MOTH}	Input current when MOT = Vcc			-275	µA	Internal 20K pull-down
ICE	Chip enable input current			100	µA	Internal 50K pull-up

Note: Typical values indicate operation at T_A = 25°C, Vcc = 5V or V_{BC} = 3V.

DC Electrical Characteristics—bq4285L ($T_A = T_{OPR}$, V_{CC} = 3.13V ± 0.45%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current			± 1	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current			± 1	µA	AD_0–AD_7, $\overline{INT}$, and SQW in high impedance, $V_{OUT} = V_{SS}$ to V_{CC}
V_{OH}	Output high voltage	2.2			V	I_{OH} = -2.0 mA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 4.0 mA
I_{CC}	Operating supply current		5	9	mA	Mia cycle, duty = 100%, I_{OH} = 0mA, I_{OL} = 0mA
V_{SO}	Supply switch-over voltage		V_{PFD}		V	$V_{BC} > V_{PFD}$
			V_{BC}		V	$V_{BC} < V_{PFD}$
I_{CCB}	Battery operation current	-	0.3	0.5	µA	V_{BC} = 3V, T_A = 25°C, no load on V_{OUT} or $\overline{CE}_{OUT}$
I_{CCSB}	Standby supply current	-	100	-	µA	$V_{IN} = V_{CC}$ or V_{SS}, $\overline{CS} \geq V_{CC}$ - 0.2, no load on Vovr
V_{PFD}	Power-fail-detect voltage	2.4	2.53	2.65	V	
V_{OUT1}	V_{OUT} voltage	V_{CC} - 0.3V	-		V	Iovr = 80mA, $V_{CC} > V_{BC}$
V_{OUT2}	V_{OUT} voltage	V_{BC} - 0.3V				I_{OUT} = 100µA, Vcc < V_{BC}
I_{MOTH}	Input current when MOT = V_{CC}	-	-	-185	µA	Internal 30K pull-down
Ice	chip enable input current	-	-	120	µA	Internal 30K pull-up

Note: Typical values indicate operation at T_A = 25°C, Vcc = 3V.

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Capacitance—bq4285E/bq4285L (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance			7	pF	V_{OUT} = 0V
C_{IN}	Input capacitance			5	pF	V_{IN} = 0V

Note: This parameter is sampled and not 100% tested. It does not include the X1 or X2 pin.

AC Test Conditions—bq4285E

Parameter	Test Conditions
Input pulse levels	0 to 3.0 V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 5 and 6

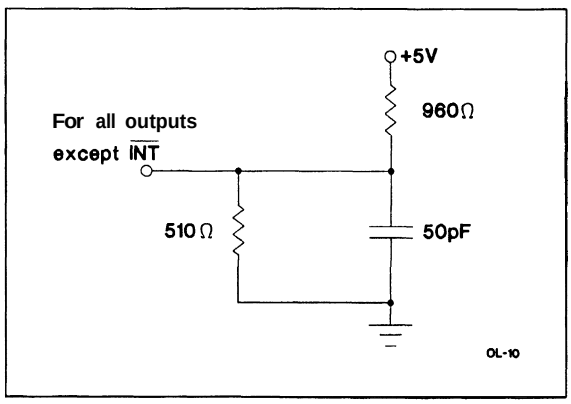

Figure 5. Output Load A—bq4285E

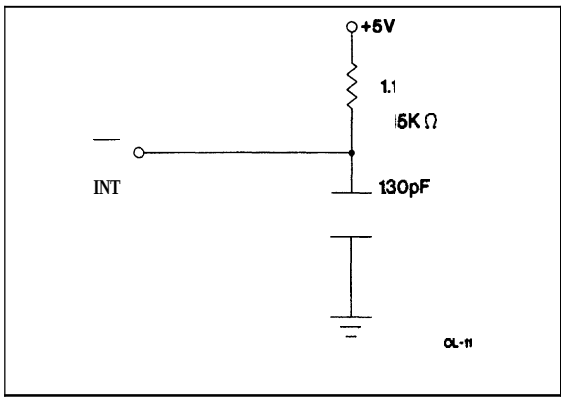

Figure 6. Output Load B—bq4285E

AC Test Conditions—bq4285L

Parameter	Test Conditions
Input pulse levels	0 to 2.3 V
Input rise and fall times	5 ns
Input and output timing reference levels	1.2 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 7 and 8

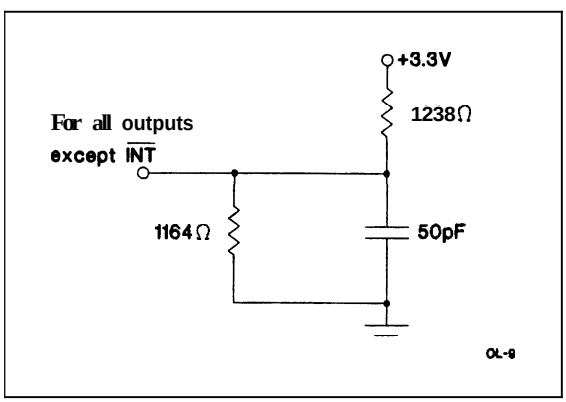

Figure 7. Output Load A—bq4285L

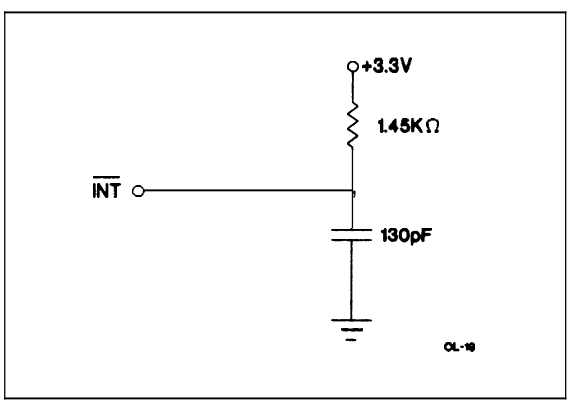

Figure 8. Output Load B—bq4285L

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Read/Write Timing—bq4285E (T_A = TOPR, V_{CC} = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYC}	Cycle time	160			ns	
t_{DSL}	DS low or $\overline{RD}/\overline{WR}$ high time	80			ns	
t_{DSH}	DS high or $\overline{RD}/\overline{WR}$ low time	55			ns	
t_{RWH}	R/$\overline{W}$ hold time	0			ns	
t_{RWS}	R/$\overline{W}$ setup time	10			ns	
t_{CS}	Chip select setup time	5			ns	
t_{CH}	Chip select hold time	0			ns	
t_{DHR}	Read data hold time	0		25	ns	
t_{DHW}	Write data hold time	0			ns	
t_{AS}	Address setup time	20			ns	
t_{AH}	Address hold time	5			ns	
t_{DAS}	Delay time, DS to AS rise	10			ns	
t_{ASW}	Pulse width, AS high	30			ns	
t_{ASD}	Delay time, AS to DS rise ($\overline{RD}/\overline{WR}$ fall)	35			ns	
t_{OD}	Output data delay time from DS rise ($\overline{RD}$ fall)			50	ns	
t_{DW}	Write data setup time	30			ns	
t_{BUC}	Delay time before update		244		µs	
t_{PI}	Periodic interrupt time interval					See Table 3
t_{UC}	Time of update cycle		1		µs	

Read/Write Timing—bq4285L ($T_A = T_{OPR}$, V_{CC} = 3.15V ± 0.45%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYC}	Cycle time	270			ns	
t_{DSL}	DS low or $\overline{RD}/\overline{WR}$ high time	135			ns	
t_{DSH}	DS high or $\overline{RD}/\overline{WR}$ low time	90			ns	
t_{RWH}	R/$\overline{W}$ hold time	0			ns	
t_{RWS}	R/$\overline{W}$ setup time	15			ns	
t_{CS}	Chip select setup time	8			ns	
t_{CH}	Chip select hold time	0			ns	
t_{DHR}	Read data hold time	0		40	ns	
t_{DHW}	Write data hold time	0			ns	
t_{AS}	Address setup time	30			ns	
t_{AH}	Address hold time	15			ns	
t_{DAS}	Delay time, DS to AS rise	15			ns	
t_{ASW}	Pulse width. AS high	50			ns	
t_{ASD}	Delay time, AS to DS rise ($\overline{RD}/\overline{WR}$ fall)	55			ns	
t_{OD}	Output data delay time from DS rise ($\overline{RD}$ fall)			100	ns	
t_{DW}	Write data setup time	50			ns	
t_{BUC}	Delay time before update		244		µs	
t_{PI}	Periodic interrupt time interval					See Table 3
t_{UC}	Time of update cycle		1		µs	

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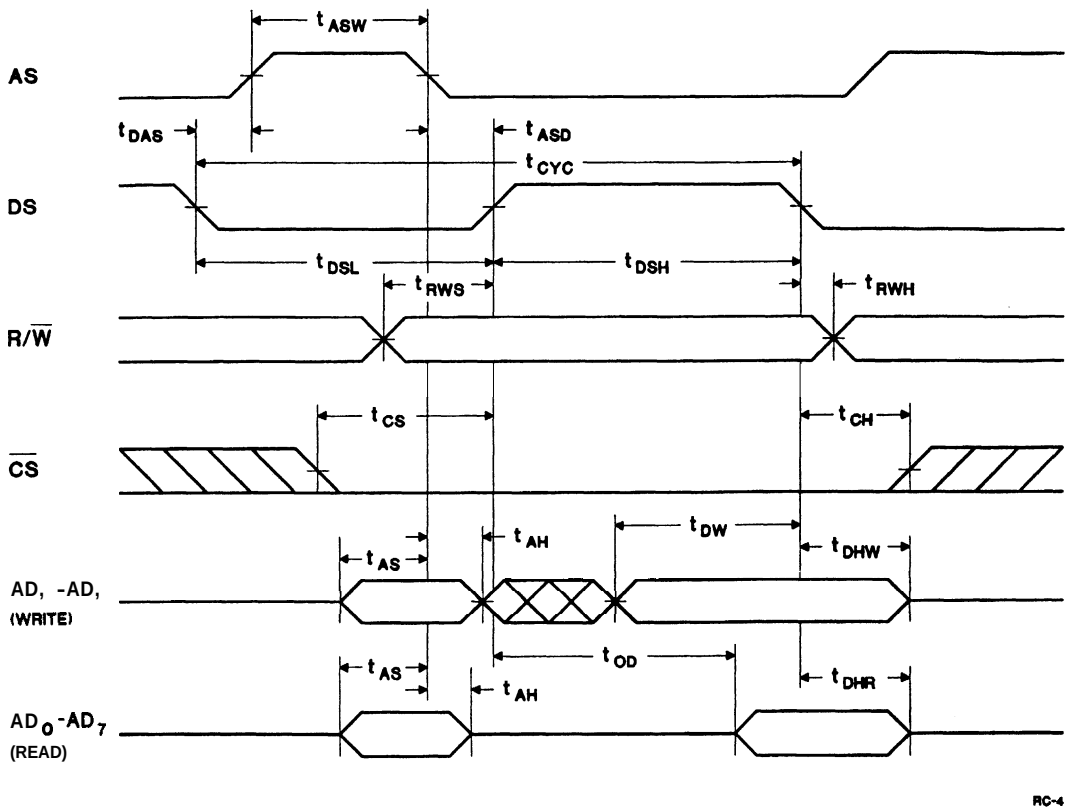
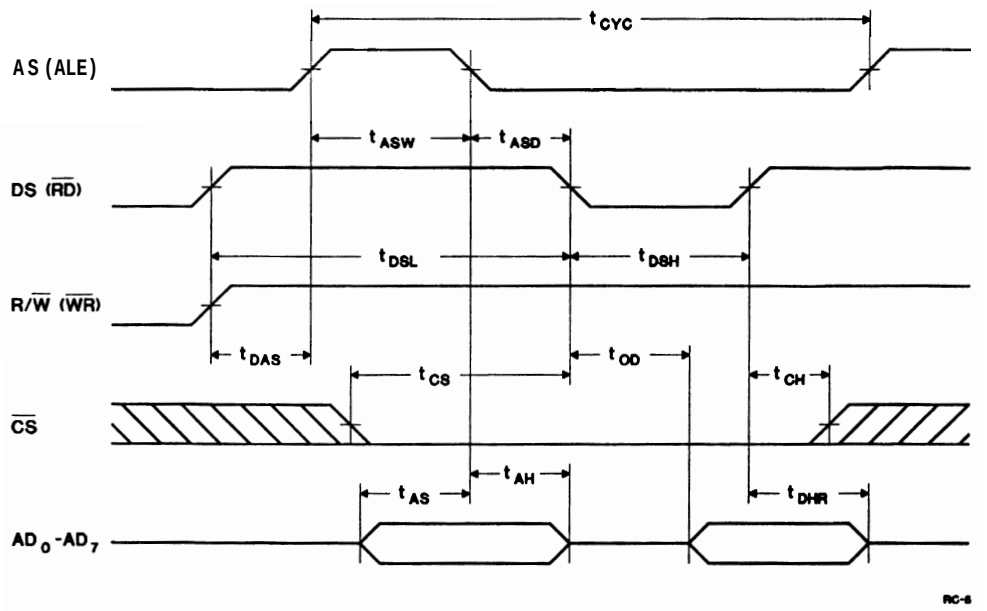
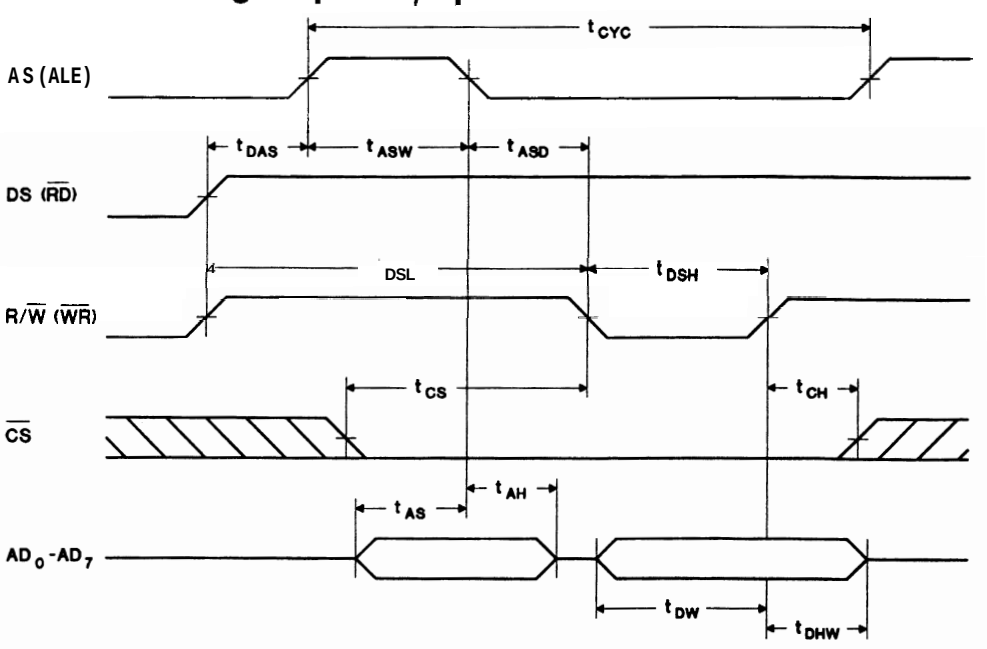
Motorola Bus **Read/Write Timing—bq4285E/bq4285L** (PLCC Package Only)



Intel Bus Read Timing—bq4285E/bq4285L



Intel Bus Write Timing—bq4285E/bq4285L

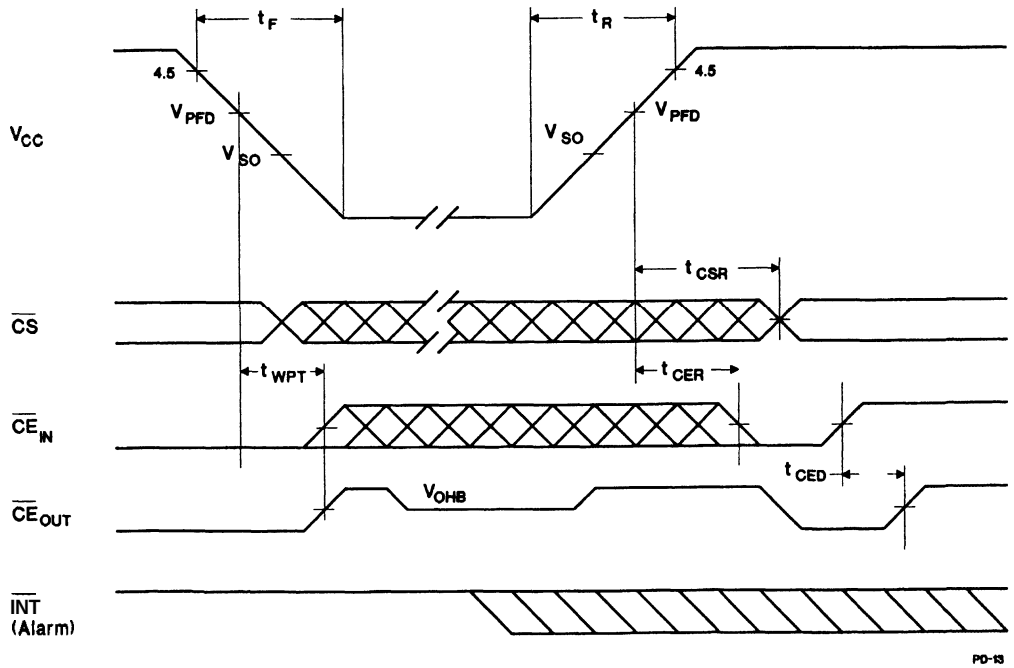


Power-Down/Power-Up Timing—bq4285E (T_A = T_{OPR})

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_F	V_{CC} slew from 4.5V to 0V	300			µs	
t_R	V_{CC} slew from 0V to 4.5V	100				
t_{CSR}	$\overline{CS}$ at V_{IH} after power-up	20		200	ms	Internal write-protection period after V_{CC} passes V_{PFD} on power-up.
t_{WPT}	Write-protect time for external RAM	10	16	30	µs	Delay after V_{CC} slows down past V_{PFD} before SRAM is write-protected.
t_{CER}	Chip enable recovery time	t_{CSR}		t_{CSR}	ms	Time during which external SRAM is write-protected after V_{CC} passes V_{PFD} on power-up.
t_{CED}	Chip enable propagation delay to external SRAM		7	10	ns	

Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

Power-Down/Power-Up Timing—bq4285E

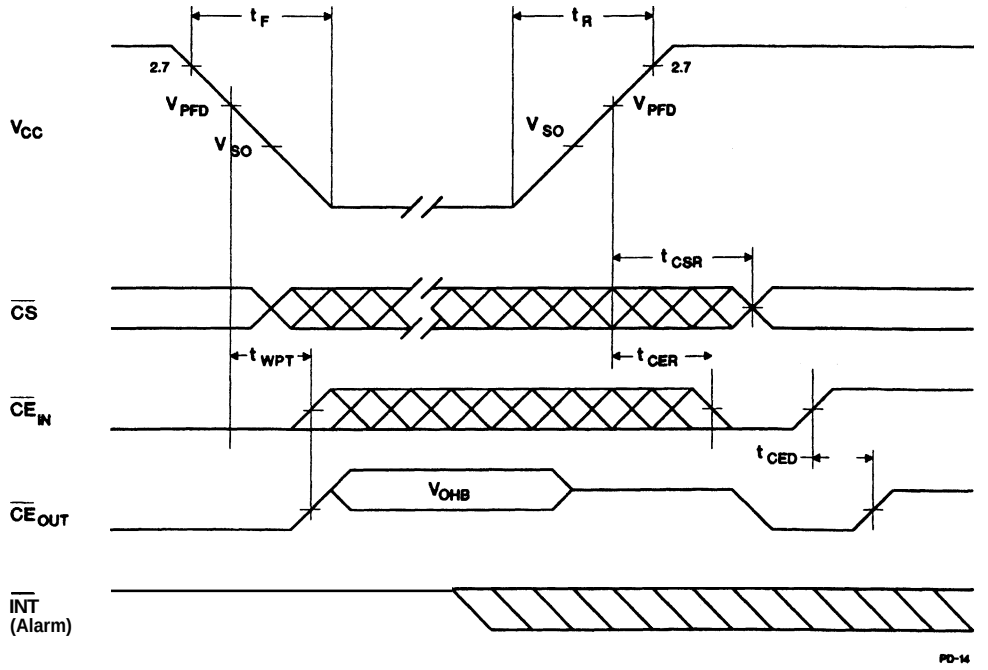


Power-Down/Power-Up Timing—bq4285L (TA = TOPR)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_F	V_{CC} slew from 2.7V to 0V	300				
t_R	V_{CC} slew from 0V to 2.7V	100			µs	
t_{CSR}	$\overline{CS}$ at V_{IH} after power-up	20		200	ms	Internal write-protection period after V_{CC} passes V_{PFD} on power-up.
t_{WPT}	Write-protect time for external RAM		0			$V_{BC} > V_{PFD}$
		10	16	30	µs	$V_{BC} < V_{PFD}$
t_{CER}	Chip enable recovery time	t_{CSR}		t_{CSR}	ms	Time during which external SRAM is write-protected after V_{CC} passes V_{PFD} on power-up.
t_{CED}	Chip enable propagation delay to external SRAM		9	15	ns	

Caution. Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

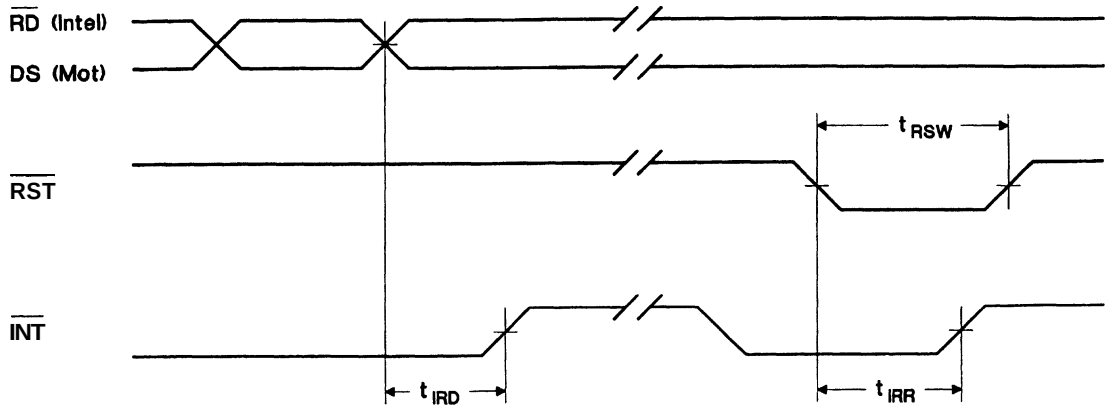
Power-Down/Power-Up Timing—bq4285L



Interrupt Delay Timing—bq4285E/bq4285L (TA = TOPR)

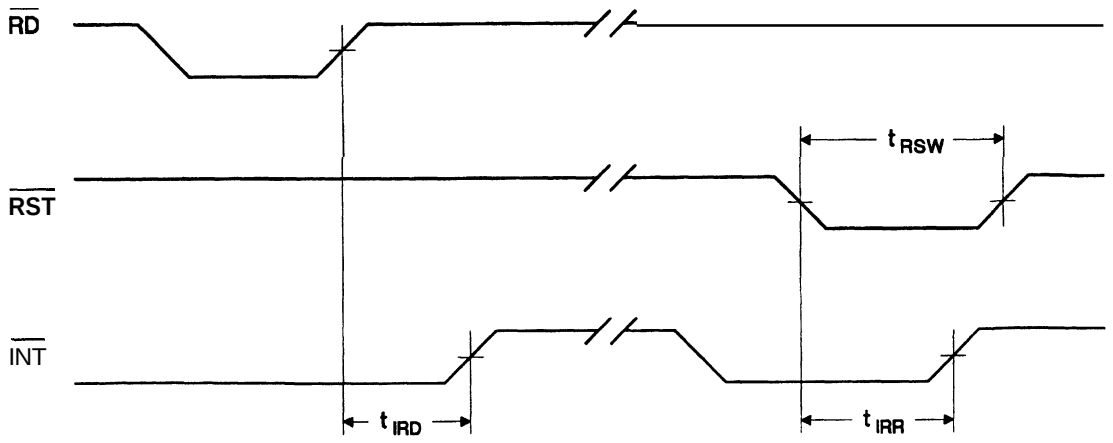
Symbol	Parameter	Minimum	Typical	Maximum	Unit
t_{RSW}	Reset pulse width	5			µs
t_{IRR}	$\overline{INT}$ release from $\overline{RST}$			2	µs
t_{IRD}	$\overline{INT}$ release from DS ($\overline{RD}$)			2	µs

Interrupt Delay Timing—bq4285E/bq4285L (PLCC Package Only)



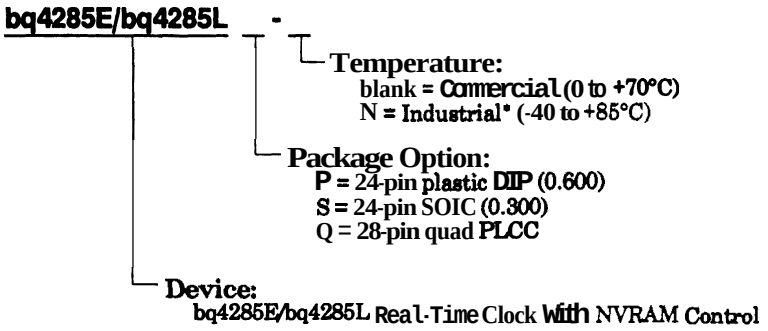
INT-1

Interrupt Delay Timing—bq4285E/bq4285L (SOIC, DIP Packages)



INT-4

Ordering Information



*bq4285E Q and S packages only.

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Notes

BENCHMARQ

bq4287

Real-Time Clock Module With NVRAM Control

Features

- Direct clock/calendar replacement for IBM® AT-compatible computers and other applications
- Functionally compatible with the DS1287/DS1287A and MC146818A
- 114 bytes of general nonvolatile storage
- Automatic backup supply and write-protection to make external SRAM nonvolatile
- Integral lithium cell and crystal
- 160 ns cycle time allows fast bus operation
- Intel bus timing
- 14 bytes for clock/calendar and control
- BCD or binary format for clock and calendar data
- Calendar in day of the week, day of the month, months, and years with automatic leap-year adjustment
- Time of day in seconds, minutes. and hours
  - 12- or 24-hour format
  - Optional daylight saving adjustment
- Programmable square wave output
- Three individually maskable interrupt event flags:
  - Periodic rates from 122 µs to 500 ms
  - Time-of-day alarm once per second to once per day
  - End-of-clock update cycle
- Better than one minute per month clock accuracy

General Description

The CMOS bq4287 is a low-power microprocessor peripheral providing a time-of-day clock and 100-year calendar with alarm features and battery operation. Other features include three maskable interrupt sources, square wave output, and 114 bytes of general nonvolatile storage.

The bq4287 write-protects the clock, calendar, and storage registers during power failure. The integral backup energy source then maintains data and operates the clock and calendar.

The bq4287 uses its integral battery-backup controller and battery to make a standard CMOS SRAM nonvolatile during power-fail conditions. During power-fail, the bq4287 automatically write-protects the external SRAM and provides a V_{CC} output sourced from its internal battery.

The bq4287 is a fully compatible real-time clock for IBM AT-compatible computers and other applications.

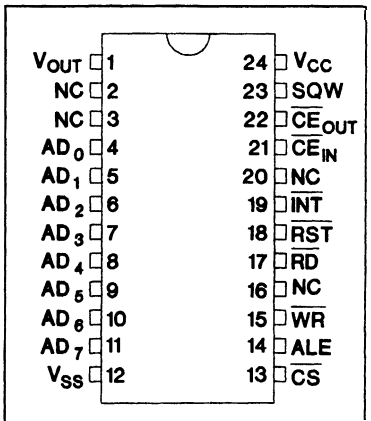
As shipped from Benchmarq, the backup cell is electrically isolated from the memory. Following the first application of V_{CC}, this isolation is broken, and the backup cell provides data retention to the clock, internal RAM, V_{OUT}, and $\overline{CE}_{OUT}$ on subsequent power-downs.

The bq4287 is functionally equivalent to the bq4285, except that the battery (16, 20) and crystal pins (2, 3) are not accessible. These pins are connected internally to a coin cell and quartz crystal. The coin cell provides 130mAh of capacity. For a complete description of features, operating conditions, electrical characteristics, bus timing, and pin descriptions, see the bq4285 data sheet.

Caution:

Take care to avoid inadvertent discharge through V_{OUT} and $\overline{CE}_{OUT}$ after battery isolation has been broken.

Pin Connections



24-Pin DIP Module

PN-29

Pin Names

AD0–AD7	Multiplexed address/data input/output
$\overline{CS}$	Chip select input
ALE	Address strobe input
	Data strobe input
$\overline{WR}$	Read/write input
$\overline{INT}$	Interrupt request output
$\overline{RST}$	Reset input
SQW	Square wave output
$\overline{CE}_{IN}$	RAM chip enable input
$\overline{CE}_{OUT}$	RAM chip enable output
NC	No connect
V_{OUT}	Supply output
V_{CC}	+5V supply
V_{SS}	Ground

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Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on Vcc relative to Vss	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding Vcc relative to Vss	-0.3 to 7.0	V	$V_T \le V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
T_{STG}	Storage temperature	-40 to +70	°C	Commercial
T_{BIAS}	Temperature under bias	-10 to +70	°C	Commercial
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IL}	Input low voltage	-0.3	-	0.8	V
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V

Note: Typical values indicate operation at $T_A = 25°C$.

DC Electrical Characteristics ($T_A = T_{OPR}$, $V_{CC} = 5V \pm 10\%$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
C	Battery capacity		130		mAh	Refer to graphs in *Typical* Battery Characteristics section
I_{LI}	Input leakage current			± 1	µA	V_{IN} = Vss to Vcc
I_{LO}	Output leakage current			± 1	µA	AD_0–AD_7, $\overline{INT}$ and SQW in high impedance
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 4.0 mA
I_{CC}	Operating supply current	-	7	15	mA	Min. cycle, duty = 100%, I_{OH} = 0mA, I_{OL} = 0mA
I_{CCB}	Battery operation current	-	0.3	0.5	µA	V_{BC} = 3V, T_A = 25°C, no load on V_{OUT} or $\overline{CE}_{OUT}$
V_{SO}	Supply switch-over voltage	-	3.0	-	V	
V_{PFD}	Power-fail-detect voltage	4.0	4.17	4.35	V	
V_{BC}	Backup cell voltage	-	3.0	-	V	Internal backup cell voltage; refer to graphs in Typical Battery Characteristics section
V_{OUT1}	V_{OUT} voltage	V_{CC} - 0.3V	-	-	V	I_{OUT} = 100mA, $V_{CC} > V_{BC}$
V_{OUT2}	V_{OUT} voltage	V_{BC} - 0.3V	-	-	V	I_{OUT} = 100µA, $V_{CC} < V_{BC}$
$I_{\overline{CE}}$	Chip enable input current	-	-	100	µA	Internal 50K pull-up

Note: Typical values indicate operation at $T_A = 25°C$, $V_{CC} = 5V$.

Power-Down/Power-Up Timing ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_F	V_{CC} slew from 4.5V to 0V	300			µs	
t_R	V_{CC} slew from 0V to 4.5V	100			µs	
t_{CSR}	$\overline{CS}$ at V_{IH} after power-up	20		200	me	Internal write-pmtection period after V_{CC} passes V_{PFD} on power-up.
t_{DR}	Data-retention and timekeeping time	10			years	T_A = 25°C, no load on V_{OUT} or $\overline{CE}_{OUT}$.
t_{WPT}	Write-protect time for external RAM	10	16	30	µs	Delay after V_{CC} slows down past V_{PFD} before SRAM is write-protected.
t_{CER}	Chip enable recovery time	t_{CSR}		t_{CSR}	ms	Time during which external SRAM is write-protected after V_{CC} passes V_{PFD} on power-up.
t_{CED}	Chip enable pmpagation delay to external SRAM		7	10	ns	

Note: Clock accuracy is better than ± 1 minute per month at 25°C for the period of t_{DR}.

Caution. Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

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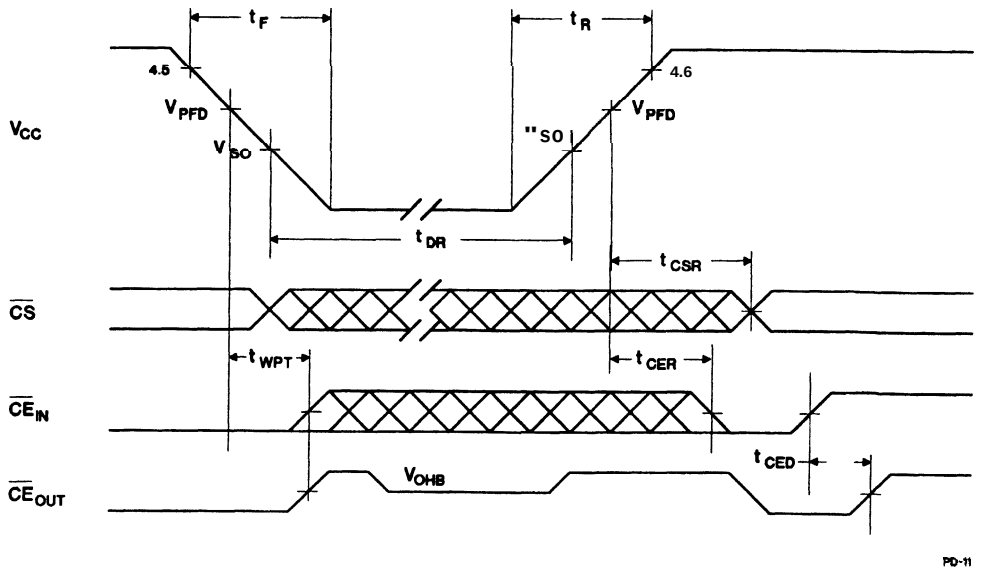
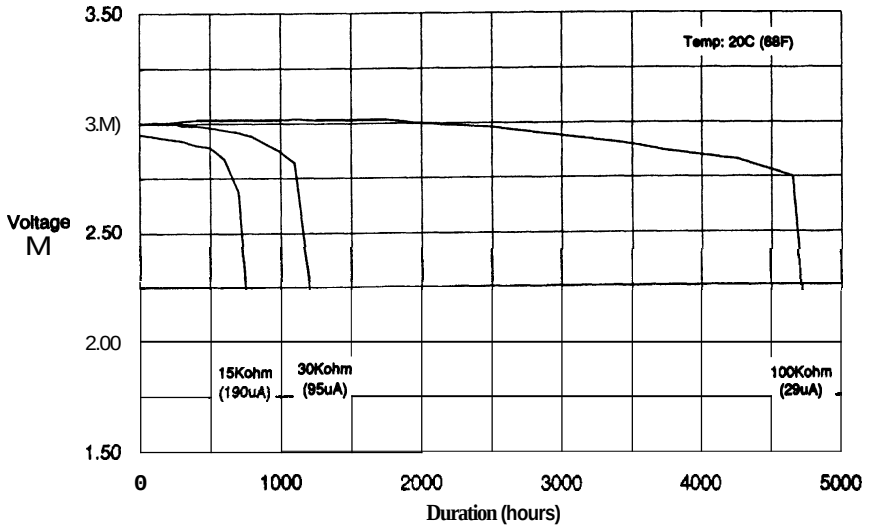
Power-Down/Power-Up Timing

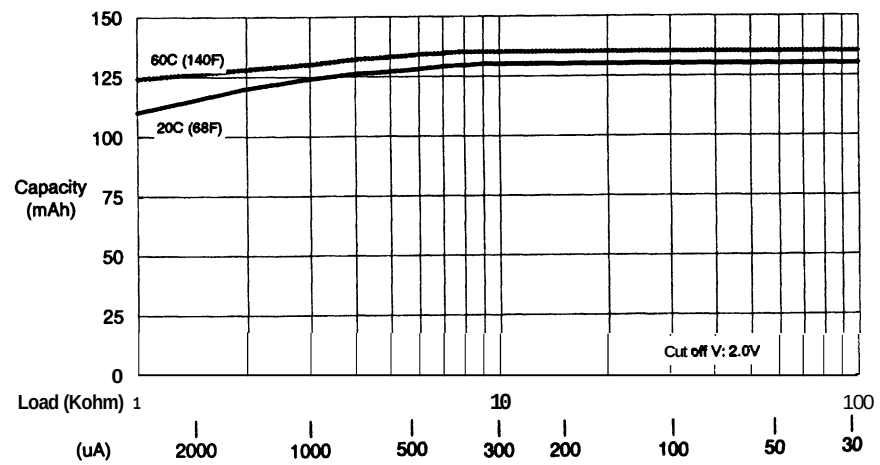


Typical Battery Characteristics (source = Panasonic)

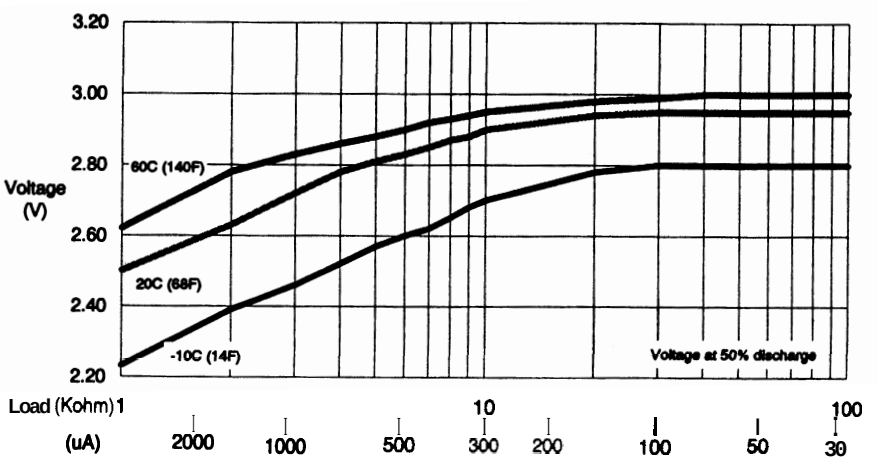
CR1632 Load Characteristics



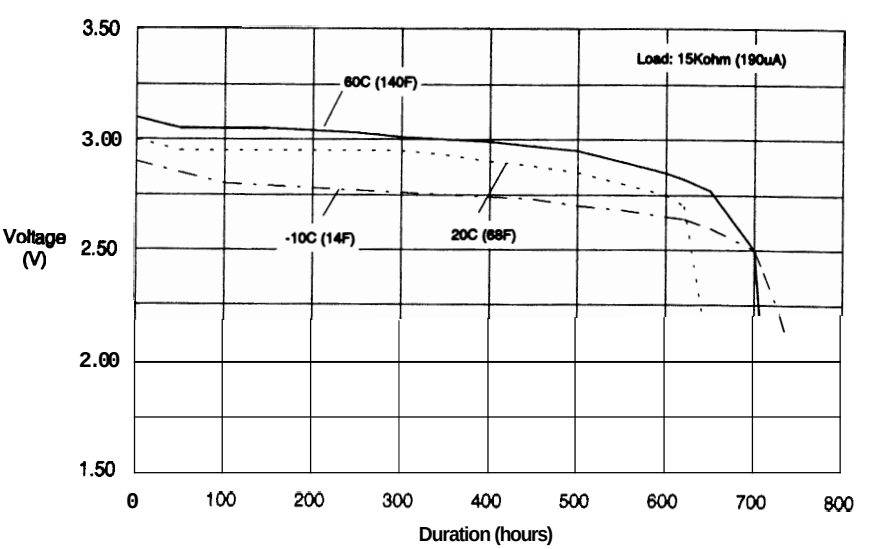
CR1632 Capacity vs. Load Resistance



CR1632 Operating Voltage vs. Load Resistance



CR1632 Temperature Characteristics

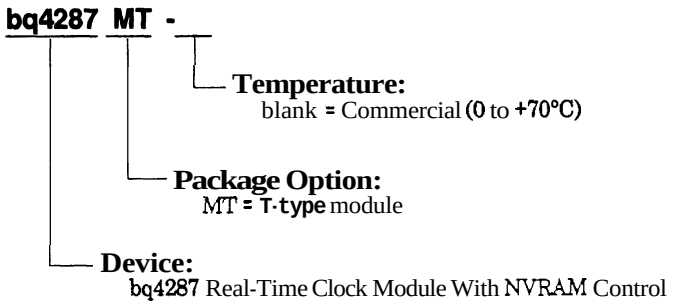


Data Sheet Revision History

Change	Page No.	Description	*Nature of* Change
1	2	Power-fail detect voltage VPFD	Was 4.1 min, 4.25 max; is 4.0 min, 4.36 max
1	2	Chip enable input current	Additional specification
2	9	Was: "As shipped from Benchmarq, the backup cell is electrically isolated from the memory." Is: 'As shipped from Benchmarq, the backup cell is electrically isolated from the active circuitry."	Clarification
2	14	Deleted specifications for t_{RWH} and t_{RWS}	Clarification; these parameters are not supported by the bq4287

Note: Change 1 = Nov. 1992 B changes from June 1991 A.
Change 2 = Nov. 1993 C changes from Nov. 1992 B.

Ordering Information



bq4287E

Enhanced RTC Module With NVRAM Control

Features

- Direct clock/calendar replacement for IBM® AT-compatible computers and other applications
- 114 bytes of general nonvolatile storage
- Enhanced features include:
  - System wake-up capability — alarm interrupt output active in battery-backup mode
  - 32kHz output for power management
- Automatic backup and write-protect control to external SRAM
- Integral lithium cell and crystal in 24-pin DIP module
- 160 ns cycle time allows fast bus operation
- Better than one minute per month clock accuracy
- 14 bytes for clock/calendar and control
- BCD or binary format for clock and calendar data
- Calendar in day of the week, day of the month, months, and years, with automatic leap-year adjustment
- Time of day in seconds, minutes, and hours
- Programmable square wave output
- Three individually maskable interrupt event flags:
  - Periodic rates from 122µs to 500ms
  - Time-of-day alarm once per second to once per day
  - End-of-clock update cycle

General Description

The CMOS bq4287E is a low-power microprocessor peripheral providing a time-of-day clock and 100-year calendar with alarm features and battery operation Other features include three maskable interrupt sources, square wave output, and 114 bytes of general nonvolatile storage.

A 32.768kHz output is available for sustaining power-management activitiee. Wake-up capability is provided by an alarm interrupt, which is active in battery-backup mode.

The bq4287E write-protects the clock, calendar, and storage registers during power failure. The integral backup energy source then maintains data and operates the clock and calendar.

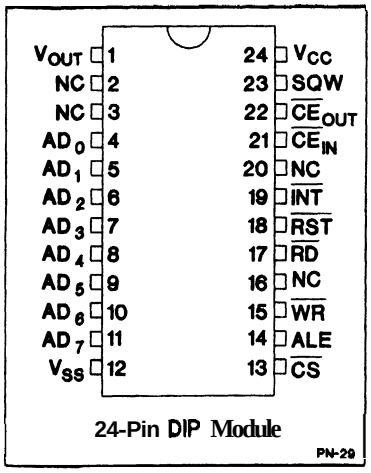
The bq4287E is a fully compatible real-time clock for IBM AT-compatible computers and other applications.

The bq4287E integrates a battery-backup controller and battery to make a standard CMOS SRAM nonvolatile during power-fail conditions. During power-fail, the bq4287E automatically write-protects the external SRAM and provides a V_{CC} output sourced from its internal battery.

As shipped from Benchmarq, the backup cell is electrically isolated from the memory. Following the first application of Vcc, this isolation is broken, and the backup cell provides data retention to the clock, internal RAM, V_{OUT}, and $\overline{CE}_{OUT}$ on subsequent power-downs.

The bq4287E is functionally equivalent to the bq4285E, except the battery (16, 20) and crystal pin (2, 3) are not accessible. These pins are connected internally to a coin cell and quartz crystal. The coin cell provides 130mAh of capacity. For a complete description of features, operating conditions, electrical characteristics, bus timing, and pin descriptions, see the bq4285E data sheet.

Pin Connections



24-Pin DIP Module

Pin Names

AD_0-AD_7	Multiplexed address/data input/output
$\overline{CS}$	Chip select input
ALE	Address strobe input
$\overline{RD}$	Data strobe input
$\overline{WR}$	Read/write input
$\overline{INT}$	Interrupt request output
$\overline{RST}$	Reset input
SQW	Square wave output
$\overline{CE}_{IN}$	RAM chip enable input
$\overline{CE}_{OUT}$	RAM chip enable output
NC	No connect
V_{OUT}	Supply output
V_{CC}	+5V supply
V_{SS}	Ground

Caution:

Take care to avoid inadvertent discharge through V_{OUT} and $\overline{CE}_{OUT}$ after battery isolation has been broken.

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Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on Vcc relative to Vss	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding Vcc relative to Vss	-0.3 to 7.0	V	$V_T \le V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	"C	Commercial
		-40 to +85	°C	Industrial "N"
T_{STG}	Storage temperature	-40 to +70	"C	Commercial
		-40 to +85	°C	Industrial "N"
T_{BIAS}	Temperature under bias	-10 to +70	°C	Commercial
		-40 to +85	"C	Industrial "N"
T_{SOLDER}	Soldering temperature	260	"C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Electrical Characteristics ($T_A = T_{OPR}$, $V_{CC} = 5V \pm 10\%$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
C	Battery capacity		130		mAh	Refer to graphs in Typical Battery Characteristics section
I_{LI}	Input leakage current			± 1	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current			± 1	µA	AD_0–AD_7, $\overline{INT}$ and SQW in highimpedance
V_{OH}	Output high voltage	2.4			V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage			0.4	V	I_{OL} = 4.0 mA
I_{CC}	Operating supply current		7	15	mA	Min. cycle, duty = 100%, I_{OH} = 0mA, I_{OL} = 0mA
I_{CCB}	Battery operation current		0.3	0.5	µA	V_{BC} = 3V, T_A = 25°C, no load on Vow or $\overline{CE}_{OUT}$
I_{CCSB}	Standby supply current		300		µA	$V_{IN} = V_{CC}$ or V_{SS}, $\overline{CS} = \overline{CE}_{IN} \ge V_{CC} - 0.2$, no load on Vom
V_{SO}	Supply switch-over voltage		3.0		V	
V_{PFD}	Power-fail-detect voltage	4.0	4.17	4.35	V	
V_{BC}	Backup cell voltage		3.0		V	Internal backup cell voltage; refer to graphs in Typical Battery Characteristics section
V_{OUT1}	Vow voltage	V_{CC} - 0.3V			V	I_{OUT} = 100mA, $V_{CC} > V_{BC}$
V_{OUT2}	Vow voltage	V_{BC} - 0.3V			V	I_{OUT} = 100µA, $V_{CC} < V_{BC}$
$I_{\overline{CE}}$	Chip enable input current			100	µA	Internal 50K pull-up

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.

Power-Down/Power-Up Timing ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_F	V_{CC} slew from 4.5V to 0V	300				
t_R	V_{CC} slew from 0V to 4.5V	100				
t_{CSR}	$\overline{CS}$ at V_{IH} after power-up	20		200	me	Internal write-protection period after V_{CC} passes V_{PFD} on power-up.
t_{DR}	Data-retention and timekeeping time	10			years	T_A = 25°C, no load on V_{OUT} or $\overline{CE}_{OUT}$.
t_{WPT}	Write-protect time for external RAM	10	16	30	µs	Delay after V_{CC} elews down past V_{PFD} before SRAM is write-protected.
t_{CER}	Chip enable recovery time	t_{CSR}		t_{CSR}	ms	Time during which external SRAM is write-protected after V_{CC} passes V_{PFD} on power-up.
t_{CED}	Chip enable propagation delay to external SRAM		7	10	ns	

Note: Clock accuracy is better than ± 1 minute per month at 25°C for the period of t_{DR}.

Caution. Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

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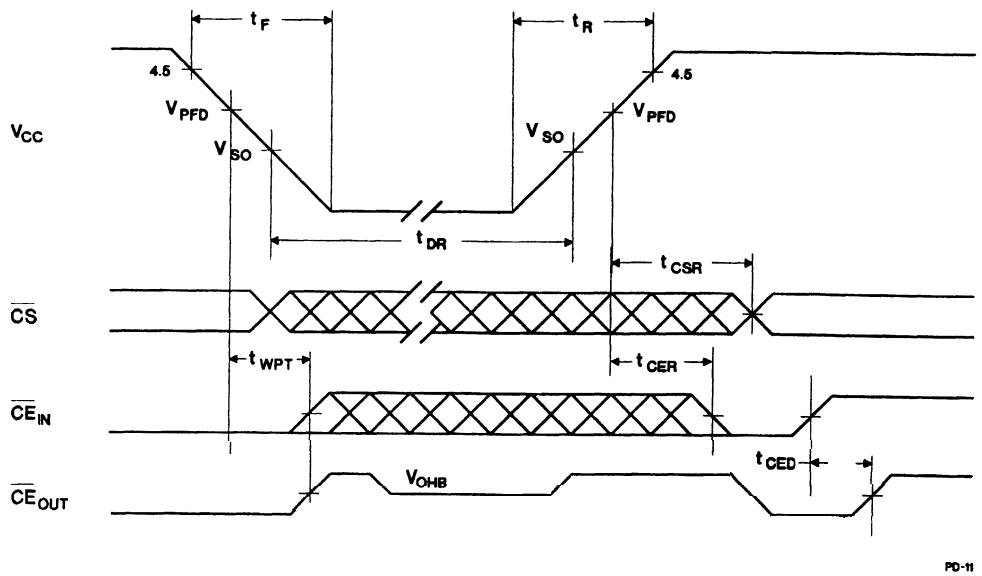
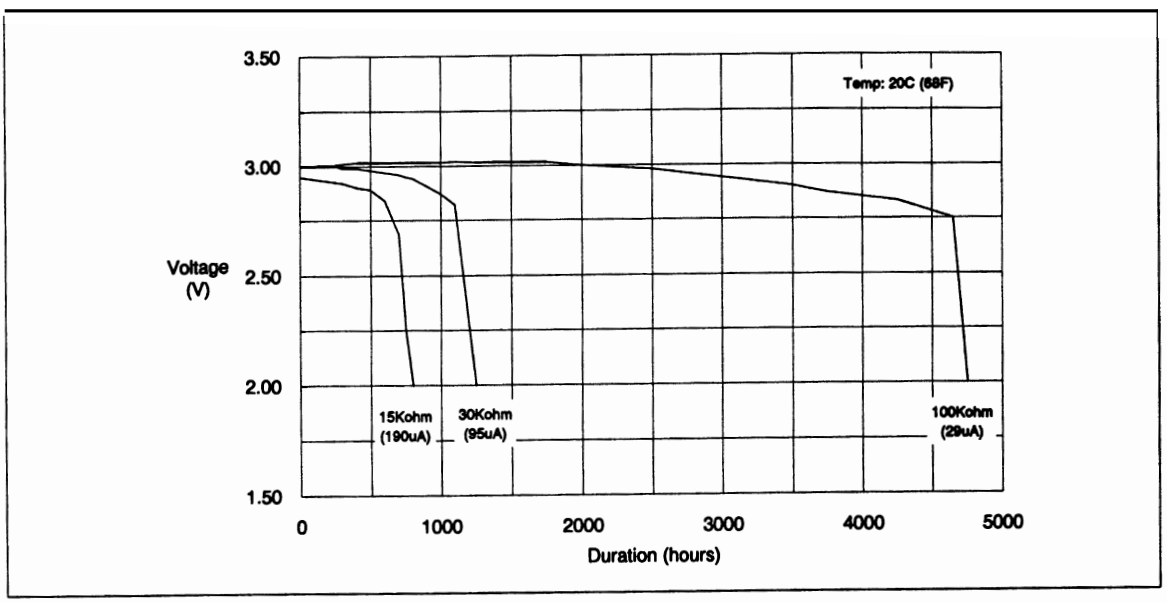
Power-Down/Power-Up Timing

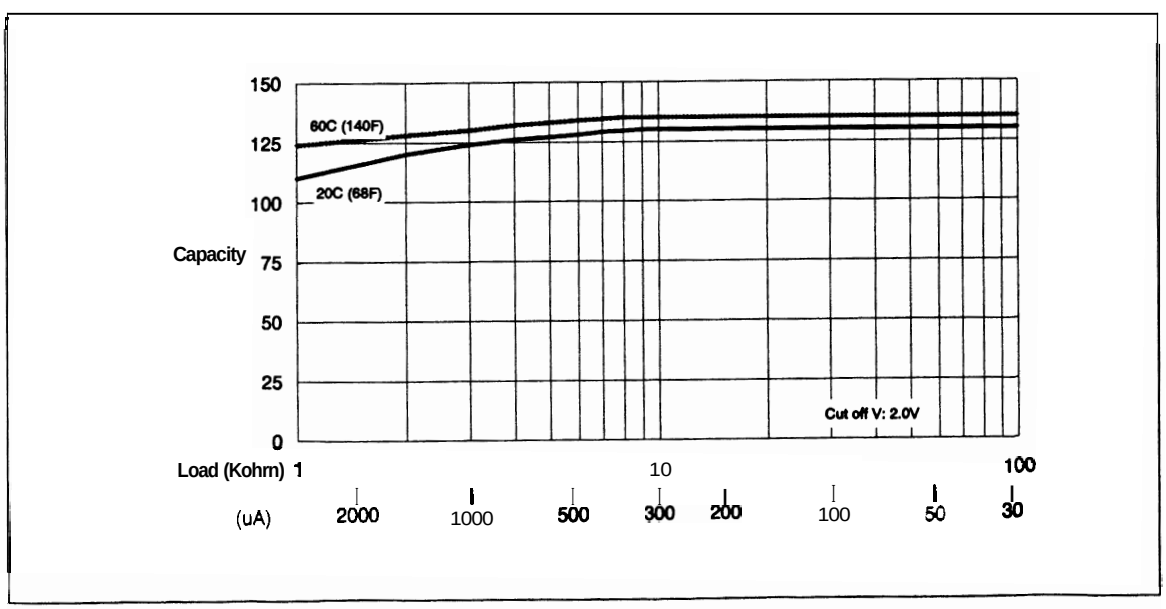


Typical Battery Characteristics (source = Panasonic)

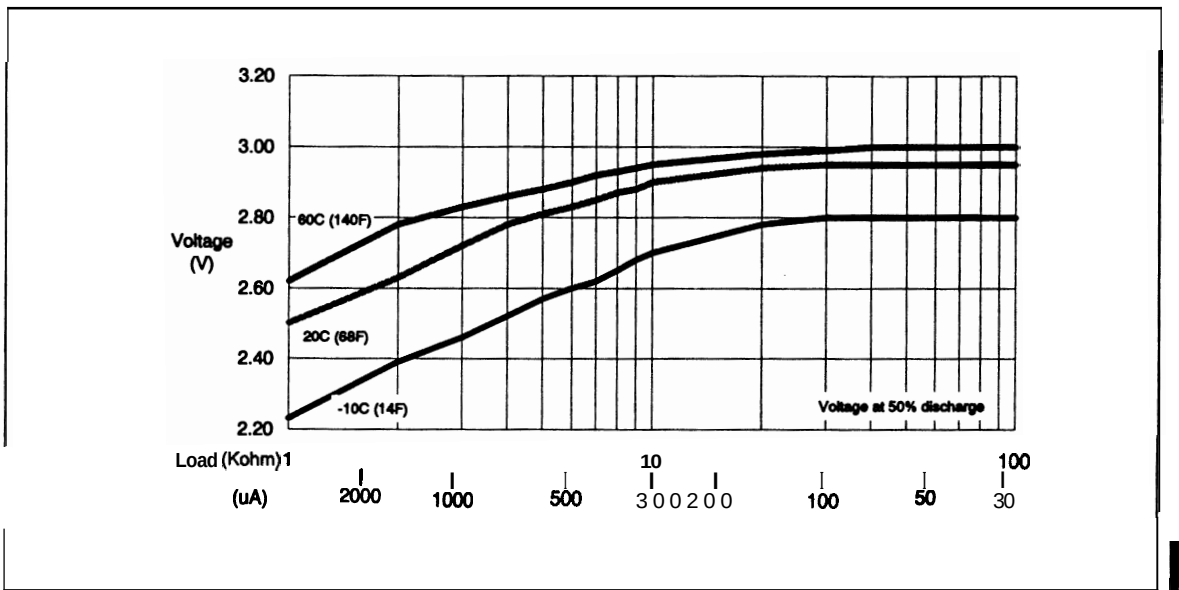
CR1632 Load Characteristics



CR1632 Capacity vs. Load Resistance



CR1632 Operating Voltage vs. Load Resistance



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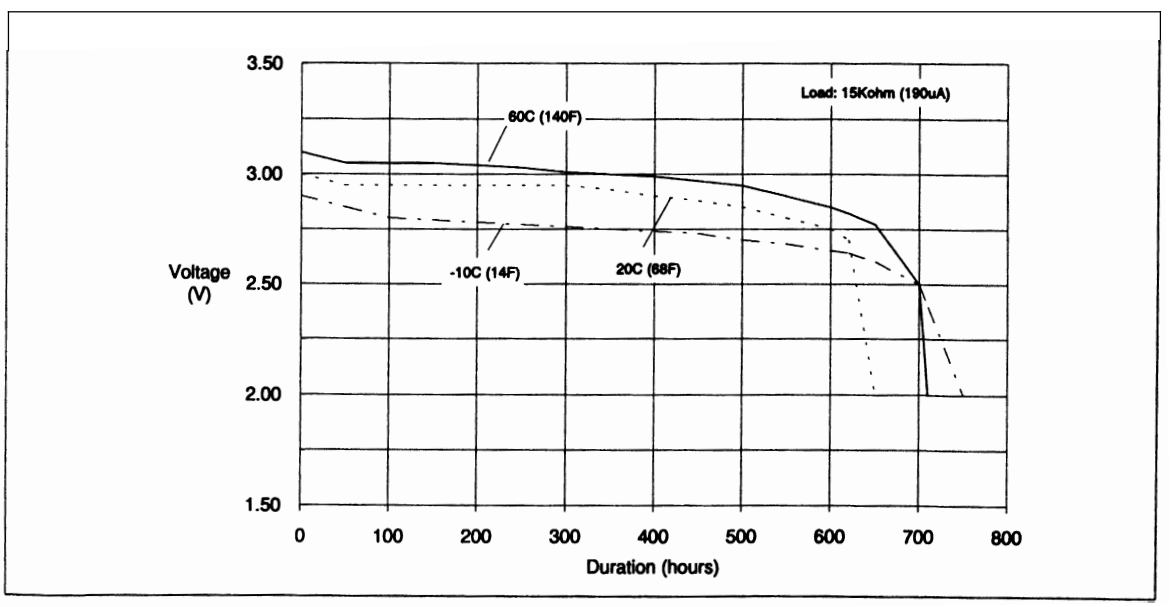
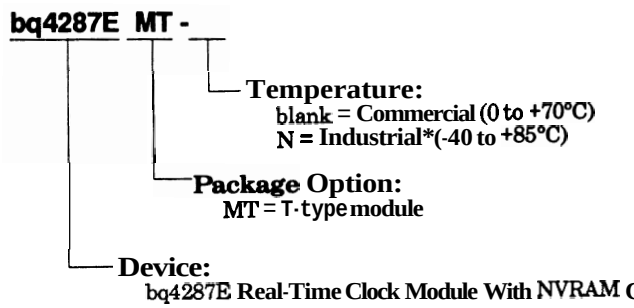
CR1632 Temperature Characteristics



Ordering Information



'Contact factory for availability.

BENCHMARQ

bq4830Y

RTC Module With 32Kx8 NVSRAM

Features

- Integrated SRAM, real-time clock, crystal, power-fail control circuit, and battery
- Real-Time Clock counts seconds through years in BCD format
- RAM-like clock access
- Pin-compatible with industry-standard 32K x 8 SRAMs
- Unlimited write cycles
- 10-year minimum data retention and clock operation in the absence of power
- Automatic power-fail chip deselect and write-protection
- Software clock calibration for greater than ±1 minute per month accuracy
- 10% tolerance of V_{CC} for write-protect

General Description

The bq4830Y RTC Module is a nonvolatile 262,144-bit SRAM organized as 32,768 words by 8 bits with an integral accessible real-time clock.

The device combines an internal lithium battery, quartz crystal, clock and power-fail chip, and a full CMOS SRAM in a plastic 28-pin DIP module. The RTC Module directly replaces industry-standard SRAMs and also fits into many EPROM and EEPROM sockets without any requirement for special write timing or limitations on the number of write cycles.

Registers for the real-time clock and clock calibration are located in registers 7FF8h–7FFFh of the memory array.

The clock registers are dual-port read/write SRAM locations that are updated once per second by a clock control circuit from the internal clock counters. The dual-part registers allow clock updates to occur without interrupting normal access to the rest of the SRAM array.

The bq4830Y also contains a power-fail-detect circuit. The circuit deselects the device whenever V_{CC} falls below tolerance, providing a high degree of data security. The battery is electrically isolated when shipped from the factory to provide maximum battery capacity. The battery remains disconnected until the first application of V_{CC}.

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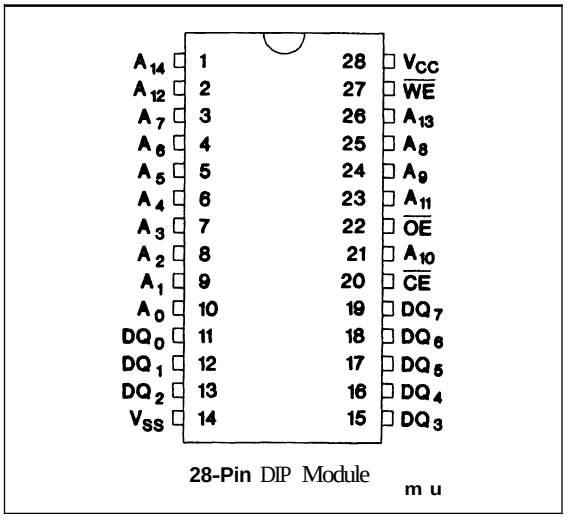
Pin Connections



28-Pin DIP Module

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Pin Names

A_0–A_{14}	Address input
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
DQ_0–DQ_7	Data in/data out
V_{CC}	+5 volts
V_{SS}	Ground

Functional Description

Figure 1 is a block diagram of the bq4830Y. The following sections describe the bq4830Y functional operation, including memory and clock interface, and data-retentionmodes.

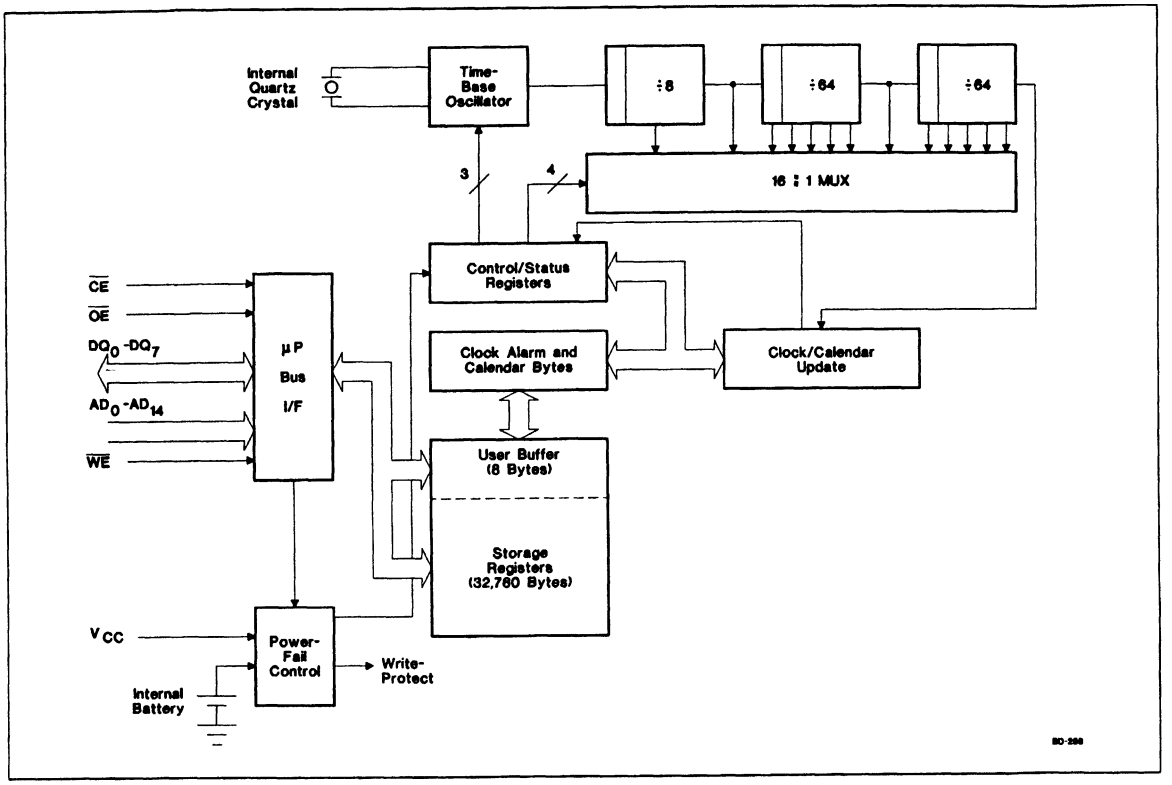


Figure 1. Block Diagram

Truth Table

Vcc	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	DQ	Power
< V_{CC}	V_{IH}	X	X	Deselect	High Z	Standby
> Vcc (min.)	V_{IL}	X	V_{IL}	Write	Dm	Active
	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
	V_{IL}	V_{IH}	V_{IH}	Read	High Z	Active
< V_{PFD} (min.) > V_{SO}	X	X	X	Deselect	High Z	CMOS standby
≤ V_{SO}	X	X	X	Deselect	High Z	Battery-backupmode

Address Map

The bq4830Y provides 8 bytes of clock and con[7FF7] registers and 32,760 bytes of storage RAM.

Figure 2 illustrates the address map for the bq4830Y. Table 1 is a map of the bq4830Y registers.

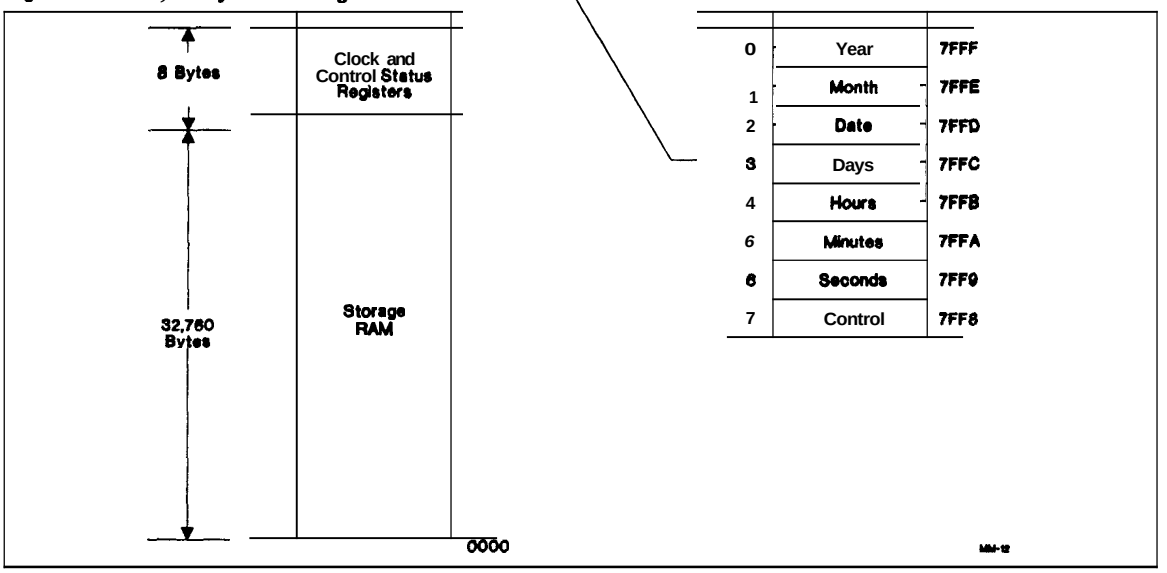


Figure 2. Address Map

5

Table 1. bq4830Y Clock and Control Register Map

Address	D7	D6	D5	D4	D3	D2	D1	D0	Range (h)	Register
7FFF	10 Years				Year				00–99	Year
7FFE	X	X	X	10 Month	Month				01–12	Month
7FFD	X	X	10 Date		Date				01–31	Date
7FFC	X	FTE	X	X	X	Day			01–07	Days
7FFB	X	X	10 Hours		Hours				00-23	Hours
7FFA	X	10 Minutes			Minutes				00–59	Minutes
7FF9	OSC	10 Seconds			Seconds				00–59	Seconds
7FF8	W	R	S	Calibration					00–31	Control

Note: X = Unused bits; can be written and read.
Clock/Calendar data in 24-hour BCD format.
OSC = 1 stops the clock oscillator.

Memory Interface

Read Mode

The bq4830Y is in read mode whenever $\overline{OE}$ (output enable) is low and $\overline{CE}$ (chip enable) is low. The device architecture allows npple-through access of data from eight of 262,144 locations in the static storage array. Thus, the unique address specified by the 15 address inputs defines which one of the 32,768 bytes of data is to be accessed. Valid data is available at the data I/O pins within t_{AA} (address access time) after the last addree input signal is stable, providing that the $\overline{CE}$ and $\overline{OE}$ (output enable) access times are also satisfied. If the $\overline{CE}$ and $\overline{OE}$ access times are not met, valid data is available after the latter of chip enable access time (t_{ACE}) or output enable access time (t_{OE}).

$\overline{CE}$ and $\overline{OE}$ control the state of the eight three-state data I/O signals. If the outputs are activated before t_{AA}, the data lines are driven to an indeterminate state until t_{AA}. If the address inputs are changed while $\overline{CE}$ and $\overline{OE}$ remain low, output data remains valid for t_{OH} (output data hold time), but goes indeterminate until the next address access.

Write Mode

The bq4830Y is in write mode whenever $\overline{WE}$ and $\overline{CE}$ are active. The start of a write is referenced from the latter-occurring falling edge of $\overline{WE}$ or $\overline{CE}$. A write is terminated by the earlier rising edge of $\overline{WE}$ or $\overline{CE}$. The addresses must be held valid throughout the cycle. $\overline{CE}$ or $\overline{WE}$ must return high for a minimum of t_{WR2} from $\overline{CE}$ or t_{WR1} from $\overline{WE}$ prior to the initiation of another read or write cycle.

Data-in must be valid t_{DW} prior to the end of write and remain valid for t_{DH1} or t_{DH2} afterward. $\overline{OE}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{CE}$ and $\overline{OE}$, a low on $\overline{WE}$ disables the outputs t_{WZ} after $\overline{WE}$ falls.

Data-Retention Mode

With valid Vcc applied, the bq4830Y operates as a conventional static RAM. Should the supply voltage decay, the RAM automatically power-fail deselects, write-protecting itself t_{WPT} after V_{CC} falls below V_{PFD}. All outputs become high impedance, and all inputs are treated as 'don't care."

If power-fail detection occurs during a valid access, the memory cycle continues to completion. If the memory cycle fails to terminate within time t_{WPT}, write-protection takes place. When Vcc drops below V_{SO}, the control circuit switches power to the internal energy source, which preserves data.

The internal coin cell maintains data in the bq4830Y after the initial application of Vcc for an accumulated period of at least 10 years when Vcc is less than V_{SO}. As system power returns and Vcc rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. Write-protection continues for t_{CER} after V_{CC} reaches V_{PFD} to allow for processor stabilization. After t_{CER}, normal RAM operation can resume.

Clock Interface

Reading the Clock

The interface to the clock and control registers of the bq4830Y is the same as that for the general-purpose storage memory. Once every second, the user-accessible clock/calendar locations are updated simultaneously from the internal real time counters. To prevent reading data in transition, updates to the bq4830Y clock registers should be halted. Updating is halted by setting the read bit D6 of the control register to 1. As long as the read bit is 1, updates to user-accessible clock locations are inhibited. Once the frozen clock information is retrieved by reading the appropriate clock memory locations, the read bit should be reset to 0 in order to allow updates to occur from the internal counters. Because the internal counters are not halted by setting the read bit, reading the clock locations has no effect on clock accuracy. Once the read bit is reset to 0, within one second the internal registers update the user-accessible registers with the correct time. A halt command issued during a clock update allows the update to occur before freezing the data.

Setting the Clock

Bit D7 of the control register is the write bit. Like the read bit, the write bit when set to a 1 halts updates to the clock/calendar memory locations. Once frozen, the locations can be written with the desired information in 24-hour BCD format. Resetting the write bit to 0 causes the written values to be transferred to the internal clock counters and allows updates to the user-accessible registers to resume within one second. Use the write bit, D7, only when updating the time registers (7FFF-7FF9).

Stopping and Starting the Clock Oscillator

The OSC bit in the seconds register turns the clock on or off. If the bq4830Y is to spend a significant period of time in storage, the clock oscillator can be turned off to preserve battery capacity. OSC set to 1 stops the clock oscillator. When OSC is reset to 0, the clock oscillator is turned on and clock updates to user-accessible memory locations occur within one second.

The OSC bit is set to 1 when shipped from the Benchmarq factory.

Calibrating the Clock

The bq4830Y real-time clock is driven by a quartz controlled oecillator with a nominal frequency of 32,768 Hz. The quartz crystal is contained within the bq4830Y package along with the battery. The clock accuracy of the bq4830Y module is tested to be within 20ppm or about 1 minute per month at 25°C. The oscillation rates of crystals change with temperature as Figure 3 shows. To compensate for the frequency shift, the bq4830Y offers onboard software clock calibration. The user can adjust the calibration based on the typical operating temperature of individual applications.

The software calibration bits are located in the control register. Bits DO–D4 control the magnitude of correction, and bit D5 the direction (positive or negative) of correction. Assuming that the oscillator is running at exactly 32,786 Hz, each calibration step of DO-D4 adjusts the clock rate by +4.068 ppm (+10.7 seconds per month) or -2.034 ppm (-5.35 seconds per month) depending on the value of the sign bit D5. When the sign bit is 1, positive adjustment occurs; a 0 activates negative adjustment. The total range of clock calibration is +5.5 or -2.75 minutes per month.

Two methods can be used to ascertain how much calibration a given bq4830Y may require in a system. The first involves simply setting the clock, letting it run for a month, and then comparing the time to an accurate known reference like WWV radio broadcasts. Based on the variation to the standard, the end user can adjust the clock to match the system's environment even after the product is packaged in a non-serviceable enclosure. The only requirement is a utility that allows the end user to access the calibration bits in the control register.

The second approach uses a bq4830Y test mode. When the frequency test mode enable bit FTE in the days register is set to a 1, and the oscillator is running at exactly 32,768 Hz, the LSB of the seconds register toggles at 512 Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.01024 Hz indicates a (1E6*0.01024)/512 or +20 ppm oscillator frequency error, requiring ten steps of negative calibration (10*-2.034 or -20.34) or 001010 to be loaded into the calibration byte for correction. To read the test frequency, the bq4830Y must be selected and held in an extended read of the seconds register, location 7FF9, without having the read bit set. The frequency appears on DQ0. The FTE bit must be set using the write bit control. The FTE bit must be reset to 0 for normal clock operation to resume.

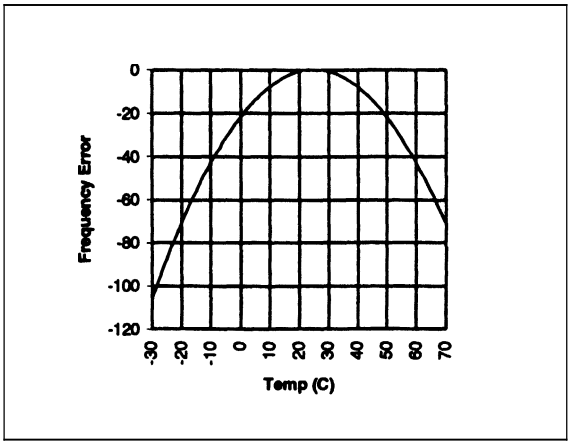


Figure 3. Frequency Error

5

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on Vcc relative to Vss	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding Vcc relative to Vss	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	
T_{STG}	Storage temperature (Vcc off; oscillator off)	-40 to +70	°C	
T_{BIAS}	Temperature under bias	-10 to +70	°C	
T_{SOLDER}	Soldering temperature	+260	°C	For 10 seconds

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C.

DC Electrical Characteristics (T_A = TOPR, VCCmin ≤ VCC ≤ VCCmax)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current			± 1	µA	V_{IN} = Vss to Vcc
I_{LO}	Output leakage current			± 1	µA	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}
V_{OH}	Output high voltage	2.4			V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage			0.4	V	I_{OL} = 2.1 mA
I_{SB1}	Standby supply current		3	6	mA	$\overline{CE}$ = V_{IH}
I_{SB2}	Standby supply current		2	4	mA	$\overline{CE}$ ≥ V_{CC} - 0.2V, 0V ≤ V_{IN} ≤ 0.2V, or V_{IN} ≥ V_{CC} - 0.2V
I_{CC}	Operating supply current		55	75	mA	Min. cycle, duty = 100%, $\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0mA
V_{PFD}	Power-fail-detectvoltage	4.30	4.37	4.50	V	
V_{SO}	Supply switch-over voltage		3		V	

Notes: Typical values indicate operation at T_A = 25°C, Vcc = 5V.

5

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance			10	pF	Output voltage = OV
C_{IN}	Input capacitance			10	pF	Input voltage = 0V

Note: These parameters are sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 4 and 5

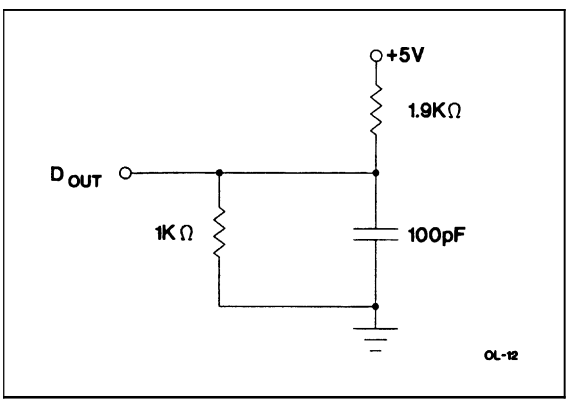


Figure 4. Output Load A

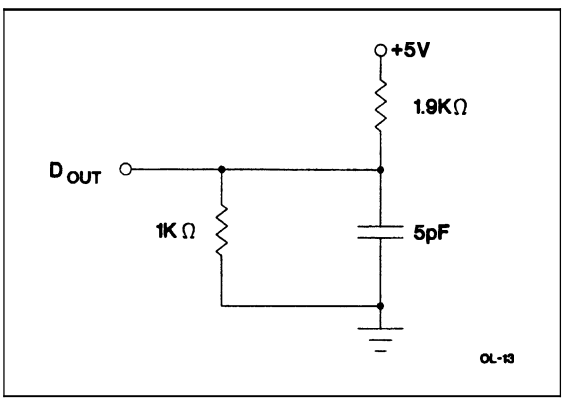
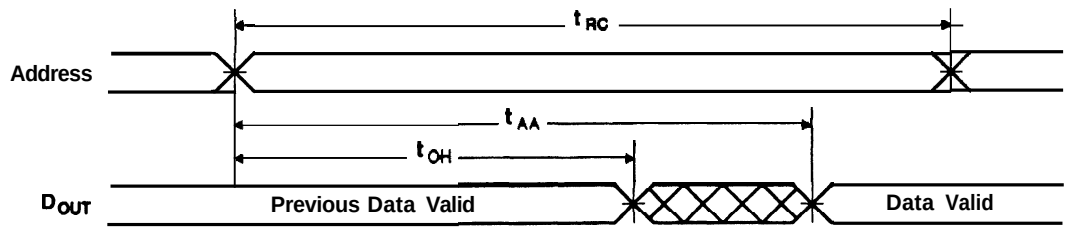


Figure 5. Output Load B

Read Cycle (TA = TOPR, VCCmin ≤ VCC ≤ VCCmax)

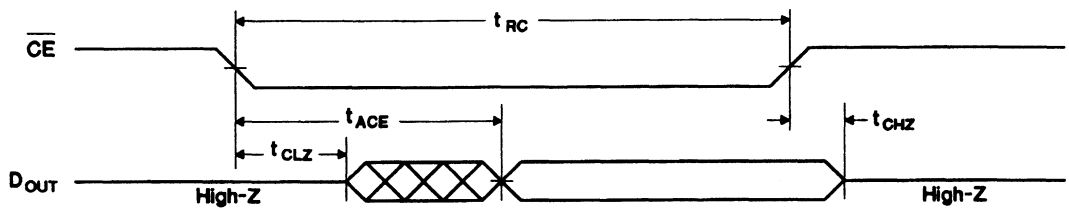
Symbol	Parameter	-85 Min.	-85 Max.	Unit	Conditions
t_{RC}	Read cycle time	85		ns	
t_{AA}	Address access time		85	ns	Output load A
t_{ACE}	Chip enable access time		85	ns	Output load A
t_{OE}	Output enable to output valid		45	ns	Output load A
t_{CLZ}	Chip enable to output in low Z	5		ns	Output load B
t_{OLZ}	Output enable to output in low Z	0		ns	Output load B
t_{CHZ}	Chip disable to output in high Z	0	35	ns	Output load B
t_{OHZ}	Output disable to output in high Z	0	25	ns	Output load B
t_{OH}	Output hold from address change	10		ns	Output load A

Read Cycle No. 1 (Address Access) [1,2]



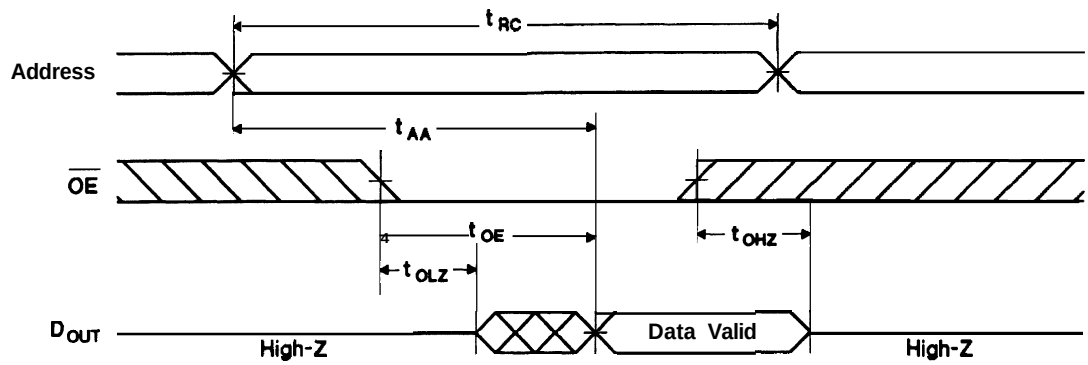
RC-1

Read Cycle No. 2 ($\overline{CE}$ Access) [1,3,4]



RC-2

Read Cycle No. 3 ($\overline{OE}$ Access) [1,5]



RC-3

Notes:
1. $\overline{WE}$ is held high for a read cycle.
2. Device is continuously selected: $\overline{CE}$ = $\overline{OE}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = V_{IL}.
6. Device is continuously selected: $\overline{CE}$ = V_{IL}.

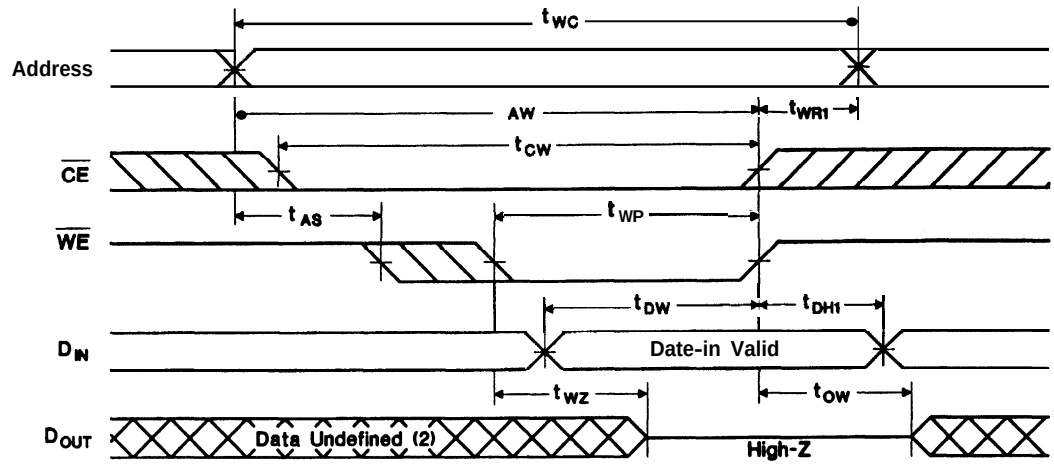
Write Cycle (TA = TOPR, VCCmin ≤ VCC ≤ VCCmax)

Symbol	Parameter	-85		Units	Conditions/Notes
		Min.	Max.		
t_{WC}	Write cycle time	85		ns	
t_{CW}	Chip enable to end of write	75		ns	(1)
t_{AW}	Address valid to end of write	75		ns	(1)
t_{AS}	Address setup time	0		ns	Measured from address valid to beginning of write. (2)
t_{WP}	Write pulse width	65		ns	Measured from beginning of write to end of write. (1)
t_{WR1}	Write recovery time (write cycle 1)	5		ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
t_{WR2}	Write recovery time (write cycle 2)	15		ns	Measured from $\overline{CE}$ going high to end of write cycle. (3)
t_{DW}	Data valid to end of write	35		ns	Measured to first low-to-high transition of either $\overline{CE}$ or $\overline{WE}$.
t_{DH1}	Data hold time (write cycle 1)	0		ns	Measured from $\overline{WE}$ going high to end of write cycle. (4)
t_{DH2}	Data hold time (write cycle 2)	10		ns	Measured from $\overline{CE}$ going high to end of write cycle. (4)
t_{WZ}	Write enabled to output in high Z	0	30	ns	I/O pins are in output state. (5)
t_{OW}	Output active from end of write	0		ns	I/O pins are in output state. (5)

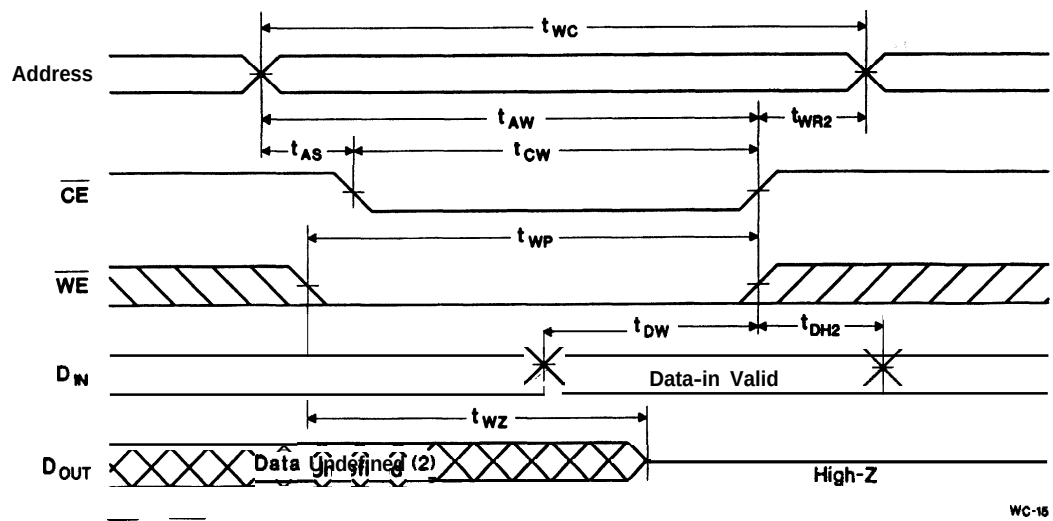
Notes:

1. A write ends at the earlier transition of $\overline{CE}$ going high and $\overline{WE}$ going high.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CE}$ going low and $\overline{WE}$ going low.
3. Either t_{WR1} or t_{WR2} must be met.
4. Either t_{DH1} or t_{DH2} must be met.
5. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

Write Cycle No. 1 ($\overline{WE}$-Controlled) 1,2,3



Write Cycle No. 2 ($\overline{CE}$-Controlled) 1,2,3,4,5



Notes:
1. $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
2. Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
3. If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.
4. Either t_{WR1} or t_{WR2} must be met.
5. Either t_{DH1} or t_{DH2} must be met.

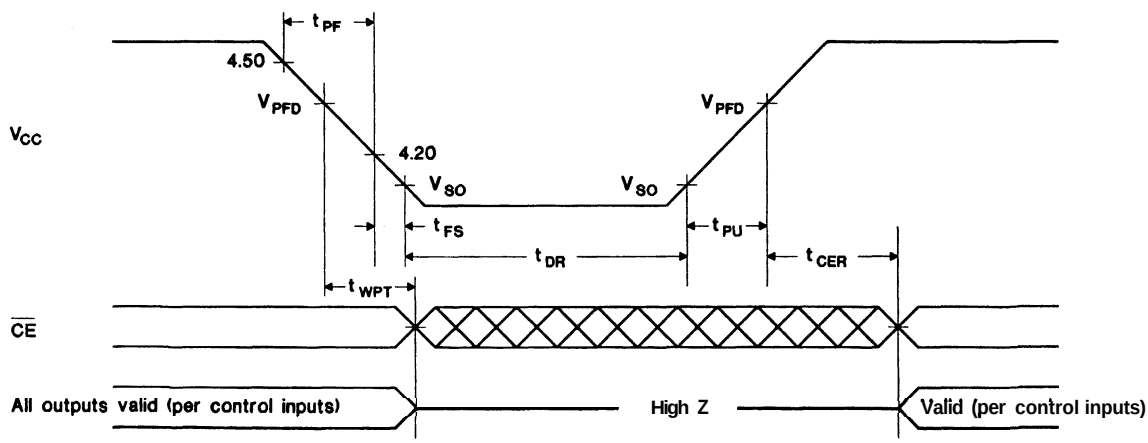
Power-Down/Power-Up Cycle ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_{PF}	V_{CC} slew, 4.50 to 4.20 V	300			µs	
t_{FS}	V_{CC} slew, 4.20 to V_{SO}	10	-	-	µs	
t_{PU}	V_{CC} slew, V_{SO} to V_{PFD} (max.)	0			µs	
t_{CER}	Chip enable recovery time	40	100	200	ms	Time during which SRAM is write-protected after Vcc passes V_{FPD} on power-up.
t_{DR}	Data-retention time in absence of V_{CC}	10			years	T_A = 25°C. (2)
t_{WPT}	write-protect time	40	100	160	µs	Delay after Vcc slews down past V_{PFD} before SRAM is write-protected.

Notes:
1. Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.
2. Battery is disconnected from circuit until after V_{CC} is applied for the first time. t_{DR} is the accumulated time in absence of power beginning when power is first applied to the device.

Caution: **Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.**

Power-Down/Power-Up Timing



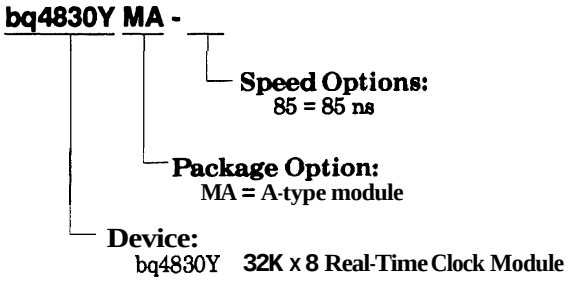
Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	7	Valuechange	I_{SB1} typ. and max. were 4, 7; are now 3, 6.
1	7	Value change	I_{SB2} typ. was 2.5; is now 2.

Note: Change 1 = Sept. 1996 B changes from Oct. 1995.

5

Ordering Information



BENCHMARQ

bq4832Y

RTC Module With 32Kx8 NVSRAM

Features

- Integrated SRAM, real-time clock, CPU supervisor, crystal, power-fail circuit, and battery
- Real-Time Clock counts hundredths of seconds through years in BCD format
- RAM-like clock access
- Compatible with industry-standard 32K x 8 SRAMs
- Unlimited write cycles
- 10-year minimum data retention and clock operation in the absence of power
- Automatic power-fail chip deselect and write-protection
- Watchdog timer, power-on reset, alarm/periodic interrupt, power-fail and battery-low warning
- Software clock calibration for greater than ±1 minute per month accuracy

General Description

The bq4832Y RTC Module is a non-volatile 262,144-bit SRAM organized as 32,768 words by 8 bits with an integral real-time clock and CPU supervisor. The CPU supervisor provides a programmable watchdog timer and a microprocessor reset. Other features include an alarm, power-fail and periodic interrupt, and a battery low warning.

The device combines an internal lithium battery, quartz crystal, clock and power-fail chip, and a full CMOS SRAM in a plastic 32-pin DIP module. The RTC Module directly replaces industry-standard SRAMs and also fits into many EPROM and EEPROM sockets without any requirement for special write timing or limitations on the number of write cycles.

Registers for the real-time clock, alarm and other special functions are located in registers 7FF0h–7FFFh of the memory array.

The clock and alarm registers are dual-port read/write SRAM locations that are updated once per second by a clock control circuit from the internal clock counters. The dual-port registers allow clock updates to occur without interrupting normal access to the rest of the SRAM array.

The bq4832Y also contains a power-fail-detect circuit. The circuit deselects the device whenever V_{CC} falls below tolerance, providing a high degree of data security. The battery is electrically isolated when shipped from the factory to provide maximum battery capacity. The battery remains disconnected until the first application of V_{CC}.

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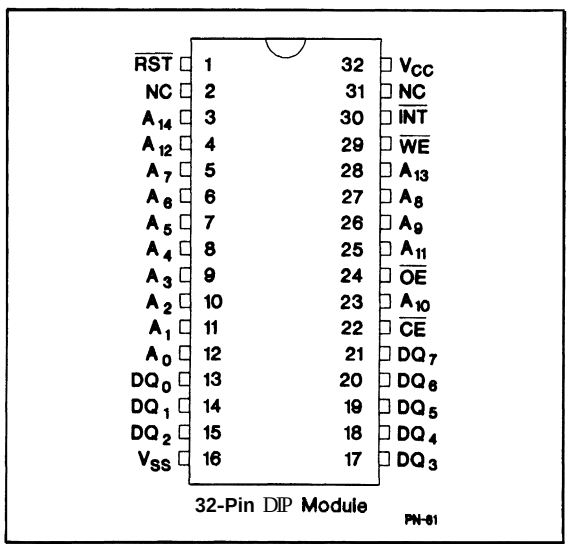
Pin Connections



Pin Names

A_0-A_{14}	Address input
$\overline{CE}$	Chip enable
$\overline{RST}$	Microprocessor reset
$\overline{WE}$	Write enable
OE	Output enable
DQ_0-DQ_7	Data in/data out
$\overline{INT}$	Programmable interrupt
V_{CC}	+5 volts
V_{SS}	Ground

Functional Description

Figure 1 is a block diagram of the bq4832Y. The following sections describe the bq4832Y functional operation, including memory and clock interface, data-retention modes, power-on reset timing, watchdog timer activation, and interrupt generation.

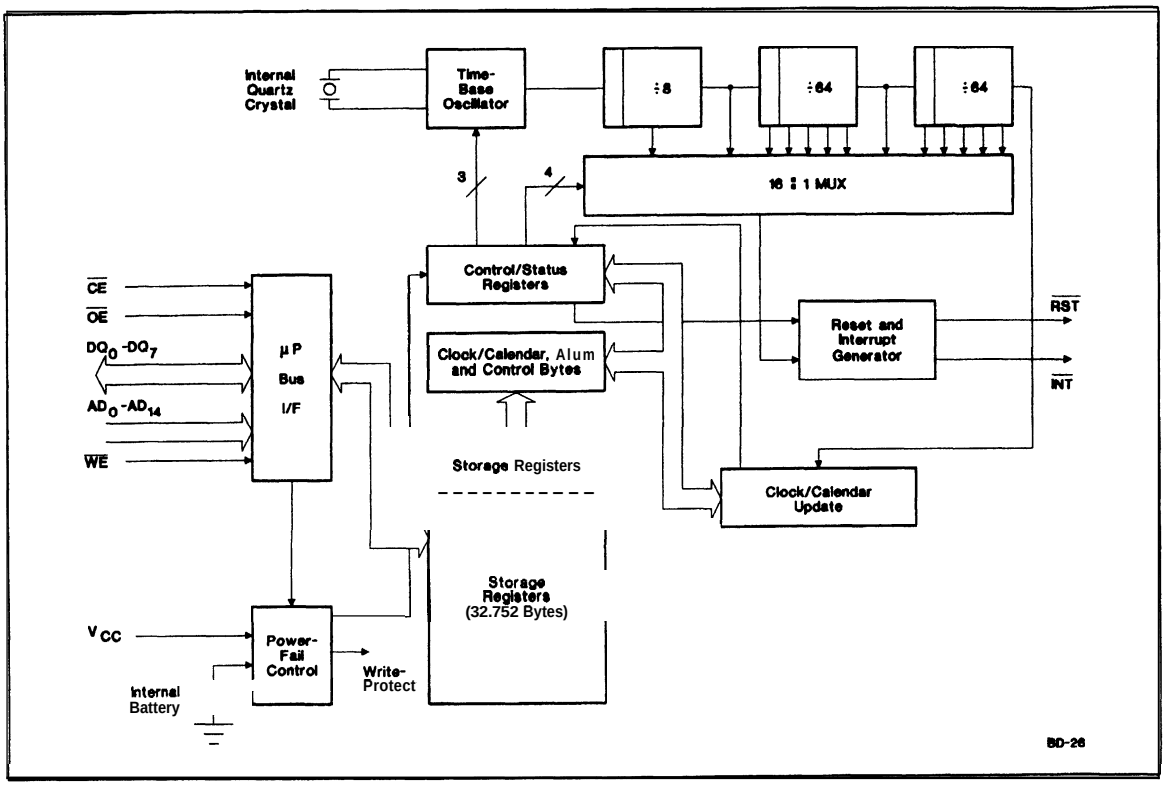


Figure 1. Block Diagram

Truth Table

Vcc	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	DQ	Power
< Vcc (max.)	V_{IH}	X	X	Deselect	High Z	Standby
> Vcc (min.)	V_{IL}	X	V_{IL}	Write	D_{IN}	Active
	V_{IL}	V_{IL}	Vm	Read	D_{OUT}	Active
	V_{IL}	V_{IH}	V_{IH}	Read	High Z	Active
< V_{PFD} (min.) > V_{SO}	X	X	X	Deselect	High Z	CMOS standby
≤ V_{SO}	X	X	X	Deselect	High Z	Battery-backup mode

Address Map

The bq4832Y provides 16 bytes of clock and control status registers and 32,752 bytes of storage RAM.

Figure 2 illustrates the address map for the bq4832Y. Table 1 is a map of the bq4832Y registers, and Table 2 describes the register bite.

Memory Interface

Read Mode

The bq4832Y ie in read mode whenever $\overline{OE}$ (output enable) is low and $\overline{CE}$ (chip enable) is low. The device architecture allows ripple-through access of data from eight of 262,144 locations in the static storage array. Thus, the unique address specified by the 15 address inpute defines which one of the 32,768 bytes of data is to be accessed. Valid data is available at the data I/O pins within t_{AA} (address access time) after the last address input signal is stable, providing that the $\overline{CE}$ and $\overline{OE}$ (output enable) access times are also satisfied. If the $\overline{CE}$ and $\overline{OE}$ access times are not met, valid data is available after the latter of chip enable access time (t_{ACE}) or output enable access time (t_{OE}).

$\overline{CE}$ and $\overline{OE}$ control the state of the eight three-state data I/O signals. If the outputs are activated before t_{AA}, the data lines are driven to an indeterminate state until t_{AA}. If the address inputs are changed while $\overline{CE}$ and $\overline{OE}$ remain low, output data remains valid for t_{OH} (output data hold time), but goes indeterminate until the next address access.

Write Mode

The bq4832Y is in write mode whenever $\overline{WE}$ and $\overline{CE}$ are active. The start of a write is referenced from the latter-occurring falling edge of $\overline{WE}$ or $\overline{CE}$. A write is terminated by the earlier rising edge of $\overline{WE}$ or $\overline{CE}$. The addresses must be held valid throughout the cycle. $\overline{CE}$ or $\overline{WE}$ must return high for a minimum of t_{WR2} from $\overline{CE}$ or t_{WR1} from $\overline{WE}$ prior to the initiation of another read or write cycle.

Data-in must be valid t_{DW} prior to the end of write and remain valid for t_{DH1} or t_{DH2} afterward. $\overline{OE}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{CE}$ and $\overline{OE}$, a low on $\overline{WE}$ disables the outputs t_{WZ} after $\overline{WE}$ falls.

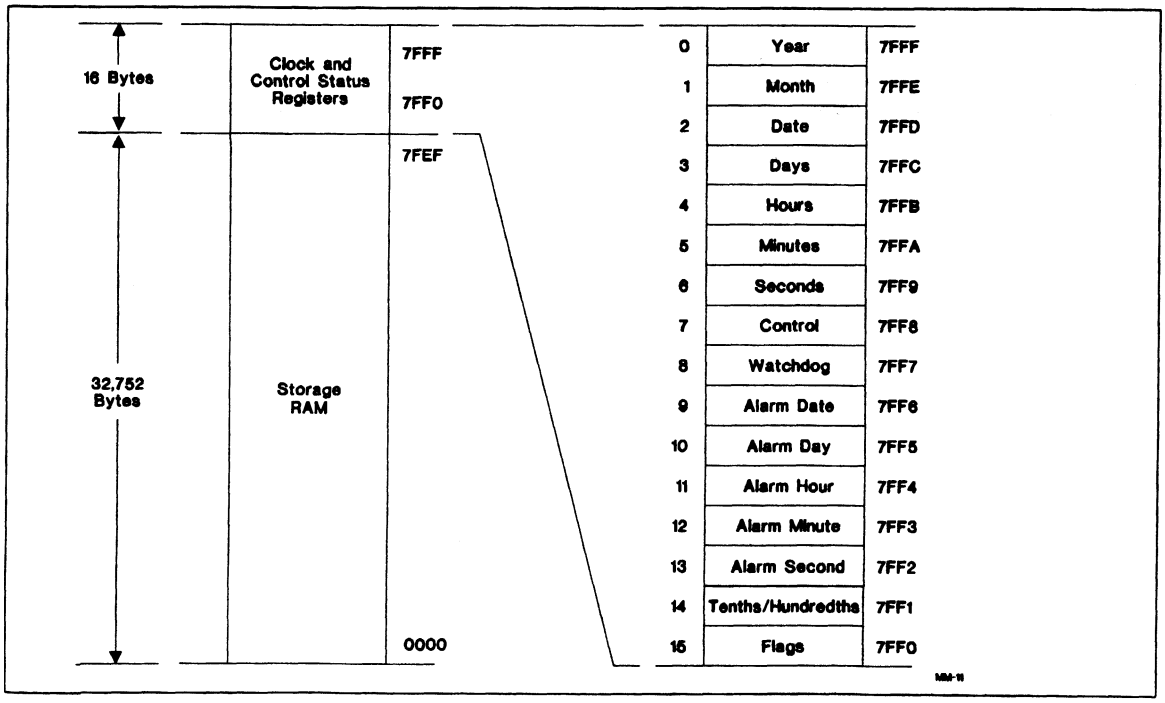


Figure 2. Address Map

Data-Retention Mode

With valid Vcc applied, the bq4832Y operates as a conventional static RAM. Should the supply voltage decay, the RAM automatically power-fail deselects, write-protecting itself t_{WPT} after Vcc falls below V_{PFD}. All outputs become high impedance, and all inputs are treated as 'don't care.'

If power-fail detection occurs during a valid access, the memory cycle continues to completion. If the memory cycle fails to terminate within time t_{WPT}, write-protection takes place. When Vcc drops below V_{SO}, the control circuit switches power to the internal energy source, which preserves data.

The internal coin cell maintains data in the bq4832Y after the initial application of Vcc for an accumulated period of at least 10 years when Vcc is less than V_{SO}. As system power returns and Vcc rises above V_{SO}, the battery is disconnected, and the power supply is switched to external Vcc. Write-protection continues for t_{CER} after Vcc reaches V_{PFD} to allow for processor stabilization. After t_{CER}, normal RAM operation can resume.

Clock Interface

Reading the Clock

The interface to the clock and control registers of the bq4832Y is the same as that for the general-purpose storage memory. Once every second, the user-accessible clock/calendar locations are updated simultaneously from the internal real time counters. To prevent reading data in transition, updates to the bq4832Y clock registers should be halted. Updating is halted by setting the read bit D6 of the control register to 1. As long as the read bit is 1, updates to user-accessible clock locations are inhibited. Once the frozen clock information is retrieved by reading the appropriate clock memory locations, the read bit should be reset to 0 in order to allow updates to occur from the internal counters. Because the internal counters are not halted by setting the read bit, reading the clock locations has no effect on clock accuracy. Once the read bit is reset to 0, within one second the internal registera update the user-accessible registers with the correct time. A halt command issued during a clock update allows the update to occur before freezing the data.

Table 1. bq4832Y Clock and Control Register Map

Address	D7	D6	D5	D4	D3	D2	D1	D0	Range (h)	Register
7FFF	10 Years				Year				00–99	Year
7FFE	X	X	X	10 Month	Month				01–12	Month
7FFD	X	X	10 Date		Date				01–31	Date
7FFC	X	FTE	X	X	X	Day			01–07	Days
7FFB	X	X	10 Hours		Hours				00–23	Hours
7FFA	X	10 Minutes			Minutes				00–59	Minutes
7FF9	OSC	10 Seconds			Seconds				00–59	Seconds
7FF8	W	R	S	Calibration					00–31	Control
7FF7	WDS	BM4	BM3	BM2	BM1	BM0	WD1	WD0		Watchdog
7FF6	AIE	PWRIE	ABE	PIE	RS3	RS2	RS1	RS0		Interrupts
7FF5	ALM3	X	10-date alarm		Alarm date				01–31	Alarm date
7FF4	ALM2	X	10-hour alarm		Alarm hours				00–23	Alarm hours
7FF3	ALM1	Alarm 10 minutes			Alarm minutes				00–59	Alarm minutes
7FF2	ALM0	Alarm 10 seconds			Alarm seconds				00–59	Alarm seconds
7FF1	0.1 seconds				0.01 seconds				00-99	0.1/0.01 seconds
7FF0	WDF	AF	PWRF	BLF	PF	X	X	X		Flags

Notes: X = Unused bits; can be written and read.
Clock/Calendar data in 24-hour BCD format.
BLF = 1 for valid battery.
OSC = 1 stops the clock oscillator.
Interrupt enables are cleared on power-up.

Table 2. Clock and Control Register Bits

Bits	Description
ABE	Alarm interrupt enable in battery-backup mode
AF	Alarm interrupt flag
AIE	Alarm interrupt enable
ALM0–ALM3	Alarm repeat rate
BLF	Battery-low flag
BM0–BM4	Watchdog multiplier
FTE	Frequency test mode enable
OSC	Oscillator stop
PF	Periodic interrupt flag
PIE	Periodic interrupt enable
PWRF	Power-fail interrupt flag
PWRIE	Power-fail interrupt enable
R	Read clock enable
RS0–RS3	Periodic interrupt rate
S	Calibration sign
W	Write clock enable
WD0–WD1	Watchdog resolution
WDF	Watchdog flag
WDS	Watchdog steering

Setting the Clock

Bit D7 of the control register is the write bit. Like the read bit, the write bit when set to a 1 halts updates to the clock/calendar memory locations. Once frozen, the locations can be written with the desired information in 24-hour BCD format. Resetting the write bit to 0 causes the written values to be transferred to the internal clock counters and allows updates to the user-accessible registers to resume within one second. Use the write bit, D7, only when updating the time registers (7FFF-7FF9).

Stopping and Starting the Clock Oscillator

The OSC bit in the seconds register turns the clock on or off. If the bq4832Y is to spend a significant period of time in storage, the clock oscillator can be turned off to preserve battery capacity. OSC set to 1 stops the clock oscillator. When OSC is reset to 0, the clock oscillator is turned on and clock updates to user-accessible memory locations occur within one second.

The OSC bit is set to 1 when shipped from the Benchmarq factory.

Calibrating the Clock

The bq4832Y real-time clock is driven by a quartz controlled oscillator with a nominal frequency of 32,768 He. The quartz crystal is contained within the bq4832Y package along with the battery. The clock accuracy of the bq4832Y module is tested to be within 20ppm or about 1 minute per month at 25°C. The oscillation rates of crystab change with temperature as Figure 3 shorn. To compensate for the frequency shift, the bq4832Y offers onboard software clock calibration. The user can adjust the calibration based on the typical operating temperature of individual applications.

The software calibration bite are located in the control register. Bits D0–D4 control the magnitude of correction, and bit D5 the direction (positive or negative) of correction. Assuming that the oscillator is running at exactly 32,786 Hz, each calibration step of D0–D4 adjusts the clock rate by +4.068 ppm (+10.7 seconds per month) or -2.034 ppm (-5.35 seconds per month) depending on the value of the sign bit D5. When the sign bit is 1, positive adjustment occurs; a 0 activates negative adjustment. The total range of clock calibration is +5.5 or -2.75 minutes per month.

Two methods can be used to ascertain how much calibration a given bq4832Y may require in a system. The first involves simply setting the clock, letting it run for a month, and then comparing the time to an accurate known reference like WWV radio broadcasts. Based on the variation to the standard, the end user can adjust the clock to match the system's environment wen after the product is packaged in a non-serviceable enclosure. The only requirement is a utility that allows the end user to access the calibration bits in the control register.

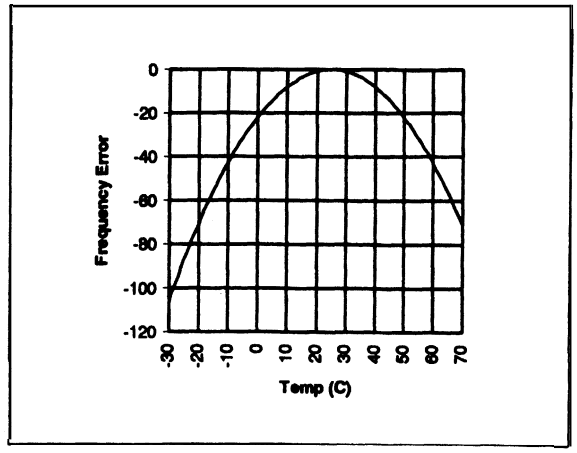


Figure 3. Frequency Error

The second approach uses a bq4832Y test mode. When the frequency test mode enable bit FTE in the days register is set to a 1, and the oscillator is running at exactly 32,768 Hz, the LSB of the seconds register toggles at 512 Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.01024 Hz indicates a (1E6•0.01024)/512 or +20 ppm oscillator frequency error, requiring ten steps of negative calibration (10•-2.034 or -20.34) or 001010 to be loaded into the calibration byte for correction. To read the test frequency, the bq4832Y must be selected and held in an extended read of the seconds register, location 7FF9, without having the read bit set. The frequency appears on DQ0. The FTE bit must be set using the write bit control. The FTE bit must be reset to 0 for normal clock operation to resume.

Power-On Reset

The bq4832Y provides a power-on reset, which pulls the $\overline{RST}$ pin low on power-down and remains low on power-up for t_{CER} after V_{CC} passes V_{PFD}.

Watchdog Timer

The watchdog circuit monitors the microprocessor's activity. If the processor does not reset the watchdog timer within the programmed time-out period, the circuit asserts the $\overline{INT}$ or $\overline{RST}$ pin. The watchdog timer is activated by writing the desired time-out period into the eight-bit watchdog register described in Table 3 (device address 7FF7). The five bits (BM4–BM0) store a binary multiplier, and the two lower-order bits (WD1–WD0) select the resolution, where 00 = 1/16 second, 01 = 1/4 second, 10 = 1 second, and 11 = 4 seconds.

The time-out period is the multiplication of the five-bit multiplier with the two-bit resolution. For example, writing 00011 in BM4–BMO and 10 in WD1–WD0 results in a total time-out setting of 3 x 1 or 3 seconds. A multiplier of zero disables the watchdog circuit. Bit 7 of the watchdog register (WDS) is the watchdog steering bit. When WDS is set to a 1 and a time-out occurs, the watchdog asserts a reset pulse for t_{CER} on the $\overline{RST}$ pin. During the reset pulse, the watchdog register is cleared to all zeros disabling the watchdog. When WDS is set to a 0, the watchdog asserts the $\overline{INT}$ pin on a time-out. The $\overline{INT}$ pin remains low until the watchdog is reset by the microprocessor or a power failure occurs. Additionally, when the watchdog times out, the watchdog flag bit (WDF) in the flags register, location 7FF0, is set.

To reset the watchdog timer, the microprocessor must write to the watchdog register. After being reset by a write, the watchdog time-out period starts over. As a precaution, the watchdog circuit is disabled on a power failure. The user must, therefore, set the watchdog at boot-up for activation.

Interrupts

The bq4832Y allows four individually selected interrupt events to generate an interrupt request on the $\overline{INT}$ pin. These four interrupt events are:

- The watchdog timer interrupt, programmable to occur according to the time-out period and conditions described in the watchdog timer section.
- The periodic interrupt, programmable to occur once every 122µs to 500ms.
- The alarm interrupt, programmable to occur once per second to once per month.
- The power-fail interrupt, which can be enabled to be asserted when the bq4832Y detects a power failure.

The periodic, alarm, and power-fail interrupts are enabled by an individual interrupt-enable bit in register 7FF6, the interrupts register. When an event occurs, its event flag bit in the flags register, location 7FF0, is set. If the corresponding event enable bit is also set, then an interrupt request is generated. Reading the flags register clears all flag bits and makes $\overline{INT}$ high impedance. To reset the flag register, the bq4832Y addresses must be held stable at location 7FF0 for at least 50ns to avoid inadvertent resets.

Periodic Interrupt

Bits RS3–RS0 in the interrupts register program the rate for the periodic interrupt. The user can interpret the interrupt in two ways: either by polling the flags register for PF assertion or by setting PIE so that $\overline{INT}$ goes active when the bq4832Y sets the periodic flag. Reading the flags register resets the PF bit and returns $\overline{INT}$ to the high-impedance state. Table 4 shows the periodic rates.

Table 3. Watchdog Register Bits

MSB			Bits				LSB
7	6	5	4	3	2	1	0
WDS	BM4	BM3	BM2	BM1	BMO	WD1	WD0

Table 4. Periodic Rates

RS3	RS2	RS1	RSO	Interrupt Rate
0	0	0	0	None
0	0	0	1	10ms
0	0	1	0	100ms
0	0	1	1	122.07µs
0	1	0	0	244.14µs
0	1	0	1	488.281µs
0	1	1	0	976.5625
0	1	1	1	1.953125ms
1	0	0	0	3.90625ms
1	0	0	1	7.8125ms
1	0	1	0	15.625ms
1	0	1	1	31.25ms
1	1	0	0	62.5ms
1	1	0	1	125ms
1	1	1	0	250ms
1	1	1	1	500ms

Alarm Interrupt

Registers 7FF5–7FF2 program the real-time clock alarm. During each update cycle, the bq4832Y compares the date, hours, minutes, and seconds in the clock registers with the corresponding alarm registers. If a match between all the correaponding bytes is found, the alarm flag AF in the flags register is set. If the alarm interrupt is enabled with AIE, an interrupt request is generated on $\overline{INT}$. The alarm condition is cleared by a read to the flags register. ALM3–ALM0 puts the alarm into a periodic mode of operation. Table 5 describes the selectable rates.

Table 5. Alarm Frequency(Alarm Bits DQ7 of Alarm Registers)

ALM3	ALM2	ALM1	ALM0	Alarm Frequency
1	1	1	1	Once per second
1	1	1	0	Once per minute when seconds match
1	1	0	0	Once per hour when minutes, and seconds match
1	0	0	0	Once per day when hours, minutes, and seconds match
0	0	0	0	When date, hours, minutes, and seconds match

The alarm interrupt can be made active while the bq4832Y is in the battery-backup mode by setting ABE in the interrupts register. Normally, the $\overline{INT}$ pin tri-states during battery backup. With ABE set, however, $\overline{INT}$ is driven low if an alarm condition occurs and the AIE bit in set. Because the AIE bit is reset during power-on reset, an alarm generated during power-on reset updates only the flags register. The user can read the flags register during boot-up to determine if an alarm was generated during power-on reset.

Power-Fail Interrupt

When V_{CC} falls to the power-fail-detect point, the power-fail flag PWRF is set. If the power-fail interrupt enable bit (PWRIE) is also set, then $\overline{INT}$ in asserted low. The power-fail interrupt occurs t_{WPT} before the bq4832Y generates a reset and deselects. The PWRIE bit is cleared on power-up.

Battery-Low Warning

The bq4832Y checks the internal battery on power-up. If the battery voltage is below 2.2V, the battery-low flag BLF in the flags register is set to a 1 indicating that clock and RAM data may be invalid.

5

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to Vss	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	
T_{STG}	Storage temperature (V_{CC} off; oscillator off)	-40 to +70	°C	
T_{BIAS}	Temperature under bias	-10 to +70	°C	
T_{SOLDER}	Soldering temperature	+260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are *exceeded*. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may *affect* device reliability.

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3		0.8	V	
V_{IH}	Input high voltage	2.2		V_{CC} + 0.3	V	

Note: *Typical* values indicate operation at T_A = 25°C.

DC Electrical Characteristics ($T_A = T_{OPR}$, $V_{CCmin} \le V_{CC} \le V_{CCmax}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current			± 1	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current			± 1	µA	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
V_{OH}	Output high voltage	2.4			V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage			0.4	V	I_{OL} = 2.1 mA
I_{OD}	$\overline{RST}$, $\overline{INT}$ sink current	10			mA	V_{OL} = 0.4V
I_{SB1}	Standby supply current		3	6	mA	$\overline{CE} = V_{IH}$
I_{SB2}	Standby supply current		2	4	mA	$\overline{CE} \ge V_{CC}$ - 0.2V, OV ≤ V_{IN} ≤ 0.2V, or $V_{IN} \ge$ Vcc - 0.2V
I_{CC}	Operating supply current		55	75	mA	Min. cycle, duty = 100%, $\overline{CE} = V_{IL}$, $I_{I/O}$ = 0mA
V_{PFD}	Power-fail-detectvoltage	4.30	4.37	4.50	V	
V_{SO}	Supply switch-over voltage		3		V	

Notes: Typical values indicate operation at T_A = 25°C, Vcc = 5V.
$\overline{RST}$ and $\overline{INT}$ are open-drain outputs.

5

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance			10	pF	Output voltage = OV
C_{IN}	Input capacitance			10	pF	Input voltage = 0V

Note: These parameters are sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 4 and 5

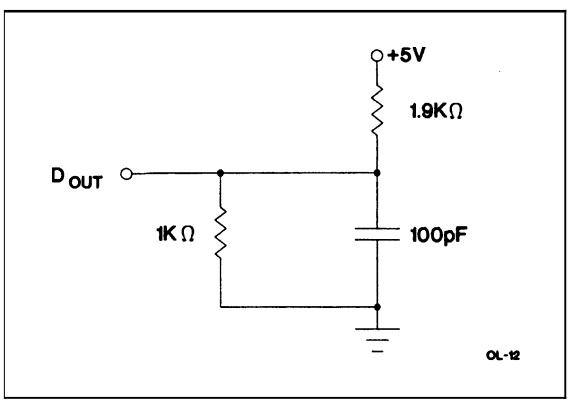


Figure 4. Output Load A

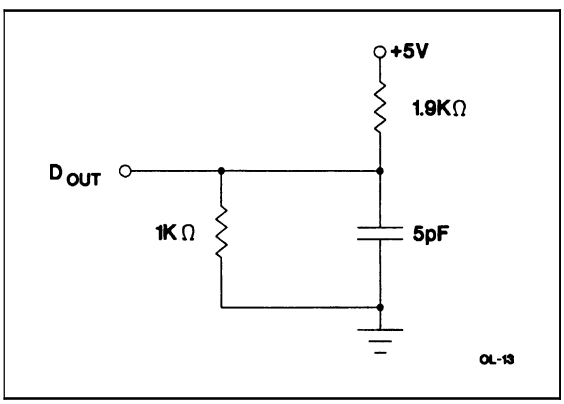
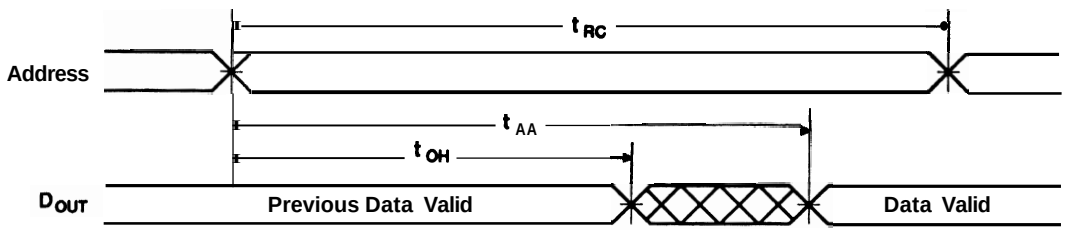


Figure 5. Output Load B

Read Cycle (TA = TOPR, VCCmin ≤ VCC ≤ VCCmax)

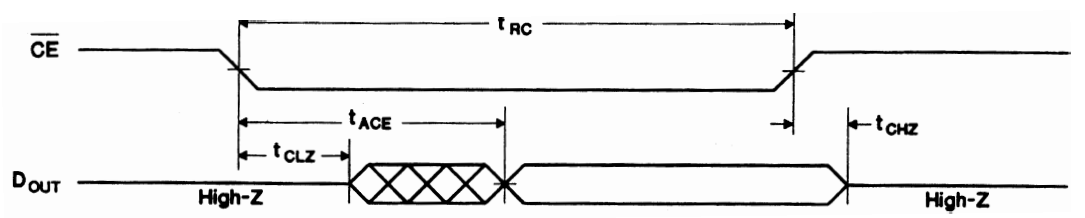
Symbd	Parameter	-85 Min.	-85 Max.	Unit	Conditions
t_{RC}	Read cycle time	85		ns	
t_{AA}	Address access time		85	ns	Output load A
t_{ACE}	Chip enable access time		85	ns	Output load A
t_{OE}	Output enable to output valid		45	ns	Output load A
t_{CLZ}	Chip enable to output in low Z	5		ns	Output load B
t_{OLZ}	Output enable to output in low Z	0		ns	Output load B
t_{CHZ}	Chip disable to output in high Z	0	35	ns	Output load B
t_{OHZ}	Output disable to output in high Z	0	25	ns	Output load B
t_{OH}	Output hold from address change	10		ns	Output load A

Read Cycle No. 1 (Address Access) [1,2]



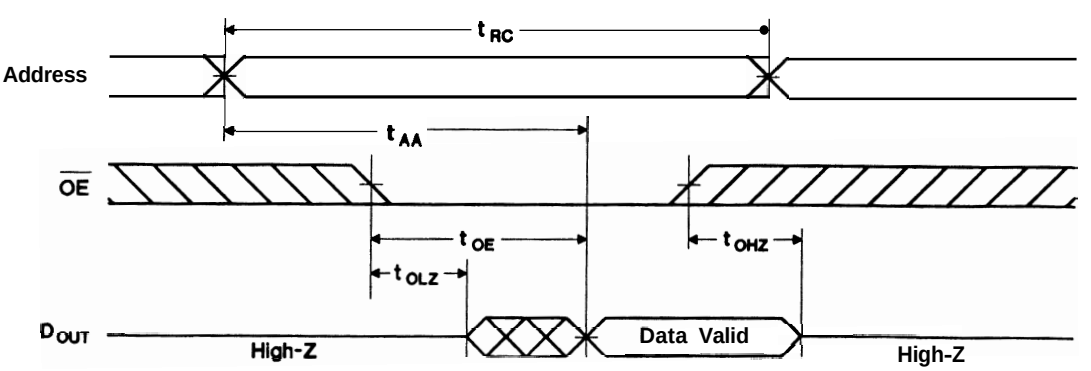
RC-1

Read Cycle No. 2 ($\overline{CE}$ Access) [1,3,4]



RC-2

Read Cycle No. 3 ($\overline{OE}$ Access) [1,5]



RC-a

Notes:
1. $\overline{WE}$ is held high for a read cycle.
2. Device is continuously selected: $\overline{CE}$ = $\overline{OE}$ = V_{IL}
3. Address is valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Device is continuously selected: $\overline{CE}$ = V_{IL}.

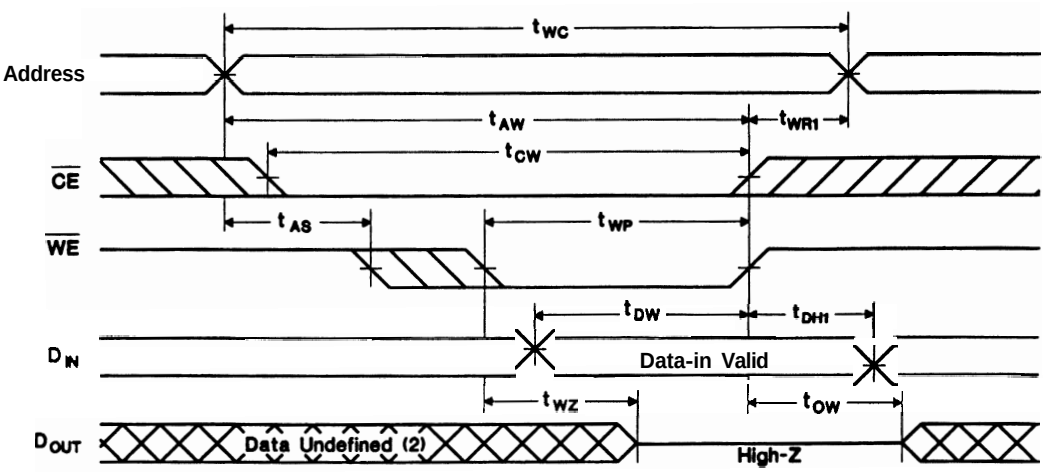
Write Cycle (TA = TOPR, VCCmin ≤ VCC ≤ VCCmax)

Symbol	Parameter	-85		Units	Conditions/Notes
		Min.	Max.		
t_{WC}	Write cycle time	85		ns	
t_{CW}	Chip enable to end of write	75		ns	(1)
t_{AW}	Address valid to end of write	75		ns	(1)
t_{AS}	Address setup time	0		ns	Measured from address valid to beginning of write. (2)
t_{WP}	Write pulse width	65		ns	Measured from beginning of write to end of write. (1)
t_{WR1}	Write recovery time (write cycle 1)	5		ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
t_{WR2}	Write recovery time (write cycle 2)	15		ns	Measured from $\overline{CE}$ going high to end of write cycle. (3)
t_{DW}	Data valid to end of write	35		ns	Measured to first low-to-high transition of either $\overline{CE}$ or $\overline{WE}$.
t_{DH1}	Data hold time (write cycle 1)	0		ns	Measured from $\overline{WE}$ going high to end of write cycle. (4)
t_{DH2}	Data hold time (write cycle 2)	10		ns	Measured from $\overline{CE}$ going high to end of write cycle. (4)
t_{WZ}	Write enabled to output in high Z	0	30	ns	I/O pins are in output state. (5)
tow	Output active from end of write	0		ns	I/O pins are in output state. (5)

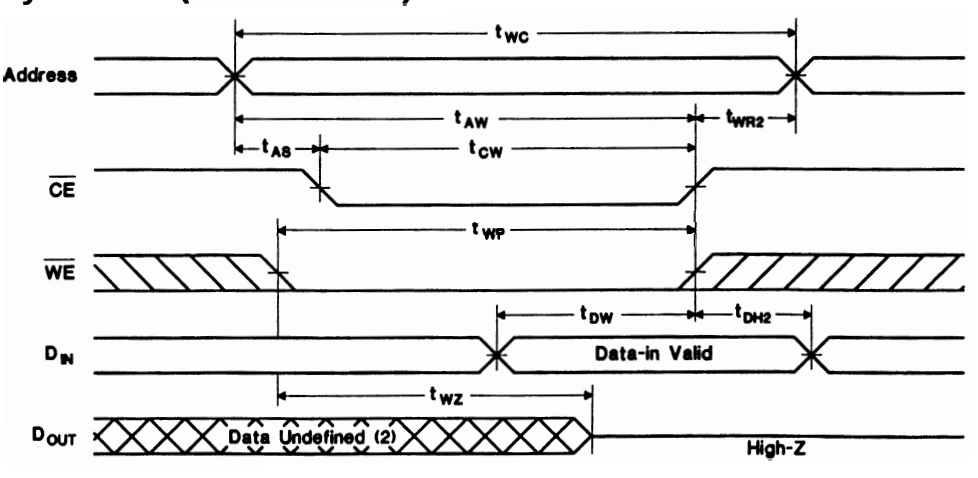
Notes:

1. A write ends at the earlier transition of $\overline{CE}$ going high and $\overline{WE}$ going high.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CE}$ going low and $\overline{WE}$ going low.
3. Either t_{WR1} or t_{WR2} must be met.
4. Either t_{DH1} or t_{DH2} must be met.
5. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

Write Cycle No. 1 ($\overline{WE}$-Controlled) 1,2,3



Write Cycle No. 2 ($\overline{CE}$-Controlled) 1,2,3,4,5



Notes:

1. $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
2. Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
3. If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.
4. Either t_{WR1} or t_{WR2} must be met.
5. Either t_{DH1} or t_{DH2} must be met.

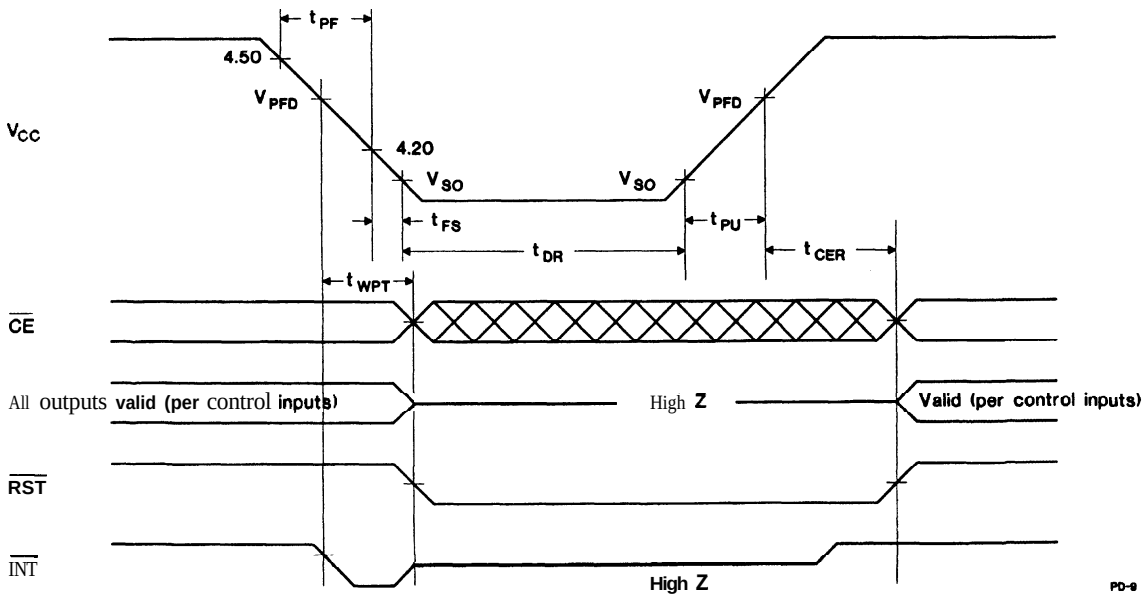
Power-Down/Power-Up Cycle (TA = TOPR)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_{PF}	V_{CC} slew, 4.50 to 4.20 V	300			µs	
t_{FS}	V_{CC} slew, 4.20 to V_{SO}	10			µs	
t_{PU}	V_{CC} slew, V_{SO} to V_{PFD} (max.)	0			µs	
t_{CER}	Chip enable recovery time	40	100	200	ms	Time during which SRAM is write-protected after V_{CC} passes V_{FPD} onpower-up.
t_{DR}	Data-retention time in absence of V_{CC}	10			years	T_A = 25°C. (2)
t_{WPT}	Write-protect time	40	100	160	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.

Notes:
1. Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.
2. Battery is disconnected from circuit until after V_{CC} is applied for the f i t time. t_{DR} is the accumulated time in absence of power beginning when power is first applied to the device.

Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

Power-Down/Power-Up Timing



Notes:
1. PWRIE is set to "1" to enable power fail interrupt.
2. $\overline{RST}$ and $\overline{INT}$ are open drain and require an external pull-up resistor.

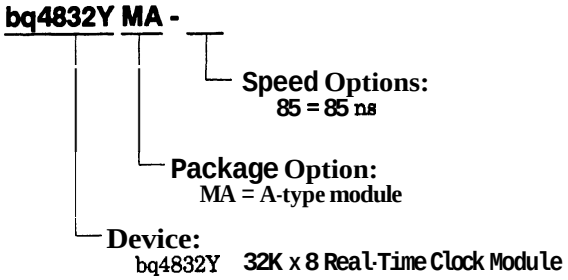
Data Sheet Revision History

Change No.	Page No.	Description
1	4	Corrected the locations of bits D6 and D4 of the Interrupts Register and the corresponding bits D5 and D3 of the Flags Register (these were reversed).
2	4	Corrected the alarm date register (7FF5) to allow for 01-31 days in a month instead of 01-07 days.
2	9	lowered I_{SB1} from 4, 7mA to 3, 6mA; lowered I_{SB2} typical from 2.5mA to 2mA.

Notes: Change 1 = Mar. 1996 B changes from Oct. 1995 A.
Change 2 = Sept. 1996 C changes from Mar. 1996 B.

5

Ordering Information



BENCHMARQ

bq4842Y

RTC Module With 128Kx8 NVSRAM

Features

- Integrated SRAM, real-time clock, CPU supervisor, crystal, power-fail control circuit, and battery
- Real-Time Clock counts hundredths of seconds through years in BCD format
- RAM-like clock access
- Compatible with industry-standard 128K x 8 SRAMs
- Unlimited write cycles
- 10-year minimum data retention and clock operation in the absence of power
- Automatic power-fail chip deselect and write-protection
- Watchdog timer, power-on reset, alarm/periodic interrupt, power-fail and battery-low warning
- Software clock calibration for greater than ±1 minute per month accuracy

General Description

The bq4842Y RTC Module is a non-volatile 1,048,576-bit SRAM organized as 131,072 words by 8 bits with an integral accessible real-time clock and CPU supervisor. The CPU supervisor provides a programmable watchdog timer and a microprocessor reset. Other features include an alarm, power-fail, and periodic interrupt and a battery low warning.

The device combines an internal lithium battery, quartz crystal, clock and power-fail chip, and a full CMOS SRAM in a plastic 32-pin DIP module. The RTC Module directly replaces industry-standard SRAMs and also fits into many EPROM and EEPROM sockets without any requirement for special write timing or limitations on the number of write cycles.

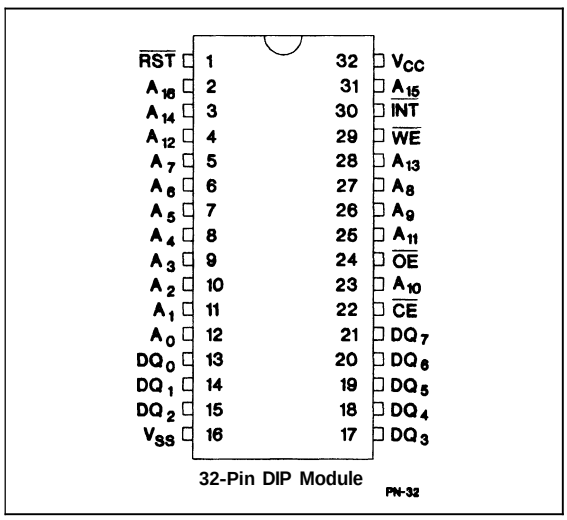
Registers for the real-time clock, alarm and other special functions are located in registers 1FFF0h–1FFFFh of the memory array.

The clock and alarm registers are dual-port read/write SRAM locations that are updated once per second by a clock control circuit from the internal clock counters. The dual-port registers allow clock updates to occur without interrupting normal access to the rest of the SRAM array.

The bq4842Y also contains a power-fail-detect circuit. The circuit deselects the device whenever V_{CC} falls below tolerance, providing a high degree of data security. The battery is electrically isolated when shipped from the factory to provide maximum battery capacity. The battery remains disconnected until the first application of V_{CC}.

5

Pin Connections



32-Pin DIP Module

PN-32

Pin Names

A_0–A_{16}	Address input
$\overline{CE}$	Chip enable
$\overline{RST}$	Microprocessor reset
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
DQ_0–DQ_7	Data in/data out
$\overline{INT}$	Programmable interrupt
V_{CC}	+5 volts
V_{SS}	Ground

Functional Description

Figure 1 is a block diagram of the bq4842Y. The following sections describe the bq4842Y functional operation, including memory and clock interface, data-retention modes, power-on reset timing, watchdog timer activation, and interrupt generation.

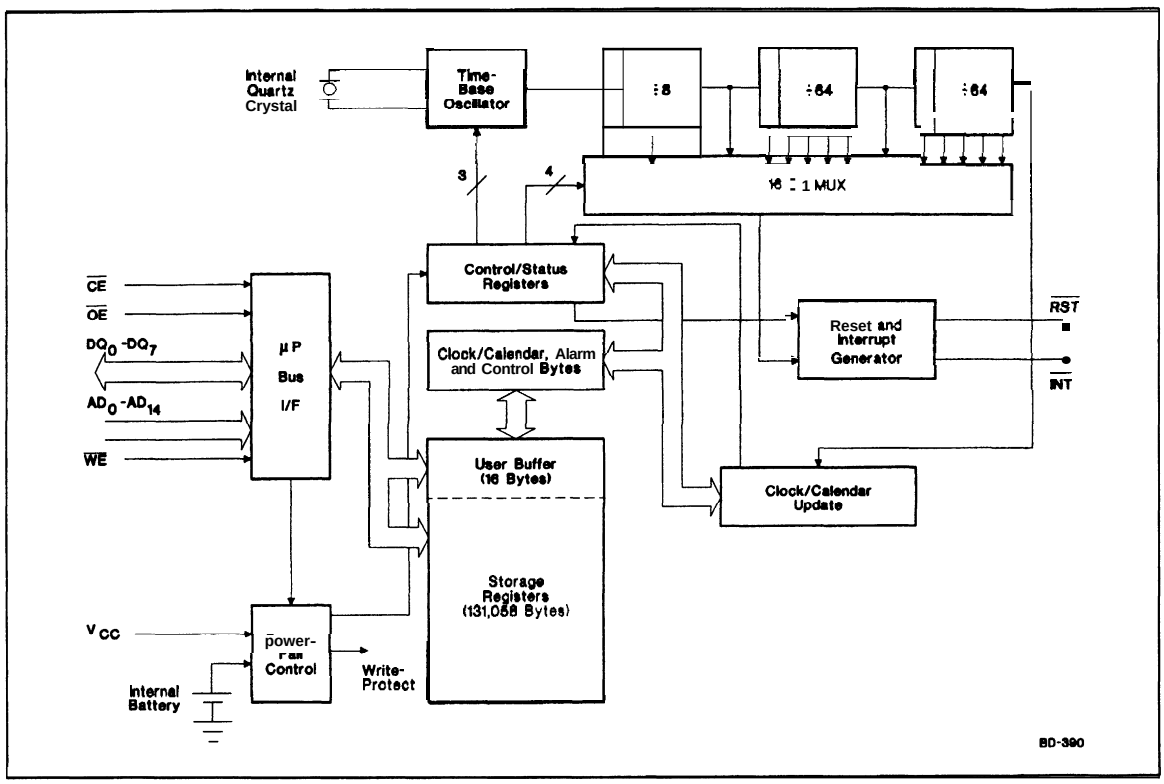


Figure 1. Block Diagram

Truth Table

Vcc	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	DQ	Power
< V_{CC} (max.)	V_{IH}	X	X	Deselect	High Z	Standby
	V_{IL}	X	V_{IL}	Write	Dm	Active
> Vcc (min.)	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
	V_{IL}	V_{IH}	V_{IH}	Read	High Z	Active
< V_{PFD} (min.) > V_{SO}	X	X	X	Deselect	High Z	CMOS standby
≤ V_{SO}	X	X	X	Deselect	High Z	Battery-backup mode

Address Map

The bq4842Y provides 16 bytes of clock and control status registers and 131,056 bytes of storage RAM.

Figure 2 illustrates the address map for the bq4842Y. Table 1 is a map of the bq4842Y registers, and Table 2 describes the register bite.

Memory Interface

Read Mode

The bq4842Y is in read mode whenever $\overline{OE}$ (output enable) is low and $\overline{CE}$ (chip enable) is low. The device architecture allows ripple-through access of data from eight of 1,048,576 locations in the static storage array. Thus, the unique address specified by the 17 address inputs defines which one of the 131,072 bytes of data is to be accessed. Valid data is available at the data I/O pins within t_{AA} (address access time) after the last address input signal is stable, providing that the $\overline{CE}$ and $\overline{OE}$ (output enable) access times are also satisfied. If the $\overline{CE}$ and $\overline{OE}$ access times are not met, valid data is available after the latter of chip enable access time (t_{ACE}) or output enable access time (t_{OE}).

$\overline{CE}$ and $\overline{OE}$ control the state of the eight three-state data I/O signals. If the outputs are activated before t_{AA}, the data lines are driven to an indeterminate state until t_{AA}. If the address inputs are changed while $\overline{CE}$ and $\overline{OE}$ remain low, output data remains valid for t_{OH} (output data hold time), but goes indeterminate until the next address access.

Write Mode

The bq4842Y is in write mode whenever $\overline{WE}$ and $\overline{CE}$ are active. The start of a write is referenced from the latter-occurring falling edge of $\overline{WE}$ 3 $\overline{CE}$. A write is terminated by the earlier rising edge of $\overline{WE}$ or $\overline{CE}$. The addresses must be held valid throughout the cycle. $\overline{CE}$ or $\overline{WE}$ must return high for a minimum of t_{WR2} from $\overline{CE}$ or t_{WR1} from $\overline{WE}$ prior to the initiation of another read or write cycle.

Data-in must be valid t_{DW} prior to the end of write and remain valid for t_{DH1} or t_{DH2} afterward. $\overline{OE}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{CE}$ and $\overline{OE}$, a low on $\overline{WE}$ disables the outputs t_{WZ} after $\overline{WE}$ falls.

Data-Retention Mode

With valid VCC applied, the bq4842Y operates as a conventional static RAM. Should the supply voltage decay, the RAM automatically power-fail deselects, write-protecting itself t_{WPT} after V_{CC} falls below V_{PFD}. All outputs become high impedance, and all inputs are treated as "don't care."

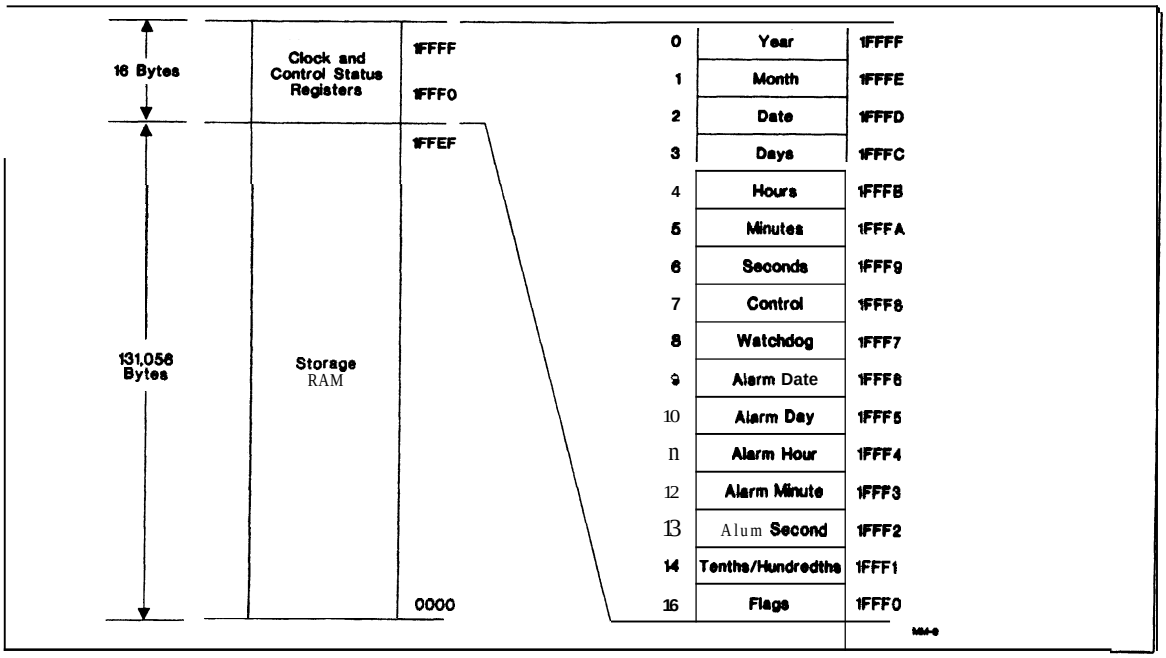


Figure 2. Address Map

If power-fail detection occurs during a valid access, the memory cycle continues to completion If the memory cycle fails to terminate within time t_{WPT}, write-protection takes place. When V_{CC} drops below V_{SO}, the control circuit switches power to the internal energy source, which preserve8 data.

The internal coin cell maintains data in the bq4842Y after the initial application of V_{CC} for an accumulated period of at least 10 years when V_{CC} is less than V_{SO}. As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. Write-prokctioncontinues for t_{CER} after V_{CC} reaches V_{PFD} to allow for processor stabilization After t_{CER}, normal RAM operation can resume.

Clock Interface

Reading the Clock

The interface to the clock and control registers of the bq4842Y is the same as that for the general-purpose storage memory. Once every second, the user-accessible clock/calendar locations are updated simultaneously from the internal real time counters. To prevent reading data in transition, updates to the bq4842Y clock registers should be halted. Updating ia halted by setting the read bit D6 of the control register to 1. As long as the read bit is 1, updates to user-accessible clock locations are inhibited. Once the frozen clock information is retrieved by reading the appropriate clock memory locations, the read bit should be reset to 0 in order to allow updates to *occur* from the internal counters. Because the internal counters are not halted by setting the read bit, reading the clock locations has no effect on clock accuracy. *Once* the read bit ia reset to 0, within one second the internal registers update the user-accessible registers with the correct time. A halt command issued during a clock update allows the update to occur before freezing the data.

Setting the Clock

Bit D7 of the control register is the write bit. Like the read bit, the write bit when set to a 1 halts updates to the clock/calendar memory locations. Once frozen, the locations can be written with the desired information in 24-hour BCD format. Resetting the write bit to 0 causes the written values to be transferred to the internal clock counters and allows updates to the user-accessible registers to resume within one second. Use the write bit, D7, only when updating the time registers (1FFF-1FFF9).

Table 1. bq4842 Clock and Control Register Map

Address	D7	D6	D5	D4	D3	D2	D1	D0	Range (h)	Register
1FFFF	10 Years				Year				00–99	Year
1FFFF	X	X	X	10 Month	Month				01–12	Month
1FFFD	X	X	10 Date		Date				01–31	Date
1FFFC	X	FTE	X	X	X	Day			01–07	Days
1FFFB	X	X	10 Hours		Hours				00–23	Hours
1FFFA	X	10 Minutes			Minutes				00–59	Minutes
1FFF9	OSC	10 Seconds			Seconds				00–59	Seconds
1FFF8	W	R	S	Calibration					00–31	Control
1FFF7	WDS	BM4	BM3	BM2	BM1	BM0	WD1	WD0		Watchdog
1FFF6	AIE	PWRIE	ABE	PIE	RS3	RS2	RS1	RS0		Interrupts
1FFF5	ALM3	X	10-date alarm		Alarm date				01–31	Alarm date
1FFF4	ALM2	X	10-hour alarm		Alarm hours				00–23	Alarm hours
1FFF3	ALM1	Alarm 10 minutes			Alarm minutes				00–59	Alarm minutes
1FFF2	ALM0	Alarm 10 seconds			Alarm seconds				00–59	Alarm seconds
1FFF1	0.1 seconds				0.01 seconds				00–99	0.1/0.01 seconds
1FFF0	WDF	AF	PWRF	BLF	PF	X	X	X		Flags

Note: X = Unused bits; can be written and read.
Clock/Calendar data in 24-hour BCD format.
BLF = 1 for valid battery.
OSC = 1 stops the clock oscillator.
Interrupt enables are cleared on power-up.

Table 2. Clock and Control Register Bits

Bits	Description
ABE	Alarm interrupt enable in battery-backup mode
AF	Alarm interrupt flag
AIE	Alarm interrupt enable
ALM0–ALM3	Alarm repeat rate
BLF	Battery-low flag
BM0–BM4	Watchdog multiplier
FTE	Frequency test mode enable
OSC	Oscillator stop
PF	Periodic interrupt flag
PIE	Periodic interrupt enable
PWRF	Power-fail interrupt flag
PWRIE	Power-fail interrupt enable
R	Read clock enable
RS0–RS3	Periodic interrupt rate
S	Calibration sign
W	Write clock enable
WD0–WD1	Watchdog resolution
WDF	Watchdog flag
WDS	Watchdog steering

Stopping and Starting the Clock Oscillator

The OSC bit in the seconds register turns the clock on or off. If the bq4842Y is to spend a significant period of time in storage, the clock oscillator can be turned off to preserve battery capacity. OSC set to 1 stops the clock oscillator. When OSC is reset to 0, the clock oscillator is turned on and clock updates to user-accessible memory locations occur within one second.

The *OSC* bit is set to 1 when shipped from the Benchmarq factory.

Calibrating the Clock

The bq4842Y real-time clock is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. The quartz crystal is contained within the bq4842Y package along with the battery. The clock accuracy of the bq4842Y module is tested to be within 20ppm a about 1 minute per month at 25°C. The oscillation rates of crystals change with temperature as Figure 3 shows. To compensate for the frequency shift, the bq4842Y offers onboard software clock calibration. The user can adjust the calibration based on the typical operating temperature of individual applications.

The software calibration bits are located m the control *register*. Bite D0–D4 control the magnitude of correction, and bit D5 the direction (positive or negative) of correction. Assuming that the oscillator is running at exactly 32,786 Hz, *each* calibration step of D0–D4 adjusts the clock rate by +4.068 ppm (+10.7 seconds per month) or -2.034 ppm (-5.35 seconds per month) depending on the value of the sign bit D6. When the sign bit is 1, positive adjustment occurs; a 0 activates negative adjustment. The total range of *clock* calibration is +5.5 *or* -276 minutes per month.

Two methods can be used to ascertain how much calibration a given bq4842Y may require in a system. The first involves simply setting the dock, letting it run for a month, and then comparing the time to an accurate known reference like WWV radio broadcasts. Based on the variation to the standard, the end user can adjust the clock to match the system's environment even after the product is packaged in a non-serviceable enclosure. The only requirement is a utility that allows the end user to access the calibration bits in the control register.

The second approach uses a bq4842Y test mode. When the frequency test mode enable bit FTE in the days register is set to a 1, and the oscillator is running at exactly 32,768 Hz, the LSB of the seconds register toggles at 512 Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.01024 Hz indicates a (1E6*0.01024)/512 or +20 ppm oscillator frequency error, requiring ten steps of negative calibration (10*-2.034 *or* -20.34) or 001010 to be loaded into the calibration byte for correction. To read the test frequency, the bq4842Y must be selected and held in an extended read of the seconds register, location 1FFF9, without having the read

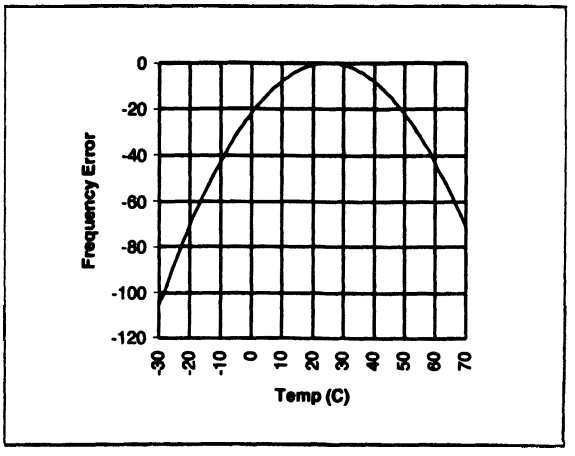


Figure 3. Frequency Error

bit set. The frequency appears on DQ0. The FTE bit must be set using the write bit control. The FTE bit must be reset to 0 for normal clock operation to resume.

Power-On Reset

The bq4842Y provides a power-on reset, which pulls the $\overline{RST}$ pin low on power-down and remains low on power-up for t_{CER} after V_{CC} passes V_{PFD}.

Watchdog Timer

The watchdog circuit monitors the microprocessor's activity. If the processor does not reset the watchdog timer within the programmed time-out period, the circuit asserts the $\overline{INT}$ or $\overline{RST}$ pin. The watchdog timer is activated by writing the desired time-out period into the eight-bit watchdog register described in Table 3 (device address 1FFF7). The five bits (BM4–BM0) store a binary multiplier, and the two lower-order bits (WD1–WD0) select the resolution, where 00 = 1/16 second, 01 = 1/4 second, 10 = 1 second, and 11 = 4 seconds.

The time-out period is the multiplication of the five-bit multiplier with the two-bit resolution. For example, writing 00011 in BM4–BM0 and 10 in WD1–WD0 results in a total time-out setting of 3 x 1 or 3 seconds. A multiplier of zero disables the watchdog circuit. Bit 7 of the watchdog register (WDS) is the watchdog steering bit. When WDS is set to a 1 and a time-out occurs, the watchdog asserts a reset pulse for t_{CER} on the $\overline{RST}$ pin. During the reset pulse, the watchdog register is cleared to all zeros disabling the watchdog. When WDS is set to a 0, the watchdog asserts the $\overline{INT}$ pin on a time-out. The $\overline{INT}$ pin remains low until the watchdog is reset by the microprocessor or a power failure occurs. Additionally, when the watchdog times out, the watchdog flag bit (WDF) in the flags register, location 1FFF0, is set.

To reset the watchdog timer, the microprocessor must write to the watchdog register. After being reset by a write, the watchdog time-out period starts over. As a precaution, the watchdog circuit is disabled on a power failure. The user must, therefore, set the watchdog at boot-up for activation.

Interrupts

The bq4842Y allows four individually selected interrupt events to generate an interrupt request on the $\overline{INT}$ pin. These four interrupt eventa are:

- The watchdog timer interrupt, programmable to occur according to the time-out period and conditions described in the watchdog timer section.
- The periodic interrupt, programmable to occur once every 122µs to 500ms.
- The alarm interrupt, programmable to occur once per second to once per month.
- The power-fail interrupt, which can be enabled to be asserted when the bq4842Y detects a power failure.

The periodic, alarm, and power-fail interrupts are enabled by an individual interrupt-enable bit in register 1FFF6, the interrupta register. When an event occurs, its event flag bit in the flage register, location 1FFF0, is set. If the corresponding event enable bit is also set, then an interrupt request is generated. Reading the flags register clears all flag bite and makes $\overline{INT}$ high impedance. To reset the flag register, the bq4842Y addresses must be held stable at location 1FFF0 for at least 50ns to avoid inadvertent resets.

Periodic Interrupt

Bits RS3–RS0 in the interrupts register program the rate for the periodic interrupt. The user can interpret the interrupt in two ways: either by polling the flags register for PF assertion or by setting PIE so that $\overline{INT}$ goes active when the bq4842Y sets the periodic flag. Reading the flags register resets the PF bit and returns $\overline{INT}$ to the high-impedance state. Table 4 shows the periodic rates.

Alarm Interrupt

Registers 1FFF5–1FFF2 program the real-time clock alarm. During each update cycle, the bq4842Y compares the date, hours, minutes, and seconds in the clock registers with the corresponding alarm registers. If a match between all the corresponding bytes is found, the alarm flag AF in the flags register is set. If the alarm interrupt is enabled with AIE, an interrupt request is generated on $\overline{INT}$. The alarm condition is cleared by a read to the flags

Table 3. Watchdog Register Bits

MSB			Bits				LSB
7	6	5	4	3	2	1	0
WDS	BM4	BM3	BM2	BM1	BMO	WD1	WD0

register. ALM3–ALM0 puts the alarm into a periodic mode of operation. Table 5 describes the selectable ratee.

The alarm interrupt can be made active while the bq4842Y is in the battery-backup mode by setting ABE in the interrupts register. Normally, the $\overline{INT}$ pin tri-states during battery backup. With ABE set, however, $\overline{INT}$ is driven low if an alarm condition occurs and the AIE bit is set. Because the AIE bit is reset during power-on reset, an alarm generated during power-on reset updates only the flags register. The user can read the flags register during boot-up to determine if an alarm was generated during power-on reset.

Power-Fail Interrupt

When V_{CC} falls to the power-faildetect point, the power-fail flag PWRF is set. If the power-fail interrupt enable bit (PWRIE) is also set, then $\overline{INT}$ is asserted low. The power-fail interrupt occurs t_{WPT} before the bq4842Y generates a reset and deselects. The PWIE bit is cleared *on* power-up.

Battery-Low Warning

The bq4842Y checks the internal battery on power-up. If the battery voltage is below 2.2V, the battery-low flag BLF in the flags register is set to a 1 indicating that clock and RAM data may be invalid.

Table 4. Periodic Rates

RS3	RS2	RS1	RS0	Interrupt Rate
0	0	0	0	None
0	0	0	1	10ms
0	0	1	0	100ms
0	0	1	1	122.07µs
0	1	0	0	244.14µs
0	1	0	1	488.281
0	1	1	0	976.5625
0	1	1	1	1.953125ms
1	0	0	0	3.90625ms
1	0	0	1	7.8125ms
1	0	1	0	15.625ms
1	0	1	1	31.25ms
1	1	0	0	62.5ms
1	1	0	1	125ms
1	1	1	0	250ms
1	1	1	1	500ms

Table 5. Alarm Frequency (Alarm Bits DQ7 of Alarm Registers)

ALM3	ALM2	ALM1	ALM0	Alarm Frequency
1	1	1	1	Once per second
1	1	1	0	Once per minute when seconds match
1	1	0	0	Once per hour when minutes, and seconds match
1	0	0	0	Once per day when hours, minutes, and seconds match
0	0	0	0	When date, hours, minutes, and seconds match

Absolute Maximum Ratings

Symbol	Parameter	Valw	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3to 7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	
T_{STG}	Storage temperature (V_{CC} off; oscillator off)	-40 to +70	°C	
T_{BIAS}	Temperature under bias	-10 to +70	°C	
T_{SOLDER}	Soldering temperature	+260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings are** exceeded. **Functional** operation should be limited to the Recommended DC **Operating Conditions** detailed in this data **sheet. Exposure** to **conditions** beyond the operational **limits** for extended periods of time may affect device reliability.

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	

Note: Typical values **indicate** operation at T_A = 25°C.

DC Electrical Characteristics (TA = TOPR, VCCmin ≤ VCC ≤ VCCmax)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current			± 1	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current			± 1	µA	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
V_{OH}	Output high voltage	2.4			V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage			0.4	V	I_{OL} = 2.1 mA
I_{OD}	$\overline{RST}$, $\overline{INT}$ sink current	10			mA	V_{OL} = 0.4V
I_{SB1}	Standby supply current		3	6	mA	$\overline{CE} = V_{IH}$
I_{SB2}	Standby supply current		2	4	mA	$\overline{CE} \geq V_{CC}$ - 0.2V, $V_{IN} \leq 0.2V$, or $V_{IN} \geq V_{CC}$ - 0.2V
I_{CC}	Operating supply current		75	105	mA	Min. cycle, duty = 100%, $\overline{CE} = V_{IL}$, $I_{I/O}$ = 0mA
V_{PFD}	Power-fail-detect voltage	4.30	4.37	4.50	V	
V_{SO}	Supply switch-over voltage		3		V	

Notes: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.
$\overline{RST}$ and $\overline{INT}$ are open-drain outputs.

5

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance			10	pF	Output voltage = 0V
C_{IN}	Input capacitance			10	pF	Input voltage = 0V

Note: These parameters are sampled and not 100% tested.

AC Test Conditions

Parameter	Test Condition8
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 4 and 5

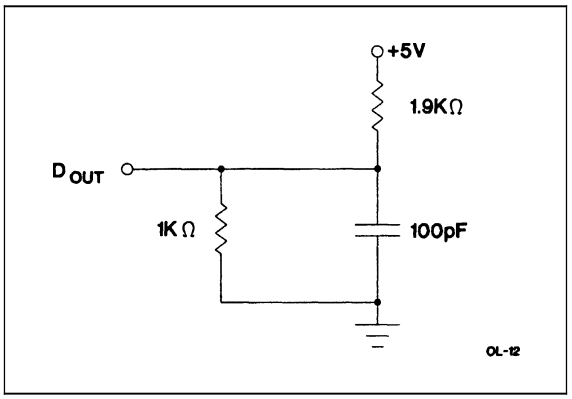


Figure 4. Output Load A

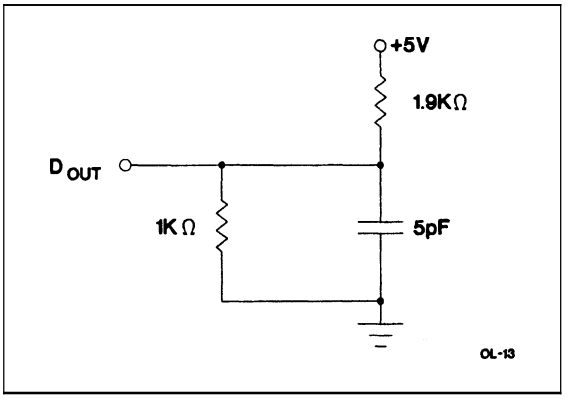
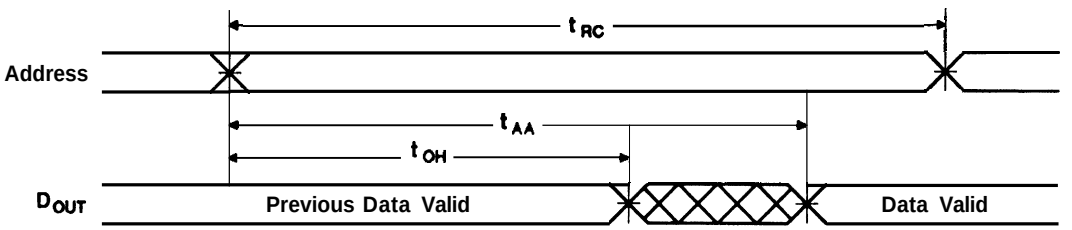


Figure 5. Output Load B

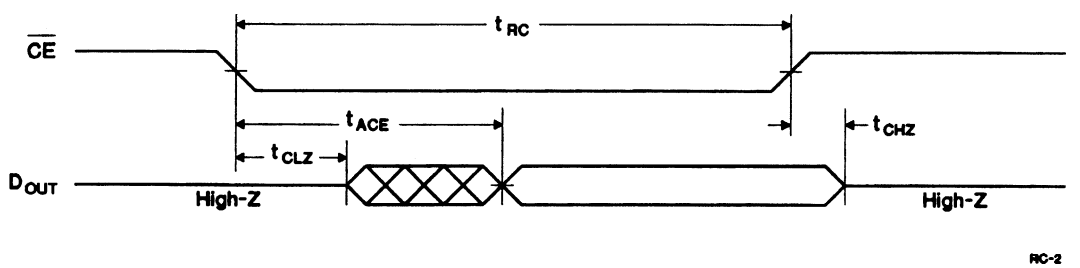
Read Cycle (TA = TOPR, VCCmin ≤ VCC ≤ VCCmax)

Symbol	Parameter	-85 Min.	-85 Max.	Unit	Conditions
t_{RC}	Read cycle time	85		ns	
t_{AA}	Address access time		85	ns	Output load A
t_{ACE}	Chip enable access time		85	ns	Outputload A
t_{OE}	Output enable to output valid		45	ns	Outputload A
t_{CLZ}	Chip enable to output in low Z	5		ns	Output load B
t_{OLZ}	Output enable to output in low Z	0		ns	Output load B
t_{CHZ}	Chip disable to output in high Z	0	35	ns	Output load B
t_{OHZ}	Output disable to output in high Z	0	25	ns	Outputload B
t_{OH}	Output hold from address change	10		ns	Output load A

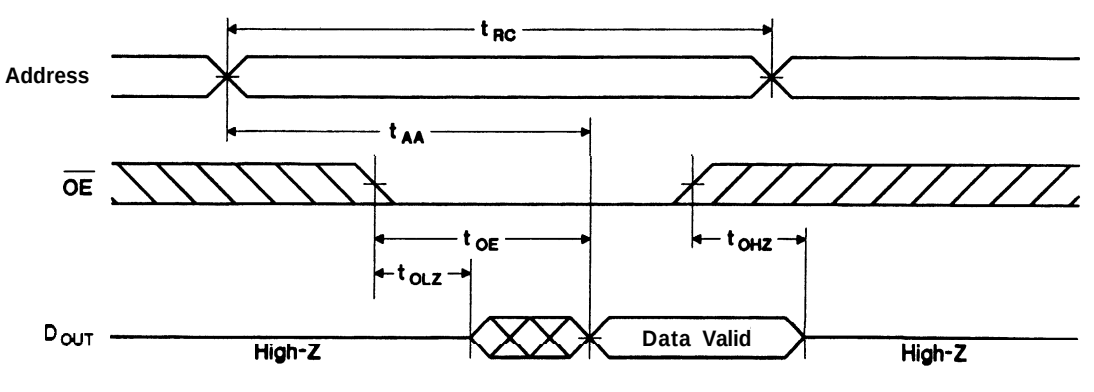
Read Cycle No. 1 (Address Access) [1,2]



Read Cycle No. 2 ($\overline{CE}$ Access) [1,3,4]



Read Cycle No. 3 ($\overline{OE}$ Access) [1,5]



Notes:
1. $\overline{WE}$ is held high for a read cycle.
2. Device is continuously selected: $\overline{CE}$ = $\overline{OE}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Device is continuously selected: $\overline{CE}$ = V_{IL}.

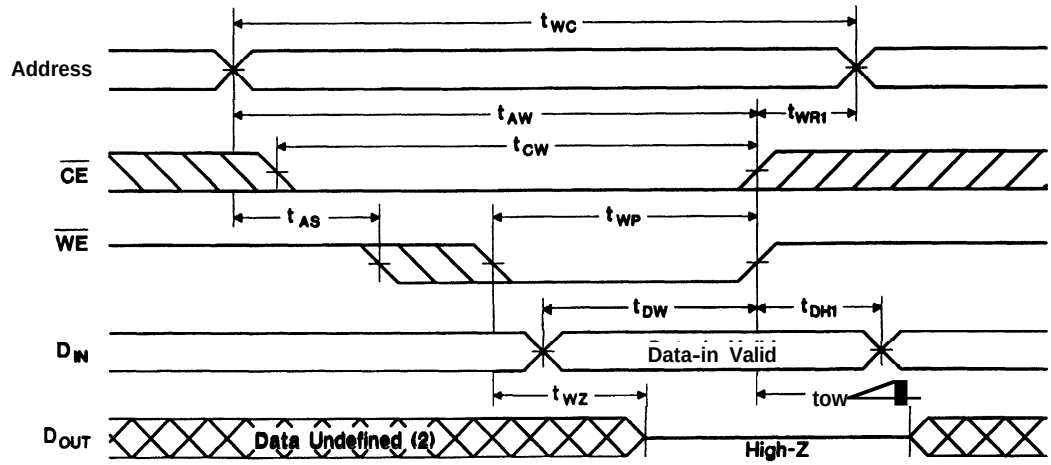
Write Cycle (TA = TOPR, VCCmin ≤ VCC ≤ VCCmax)

Symbol	Parameter	-85		Units	Conditions/Notes
		Min.	Max.		
t_{WC}	Write cycle time	85		ns	
t_{CW}	Chip enable to end of write	75		ns	(1)
t_{AW}	Address valid to end of write	75		ns	(1)
t_{AS}	Address setup time	0		ns	Measured from address valid to beginning of write. (2)
t_{WP}	Write pulse width	65		ns	Measured from beginning of write to end of write. (1)
t_{WR1}	Write recovery time (write cycle 1)	5		ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
t_{WR2}	Write recovery time (write cycle 2)	15		ns	Measured from $\overline{CE}$ going high to end of write cycle. (3)
t_{DW}	Data valid to end of write	35		ns	Measured to first low-to-high transition of either $\overline{CE}$ or $\overline{WE}$.
t_{DH1}	Data hold time (write cycle 1)	0		ns	Measured from $\overline{WE}$ going high to end of write cycle. (4)
t_{DH2}	Data hold time (write cycle 2)	10		ns	Measured from $\overline{CE}$ going high to end of write cycle. (4)
t_{WZ}	Write enabled to output in high Z	0	30	ns	I/O pins are in output state. (5)
t_{OW}	Output active from end of write	0		ns	I/O pins are in output state. (5)

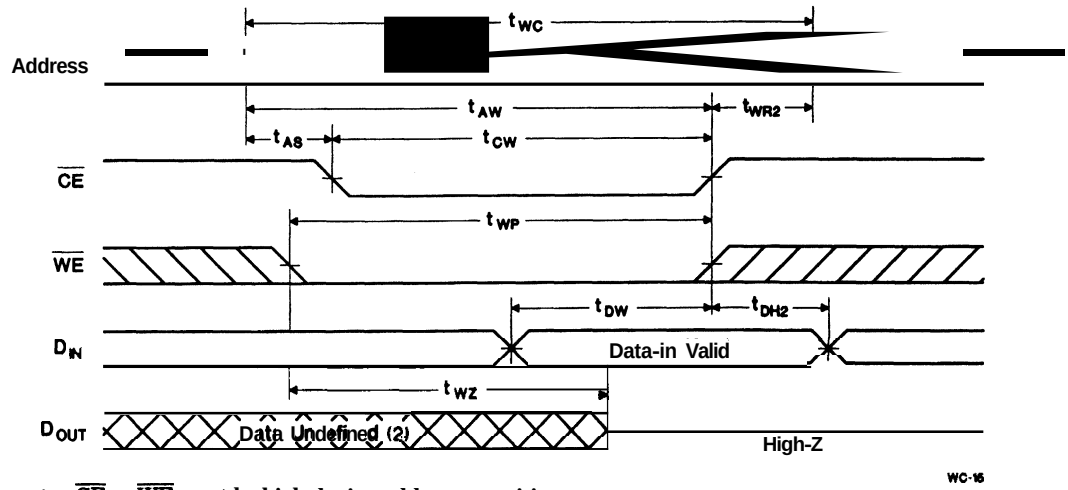
Notes:

1. A write ends at the earlier transition of $\overline{CE}$ going high and $\overline{WE}$ going high.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CE}$ going low and $\overline{WE}$ going low.
3. Either t_{WR1} or t_{WR2} must be met.
4. Either t_{DH1} or t_{DH2} must be met.
5. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

Write Cycle No. 1 ($\overline{WE}$-Controlled) 1,2,3



Write Cycle No. 2 ($\overline{CE}$-Controlled) 1,2,3,4,5



Notes:
1. $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
2. Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
3. If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.
4. Either t_{WR1} or t_{WR2} must be met.
5. Either t_{DH1} or t_{DH2} must be met.

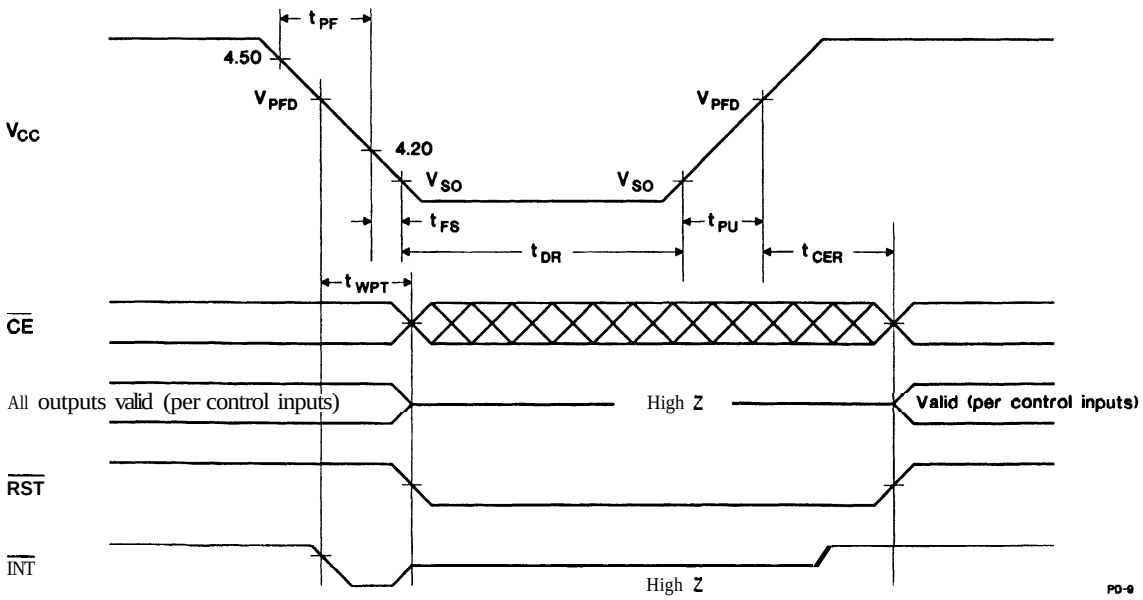
Power-Down/Power-Up Cycle (TA = TOPR)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_{PF}	V_{CC} slew, 4.50 to 4.20 V	300			µs	
t_{FS}	V_{CC} slew, 4.20 to V_{SO}	10			µs	
t_{PU}	V_{CC} slew, V_{SO} to V_{PFD} (max.)	0			µs	
t_{CER}	Chip enable recovery time	40	100	200	ms	Time during which SRAM is write-protected after V_{CC} passes V_{FPD} on power-up.
t_{DR}	Data-retention time in absence of V_{CC}	10			years	T_A = 25°C. (2)
t_{WPT}	Write-protect time	40	100	160	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.

Notes:
1. Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.
2. Battery is disconnected from circuit until after V_{CC} is applied for the first time. t_{DR} is the accumulated time in absence of power beginning when power is first applied to the device.

Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

Power-Down/Power-Up Timing



Notes:
1. PWRIE is set to '1' to enable power fail interrupt.
2. $\overline{RST}$ and $\overline{INT}$ are open drain and require an external pull-up resistor.

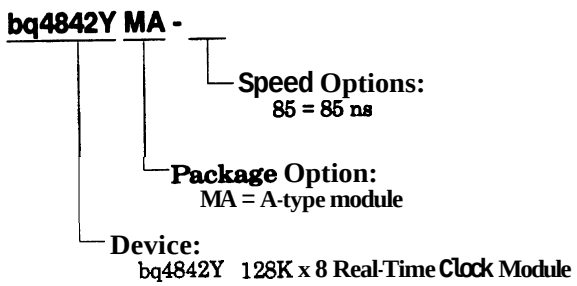
Data Sheet Revision History

Change No.	Page No.	Description
1	4	Corrected the locations of bits D6 and D4 of the Interrupts Register and the corresponding bits D5 and D3 of the Flaw Register (these were reversed).
2	4	Corrected the alarm date register (7FF5) to allow for 01-31 days in a month instead of 01-07 days.
2	9	Lowered I_{SB1} from 4 typ. and 7 max. to 3, 6. Lowered I_{SB2} typ. from 2.5 to 2.

Notes: Change 1 = Mar. 1996 B changes from Oct. 1995 A.
Change 2 = Sept. 1996 C changes from Mar. 1996 B.

5

Ordering Information



BENCHMARQ

bq4845/bq4845Y

Parallel RTC With CPU Supervisor

Features

- Real-Time Clock counts seconds through years in BCD fonnat
- On-chip battery-backup switchover circuit with nonvolatile control for external SRAM
- Less than 500nA of clock operation current in backup mode
- Microprocessor reset valid to $V_{CC} = V_{SS}$
- Independent watchdog timer with a programmable time-out period
- Power-fail interrupt warning
- Programmable clock alarm interrupt active in battery-backup mode
- ➤ Programmable periodic interrupt
- Battery-low warning

General Description

The bq4845 Real-Time Clock is a low-power microprocessor peripheral that integrates a time-of-day clock, a 100-year calendar, and a CPU supervisor in a 28-pin SOIC or DIP. The bq4845 is ideal for fax machines, copiers, industrial control system, point-of-sale terminals, data loggers, and computers.

The bq4845 provides direct connections for a 32.768KHz quartz crystal and a 3V backup battery. Through the use of the conditional chip enable output ($\overline{CE}_{OUT}$) and battery voltage output (V_{OUT}) pins, the bq4845 can write-protect and make nonvolatile external SRAMs. The backup cell powers the real-time clock and maintains SRAM information in the absence of system voltage.

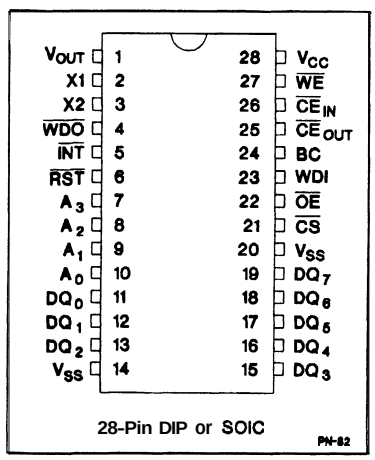
The bq4845 contains a temperature compensated reference and comparator circuit that monitors the status of its voltage supply. When the bq4845 detects an out-of-tolerance condition, it generates an interrupt warning and subsequently a microprocessor reset. The reset stays active for 200ms after V_{CC} rises within tolerance, to allow for power supply and processor stabilization.

The bq4845 also has a built-in watchdog timer to monitor processor operation. If the microprocessor does not toggle the watchdog input (WDI) within the programmed time-out period, the bq4845 asserts $\overline{WDO}$ and $\overline{RST}$. WDI unconnected disables the watchdog timer.

The bq4845 can generate other interrupta based on a clock alarm condition or a periodic setting. The alarm interrupt *can* be set to occur from once per second to once per month. The alarm *can* be made active in the battery-backup mode to serve as a system wake-up call. For interrupts at a rate beyond once per second, the periodic interrupt *can* be programmed with periods of 30.5µs to 500ms.

5

Pin Connections



Pin Names

A_0-A_3	Clock/control address inputs	BC	Backup battery input
DQ_0-DQ_7	Data inputs/outputs	V_{OUT}	Back-up battery output
$\overline{WE}$	Write enable	$\overline{INT}$	Interrupt output
$\overline{OE}$	Output enable	$\overline{RST}$	Microprocessor reset
$\overline{CS}$	Chip select input	WDI	Watchdog input
$\overline{CE}_{IN}$	External RAM chip enable	$\overline{WDO}$	Watchdog output
$\overline{CE}_{OUT}$	Conditional RAM chip enable	V_{CC}	+5V supply
X1, X2	Crystal inputs	V_{SS}	Ground

Functional Description

Figure 1 is a block diagram of the bq4845. The following sections describe the bq4845 functional operation including clock interface, data-retention modes, power-on reset timing, watchdog timer activation, and interrupt generation.

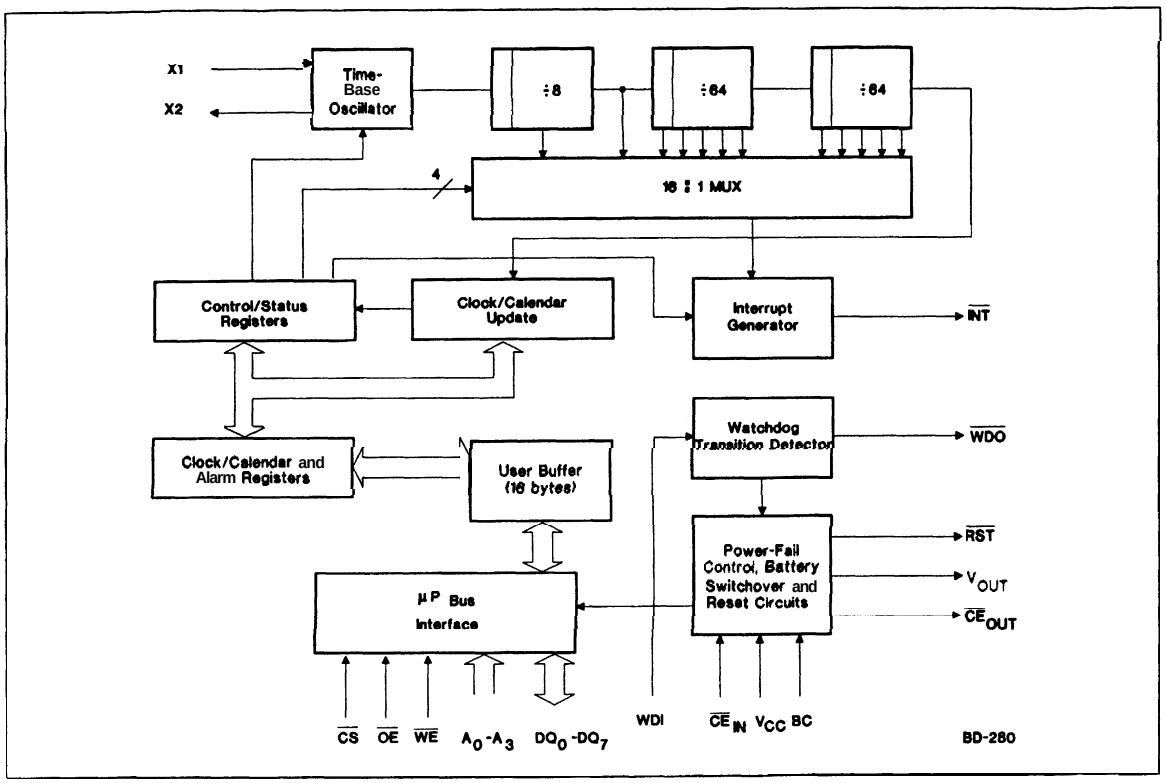


Figure 1. Block Diagram

Truth Table

VCC	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{CE}_{OUT}$	VOUT	Mode	DQ	Power
< VCC (max.)	VIH	X	X	$\overline{CE}_{IN}$	VOUT1	Deselect	High Z	Standby
	VIL	X	VIL	$\overline{CE}_{IN}$	VOUT1	Write	DIN	Active
> VCC (min.)	VIL	VIL	VIH	$\overline{CE}_{IN}$	VOUT1	Read	DOUT	Active
	VIL	VIH	VIH	$\overline{CE}_{IN}$	VOUT1	Read	High Z	Active
< VPFD (min.) > VSO	X	X	X	VOH	VOUT1	Deselect	High Z	CMOS standby
≤ VSO	X	X	X	VOHB	VOUT2	Deselect	High Z	Battery-backup mode

Pin Descriptions

X1, X2 **Crystal inputs**

X1 and X2 are a direct connection for a 32.768kHZ, 6pF crystal.

$\overline{RST}$ **Reset output**

$\overline{RST}$ goes low whenever V_{CC} falls below the power fail threshold. $\overline{RST}$ will remain low for 200ms typical after V_{CC} crosses the threshold on power-up. $\overline{RST}$ also goes low whenever a watchdog timeout occurs. $\overline{RST}$ is an open-drain output.

$\overline{INT}$ **Interrupt output**

$\overline{INT}$ goes low when a power fail, periodic, or alarm condition occurs. $\overline{INT}$ is an open-drain output.

WDI **Watchdog input**

WDI is a three-level input. If WDI remains either high or low for longer than the watchdog time-out period (1.5 seconds default), $\overline{WDO}$ goes low. $\overline{WDO}$ remains low until the next transition at WDI. Leaving WDI unconnected disables the watchdog function. WDI connects to an internal voltage divider between V_{OUT} and V_{SS}, which sets it to mid-supply when left unconnected.

$\overline{WDO}$ **Watchdog output**

$\overline{WDO}$ goes low if WDI remains either high or low longer than the watchdog time-out period. $\overline{WDO}$ e—— high on the next transition at WDI. WDO remains high if WDI is unconnected.

A_0-A_3 **Clock address inputs**

Ao-As allow access to the 16 bytes of real-time clock and control registers.

DQ_0-DQ_7 **Data input and output**

DQ_0-DQ_7 provide x8 data for real-time clock information. These pins connect to the memory data bus.

V_{SS} **Ground**

$\overline{CS}$ **Chip select**

$\overline{OE}$ **Output enable**

$\overline{OE}$ provides the read control for the RTC memory locations.

$\overline{CE}_{OUT}$ **Chip enable output**

$\overline{CE}_{OUT}$ goes low only when $\overline{CE}_{IN}$ is low and V_{CC} is above the power fail threshold. If $\overline{CE}_{IN}$ is low, and power fail occurs, $\overline{CE}_{OUT}$ will stay low for 100µs or until $\overline{CE}_{IN}$ goes high, whichever occurs first.

$\overline{CE}_{IN}$ **Chip enable input**

$\overline{CE}_{IN}$ is the input to the chip-enable gating circuit.

BC **Backup battery input**

BC should be connected to a 3V backup cell. A voltage within the V_{BC} range on the BC pin should be present upon power up to provide proper oscillator start-up.

V_{OUT} **Output supply** voltage

V_{OUT} provides the higher of V_{CC} or V_{BC}, switched internally, to supply external RAM.

$\overline{WE}$ **Write enable**

$\overline{WE}$ provides the write control for the RTC memory locations.

V_{CC} **Input supply** voltage

+5V input

5

Address Map

The bq4845 provides 16 bytes of clock and control status registers. Table 1 is a map of the bq4845 registers, and Table 2 describes the register bits.

Clock Memory Interface

The bq4845 has the same interface for clock/calendar and control information as standard SRAM. To read and write to these locations, the user must put the bq4845 in the proper mode and meet the timing requirements.

Read Mode

The bq4845 is in read mode whenever $\overline{OE}$ (Output enable) is low and $\overline{CS}$ (chip select) is low. The unique address, specified by the 4 address inputs, defines which one of the 16 clock/calendar bytes is to be accessed. The bq4845 makes valid data available at the data I/O pins within t_{AA} (address access time). This occurs after the last address input signal is stable, and providing the $\overline{CS}$ and $\overline{OE}$ (output enable) access times are met. If the $\overline{CS}$ and $\overline{OE}$ access times are not met, valid data is available after the latter of chip select access time (t_{ACS}) or output enable access time (t_{OE}).

$\overline{CS}$ and $\overline{OE}$ control the state of the eight three-state data I/O signals. If the outputs are activated before t_{AA}, the

Table 1. bq4845 Clock and Control Register Map

Address (h)	D7	D6	D5	D4	D3	D2	D1	D0	12-Hour Range (h)	Register
0	0	10-second digit			1-second digit				00–59	Seconds
1	ALM1	ALM0	10-second digit		1-second digit				00–59	Seconds alarm
2	0	10-minute digit			1-minute digit				00–59	Minutes
3	ALM1	ALM0	10-minute digit		1-minute digit				00–59	Minutes alarm
4	PM/AM	0	10-hour digit		1-hour digit				01–12 AM/ 81–92 PM	Hours
5	ALM1 / PM/AM	ALM0	10-hour digit		1-hour digit				01–12 AM/ 81–92 PM	Hours alarm
6	0	0	10-day digit		1-day digit				01–31	Day
7	ALM1	ALM0	10-day digit		1-day digit				01–31	Day alarm
8	0	0			0	Day-of-week digit			01–07	Day-of-week
9	0	0	0	10 mo.	1-month digit				01–12	Month
A	10-year digit				1-year digit				00–99	Year
B	*	WD2	WD1	WD0	RS3	RS2	RS1	RS0		Programmable rates
C	*	*			AIE	PIE	PWRIE	ABE		Interrupt enables
D	*	*			AF	PF	PWRF	BVF		Flags
E	*	*			UTI	$\overline{STOP}$	24/12	DSE		Control
F	*	*	*	*	*	*	*	*		Unused

Notes: * = Unused bits; unwritable and read as 0.
0 = should be set to 0 for valid time/calendar range.
Clock calendar data in BCD. Automatic leap year adjustment.
PM/AM = 1 for PM; PM/AM = 0 for AM.
DSE = 1 enables daylight savings adjustment.
24/12 = 1 enables 24-hour data representation; 24/12 = 0 enables 12-hour data representation.
Day-of-Week coded as Sunday = 1 through Saturday = 7.
BVF = 1 for valid battery.
$\overline{STOP}$ = 1 turns the RTC on; $\overline{STOP}$ = 0 stops the RTC in back-up mode.
Register C is cleared on power-up.

Table 2. Clock and Control Register Bits

Bits	Description
24/12	24- or 12-hour representation
ABE	Alarm interrupt enable in battery-backup mode
AF	Alarm interrupt flag
AIE	Alarm interrupt enable
ALM0–ALM1	Alarm mask bits
BVF	Battery-valid flag
DSE	Daylight savings time enable
PF	Periodic interrupt flag
PIE	Periodic interrupt enable
PM/AM	PM or AM indication
PWRF	Power-fail interrupt flag
PWRIE	Power-fail interrupt enable
RS0–RS3	Periodic interrupt rate
$\overline{STOP}$	Oscillator stop and start
UTI	Update transfer inhibit
WD0 - WD2	Watchdog time-out rate

data lines are driven to an indeterminate state until t_{AA}. If the address inputs are changed while $\overline{CS}$ and $\overline{OE}$ remain low, output data remains valid for t_{OH} (output data hold time), but goes indeterminate until the next address access.

Write Mode

The bq4845 is in write mode whenever $\overline{WE}$ and $\overline{CS}$ are active. The *start* of a write is referenced from the latter-occurring falling edge of $\overline{WE}$ or $\overline{CS}$. A write is terminated by the earlier rising edge of $\overline{WE}$ or $\overline{CS}$. The addresses muet be held valid throughout the cycle. $\overline{CS}$ or $\overline{WE}$ must return high for a minimum of t_{WR2} from $\overline{CS}$ or t_{WR1} from $\overline{WE}$ prior to the initiation of another read or write cycle.

Data-in must be valid t_{DW} prior to the end of write and remain valid for t_{DH1} or t_{DH2} afterward. $\overline{OE}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{CS}$ and $\overline{OE}$, a low on $\overline{WE}$ disables the outputs t_{WZ} after $\overline{WE}$ falls.

Reading the Clock

Once every second, the user-accessible clock/calendar locations are updated simultaneously from the internal real time counters. To prevent reading data in transition, updatee to the bq4845 clock registers should be halted. Updating is halted by setting the update transfer inhibit (UTI) bit D3 of the control register E. As long as the UTI bit is 1, updatee to user-accessible clock locations are inhibited. Once the frozen clock information b retrieved by reading the appropriate clock memory locations, the UTI bit should be reset to 0 in order to allow updatee to occur from the internal counters. Because the internal counters are not halted by setting the UTI bit, reading the clock locations has no effect on clock accuracy. Once the UTI bit is reset to 0, the internal registers update within one second the user-accessible registers with the correct time. A halt command issued during a clock update allows the update to occur before freezing the data.

Setting the Clock

The UTI bit must also be used to set the bq4845 clock. Once set, the locations can be written with the desired information in BCD format. Resetting the UTI bit to 0 causes the written values to be transferred to the internal clock counters and allows updates to the user-accessible registers to resume within one second.

Stopping and Starting the Clock Oscillator

The bq4845 clock can be programmed to turn off when the part goes into battery back-up mode by setting $\overline{STOP}$ to 0 prior to power down. If the board using the bq4845 is to spend a significant period of time in storage, the $\overline{STOP}$ bit can be used to preserve some battery capacity. $\overline{STOP}$ set to 1 keeps the clock running when V_{CC} drops below V_{SO}. With V_{CC} greater than V_{SO}, the bq4845 clock runs regardless of the state of $\overline{STOP}$.

Power-Down/Power-Up Cycle

The bq4845 continuously monitors V_{CC} for out-of-tolerance. During a power failure, when V_{CC} falls below V_{PFD}, the bq4845 write-protects the clock and storage registers. When V_{CC} is below V_{BC} (3V typical), the power source is switched to BC. RTC operation and storage data are sustained by a valid backup energy source. When V_{CC} is above V_{BC}, the power source is V_{CC}. Write-protection continues for t_{CSR} time after V_{CC} rises above V_{PFD}.

An external CMOS static RAM is battery-backed using the V_{OUT} and chip enable output pins from the bq4845. As the voltage input V_{CC} slews down during a power failure, the chip enable output, $\overline{CE}_{OUT}$, is forced inactive independent of the chip enable input $\overline{CE}_{IN}$.

This activity unconditionally write-protects the external SRAM as V_{CC} falls below V_{PFD}. If a memory access is in progress to the external SRAM during power-fail detection, that memory cycle continues to completion before the memory is write-protected. If the memory cycle is not terminated within time t_{WPT}, the chip enable output is unconditionally driven high, write-protecting the controlled SRAM.

As the supply continues to fall past V_{PFD}, an internal switching device forces VOW to the external backup energy source. $\overline{CE}_{OUT}$ is held high by the V_{OUT} energy source.

During power-up, V_{OUT} is switched back to the 5V supply as V_{CC} rises above the backup cell input voltage sourcing V_{OUT}. $\overline{CE}_{OUT}$ is held inactive for time t_{CER} after the power supply has reached V_{PFD}, independent of the $\overline{CE}_{IN}$ input, to allow for processor stabilization.

During power-valid operation, the $\overline{CE}_{IN}$ input is passed through to the CEom output with a propagation delay of less than 12ns.

Figure 2 shows the hardware. hookup for the external RAM, battery, and crystal.

A primary backup energy source input is provided on the bq4845. The BC input accepts a 3V primary battery, typically some type of lithium chemistry. Since the bq4845 provides for reverse battery charging protection, no diode or current limiting resistor is needed in series with the cell. To prevent battery drain when there is no valid data to retain, V_{OUT} and $\overline{CE}_{OUT}$ are internally isolated from BC by the initial connection of a battery. Following the first application of V_{CC} above V_{PFD}, this isolation is broken, and the backup cell provides power to V_{OUT} and $\overline{CE}_{OUT}$ for the external SRAM.

The crystal should be located as close to X1 and X2 as possible and meet the specifications in the *Crystal* Specification Table. With the specified crystal, the bq4845 RTC will be accurate to within one minute per month at room temperature. In the absence of a crystal, a 32.768 kHz waveform can be fed into X1 with X2 grounded.

Power-On Reset

The bq4845 provides a power-on reset, which pulls the $\overline{RST}$ pin low on power-down and remains low on power-up for t_{RST} after V_{CC} passes V_{PFD}. With valid battery voltage on BC, $\overline{RST}$ remains valid for V_{CC}= V_{SS}.

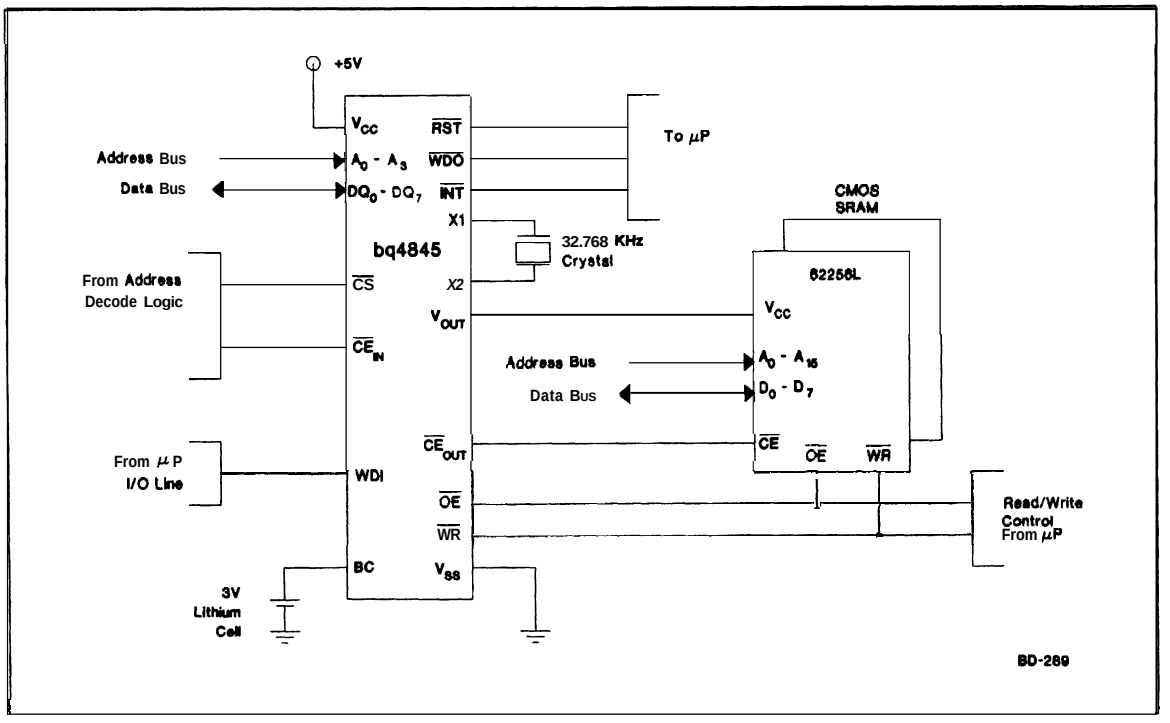


Figure 2. bq4845 Application Circuit

Watchdog Timer

The watchdog monitors microprocessor activity through the Watchdog input (WDI). To use the watchdog function, connect WDI to a bus line or a microprocessor I/O line. If WDI remains high or low for longer than the watchdog time-out period (1.5 seconds default), the bq4845 asserts $\overline{WDO}$ and $\overline{RST}$.

Watchdog Input

The bq4845 resets the watchdog timer if a change of state (high to low, low to high, or a minimum 100ns pulse) occurs at the Watchdog input (WDI) during the watchdog period. The watchdog time-out is set by WD0-WD2 in register B. The bq4845 maintains the watchdog time-out programming through power cycles. The default state (no valid battery power) of WD0-WD2 is 000 or 1.5s on power-up. Table 3 shows the programmable watchdog time-out rates. The watchdog time-out period immediately after a reset is equal to the programmed watchdog time-out.

To disable the watchdog function, leave WDI floating. An internal resistor network (100kΩ equivalent impedance at WDI) biases WDI to approximately 1.6V, internal comparators detect this level and disable the watchdog timer. When V_{CC} is below the power fail threshold, the bq4845 disables the watchdog function and disconnects WDI from its internal resistor network, thus making it high impedance.

Watchdog Output

The Watchdog output ($\overline{WDO}$) remains high if there is a transition or pulse at WDI during the watchdog time-out period. The bq4845 disables the watchdog function and $\overline{WDO}$ is a logic high when V_{CC} is below the power fail threshold, battery-backup mode is enabled, or WDI is an open circuit. In watchdog mode, if no transition occurs at WDI during the watchdog time-out period, the bq4845 asserts $\overline{RST}$ for the reset time-out period t_1. $\overline{WDO}$ goes low and remains low until the next transition at WDI. If WDI is held high or low indefinitely, $\overline{RST}$ will generate pulses (t_1 seconds wide) every t_3 seconds. Figure 3 shows the watchdog timing.

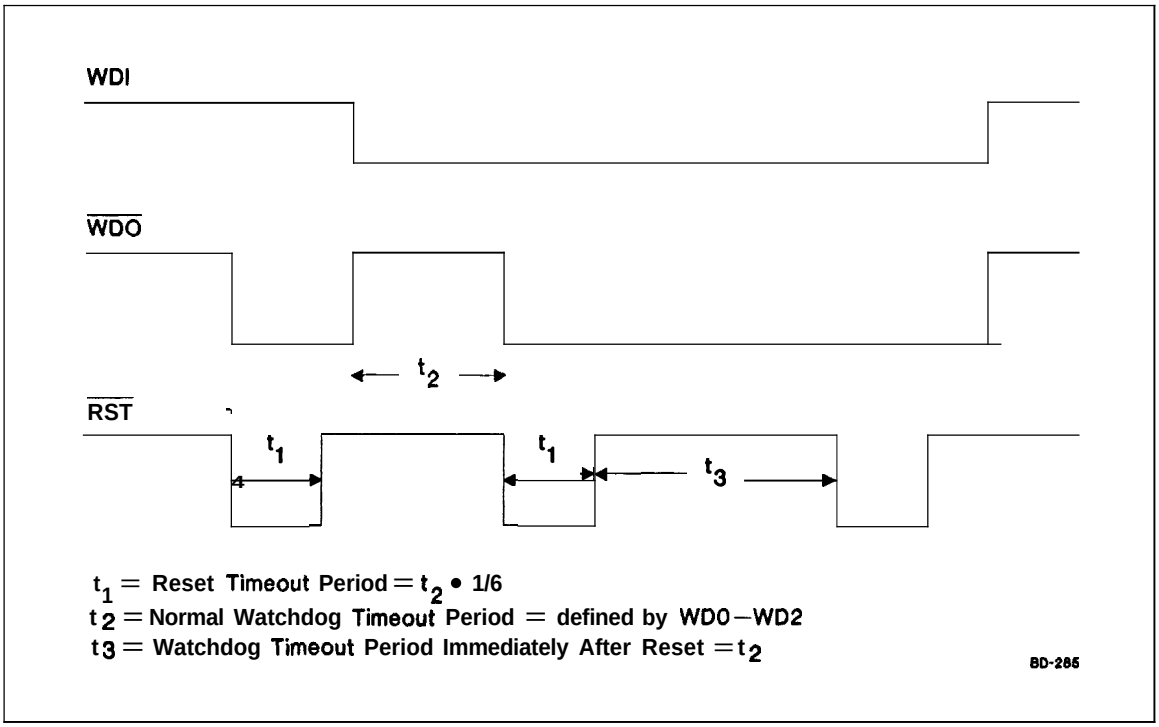


Figure 3. Watchdog Time-out Period and Reset Active Time

Interrupts

The bq4845 allows three individually selected interrupt events to generate an interrupt request on the $\overline{INT}$ pin. These three interrupt events are:

- The periodic interrupt, programmable to occur once every 30.5µs to 500ms
- The alarm interrupt, programmable to occur once per second to once per month
- The power-fail interrupt, which can be enabled to be asserted when the bq4845 detects a power failure

The periodic, alarm, and power-fail interrupts are enabled by an individual interrupt-enable bit in register C, the interrupts register. When an event occurs, its event flag bit in the flags register, register D, is set. If the corresponding event enable bit is also set, then an interrupt request is generated. Reading the flags register clears all flag bits and makes $\overline{INT}$ high impedance. To reset the flag register, the bq4845 addresses must be held stable at register D for at least 50ns to avoid inadvertent resets.

Periodic Interrupt

Bits RS3–RS0 in the interrupts register program the rate for the periodic interrupt. The user can interpret the interrupt in two ways: either by polling the flags register for PF assertion or by setting PIE so that $\overline{INT}$ goes active when the bq4845 sets the periodic flag. Reading the flags register resets the PF bit and returns $\overline{INT}$ to the high-impedance state. Table 4 shows the periodic rates.

Alarm Interrupt

Registers 1, 3, 5, and 7 program the real-time clock alarm. During each update cycle, the bq4845 compares the date, hours, minutes, and seconds in the clock registers with the corresponding alarm registers. If a match between all the corresponding bytes is found, the alarm flag AF in the flags register is set. If the alarm interrupt is enabled with AIE, an interrupt request is generated on $\overline{INT}$. The alarm condition is cleared by a read to the flags register. ALM1 – ALM0 in the alarm registers, mask each alarm compare byte. An alarm byte is masked by setting ALM1 (D7) and ALM0 (D6) to 1. Alarm byte masking can be used to select the frequency of the alarm interrupt, according to Table 5.

The alarm interrupt can be made active while the bq4845 is in the battery-backup mode by setting ABE in the interrupts register. Normally, the $\overline{INT}$ pin goes high-impedance during battery backup. With ABE set, however, $\overline{INT}$ is driven low if an alarm condition occurs and the AIE bit is set. Because the AIE bit is reset during power-on reset, an alarm generated during power-on reset updates only the flags register. The user can read the flags register during boot-up to determine if an alarm was generated during power-on reset.

Power-Fail Interrupt

When V_{CC} falls to the power-fail-detect point, the power-fail flag PWRF is set. If the power-fail interrupt enable bit (PWRIE) is also set, then $\overline{INT}$ is asserted low. The power-fail interrupt occurs t_{WPT} before the bq4845 generates a reset and deselects. The PWRIE bit is cleared on power-up.

Battery-Low Warning

The bq4845 checks the battery on power-up. When the battery voltage is approximately 2.1V, the battery-valid flag BVF in the flags register is set to a 0 indicating that clock and RAM data may be invalid.

Table 3. Watchdog Time-out Rates

WD2	WD1	WDO	Normal Watchdog time-out Period (t_2, t_3)	Reset time-out Period (t_1)
0	0	0	1.5s	0.25s
0	0	1	23.4375ms	3.9063ms
0	1	0	46.875ms	7.8125ms
0	1	1	93.75ms	15.625ms
1	0	0	187.5ms	31.25ms
1	0	1	375ms	62.5ms
1	1	0	750ms	125ms
1	1	1	3s	0.5s

Table 4. Periodic Interrupt Rates

Register B Bits				Periodic Interrupt	
RS3	RS2	RS1	RS0	Period	Units
0	0	0	0	None	
0	0	0	1	30.5175	us
0	0	1	0	61.035	µs
0	0	1	1	122.070	µs
0	1	0	0	244.141	µs
0	1	0	1	488.281	µs
0	1	1	0	976.5625	µs
0	1	1	1	1.953125	ms
1	0	0	0	3.90625	ms
1	0	0	1	7.8125	ms
1	0	1	0	15.625	ms
1	0	1	1	31.25	ms
1	1	0	0	62.5	ms
1	1	0	1	125	ms
1	1	1	0	250	ms
1	1	1	1	500	ms

5

Table 5. Alarm Frequency (Alarm Bits D6 and D7 of Alarm Registers)

1h	3h	5h	7h	
ALM1•ALM0	ALM1•ALM0	ALM1• ALMO	ALM1• ALMO	Alarm Frequency
1	1	1	1	Once per second
0	1	1	1	Once per minute when seconds match
0	0	1	1	Once per hour when minutes, and seconds match
0	0	0	1	Once per day when hours, minutes, and seconds match
0	0	0	0	When date, hours, minutes, and seconds match

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on Vcc relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding Vcc relative to V_{SS}	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
		-40 to +85	°C	Industrial
T_{STG}	Storage temperature	-55 to +125	°C	
T_{BIAS}	Temperature under bias	-40 to +85	°C	
T_{SOLDER}	Soldering temperature	+260	°C	For 10 seconds

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions (T_A = TOPR)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	bq4845Y
		4.75	5.0	5.5	V	bq4845
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3		0.8	V	
V_{IH}	Input high voltage	2.2		Vcc + 0.3	V	
V_{BC}	Backup cell voltage	2.3		4.0	V	

Note: Typical values indicate operation at T_A = 25°C.

DC Electrical Characteristics (T_A = TOPR, VCCmin ≤ VCC ≤ VCCmax)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 1	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current	-	-	± 1	µA	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -2.0 mA
V_{OHB}	V_{OH}, BC Supply	V_{BC}- 0.3	-	-	V	$V_{BC} > V_{CC}$, I_{OH} = -10µA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 4.0 mA
I_{CC}	Operating supply current	-	12	25	mA	Min. cycle, duty = 100%, $\overline{CS} = V_{IL}$, $I_{I/O}$ = 0mA
I_{SB1}	Standby supply current	-	3	-	mA	$\overline{CS} = V_{IH}$
I_{SB2}	Standby supply current	-	1.5	-	mA	$\overline{CS} \geq V_{CC}$ - 0.2V, 0V ≤ V_{IN} ≤ 0.2V, or $V_{IN} \geq V_{CC}$ - 0.2V
V_{SO}	Supply switch-over voltage	-	V_{BC}	-	V	
I_{CCB}	Battery operation current	-	0.3	0.5	µA	V_{BC} = 3V, T_A = 25°C, no load on V_{OUT} or $\overline{CE}_{OUT}$
V_{PFD}	Power-fail-detect voltage	4.55	4.62	4.75	V	bq4845
	Power-fail-detect voltage	4.30	4.37	4.5	V	bq4845Y
V_{OUT1}	V_{OUT} voltage	V_{CC} - 0.3V	-	-	V	I_{OUT} = 100mA, $V_{CC} > V_{BC}$
V_{OUT2}	V_{OUT} voltage	V_{BC} - 0.3V	-	-	V	I_{OUT} = 100µA, $V_{CC} < V_{BC}$
V_{RST}	$\overline{RST}$ output voltage	-	-	0.4V	-	I_{RST} = 4mA
V_{INT}	$\overline{INT}$ output voltage	-	-	0.4V	-	I_{INT} = 4mA
V_{WDO}	$\overline{WDO}$ output voltage	-	-	0.4V	-	I_{SINK} = 4mA
		2.4	-	-	-	I_{SOURCE} = 2mA
I_{WDIL}	Watchdog input low current	-50	-10	-	µA	0 < V_{WDI} < 0.8V
I_{WDIH}	Watchdog input high current	-	20	50	µA	2.2 < V_{WDI} < V_{CC}

Notes: Typical values indicate operation at T_A = 25°C, Vcc = 5V.
$\overline{RST}$ and $\overline{INT}$ are open-drain outputs.

Crystal Specifications (DT-26 or Equivalent)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
f_O	Oscillation frequency		32.768		kHz
C_L	Load capacitance		6		pF
T_P	Temperature turnover point	20	25	30	°C
k	Parabolic curvature constant			-0.042	ppm/°C
Q	Quality factor	40,000	70,000		
R_1	Series resistance			45	KΩ
C_0	Shunt capacitance		1.1	1.8	pF
C_0/C_1	Capacitance ratio		430	600	
DL	Drive level			1	µW
$\Delta f/f_O$	Aging (first year at 25°C)		1		ppm

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance			7	pF	Output voltage = 0V
C_{IN}	Input capacitance			5	pF	Input voltage = 0V

Note: These parameters are sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 4 and 5

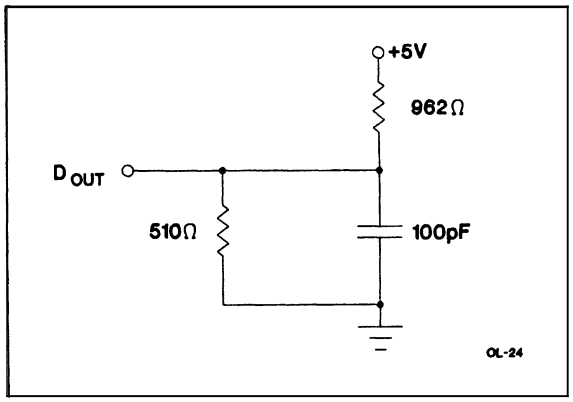


Figure 4. Output Load A

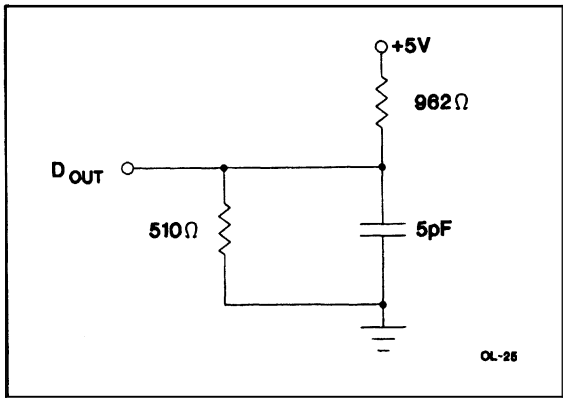


Figure 5. Output Load B

Read Cycle (TA = TOPR, VCCmin ≤ VCC ≤ VCCmax)

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RC}	Read cycle time	70		ns	
t_{AA}	Address access time		70	ns	Output load A
t_{ACS}	Chip select access time		70	ns	Output load A
t_{OE}	Output enable to output valid		35	ns	Output load A
t_{CLZ}	Chip select to output in low Z	5		ns	Output load B
t_{OLZ}	Output enable to output in low Z	0		ns	Output load B
t_{CHZ}	Chip deselect to output in high Z	0	25	ns	Output load B
t_{OHZ}	Output disable to output in high Z	0	25	ns	Output load B
t_{OH}	Output hold from address change	10		ns	Output load A

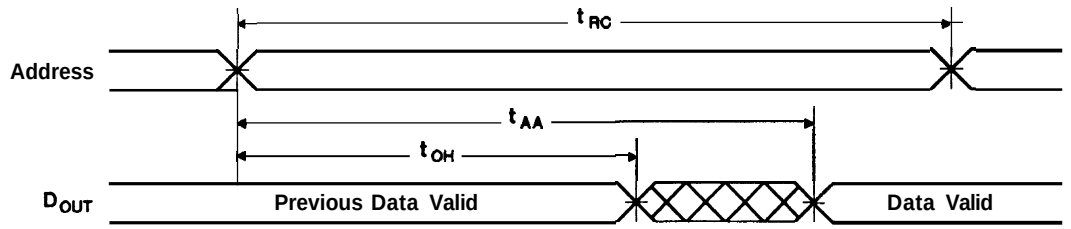
Write Cycle (TA = TOPR, VCCmin ≤ VCC ≤ VCCmax)

Symbol	Parameter	Min.	Max.	Unit	Conditions
twc	Write cycle time	70	-	ns	
t_{CW}	Chip select to end of write	65	-	ns	(1)
t_{AW}	Address valid to end of write	65	-	ns	(1)
t_{AS}	Addrees setup time	0	-	ns	Measured from address valid to beginning of write. (2)
t_{WP}	Write pulse width	55	-	ns	Measured from beginning of write to end of write. (1)
t_{WR1}	Write recovery time (write cycle 1)	5	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
t_{WR2}	Write recovery time (write cycle 2)	15	-	ns	Measured from $\overline{CS}$ going high to end of write cycle. (3)
t_{DW}	Data valid to end of write	30	-	ns	Measured to first low-to-high transition of either $\overline{CS}$ or $\overline{WE}$.
t_{DH1}	Data hold time (write cycle 1)	0		ns	Measured from $\overline{WE}$ going high to end of write cycle. (4)
t_{DH2}	Data hold time (write cycle 2)	10	-	ns	Measured from $\overline{CS}$ going high to end of write cycle. (4)
t_{WZ}	Write enabled to output in high Z	0	25	ns	I/O pins are in output state. (5)
tow	Output active from end of write	0	-	ns	I/O pins are in output state. (5)

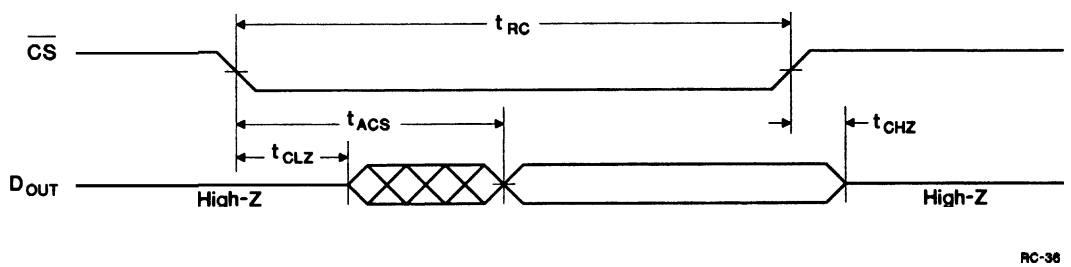
Notes:

1. A write ends at the earlier transition of $\overline{CS}$ going high and $\overline{WE}$ going high.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CS}$ going low and $\overline{WE}$ going low.
3. Either t_{WR1} or t_{WR2} must be met.
4. Either t_{DH1} or t_{DH2} must be met.
5. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

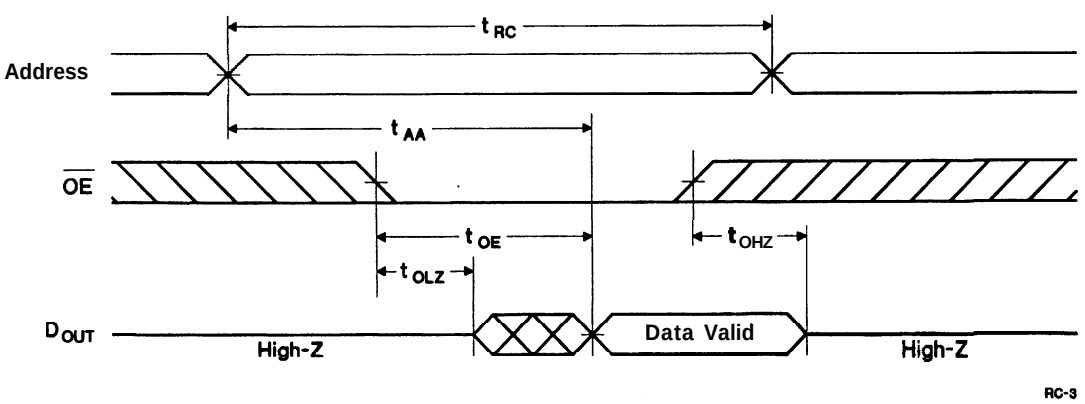
Read Cycle No. 1 (Address Access) [1,2]



Read Cycle No. 2 ($\overline{CS}$ Access) [1,3,4]

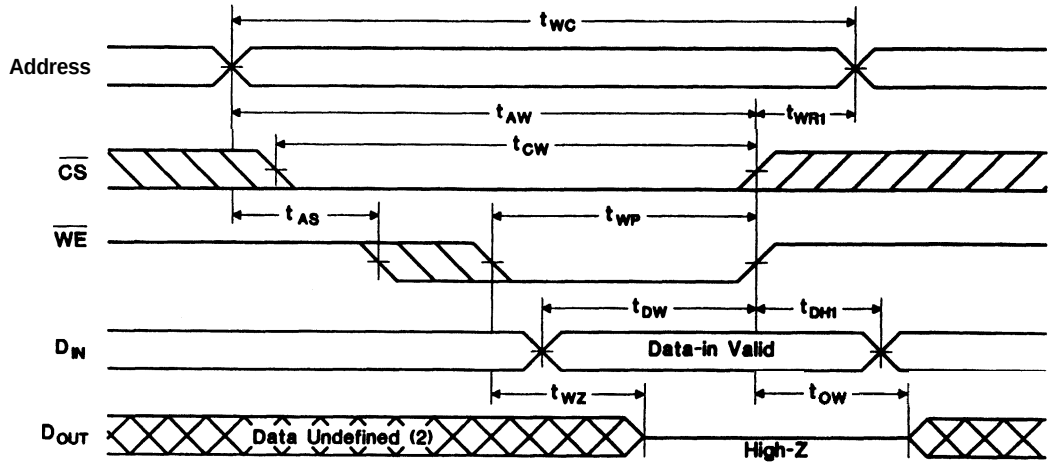


Read Cycle No. 3 ($\overline{OE}$ Access) [1,5]

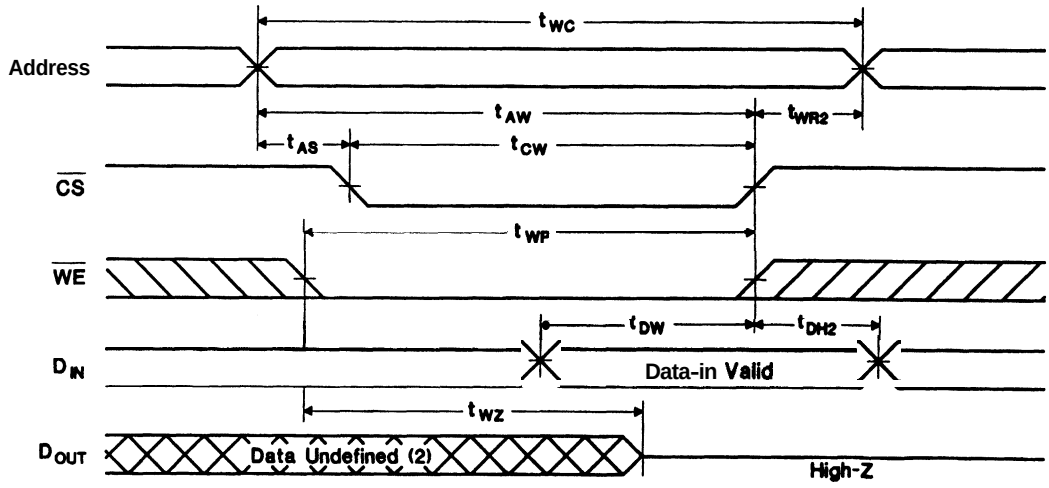


Notes:
1. $\overline{WE}$ is held high for a read cycle.
2. Device is continuously selected: $\overline{CS}$ = $\overline{OE}$ = *Vn*.
3. Address is valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Device is continuously selected: $\overline{CS}$ = V_{IL}.

Write Cycle No. 1 ($\overline{WE}$-Controlled) 1,2,3



Write Cycle No. 2 ($\overline{CS}$-Controlled) 1,2,3,4,5



Notes:
1. $\overline{CS}$ or $\overline{WE}$ must be high during address transition.
2. Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
3. If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.
4. Either t_{WR1} or t_{WR2} must be met.
5. Either t_{DH1} or t_{DH2} must be met.

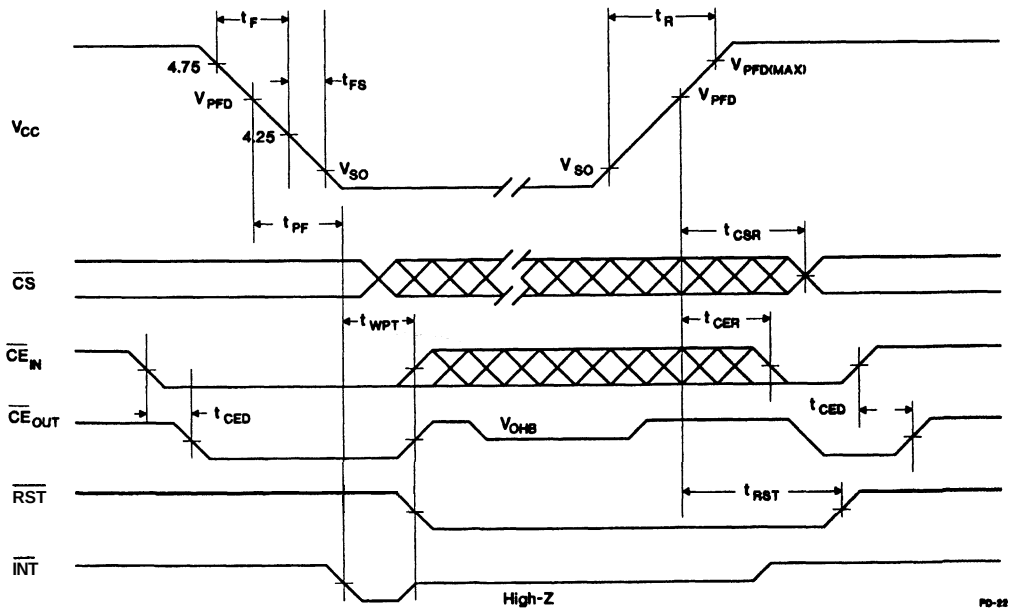
Power-Down/Power-Up Timing (TA = TOPR)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_F	V_{CC} slew from 4.75 to 4.25V	300	-	-	µs	
t_{FS}	V_{CC} slew from 4.25 to V_{SO}	10	-	-	µs	
t_R	V_{CC} slew from V_{SO} to $V_{PFD(MAX)}$	100	-	-	µs	
t_{PF}	Interrupt delay from V_{PFD}	6	-	24	µs	
t_{WPT}	Write-protect time for external RAM	90	100	125	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected and $\overline{RST}$ activated.
t_{CSR}	$\overline{CS}$ at V_{IH} after power-up	100	200	300	ms	Internal write-protection period after V_{CC} passes V_{PFD} on power-up.
t_{RST}	V_{PFD} to $\overline{RST}$ inactive	t_{CSR}	-	t_{CSR}	ms	Reset active time-out period
t_{CER}	Chip enable recovery time	t_{CSR}		t_{CSR}	ms	Time during which external SRAM is write-protected after V_{CC} passes V_{PFD} on power-up.
t_{CED}	Chip enable propagation delay to external SRAM		9	12	ns	Output load A

Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

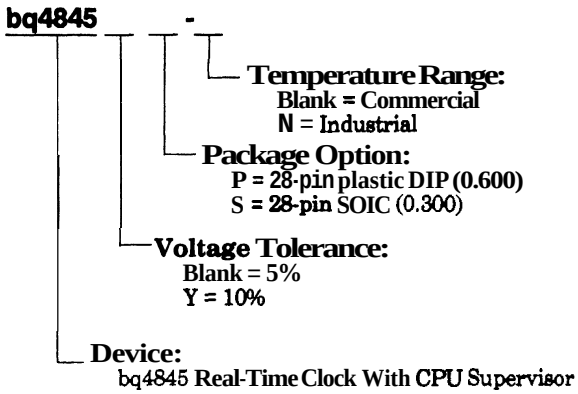
Note: Typical values indicate operation at TA = 25°C.

Power-Down/Power-Up Timing



Notes: PWRIE set to "1" to enable power fail interrupt.
$\overline{RST}$ and $\overline{INT}$ are open drain and require an external pull-up resistor.

Ordering Information



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Notes

bq4847/bq4847Y

RTC Module With CPU Supervisor

Features

- Real-Time Clock counts seconds through years in BCD format
- Integrated battery and crystal
- On-chip battery-backup switchover circuit with nonvolatile control for an external SRAM
- 130mAh battery capacity
- ±1 minute per month clock accuracy
- Less than 500nA of clock operation current in backup mode
- Microprocessor reset valid to vcc = V_{SS}
- Independent watchdog timer with a programmable time-out period
- Power-fail interrupt warning
- Programmable clock alarm interrupt active in battery-backup mode
- Programmable periodic interrupt
- Battery-low warning

General Description

The bq4847 Real-Time Clock Module is a low-power microprocessor peripheral that integrates a time-of-day clock, a 100-year calendar, a CPU supervisor, a battery, and a crystal in a 28-pin DIP module. The part is ideal for fax machines, copiers, industrial control systems, point-of-eale terminals, data loggers, and computers.

The bq4847 contains an internal battery and crystal. Through the use of the conditional chip enable output ($\overline{CE}_{OUT}$) and battery voltage output (V_{OUT}) pins, the bq4847 can write-protect and make nonvolatile an external SRAM. The backup cell powers the real-time clock and maintains SRAM information in the absence of system voltage.

The bq4847 contains a temperature-compensated reference and comparator circuit that monitors the status of its voltage supply. When an out-of-tolerance condition is detected, the bq4847 generates an interrupt warning and subsequently a microprocessor reset. The reset stays active for 200ms after V_{CC} rises within tolerance to allow for power supply and processor stabilization.

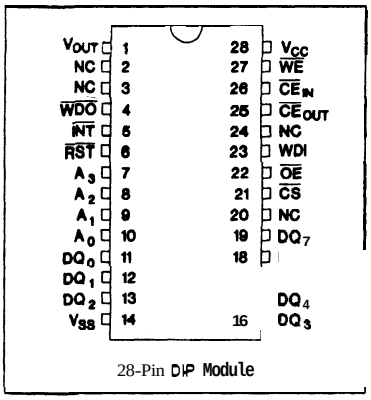
The bq4847 also has a built-in watchdog timer to monitor processor operation. If the microprocessor does not toggle the watchdog input (WDI) within the programmed time-out, the bq4847 asserts $\overline{WDO}$ and $\overline{RST}$. WDI unconnected disables the watchdog timer.

The bq4847 can generate other interrupts based on a clock alarm condition or a periodic setting. The alarm interrupt can be set to occur from once per second to once per month. The alarm can be made active in the battery-backup mode to serve as a system wake-up call. For interrupts at a rate beyond once per second, the periodic interrupt can be programmed with periods of 30.5µs to 500ms.

Caution:

Take care to avoid inadvertent discharge through V_{OUT} and $\overline{CE}_{OUT}$ after battery isolation has been broken.

Pin Connections



28-Pin DIP Module

Pin Names

A_0-A_3	Clock/Control address inputs	NC	No connect
DQ_0-DQ_7	Data inputs/outputs	V_{OUT}	Back-up battery output
$\overline{WE}$	Write enable	$\overline{INT}$	Interrupt output
$\overline{OE}$	Output enable	$\overline{RST}$	Microprocessor reset
$\overline{CS}$	Chip select input	WDI	Watchdog input
	External RAM chip enable	$\overline{WDO}$	Watchdog output
$\overline{CE}_{OUT}$	Conditional RAM chip enable	V_{CC}	+SV supply
		V_{SS}	Ground

Functional Description

Figure 1 is a block diagram of the bq4847. The bq4847 is functionally equivalent to the bq4845 except that the battery (20, 24) and crystal (2, 3) pins are not accessible. The pins are connected internally to a coin cell and quartz crystal. The coin cell provides 130mAh of capacity. It is internally isolated from V_{OUT} and $\overline{CE}_{OUT}$ until the initial application of V_{CC}. Once V_{CC} rises above V_{PFD}, this isolation is broken, and the backup cell provides power to V_{OUT} and $\overline{CE}_{OUT}$ for the external SRAM. The real-time clock keeps time to within one minute per month at room temperature. For a complete description of features, operating conditions, electrical characteristics, bus timing, and pin descriptions, see the bq4845 data sheet. Valid part types for ordering are bq4847MT (5%) and bq4847YMT (10%).

Figure 2 illustrates the address map for the bq4847. Table 1 is a map of the bq4847 registers, and Table 2 describes the register bits.

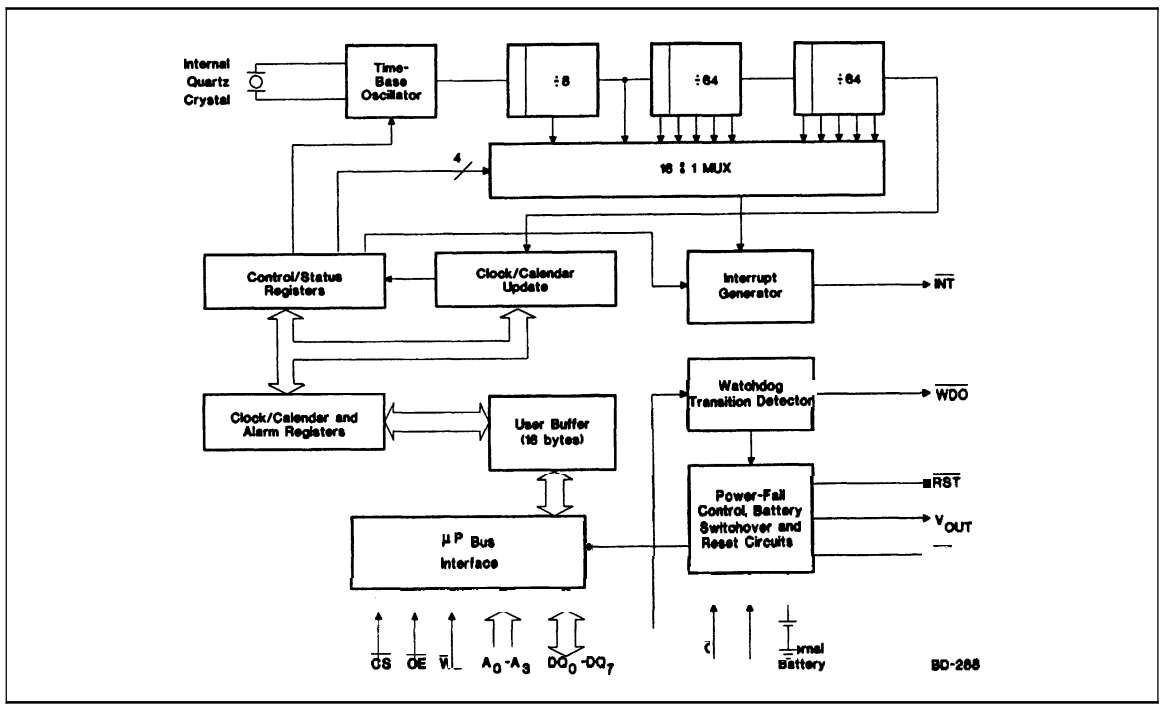
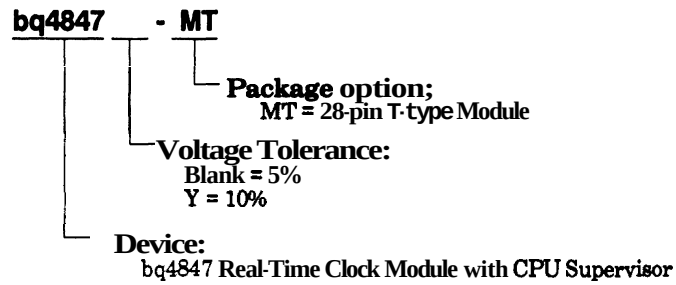


Figure 1. Block Diagram

Truth Table

V_{CC}	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{CE}_{OUT}$	V_{OUT}	Mode	DQ	Power
< V_{CC} (max.)	V_{IH}	X	X	$\overline{CE}_{IN}$	V_{OUT1}	Deselect	High Z	Standby
> V_{CC} (min.)	V_{IL}	X	V_{IL}	$\overline{CE}_{IN}$	V_{OUT1}	Write	D_{IN}	Active
	V_{IL}	V_{IL}	V_{IH}	$\overline{CE}_{IN}$	V_{OUT1}	Read	D_{OUT}	Active
	V_{IL}	V_{IH}	V_{IH}	$\overline{CE}_{IN}$	V_{OUT1}	Read	High Z	Active
< V_{PFD} (min.) > V_{SO}	X	X	X	V_{OH}	V_{OUT1}	Deselect	High Z	CMOS standby
≤ V_{SO}	X	X	X	V_{OHB}	V_{OUT2}	Deselect	High Z	Battery-backup mode

Ordering Information



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Notes

BENCHMARQ

bq4850Y

RTC Module With 512Kx8 NVSRAM

Features

- Integrated SRAM, real-time clock, crystal, power-fail control circuit, and battery
- Real-Time Clock counts seconds through years in BCD format
- RAM-like clock access
- Pin-compatible with industry-standard 512K x 8 SRAMs
- Unlimited write cycles
- 10-year minimum data retention and clock operation in the absence of power
- Automatic power-fail chip deselect and write-protection
- Software clock calibration for greater than ±1 minute per month accuracy

General Description

The bq4850Y RTC Module is a non-volatile 4,194,304-bit SRAM organized as 524,288 words by 8 bits with an integral acceeeible real-time clock.

The device combines an internal lithium battery, quartz crystal, clock and power-fail chip, and a full CMOS SRAM in a plastic 32-pin DIP module. The RTC Module directly replaces industry-standard SRAMs and also fits into many EPROM and EEPROM sockets without any requirement for special write timing or limitations on the number of write cycles.

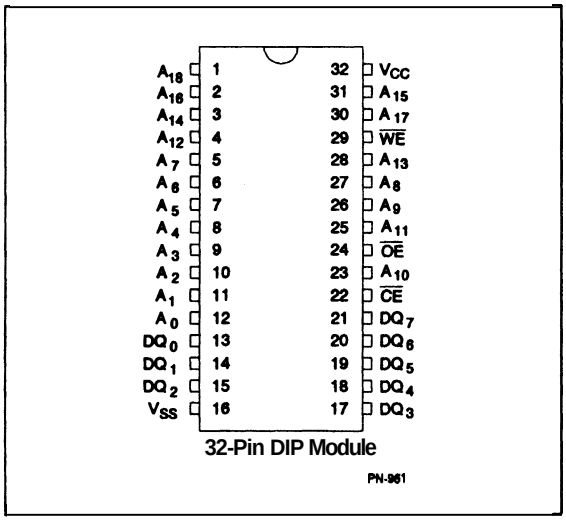
Registers for the real-time clock, alarm and other special functions are located in registers 7FFF8h-7FFFFh of the memory array.

The clock and alarm registers are dual-port read/write SRAM locations that are updated once per second by a clock control circuit from the internal clock counters. The dual-port registers allow clock updates to occur without interrupting normal access to the rest of the SRAM array.

The bq4850Y also contains a power-fail-detect circuit. The circuit deselects the device whenever V_{CC} falls below tolerance, providing a high degree of data security. The battery is electrically isolated when shipped from the factory to provide maximum battery capacity. The battery remains disconnected until the first application of V_{CC}.

5

Pin Connections



32-Pin DIP Module

PN-961

Pin Names

A_0-A_{18}	Address input
$\overline{CE}$	Chip enable
WE	Write enable
$\overline{OE}$	Output enable
DQ_0-DQ_7	Data in/data out
V_{CC}	+5 volts
V_{SS}	Ground

Functional Description

Figure 1 is a block diagram of the bq4850Y. The following sections describe the bq4850Y functional operation, including memory and clock interface, and data-retention modes.

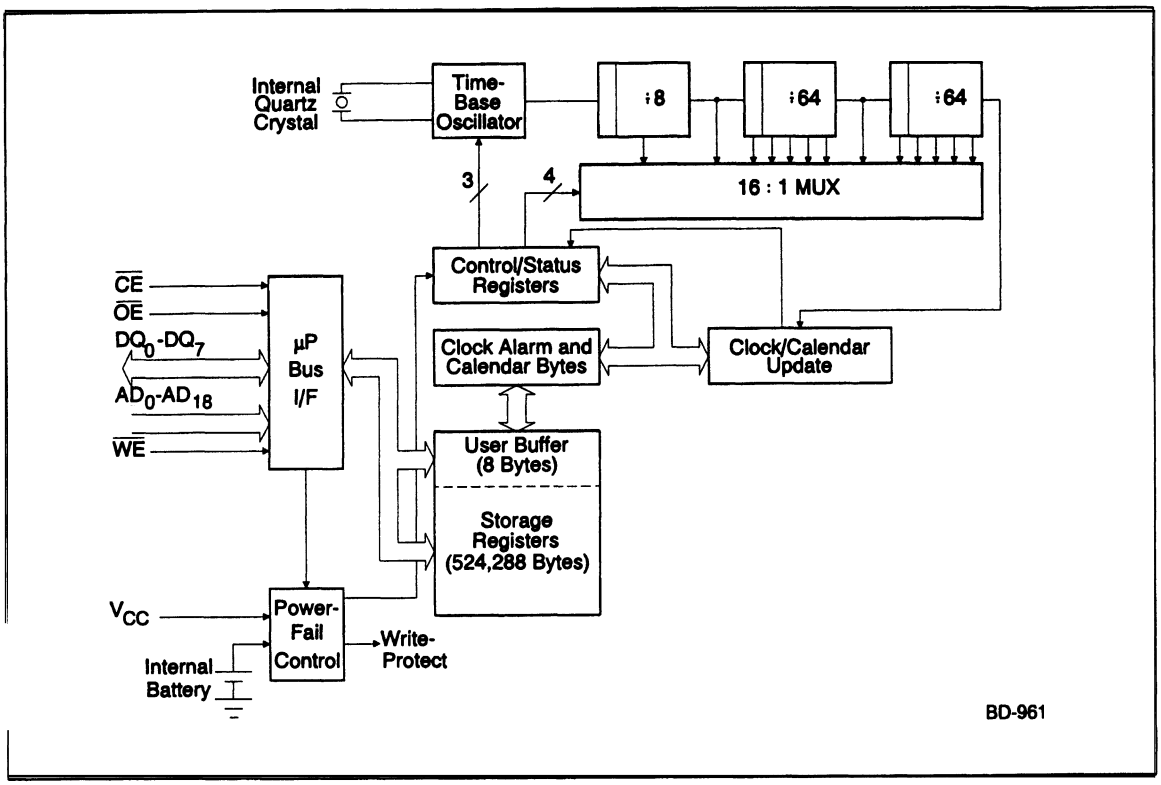


Figure 1. Block Diagram

Truth Table

Vcc	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	DQ	Power
< Vcc (max.)	V_{IH}	X	X	Deselect	High Z	Standby
> Vcc (min.)	V_{IL}	X	V_{IL}	Write	D_{IN}	Active
	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
	V_{IL}	V_{IH}	V_{IH}	Read	High Z	Active
< V_{PFD} (min.) > V_{SO}	X	X	X	Deselect	High Z	CMOS standby
≤ V_{SO}	X	X	X	Deselect	High Z	Battery-backup mode

Address Map

Figure 2 illustrates the address map for the bq4850Y. Table 1 is a map of the bq4850Y registers.

The bq4850Y provides 8 bytes of clock and control status registers and 524,288 bytes of storage RAM.

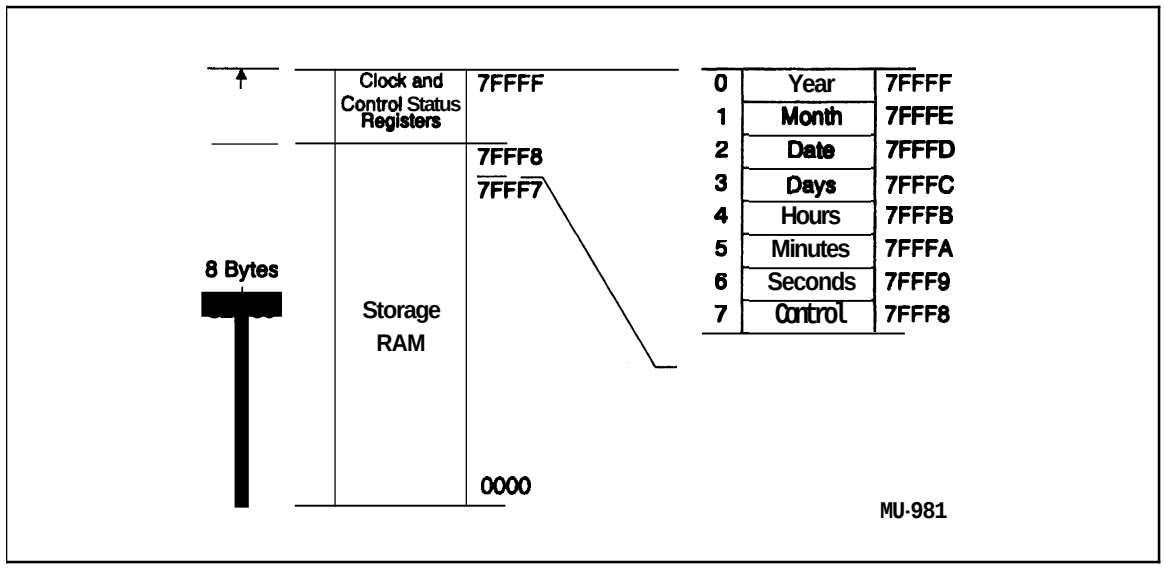


Figure 2. Address Map

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Table 1. bq4850Y Clock and Control Register Map

Address	D7	D6	D5	D4	D3	D2	D1	D0	Range (h)	Register
7FFFF	10 Years				Year				00–99	Year
7FFFE	X	X	X	10 Month	Month				01–12	Month
7FFFD	X	X	10 Date		Date				01–31	Date
7FFFC	X	FTE	X	X	X	Day			01–07	Days
7FFFB	X	X	10 Hours		Hours				00-23	Hours
7FFFA	X	10 Minutes			Minutes				00–59	Minutes
7FFF9	OSC	10 Seconds			Seconds				00–59	Seconds
7FFF8	W	R	S	Calibration					00–31	Control

Note: X = Unused bits; can be written and read.
Clock/Calendar data in 24-hour BCD format.
OSC = 1 stops the clock oscillator.

Memory Interface

Read Mode

The bq4850Y is in read mode whenever $\overline{OE}$ (output enable) is low and $\overline{CE}$ (chip enable) is low. The device architecture allows ripple-through access of data from eight of 4,194,304 locations in the static storage array. Thus, the unique address specified by the 19 address inputs defines which one of the 524,288 bytes of data is to be accessed. Valid data is available at the data I/O pins within t_{AA} (address access time) after the last address input signal is stable, providing that the $\overline{CE}$ and $\overline{OE}$ (output enable) access times are also satisfied. If the $\overline{CE}$ and OE access times are not met, valid data is available after the latter of chip enable access time (t_{ACE}) or output enable access time (t_{OE}).

$\overline{CE}$ and $\overline{OE}$ control the state of the eight three-state data I/O signals. If the outputs are activated before t_{AA}, the data lines are driven to an indeterminate state until t_{AA}. If the address inputs are changed while $\overline{CE}$ and $\overline{OE}$ remain low, output data remains valid for t_{OH} (output data hold time), but goes indeterminate until the next address access.

Write Mode

The bq4850Y is in write mode whenever $\overline{WE}$ and $\overline{CE}$ are active. The start of a write is referenced from the latter-occurring falling edge of $\overline{WE}$ or $\overline{CE}$. A write is terminated by the earlier rising edge of $\overline{WE}$ or $\overline{CE}$. The addresses must be held valid throughout the cycle. $\overline{CE}$ or $\overline{WE}$ must return high for a minimum of t_{WR2} from $\overline{CE}$ or t_{WR1} from $\overline{WE}$ prior to the initiation of another read or write cycle.

Data-in must be valid t_{DW} prior to the end of write and remain valid for t_{DH1} or t_{DH2} afterward. $\overline{OE}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{CE}$ and $\overline{OE}$, a low on $\overline{WE}$ disables the outputs t_{WZ} after $\overline{WE}$ falls.

Data-Retention Mode

With valid V_{CC} applied, the bq4850Y operates as a conventional static RAM. Should the supply voltage decay, the RAM automatically power-fail deselects, write-protecting itself t_{WPT} after V_{CC} falls below V_{PFD}. All outputs become high impedance, and all inputa are treated as 'don't care."

If power-fail detection occurs during a valid access, the memory cycle continues to completion. If the memory cycle fails to terminate within time t_{WPT}, write-protection takes place. When V_{CC} drops below V_{SO}, the control circuit switches power to the internal energy source, which preserves data.

The internal coin cell maintains data in the bq4850Y after the initial application of V_{CC} for an accumulated period of at least 10 years when V_{CC} is leas than V_{SO}. As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. Write-protection continues for t_{CER} after V_{CC} reaches V_{PFD} to allow for processor stabilization. After t_{CER}, normal RAM operation can resume.

Clock Interface

Reading the Clock

The interface to the clock and control registers of the bq4850Y is the same as that for the general-purpose storage memory. Once every second, the user-accessible clock/calendar locations are updated simultaneously from the internal real time counters. To prevent reading data in transition, updates to the bq4850Y clock registers should be halted. Updating is halted by setting the read bit D6 of the control register to 1. As long as the read bit is 1, updates to user-accessible clock locations are inhibited. Once the frozen clock information is retrieved by reading the appropriate clock memory locations, the read bit should be reset to 0 in order to allow updates to occur from the internal counters. Because the internal counters are not halted by setting the read bit, reading the clock locations has no effect on clock accuracy. Once the read bit is reset to 0, within one second the internal registers update the user-accessible registers with the correct time. A halt command issued during a clock update allows the update to occur before freezing the data.

Setting the Clock

Bit D7 of the control register is the write bit. Like the read bit, the write bit when set to a 1 halts updates to the clock/calendar memory locations. Once frozen, the locations can be written with the desired information in 24-hour BCD format. Resetting the write bit to 0 causes the written values to be transferred to the internal clock counters and allows updates to the user-accessible registers to resume within one second. Use the write bit, D7, only when updating the time registers (7FFFF-7FFF9).

Stopping and Starting the Clock Oscillator

The OSC bit in the seconds register turns the clock on or off. If the bq4850Y is to spend a significant period of time in storage, the clock oscillator can be turned off to preserve battery capacity. OSC set to 1 stops the clock oscillator. When OSC is reset to 0, the clock oscillator is turned on and clock updates to user-accessible memory locations occur within one second.

The OSC bit is set to 1 when shipped from the Benchmarq factory.

Calibrating the Clock

The bq4850Y real-time clock is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. The quartz crystal is contained within the bq4850Y package along with the battery. The clock accuracy of the bq4850Y module is tested to be within 20ppm or about 1 minute per month at 25°C. The oscillation rates of crystals change with temperature as Figure 3 shows. To compensate for the frequency shift, the bq4850Y offers onboard software clock calibration. The user can adjust the calibration based on the typical operating temperature of individual applications.

The software calibration bits are located in the control register. Bits D0–D4 control the magnitude of correction, and bit D5 the direction (positive or negative) of correction. Assuming that the oscillator is running at exactly 32,786 Hz, each calibration step of D0–D4 adjusts the clock rate by +4.068 ppm (+10.7 seconds per month) or -2.034 ppm (-6.35 seconds per month) depending on the value of the sign bit D5. When the sign bit is 1, positive adjustment occurs; a 0 activates negative adjustment. The total range of clock calibration is +5.5 or -2.75 minutes per month.

Two methods can be used to ascertain how much calibration a given bq4850Y may require in a system. The first involves simply setting the clock, letting it run for a month, and then comparing the time to an accurate known reference like WWV radio broadcasts. Based on the variation to the standard, the end user can adjust the clock to match the system's environment even after the product is packaged in a non-serviceable enclosure. The only requirement is a utility that allows the end user to access the calibration bits in the control register.

The second approach uses a bq4850Y test mode. When the frequency test mode enable bit FTE in the days register is set to a 1, and the oscillator is running at exactly 32,768 Hz, the LSB of the seconds register toggles at 512 Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.01024 Hz indicates a (1E6*0.01024)/512 or +20 ppm oscillator frequency error, requiring ten steps of negative calibration (10*-2.034 or -20.34) or 001010 to be loaded into the calibration byte for correction. To read the test frequency, the bq4850Y must be selected and held in an extended read of the seconds register, location 7FFF9, without having the read bit set. The frequency appears on DQ0. The FTE bit must be set using the write bit control. The FTE bit must be reset to 0 for normal clock operation to resume.

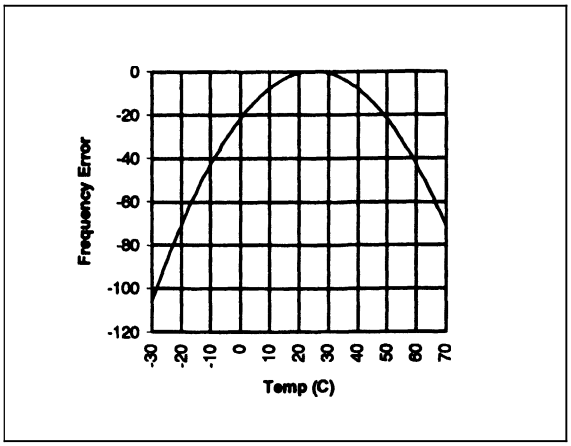

Figure 3. Frequency Error

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Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Condition,
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	
T_{STG}	Storage temperature (V_{CC} off; oscillator off)	-40 to +70	°C	
T_{BIAS}	Temperature under bias	-10 to +70	°C	
T_{SOLDER}	Soldering temperature	+260	°C	For 10 seconds

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C.

DC Electrical Characteristics (T_A = TOPR, $V_{CCmin} \le V_{CC} \le V_{CCmax}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current			±1	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current			±1	µA	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
V_{OH}	Output high voltage	2.4			V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage			0.4	V	I_{OL} = 2.1 mA
I_{SB1}	Standby supply current		3	5	mA	$\overline{CE} = V_{IH}$
I_{SB2}	Standby supply current		0.1	1	mA	$\overline{CE} \ge V_{CC}$ - 0.2V, 0V 5 V_{IN} 5 0.2V, or $V_{IN} \ge$ Vcc - 0.2V
I_{CC}	Operating supply current			90	mA	Min. cycle, duty = 100%, $\overline{CE} = V_{IL}$, $I_{I/O}$ = 0mA
V_{PFD}	Power-fail-detect voltage	4.30	4.37	4.50	V	
V_{SO}	Supply switch-over voltage		3		V	

Notes: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.

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Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition8
$C_{I/O}$	Input/output capacitance			10	pF	Output voltage = 0V
C_{IN}	Input capacitance			10	pF	Input voltage = 0V

Note: These parameters are sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 4 and 5

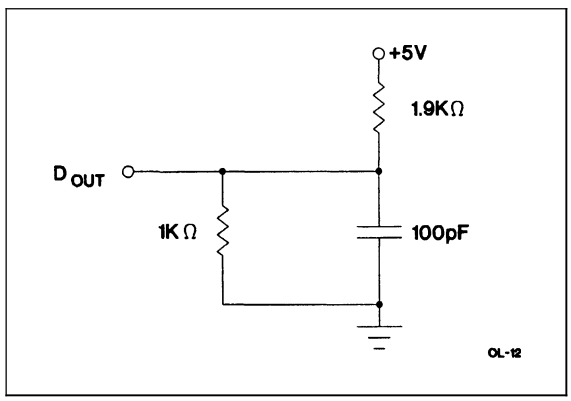


Figure 4. Output Load A

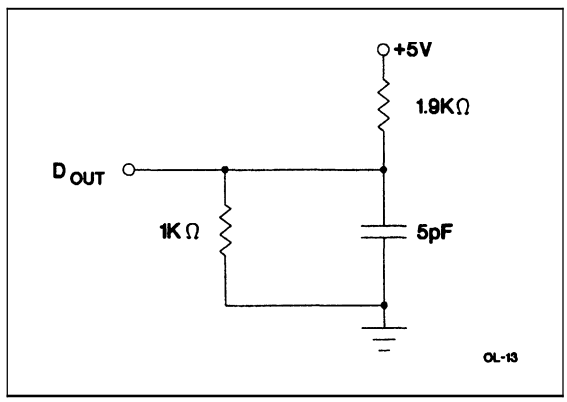
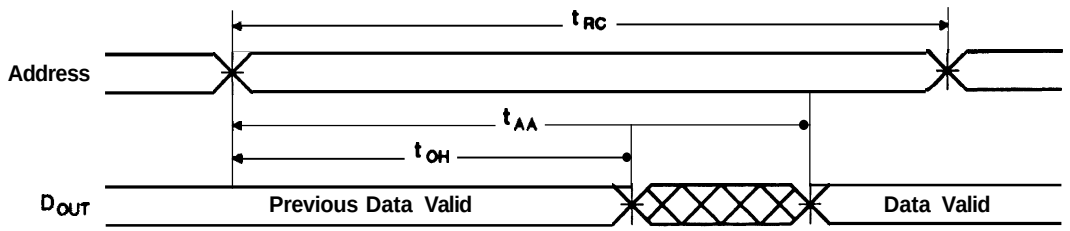


Figure 5. Output Load B

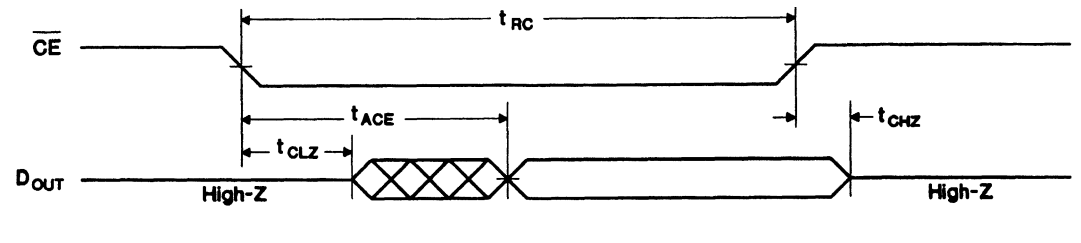
Read Cycle (TA = TOPR, VCCmin ≤ VCC ≤ VCCmax)

Symbol	Parameter	-85 Min.	-85 Max.	Unit	Conditions
t_{RC}	Read cycle time	85		ns	
t_{AA}	Address access time		85	ns	Output load A
t_{ACE}	Chip enable access time		85	ns	Output load A
t_{OE}	Output enable to output valid		45	ns	Output load A
t_{CLZ}	Chip enable to output in low Z	5		ns	Output load B
t_{OLZ}	Output enable to output in low Z	0		ns	Output load B
t_{CHZ}	Chip disable to output in high Z	0	35	ns	Output load B
t_{OHZ}	Output disable to output in high Z	0	25	ns	Output load B
t_{OW}	Output hold from address change	10	-	ns	Output load A

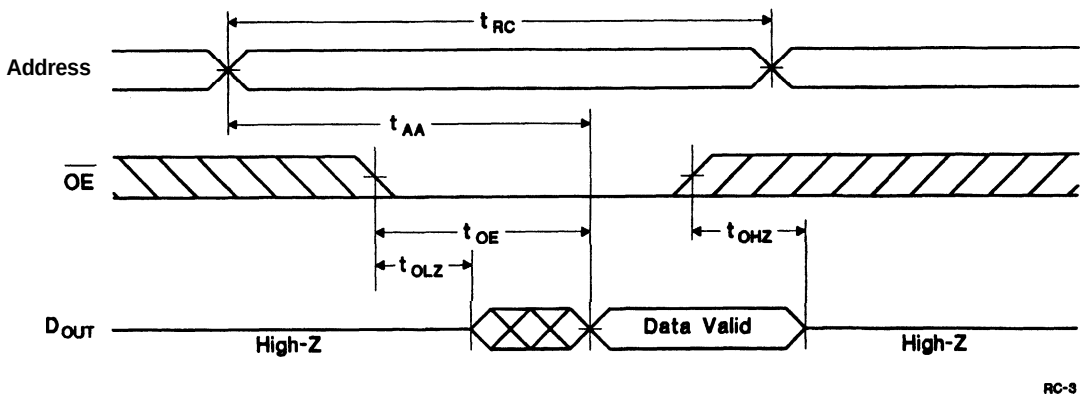
Read Cycle No. 1 (Address Access) [1,2]



Read Cycle No. 2 ($\overline{CE}$ Access) [1,3,4]



Read Cycle No. 3 ($\overline{OE}$ Access) [1,5]



Notes:
1. $\overline{WE}$ is held high for a read cycle.
2. Device is continuously selected: $\overline{CE}$ = $\overline{OE}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Device is continuously selected: $\overline{CE}$ = V_{IL}.

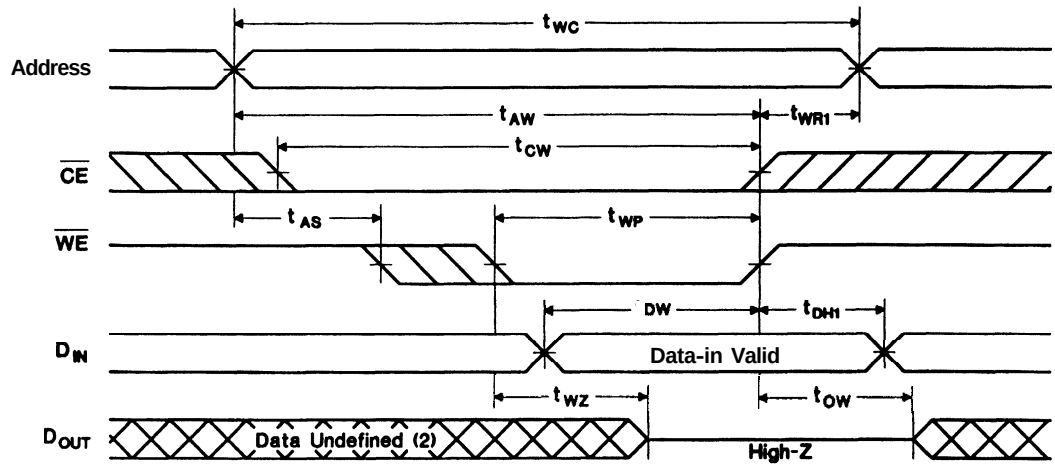
Write Cycle ($T_A = T_{OPR}$, $V_{CCmin} \le V_{CC} \le V_{CCmax}$)

Symbol	Parameter	–85 Min.	–85 Max.	Units	Conditions/Notes
t_{WC}	Write cycle time	85		ns	
t_{CW}	Chip enable to end of write	75		ns	(1)
t_{AW}	Address valid to end of write	75		ns	(1)
t_{AS}	Address setup time	0		ns	Measured from address valid to beginning of write. (2)
t_{WP}	Write pulse width	65		ns	Measured from beginning of write to end of write. (1)
t_{WR1}	Write recovery time (write cycle 1)	5	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
t_{WR2}	Write recovery time (write cycle 2)	15		ns	Measured from $\overline{CE}$ going high to end of write cycle. (3)
t_{DW}	Data valid to end of write	35		ns	Measured to first low-to-high transition of either $\overline{CE}$ or $\overline{WE}$.
t_{DH1}	Data hold time (write cycle 1)	0		ns	Measured from $\overline{WE}$ going high to end of write cycle. (4)
t_{DH2}	Data hold time (write cycle 2)	10		ns	Measured from $\overline{CE}$ going high to end of write cycle. (4)
t_{WZ}	Write enabled to output in high Z	0	30	ns	I/O pins are in output state. (5)
tow	Output active from end of write	0		ns	I/O pins are in output state. (5)

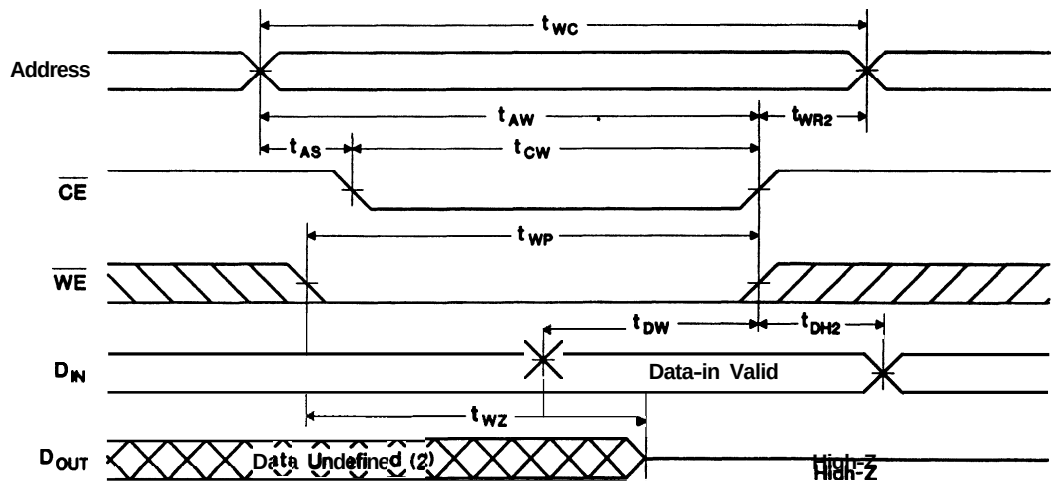
Notes:

1. A write ends at the earlier transition of $\overline{CE}$ going high and $\overline{WE}$ going high.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CE}$ going low and $\overline{WE}$ going low.
3. Either t_{WR1} or t_{WR2} must be met.
4. Either t_{DH1} or t_{DH2} must be met.
5. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

Write Cycle No. 1 ($\overline{WE}$-Controlled) 1,2,3



Write Cycle No. 2 ($\overline{CE}$-Controlled) 1,2,3,4,5



Notes:
1. $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
2. Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
3. If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.
4. Either t_{WR1} or t_{WR2} must be met.
5. Either t_{DH1} or t_{DH2} must be met.

Notes

BENCHMARQ

bq4852Y

RTC Module With 512Kx8 NVSRAM

Features

- Integrated SRAM, real-time clock, CPU supervisor, crystal, power-fail control circuit, and battery
- Real-Time Clock counts hundredths of seconds through years in BCD format
- RAM-like clock access
- Compatible with industry-standard 512K x 8 SRAMs
- Unlimited write cycles
- 10-year minimum data retention and clock operation in the absence of power
- Automatic power-fail chip deselect and write-protection
- Watchdog timer, power-on reset, alarm/periodic interrupt, power-fail and battery-low warning
- Software clock calibration for greater than ±1 minute per month accuracy

General Description

The bq4852Y RTC Module is a non-volatile 4,194,304-bit SRAM organized as 524,288 words by 8 bits with an integral accessible real-time clock and CPU supervisor. The CPU supervisor provides a programmable watchdog timer and a microprocessor reset. Other features include an alarm, power-fail, and periodic interrupt and a battery low warning.

The device combines an internal lithium battery, quartz crystal, clock and power-fail chip, and a full CMOS SRAM in a plastic 36-pin DIP module. The RTC Module directly replaces industry-standard SRAMs and also fits into many EPROM and EEPROM sockets without any requirement for special write timing or limitations on the number of write cycles.

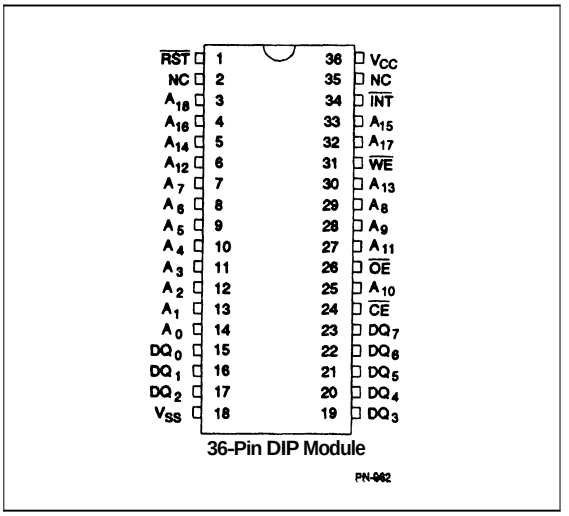
Registers for the real-time clock, alarm and other special functions are located in registers 7FFF0h–7FFFFh of the memory array.

The clock and alarm registers are dual-port read/write SRAM locations that are updated once per second by a clock control circuit from the internal clock counters. The dual-port registers allow clock updates to occur without interrupting normal access to the rest of the SRAM array.

The bq4852Y also contains a power-fail-detect circuit. The circuit deselects the device whenever V_{CC} falls below tolerance, providing a high degree of data security. The battery is electrically isolated when shipped from the factory to provide maximum battery capacity. The battery remains disconnected until the first application of V_{CC}.

5

Pin Connections



36-Pin DIP Module

Pin Names

A_0-A_{18}	Address input
$\overline{CE}$	Chip enable
$\overline{RST}$	Microprocessor reset
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
DQ_0-DQ_7	Data in/data out
$\overline{INT}$	Programmable interrupt
V_{CC}	+5 volts
V_{SS}	Ground

Functional Description

Figure 1 is a block diagram of the bq4852Y. The following sections describe the bq4852Y functional operation, including memory and clock interface, data-retention modes, power-on reset timing, watchdog timer activation, and interrupt generation.

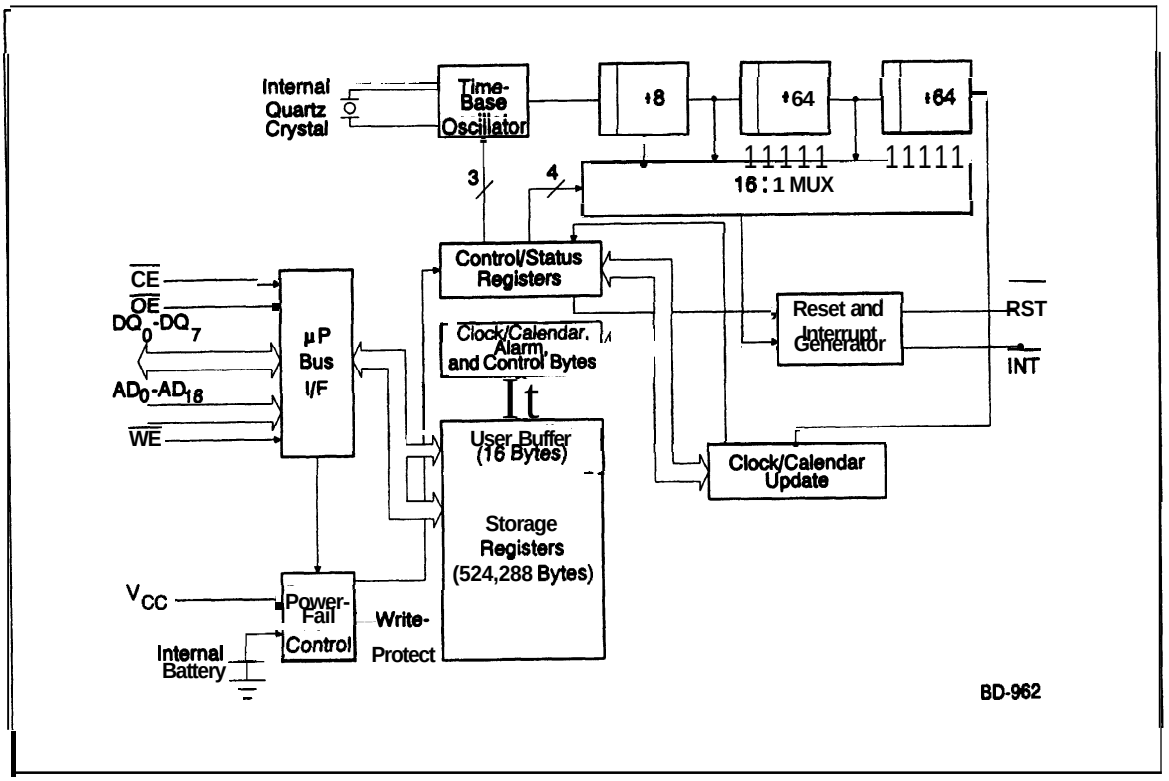


Figure 1. Block Diagram

Truth Table

V_{CC}	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	DQ	Power
< V_{CC} (max.)	V_{IH}	X	X	Deselect	High Z	Standby
	V_{IL}	X	V_{IL}	Write	Din	Active
> V_{CC} (min.)	V_{IL}	V_{IL}	V_{IH}	Read	Dout	Active
	V_{IL}	V_{IH}	V_{IH}	Read	High Z	Active
< V_{PFD} (min.) > V_{SO}	X	X	X	Deselect	High Z	CMOS standby
≤ V_{SO}	X	X	X	Deselect	High Z	Battery-backupmode

Address Map

The bq4852Y provides 16 bytes of clock and control status registers and 524,272 bytes of storage RAM.

Figure 2 illustrates the address map for the bq4852Y. Table 1 is a map of the bq4852Y registers, and Table 2 describes the register bits.

Memory Interface

Read Mode

The bq4852Y is in read mode whenever $\overline{OE}$ (output enable) is low and $\overline{CE}$ (chip enable) is low. The device architecture allows ripple-through access of data from eight of 4,194,304 locations in the static storage array. Thus, the unique address specified by the 19 address inputs defines which one of the 524,288 bytes of data is to be accessed. Valid data is available at the data I/O pins within t_{AA} (address access time) after the last address input signal is stable, providing that the $\overline{CE}$ and $\overline{OE}$ (output enable) access times are also satisfied. If the $\overline{CE}$ and $\overline{OE}$ access times are *not* met, valid data is available after the latter of chip enable access time (t_{ACE}) or output enable access time (t_{OE}).

$\overline{CE}$ and $\overline{OE}$ control the state of the eight three-state data I/O signals. If the outputs are activated before t_{AA}, the data lines are driven to an indeterminate state until t_{AA}. If the address inputs are *changed* while $\overline{CE}$ and $\overline{OE}$ remain low, output data remains valid for t_{OH} (*output* data hold time), but goes indeterminate until the next address access.

Write Mode

The bq4852Y is in write mode whenever $\overline{WE}$ and $\overline{CE}$ are active. The start of a write is referenced from the latter-occurring falling edge of $\overline{WE}$ or $\overline{CE}$. A write is terminated by the earlier rising edge of $\overline{WE}$ or $\overline{CE}$. The addresses must be held valid throughout the cycle. $\overline{CE}$ or $\overline{WE}$ must return high for a minimum of t_{WR2} from $\overline{CE}$ or t_{WR1} from $\overline{WE}$ prior to the initiation of another read or write cycle.

Data-in must be valid t_{DW} prior to the end of write and remain valid for t_{DH1} or t_{DH2} afterward. $\overline{OE}$ should be kept high *during* write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{CE}$ and $\overline{OE}$, a low on $\overline{WE}$ disables the outputs t_{WZ} after $\overline{WE}$ falls.

Data-Retention Mode

With valid V_{CC} applied, the bq4852Y operates as a conventional static RAM. Should the supply voltage decay, the RAM automatically power-fail deselects, write-protecting itself t_{WPT} after V_{CC} falls below V_{PFD}. All outputs become high impedance, and all inputs are treated as 'don't care.'

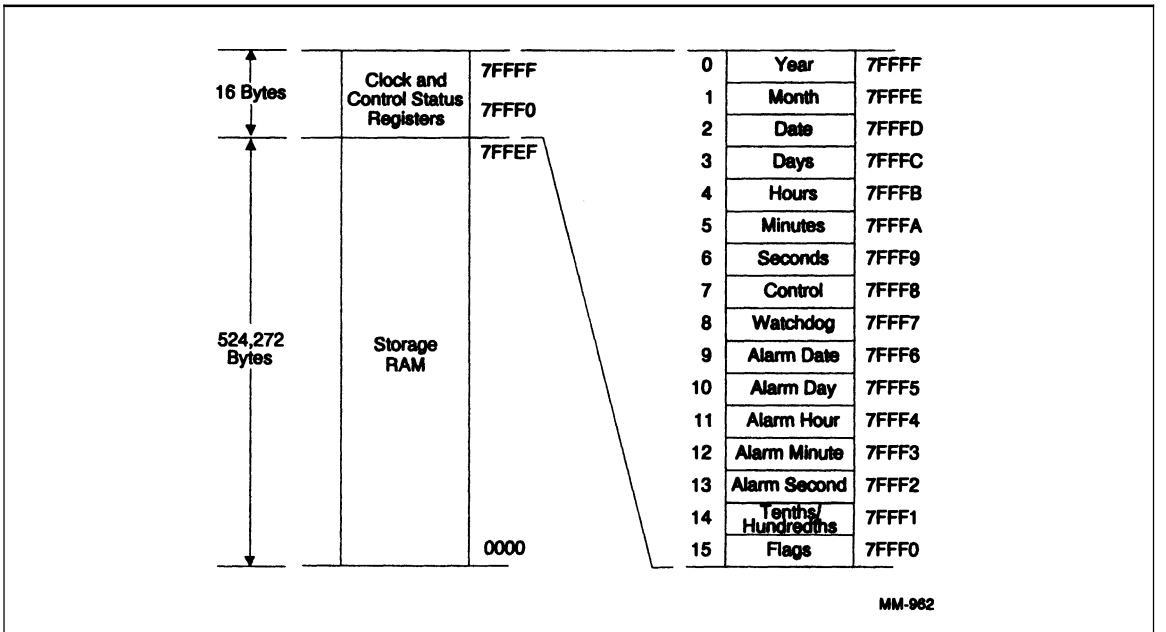


Figure 2. Address Map

If power-fail detection occurs during a valid access, the memory cycle continues to completion If the memory cycle fails to terminate within time t_{WPT}, write-protection takes place. When V_{CC} drops below V_{SO}, the control circuit switches power to the internal energy source, which preserves data.

The internal coin cell maintains data in the bq4852Y after the initial application of V_{CC} for an accumulated period of at least 10 years when V_{CC} is less than V_{SO}. As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. Write-protection continues for t_{CER} after V_{CC} reaches V_{PFD} to allow for processor stabilization. After t_{CER}, normal RAM operation can resume.

Clock Interface

Reading the Clock

The interface to the clock and control registers of the bq4852Y is the same as that for the general-purpose storage memory. Once every second, the user-accessible clock/calendar locations are updated simultaneously from the internal real time countera. To prevent reading data in transition, updates to the bq4852Y clock registers should be halted. Updating is halted by setting the read bit D6 of the control register to 1. As long as the read bit is 1, updates to user-accessible clock locations are inhibited. Once the frozen clock information is retrieved by reading the appropriate clock memory locations, the read bit should be reset to 0 in order to allow updates to occur from the internal counters. Because the internal counteras are not halted by setting the read bit, reading the clock locations has no effect on clock accuracy. Once the read bit is reset to 0, within one second the internal registera update the user-accessible registers with the correct time. A halt command issued during a clock update allows the update to occur before freezing the data.

Setting the Clock

Bit D7 of the control register is the write bit. Like the read bit, the write bit when set to a 1 halts updates to the clock/calendar memory locations. Once frozen, the locations can be written with the desired information in 24-hour BCD format. Resetting the write bit to 0 causes the written values to be transferred to the internal clock counters and allows updates to the user-accessible registera to resume within one second. Use the write bit, D7, only when updating the time registers (7FFFF-7FFF9).

Table 1. bq4842 Clock and Control Register Map

Address	D7	D6	D5	D4	D3	D2	D1	D0	Range (h)	Register
7FFFF	10 Years				Year				00–99	Year
7FFFF	X	X	X	10 Month	Month				01–12	Month
7FFFD	X	X	10 Date		Date				01–31	Date
7FFFC	X	FTE	X	X	X	Day			01–07	Days
7FFFB	X	X	10 Hours		Hours				00–23	Hours
7FFFA	X	10 Minutes			Minutes				00–59	Minutes
7FFF9	OSC	10 Seconds			Seconds				00–59	Seconds
7FFF8	W	R	S	Calibration					00–31	Control
7FFF7	WDS	BM4	BM3	BM2	BM1	BM0	WD1	WD0		Watchdog
7FFF6	AIE	PWRIE	ABE	PIE	RS3	RS2	RS1	RS0		Interrupts
7FFF5	ALM3	X	10-date alarm		Alarm date				01–31	Alarm date
7FFF4	ALM2	X	10-hour alarm		Alarm hours				00–23	Alarm hours
7FFF3	ALM1	Alarm 10 minutes			Alarm minutes				00–59	Alarm minutes
7FFF2	ALM0	Alarm 10 seconds			Alarm seconds				00–59	Alarm seconds
7FFF1	0.1 seconds				0.01 seconds				00–99	0.1/0.01 seconds
7FFF0	WDF	AF	PWRF	BLF	PF	X	X	X		Flags

Note: X = Unused bits; can be written and read.
Clock/Calendar data in 24-hour BCD format.
BLF = 1 for valid battery.
OSC = 1 stops the clock oscillator.
Interrupt enables are cleared on power-up.

Table 2. Clock and Control Register Bits

Bits	Description
ABE	Alarm interrupt enable in battery-backup mode
AF	Alarm interrupt flag
AIE	Alarm interrupt enable
ALM0–ALM3	Alarm repeat rate
BLF	Battery-low flag
BM0–BM4	Watchdog multiplier
FTE	Frequency test mode enable
OSC	Oscillator stop
PF	Periodic interrupt flag
PIE	Periodic interrupt enable
PWRF	Power-fail interrupt flag
PWRIE	Power-fail interrupt enable
R	Read clock enable
RS0–RS3	Periodic interrupt rate
S	Calibration sign
W	Write clock enable
WD0–WD1	Watchdog resolution
WDF	Watchdog tlag
WDS	Watchdog steering

Stopping and Starting the Clock Oscillator

The OSC bit in the seconds register turns the clock on or off. If the bq4852Y is to spend a significant period of time in storage, the clock oecillator can be turned off to preserve battery capacity. OSC set to 1 stops the clock oecillator. When OSC is reset to 0, the clock oscillator is turned on and clock updates to user-accessible memory locations occur within one second.

The OSC bit ie eet to 1 when ehipped from the Benchmarq factory.

Calibrating the Clock

The bq4852Y real-time clock is driven by a quartz controlled oecillator with a nominal frequency of 32,768 Hz. The quartz crystal is contained within the bq4852Y package along with the battery. The clock accuracy of the bq4852Y module is tested to be within 20ppm or about 1 minute per month at 25°C. The oscillation rates of crystals change with temperature as Figure 3 shows. To compensate for the frequency shift, the bq4852Y offers onboard software clock calibration. The user can adjust the calibration land on the typical operating temperature of individual applications.

The software calibration bits are located in the control register. Bits D0–D4 control the magnitude of correction, and bit D5 tbe direction (positive or negative) of correction. Assuming that the oscillator is running at exactly 32,786 Hz, each c a l i i o n step of D0–D4 adjusts the clock rate by +4.068 ppm (+10.7 seconds per month) or -2034 ppm (-5.35 seconds per month) depending on the value of the sign bit DS. When the sign bit is 1, positive adjustment occurs; a 0 activates negative adjustment. The total range of clock calibration is +5.5 or -2.75 minutes per month.

Two methods can be ueed to ascertain how much calibration a given bq4852Y may require in a system. The first involves simply setting the clock, letting it run for a month, and then comparing the time to an accurate known reference like WWV radio broadcasts. Based on the variation to the standard, the end user can adjust the clock to match the system's environment even after the product is packaged in a non-serviceable enclosure. The only requirement is a utility that allows the end user to access the calibration bite in the control register.

The second approach uses a bq4852Y test mode. When the frequency test mode enable bit FTE in the days register is set to a 1, and the oscillator is running at exactly 32,768 Hz, the LSB of the seconds register toggles at 512 Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. F a example, a reading of 512.01024 Hz indicates a (1E6*0.01024)/512 a +20 ppm oscillator frequency error, requiring ten steps of negative calibration (10*-2.034 or -20.34) or 001010 to be loaded into the calibration byte for correction. To mad the test frequency, the bq4852Y must be selected and held in an extended read of the seconds register, location 7FFF9, without having the mad

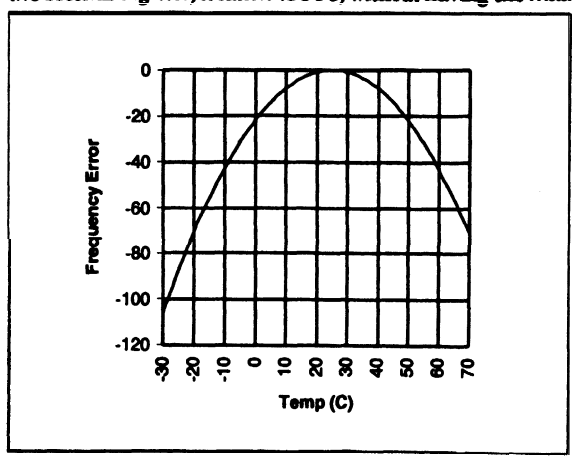


Figure 3. Frequency Error

bit set. The frequency appears on DQ0. The FTE bit must be set using the write bit control. The FTE bit must be reset to 0 for normal clock operation to resume.

Power-On Reset

The bq4852Y provides a power-on reset, which pulls the $\overline{RST}$ pin low on power-down and remains low on power-up for t_{CER} after V_{CC} passes V_{PFD}.

Watchdog Timer

The watchdog circuit monitors the microprocessor's activity. If the processor does not reset the watchdog timer within the pro—mal— time-out period, the circuit asserts the $\overline{INT}$ or RST pin. The watchdog timer is activated by writing the desired time-out period into the eight-bit watchdog register described in Table 3 (device address 7FFF7). The five bits (BM4–BM0) store a binary multiplier, and the two lower-order bita (WD1–WD0) select the resolution, where 00 = 1/16 second, 01 = 1/4 second, 10 = 1 second, and 11 = 4 seconds.

The time-out period is the multiplication of the five-bit multiplier with the two-bit resolution. For example, writing 00011 in BM4–BMO and 10 in WD1–WD0 results in a total time-out setting of 3 x 1 or 3 seconds. A multiplier of zero disables the watchdog circuit. Bit 7 of the watchdog register (WDS) is the watchdog steering bit. When WDS is aet to a 1 and a time-out occurs, the watchdog asserts a reset pulse for t_{CER} on the $\overline{RST}$ pin. During the reset pulse, the watchdog register is cleared to all zeros disabling the watchdog. When WDS is set to a 0, the watchdog asserts the $\overline{INT}$ pin on a time-out. The $\overline{INT}$ pin remains low until the watchdog is reset by the microprocessor or a power failure occurs. Additionally, when the watchdog times out, the watchdog flag bit (WDF) in the flags register, location 7FFF0, is set.

To reset the watchdog timer, the microprocessor must write to the watchdog register. After being reset by a write, the watchdog time-out period starts over. As a precaution, the watchdog circuit is disabled on a power failure. The user must, therefore, set the watchdog at boot-up for activation.

Interrupts

The bq4852Y allows four individually selected interrupt eventa to generate an interrupt request on the $\overline{INT}$ pin. These four interrupt eventa are:

- The watchdog timer interrupt, programmable to occur according to the time-out period and conditions descxibed in the watchdog timer section
- The periodic interrupt, programmable to occur once every 122µs to 500ms.
- The alarm interrupt, programmable to occur once per second to once per month
- The power-fail interrupt, which can be enabled to be asserted when the bq4852Y detects a power failure

The periodic, alarm, and power-fail interrupts are enabled by an individual interrupt-enable bit in register 7FFF6, the interrupts register. When an event occurs, its event flag bit in the flags register, location 7FFF0, is set. If the corresponding event enable bit is also set, then an interrupt request is generated. Reading the flags register clears all flag bita and makes $\overline{INT}$ high impedance. To reset the flag register, the bq4852Y addresses must be held stable at location 7FFF0 for at least 50ns to avoid inadvertent resets.

Periodic Interrupt

Bits RS3–RS0 in the interrupts register program the rate for the periodic interrupt The user can interpret the interrupt in two ways: either by polling the flags register for IF assertion or by setting PIE so that $\overline{INT}$ goes active when the bq4852Y sets the periodic flag. Reading the flags register resets the PF bit and returns $\overline{INT}$ to the high-impedance state. Table 4 shows the periodic rates.

Alarm Interrupt

Registers 7FFF5–7FFF2 program the real-time clock alarm. During each update cycle, the bq4852Y compares the date, hours, minutes, and seconds in the clock registers with the corresponding alarm registers. If a match between all the corresponding bytes is found, the alarm flag AF in the flags register is set. If the alarm interrupt is enabled with AIE, an interrupt request is generated on $\overline{INT}$. The alarm condition is cleared by a read to the flags

Table 3. Watchdog Register Bits

MSB			Bits				LSB
7	6	5	4	3	2	1	0
WDS	BM4	BM3	BM2	BM1	BMO	WD1	WD0

register. ALM3–ALM0 puts the alarm into a periodic mode of operation. Table 5 describes the selectable rates.

The alarm interrupt can be made active while the bq4852Y is in the battery-backup mode by setting ABE in the interrupts register. Normally, the $\overline{INT}$ pin tri-states during battery backup. With ABE set, however, $\overline{INT}$ is driven low if an alarm condition occurs and the AIE bit is set. Because the AIE bit is reset during power-on reset, an alarm generated during power-on reset updates only the flags register. The user can mad the flags register *during* boot-up to determine if an alarm was generated *during* power-on reset.

Power-Fail Interrupt

When V_{CC} falls to the power-faildetect point, the power-fail flag PWRF is set. If the power-fail interrupt enable bit (PWRIE) is also set, then $\overline{INT}$ is asserted low. The power-fail interrupt occurs twpr before the bq4852Y generates a reset and deselects. The PWIE bit is cleared *on* power-up.

Battery-Low Warning

The bq4852Y checks the internal battery on power-up. If the battery voltage is below 2.2V, the battery-low flag BLF in the flags register is set to a 1 indicating that clock and RAM data may be invalid.

Table 4. Periodic Rates

RS3	RS2	RS1	RS0	Interrupt Rate
0	0	0	0	None
0	0	0	1	10ms
0	0	1	0	100ms
0	0	1	1	122.07µs
0	1	0	0	244.14µs
0	1	0	1	488.281
0	1	1	0	976.5625
0	1	1	1	1.953125ms
1	0	0	0	3.90625ms
1	0	0	1	7.8125ms
1	0	1	0	15.625ms
1	0	1	1	31.25ms
1	1	0	0	62.5ms
1	1	0	1	125ms
1	1	1	0	250ms
1	1	1	1	500ms

Table 5. Alarm Frequency (Alarm Bits DQ7 of Alarm Registers)

ALM3	ALM2	ALM1	ALMO	Alarm Frequency
1	1	1	1	Once per second
1	1	1	0	Once per minute when seconds match
1	1	0	0	Once per hour when minutes, and seconds match
1	0	0	0	Once per day when hours, minutes, and seconds match
0	0	0	0	When date, hours, minutes, and seconds match

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	
T_{STG}	Storage temperature (V_{CC} off; oscillator off)	-40 to +70	°C	
T_{BIAS}	Temperature under bias	-10 to +70	°C	
T_{SOLDER}	Soldering temperature	+260	°C	For 10 seconds

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C.

DC Electrical Characteristics (TA = TOPR, VCCmin 5 VCC ≤ VCCmax)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current			±1	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current			±1	µA	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
V_{OH}	Output high voltage	2.4			V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage			0.4	V	I_{OL} = 2.1 mA
I_{OD}	$\overline{RST}$, $\overline{INT}$ sink current	10			mA	V_{OL} = 0.4V
I_{SB1}	Standby supply current		3	6	mA	$\overline{CE} = V_{IH}$
I_{SB2}	Standby supply current		2	4	mA	$\overline{CE} \geq V_{CC} \cdot 0.2V$, OV ≤ V_{IN} 5 0.2V, or $V_{IN} \geq V_{CC} \cdot 0.2V$
I_{CC}	Operating supply current			90	mA	Min. cycle, duty = 100%, $\overline{CE} = V_{IL}$, $I_{I/O}$ = 0mA
V_{PFD}	Power-fail-detectvoltage	4.30	4.37	4.50	V	
V_{SO}	Supply switch-over voltage	-	3	-	V	

Notes: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.
$\overline{RST}$ and $\overline{INT}$ are open-drain outputs.

Capacitance (TA = 25°C, F = 1MHz, VCC = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance			10	pF	Output voltage = OV
C_{IN}	Input capacitance			10	pF	Input voltage = OV

Note: These parameters are sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 4 and 5

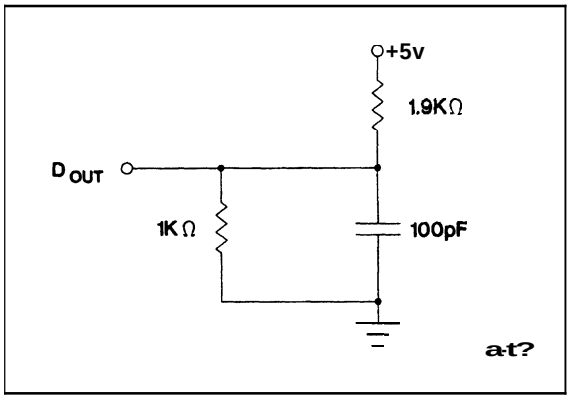


Figure 4. Output Load A

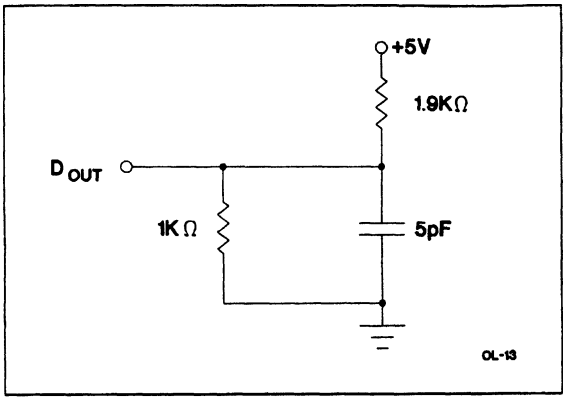
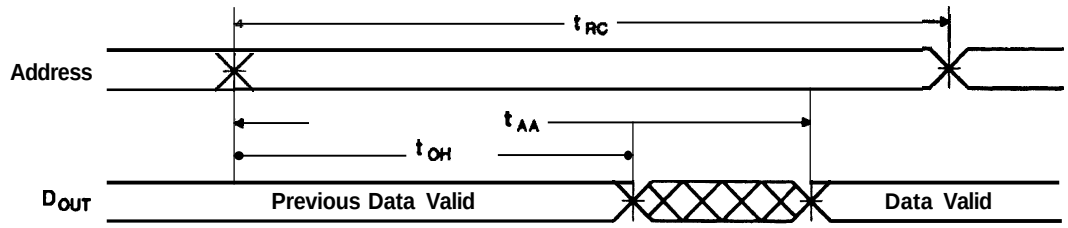


Figure 5. Output Load B

Read Cycle (TA = TOPR, VCCmin ≤ VCC 5 VCCmax)

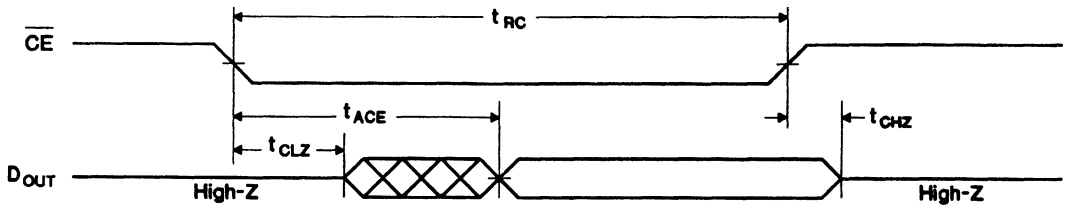
Symbol	Parameter	-85 Min.	-85 Max.	Unit	Conditions
t_{RC}	Read cycle time	85		ns	
t_{AA}	Address access time		85	ns	Output load A
t_{ACE}	Chip enable access time		85	ns	Output load A
t_{OE}	Output enable to output valid		45	ns	Output load A
t_{CLZ}	Chip enable to output in low Z	5		ns	Output load B
t_{OLZ}	Output enable to output in low Z	0		ns	Outputload B
t_{CHZ}	Chip disable to output in high Z	0	35	ns	Output load B
t_{OHZ}	Output disable to output in high Z	0	25	ns	Output load B
t_{OH}	Output hold from address change	10		ns	Output load A

Read Cycle No. 1 (Address Access) [1,2]



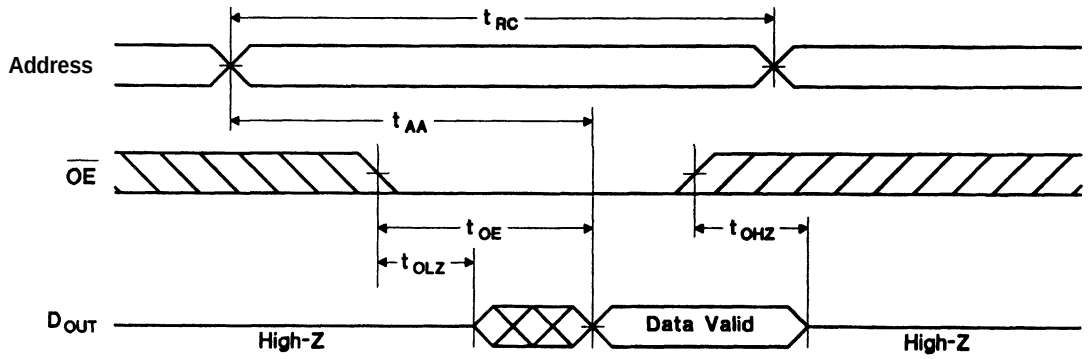
RC-1

Read Cycle No. 2 ($\overline{CE}$ Access) [1,3,4]



RC-2

Read Cycle No. 3 ($\overline{OE}$ Access) [1,5]



RC-3

Notes:

1. $\overline{WE}$ is held high for a read cycle.
2. Device is continuously selected: $\overline{CE} = \overline{OE} = V_{IL}$.
3. Address is valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Device is continuously selected: $\overline{CE} = V_{IL}$.

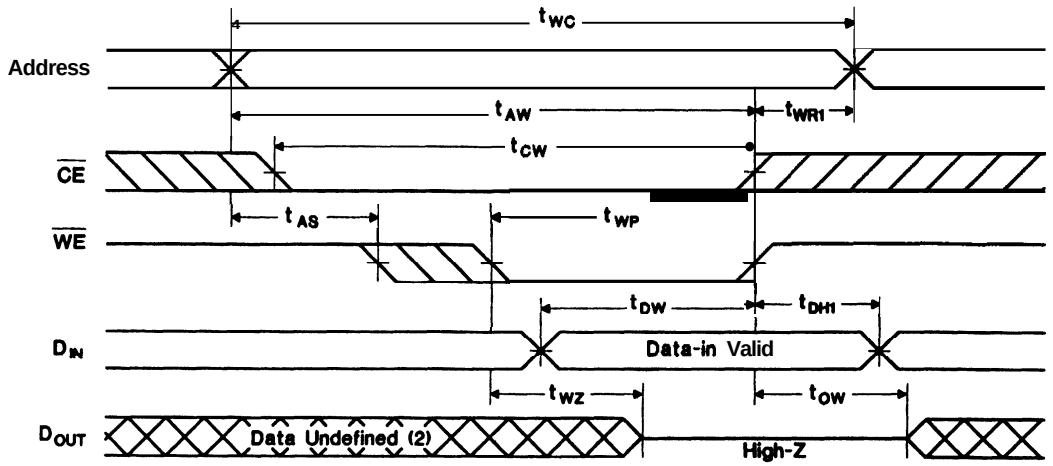
Write Cycle ($T_A = T_{OPR}$, $V_{CCmin} \le V_{CC} \le V_{CCmax}$)

Symbol	Parameter	-85 Min.	-85 Max.	Units	Conditions/Notes
t_{WC}	Write cycle time	85		ns	
t_{CW}	Chip enable to end of write	75		ns	(1)
t_{AW}	Address valid to end of write	75		ns	(1)
t_{AS}	Address setup time	0		ns	Measured from address valid to beginning of write. (2)
t_{WP}	Write pulse width	65		ns	Measured from beginning of write to end of write. (1)
t_{WR1}	Write recovery time (write cycle 1)	5		ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
t_{WR2}	Write recovery time (write cycle 2)	15		ns	Measured from $\overline{CE}$ going high to end of write cycle. (3)
t_{DW}	Data valid to end of write	35		ns	Measured* first low-to-high transition of either CE or $\overline{WE}$.
t_{DH1}	Data hold time (write cycle 1)	0		ns	Measured from $\overline{WE}$ going high to end of write cycle. (4)
t_{DH2}	Data hold time (write cycle 2)	10		ns	Measured from $\overline{CE}$ going high to end of write cycle. (4)
t_{WZ}	Write enabled to output in high Z	0	30	ns	I/O pins are in output state. (5)
tow	Output active from end of write	0		ns	I/O pins are in output state. (5)

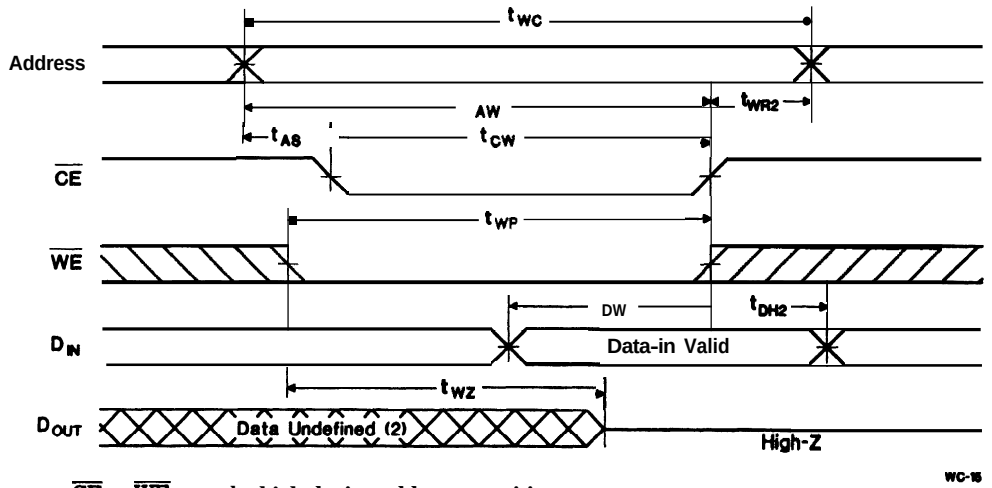
Notes:

1. A write ends at the earlier transition of $\overline{CE}$ going high and $\overline{WE}$ going high.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CE}$ going low and $\overline{WE}$ going low.
3. Either t_{WR1} or t_{WR2} must be met.
4. Either t_{DH1} or t_{DH2} must be met.
5. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

Write Cycle No. 1 ($\overline{WE}$-Controlled) 1,2,3



Write Cycle No. 2 ($\overline{CE}$-Controlled) 1,2,3,4,5



Notes:
1. $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
2. Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
3. If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.
4. Either t_{WR1} or t_{WR2} must be met.
5. Either t_{DH1} or t_{DH2} must be met.

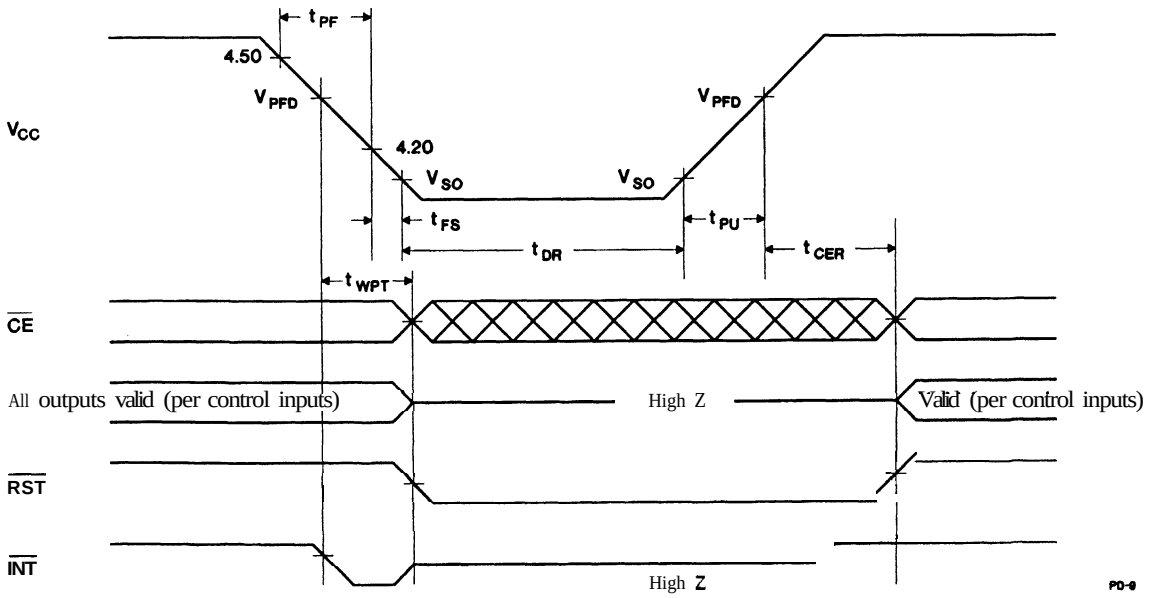
Power-Down/Power-Up Cycle (T_A = TOPR)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_{PF}	V_{CC} slew, 4.50 to 4.20 V	300			µs	
t_{FS}	V_{CC} slew, 4.20 to V_{SO}	10			µs	
t_{PU}	V_{CC} slew, V_{SO} to V_{PFD} (max.)	0			µs	
t_{CER}	Chip enable recovery time	40	100	200	ms	Time during which SRAM is write-protected after V_{CC} passes V_{PFD} on power-up.
t_{DR}	Data-retention time in absence of V_{CC}	10			years	T_A = 25°C. (2)
t_{WPT}	Write-protect time	40	100	160	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.

Notes:
1. Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.
2. Battery is disconnected from circuit until after V_{CC} is applied for the first time. t_{DR} is the accumulated time in absence of power beginning when power is first applied to the device.

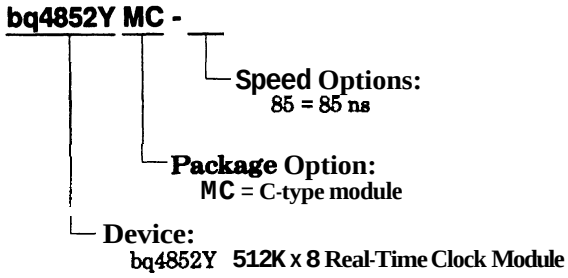
Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

Power-Down/Power-Up Timing



Notes:
1. PWRIE is set to "1" to enable power fail interrupt.
2. $\overline{RST}$ and $\overline{INT}$ are open drain and require an external pull-up resistor.

Ordering Information



5

Notes

Using the bq4845 for a Low-Cost RTC/NVSRAM Subsystem

Introduction

The bq4845 combinea a low-power real-time dock (RTC), a microcontroller supervisor, and a nonvolatile control circuit for static RAM on one IC. The part forms the basis of a low-cost, reliable RTC plus nonvolatile SRAM subsystem for many different embedded applications. By providing direct connections for a quartz crystal, an SRAM, and a backup source, the bq4845 eliminates as many as 15–20 discrete components.

The bq4845 contains 16 memory registers for clock, calendar, and control information as shown in Figure 1. The clock tracks seconds through years in binary coded decimal 12– or 24–hour format. The control information monitors and programs the onboard microcontroller supervisor and interrupts. The memory registers have the same interface as a standard byte-wide SRAM and can be mapped within the memory address space.

Figures 2A and 2B show how a typical battery backed-up RTC plus SRAM discrete solution compares with the bq4845 approach. The highly integrated bq4845 eliminates the discrete components needed in the power control, write protection, and reset circuits. It also features:

- Ultra-low backup current (< 500nA)
- Power-on reset
- Programmable watchdog timer with a separate output
- x8 real-time clock data
- Power-fail and periodic interrupt
- Low backup battery warning

0	Seconds	00
1	Seconds alarm	01
2	Minutes	02
3	Minutes alarm	03
4	Hours	04
5	Hours alarm	05
6	Day	06
7	Day alarm	07
8	Day-of-week	08
9	Month	09
10	Year	0A
11	Programmable rates	0B
12	Interrupt rates	0C
13	Flags	0D
14	Control	0E
15	Unused	0F

MM-13

Figure 1. Address Map

Contents

This application note discusses the key aspects of bq4845 operation.

5

Component Selection

SRAM

The bq4845 is designed to work with a low-power slow CMOS SRAM directly connected to V_{OUT} and $\overline{CE}_{OUT}$. Through these pins, the bq4845 provides power and a conditional chip enable to the memory. With valid system power, the output of the bq4845 supplies up to 100mA with $V_{OUT} = V_{CC} - 0.3V$, and the chip enable control passes through with a propagation delay of less than 12ns. With no system power, the bq4845 switches over to the backup source and holds the chip enable inactive. In this mode, the bq4845 supplies up to 100µA with $V_{OUT} = V_{BACKUP} - 0.3V$.

Monolithic CMOS SRAMs are available in byte-wide densitiea of 16kbits to 4Mbits. The section entitled 'Backing Up Multiple SRAMs" describes how to use multiple SRAMs with the bq4845 for word-wide or odd memory configurations.

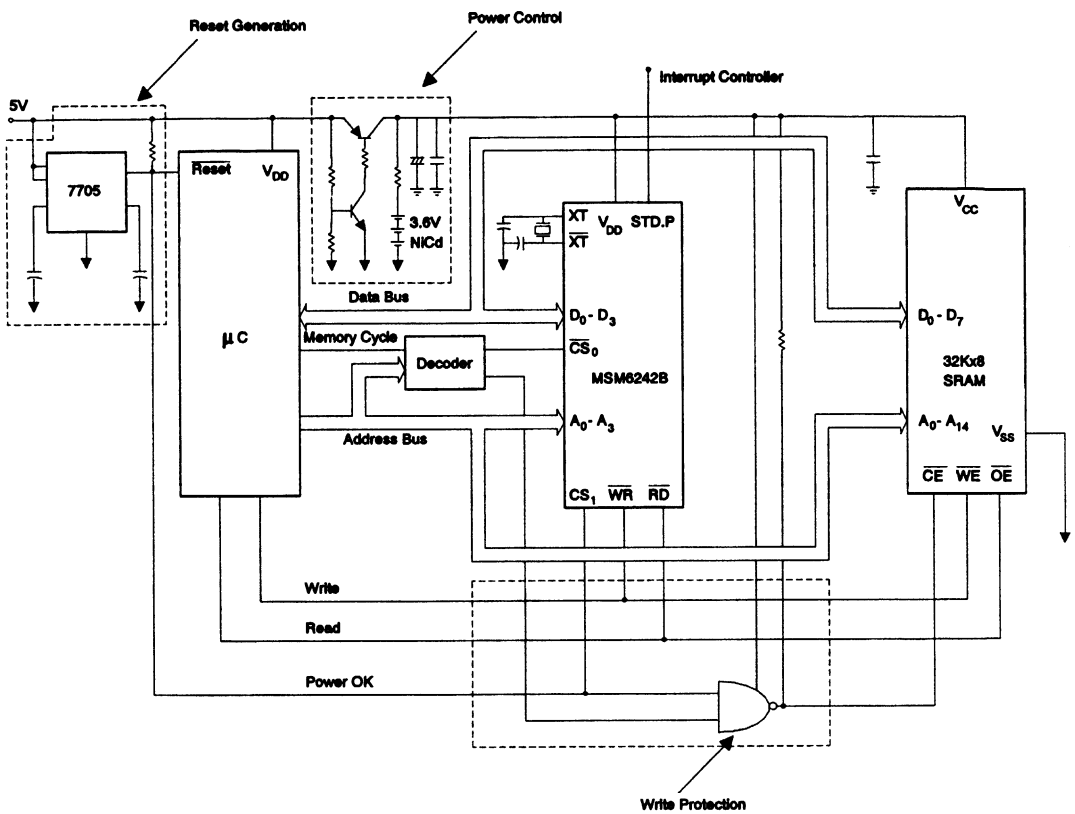


Figure 2A. Discrete Solution

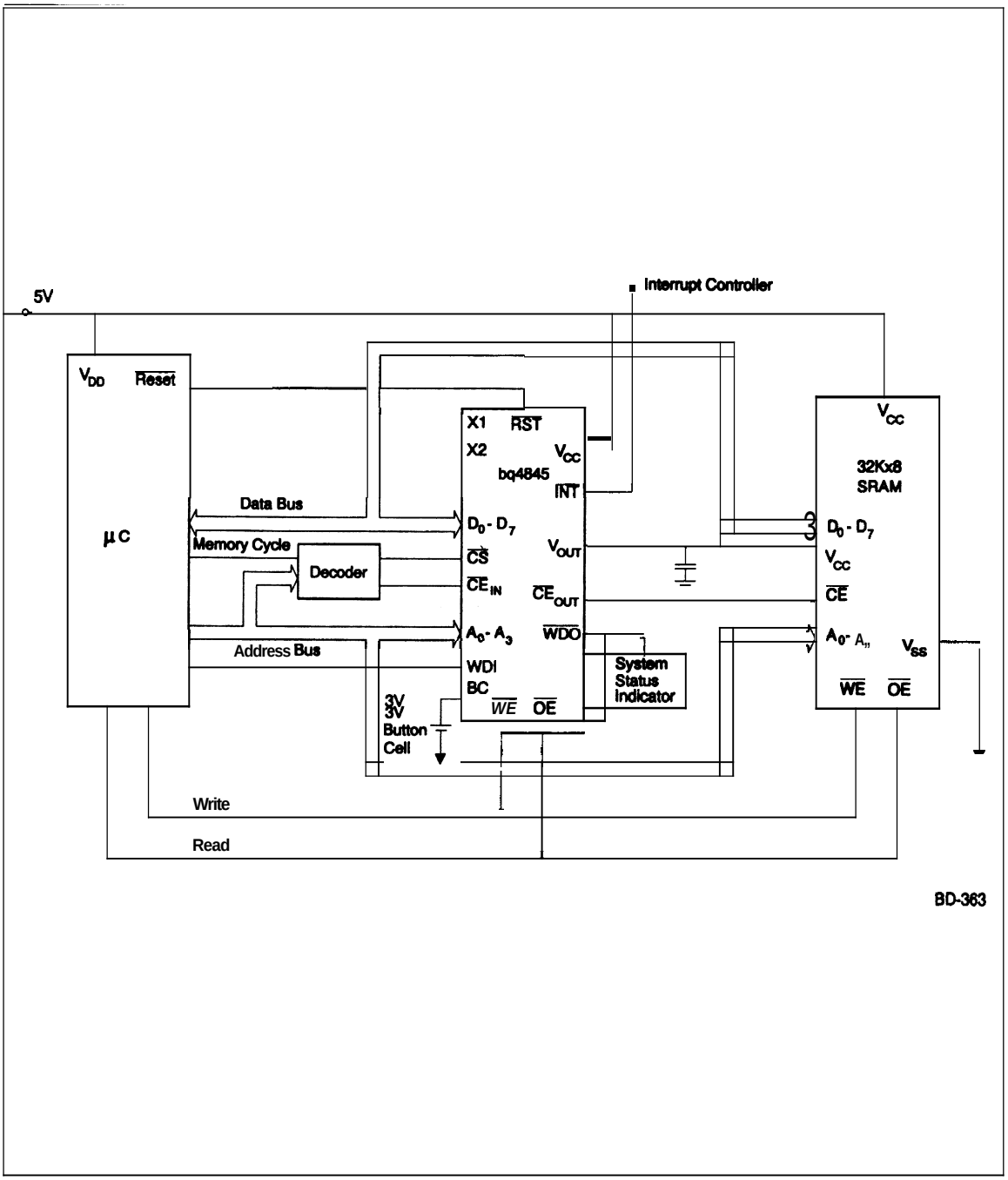


Figure 2B. bq4845 Approach

To minimize power consumption in active and backup mode, follow these recommendations:

1. Use an L-L power rated SRAM. They typically consume less than 70mA in active mode and leas than 1µA at 3V and 25°C in standby mode with a minimum data-retention voltage of 2V.
2. Use low-leakage ceramic bypass capacitors of 0.1µF across the SRAM and RTC.
3. Connect active high second chip enables (CE2) to VOUT of the bq4845, not to Vcc.

Crystal

The bq4845 oscillator is designed to work with a 32.768kHz tuning fork type crystal connected directly to X1 and X2 with no external components required. The crystal should have the characteristics described in Table 1.

With the properly selected crystal, the bq4845 real-time clock should be accurate to ±1 minute per month at room temperature with m trim capacitors. If greater accuracy is desired, a small trim capacitor of no more than 10pF can be connected from — to GND. The section entitled "Calibrating the Clock" describes how to adjust the bq4845 clock

Backup Source

The backup source on the BC input provides power to the real-time clock and the external SRAM when main system power is not applied. The backup source can be a primary (non-rechargeable) lithium cell, a secondary (rechargeable) NiCd pack, or a super capacitor. The choice of technology and capacity depends on the total data-retention load current and the anticipated amount of time the application is without power.

The total data-retention load of an RTC/NVSRAM subsystem consists of the current required to power the clock and maintain data in the SRAM, or $I_{DR} = I_{RTC} + I_{SRAM}$. I_{DR} varies with temperature and voltage. Therefore, the backup conditions of the application must be considered to determine the typical I_{DR}.

Figures 3 and 4 show how the data-retention currents of the bq4845 and an L-L rated SRAM vary over temperature. For most applications, the majority of the backup time is close to 3V and 25°C. Under these conditions, the typical data-retention current for a bq4845 application with a single L L rated SRAM is $I_{DR} = 0.5\mu A + 1\mu A$ or 1.5µA.

The bq4845 works with a primary or secondary cell. If the application spends the majority of its useful life powered-up, a super capacitor may be sufficient to meet the data-retention requirements of short intermittent power outage.. For applications with long potential system-off periods, a primary lithium cell or secondary NiCd pack should be used.

The bq4845 requires the backup source to be within 2.3V to 4.0V. The potential of the source is checked on power-up. When it is approximately 2.1V, the battery low flag is set, indicating that clock and RAM data may be invalid.

If the backup source does not make a connection to the BC pin and the BC pin is floating, then upon power-up, $\overline{RST}$ will remain low.

Table 1. Crystal Specifications

Symbol	Parameter	Minimum	Typical	Maximum	Unit
f_O	Oscillation frequency		32.768		kHz
C_L	Load capacitance		6		pF
T_P	Temperature turnover point	20	25	30	°C
k	Parabolic curvature constant			-0.042	ppm/°C
Q	Quality factor	40,000	70,000		
R_1	Series resistance			45	KΩ
C_0	Shunt capacitance		1.1	1.8	pF
C_0/C_1	Capacitance ratio		430	600	
D_L	Drive level			1	µW

Lithium

The bq4845 is best suited for uee with a primary lithium cell having a nominal voltage of 3V. The long shelf life, flat discharge curve, and high energy density allow a small lithium win cell to backup a bq4845/SRAM subsystem for greater than 10 years. The minimum required capacity is given by:

Equation 1

$$C(Ah) = L * \left(1 - \frac{T_{ON}}{100}\right) * I_{DR} * 8760$$

where:

- L = useful lifetime of the equipment (years)
- T_{ON} = % of time system power is on
- I_{DR} = total data-retention current (A).

T_{ON} can be factored into the equation because capacity of the lithium cell is not consumed when system power is applied.

An inexpensive lithium coin cell meets the data-retention requirements of most single SRAM applications. These cells range in capacity from 30mAh to 300mAh. Cylindrical lithium cells offer greater than 1000mAh. The two chemistry types are: BR and CR. BR has better shelf life characteristics at elevated temperatures and should be used in industrial temperature operating environments to ensure that storage life wearout does not limit the backup time below the calculated value. The cells are available with solder tab connections for PCB mounting, or can be socketed for user replaceability.

NiCd

A small NiCd pack can be trickle-charged from the system voltage supply using a resistor. The value of the resistor depends on the recommended trickle charge rate of the battery manufacturer. The optimum series configuration is 3 cells, since this gives a nominal voltage of 3.6V. The capacity can be sized using equation 1 with T_{ON} = 0, and L equal to the longest anticipated time the system will be without power. A small 3.6V NiCd pack can provide years of clock operation and data retention using the bq4845 and an L L rated SRAM. Like the lithium cells, the 3-cell NiCd padre are available with solder tabs.

Super Capacitor

A low-leakage super capacitor can be used to back up the bq4845 plue an external L L SRAM. The caner diode across the capacitor keeps the voltage from exceeding the 4.0V limit on the BC input. The series charge resistor depends on the size and type of capacitor. The approximate backup time is given by the equation:

Equation 2

$$T(days) = \frac{(C * \Delta V)}{(86400 * I_{DR})}$$

where:

- C = capacitor value (F)
- ΔV = valid voltage back-up range (V)
- I_{DR} = total data-retention current (A)

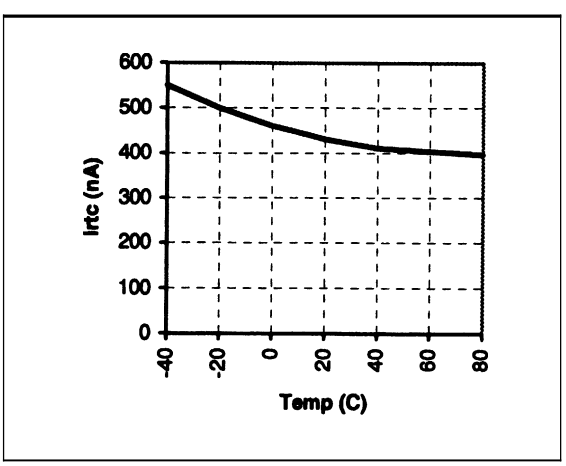


Figure 3. bq4845 Data-Retention Current at V_{BC} = 3V

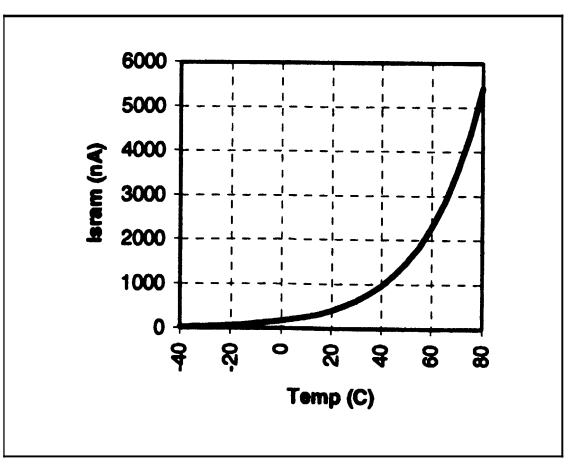


Figure 4. Typical L-LSRAM Data-Retention Current at V_{CC} = 3V

ΔV = 4.0 - 2.3 or 1.7V for a bq4845 application. Thus, a 1F or 2F super capacitor can provide weeks of backup time for the bq4845 RTC and a single L-L SRAM.

Figure 5 shows the three different backup configurations.

Board Layout

Crystal Connection

The quartz crystal should be connected directly to X1 and X2. A small trim capacitor can be placed on X2 for higher clock accuracy. To minimize the risk of noise coupling into the bq4845 RTC oscillator, follow these recommendations:

1. The crystal should be located as close as possible to the pin connections on the bq4845.
2. The pins should be surrounded by a ground guard ring.
3. No signals should run directly below the crystals or below the traces to the X1 and X2 pins.

Figure 6 shows an example configuration.

Backup Source Connection

The backup source placement is not as critical as it is for the crystal. Still, it should be placed as close to the bq4845 as possible, although the designer should also consider accessibility if the battery is to be easily replaced. The backup source should be connected directly to the BC input (+) and V_{SS} (-).

Lithium primary cells in electronic equipment require protection against reverse charging from V_{CC} when system power is on. The bq4845 battery input circuit includes two protection diodes in series between BC and V_{CC}. The protection diodes meet the UL requirements for the use of a lithium cell as a backup source in electronic circuits. **Therefore, no external reverse charging circuit is required or recommended.** The bq4845 is listed under UL file number E134016.

Calibrating the Clock

Accuracy Measurement

With a properly selected quartz crystal connected directly to X1 and X2, the bq4845 should be accurate to ±1 minute per month at room temperature with no trim capacitor. The accuracy of the clock changes with temperature as seen in Figure 7. If higher accuracy is required at room temperature, or the system operates at the temperature extremes, a small trim capacitor *can* be placed between X2 and ground. A simple calibration routine can be used to measure the frequency and trim the capacitor for optimum clock accuracy at the use temperature.

The calibration software routine uses the periodic interrupt to measure the frequency variance of the real-time clock. The interrupt rate is monitored on the $\overline{INT}$ pin. In this test setup, the $\overline{INT}$ pin is connected to a frequency meter, and should not interrupt the microcontroller. It may be beneficial to provide a jumper for the $\overline{INT}$ pin on the board design in order to disconnect it from the interrupt controller when the calibration routine is run. No test equipment should be connected directly to either crystal pin, as the added loading alters the characteristics of the oscillator and *can* make tuning impossible.

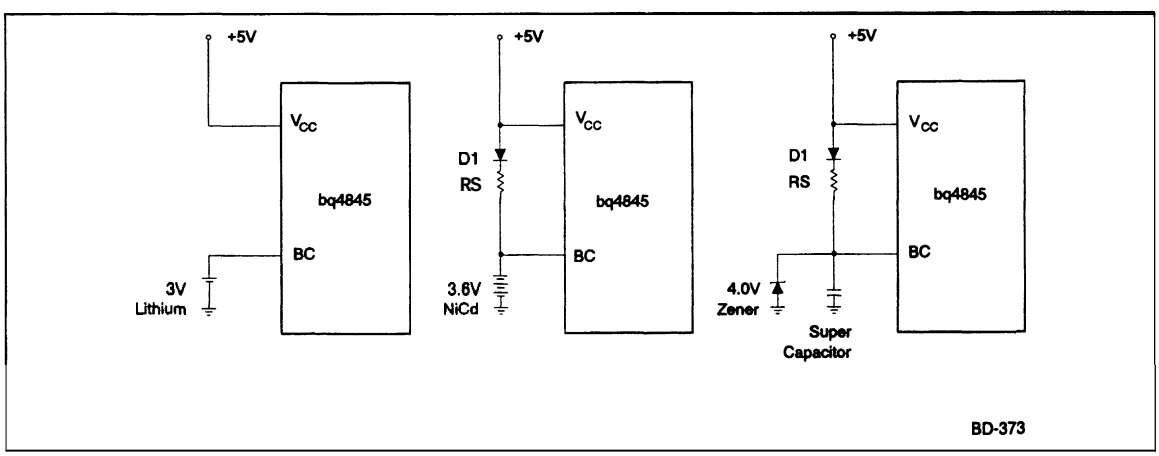


Figure 5. Backup Configurations

The calibration routine should be performed at the temperature at which the system spends the majority of its operating time. The calibration routine consists of the following sequence of operations:

1. Control Register: Write [XXXX01XX]b. Turns on the RTC.
2. Programmable Rates Register: Write [XXXX0011]b. Sets the periodic interrupt rate to 8.192kHz.
3. Interrupts Enable Register: Write [00000100]b. Enables only the periodic interrupt.
4. Flags Register: The program should *now* loop on reading this register. Reading the register resets the interrupt flag PF and returns $\overline{INT}$ high. The next interrupt will re-assert PF and $\overline{INT}$. Reading the register must *occur* at a rate which exceeds the periodic rate in order to catch all the transitions. The periodic rate can be adjusted by programming register B.

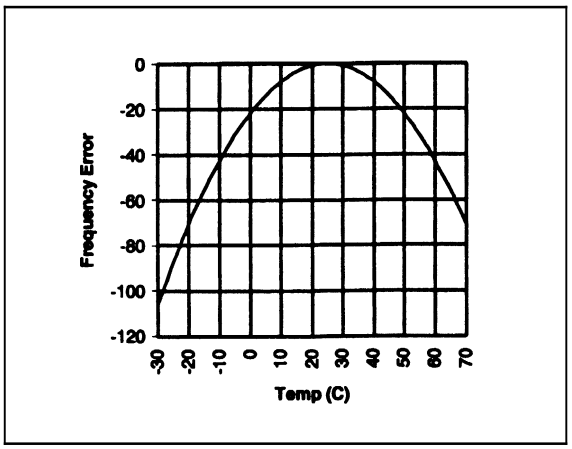


Figure 7. Frequency Error

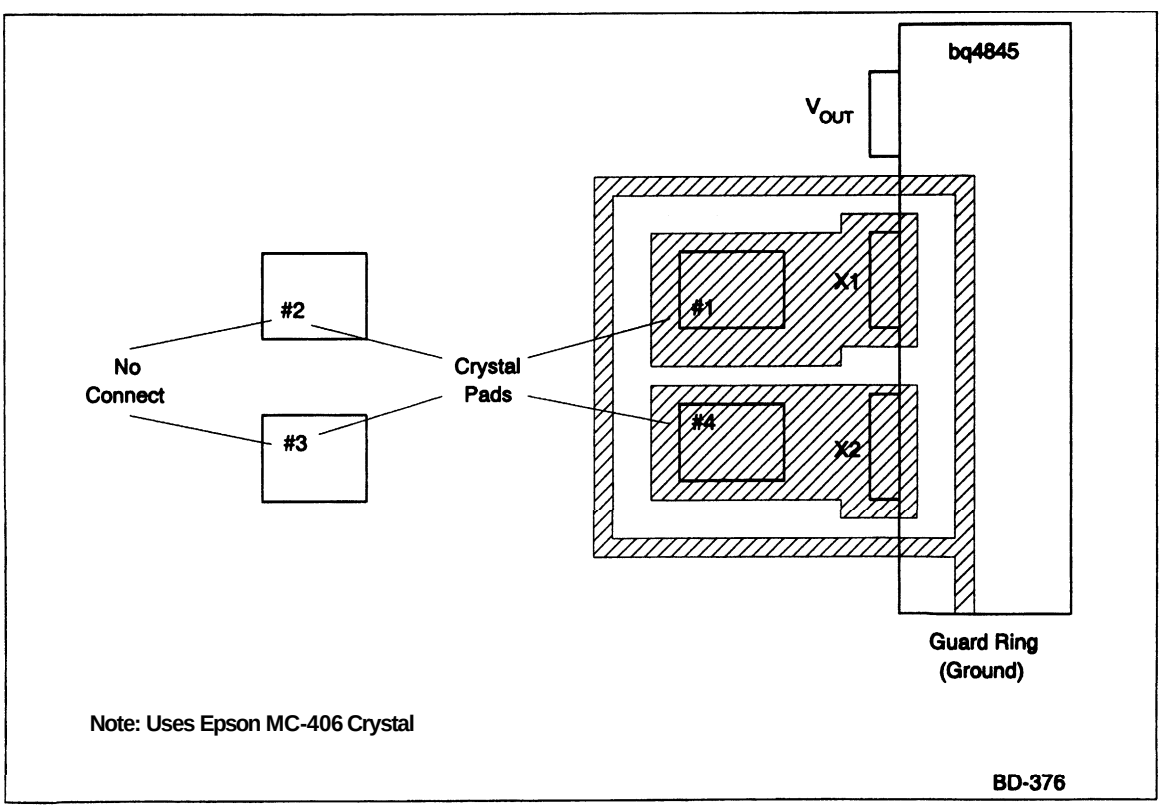


Figure 6. Crystal Connection

5. Monitor the frequency on the $\overline{INT}$ pin with a high-resolution meter. The $\overline{INT}$ pin is active low so the meter should trigger on a negative transition. Any deviation from the set periodic rate indicates clock error.
6. Adjust the trim capacitor to provide a frequency as close to the set periodic rate as possible.

Adjustment Considerations

The bq4845 uses a very low-current oscillator and is sensitive to capacitance on the crystal inputs. To ensure the real-time clock does not stop in the low-voltage battery-back-up mode, the total capacitance on X2 should be no more than 15pF, including the trace capacitance. With short lead traces, the maximum recommended trim capacitor is 10pF. As a rule of thumb, each additional 1.54pF of capacitance on X2 results in a decrease of 0.8Hz or 64 seconds per month.

System Supervision

The bq4845 includes three system supervisory functions: Power-fail monitoring, µP monitoring, and µP reset generation. The three functions work together to provide orderly power-down and restart procedures.

Power-fail Warning

The bq4845 can be programmed to generate a power-fail warning. The warning can be used to alert the microcontroller to save critical data in the SRAM prior to µP reset generation.

To program the power-fail warning, set the PWRIE bit of register C to 1. When the 5V system supply on V_{CC} drops below V_{PFD} as seen in Figure 9, the interrupt output $\overline{INT}$ goes low. Since other sources (clock alarm and periodic interrupt) can activate the the $\overline{INT}$ output, register D can be read to see if the power-fail warning flag is set to 1. If PWRF is 1, a power-fail condition has occurred and the microcontroller has 100µs to etore data prior to assertion of the µP reset by the bq4845.

The power-fail thresholds (V_{PFD}) are set at 4.62V (typical) for the bq4845 and 4.37V (typical) for the bq4845Y. The $\overline{INT}$ pin is open drain, and requires a pull-up resistor.

Power-on Reset

The active-low pow[redacted] reset is asserted 100µs after power-fail detection as seen in Figure 9. The reset remaim asserted for after valid power returns to provide for system stabilization. The output is open drain, and requires an external pull-up resistor.

Watchdog Timer

The watchdog timer is used to supervise processor operation. The watchdog monitors the WDI input. This input can be connected to a bus line or an I/O port. If WDI is not toggled within the programmed time-out period, the bq4845 asserts $\overline{WDO}$ and $\overline{RST}$. The timeout is pro-

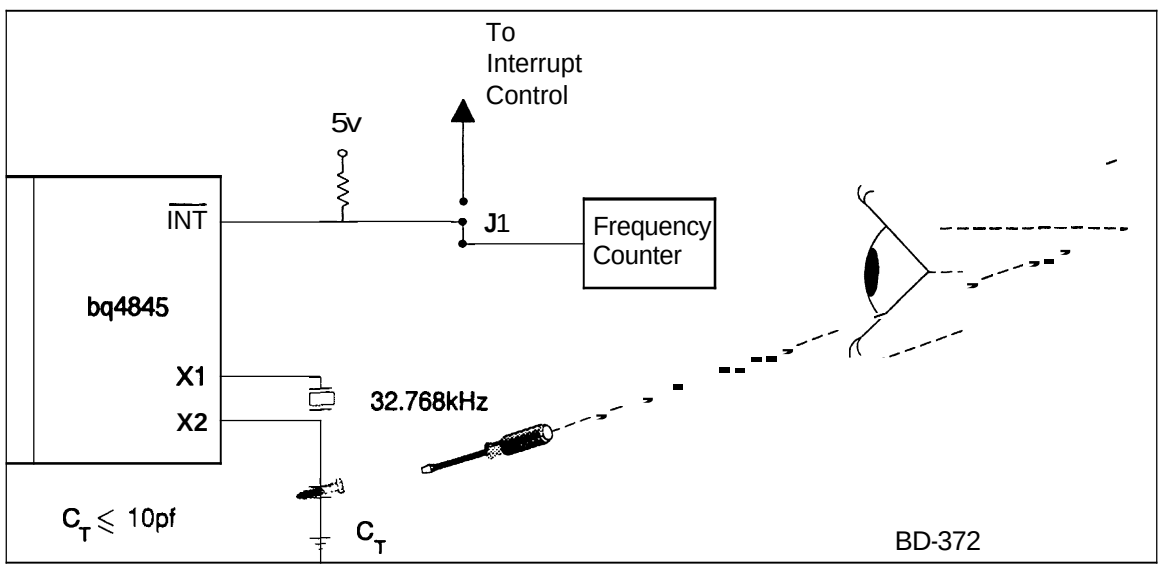
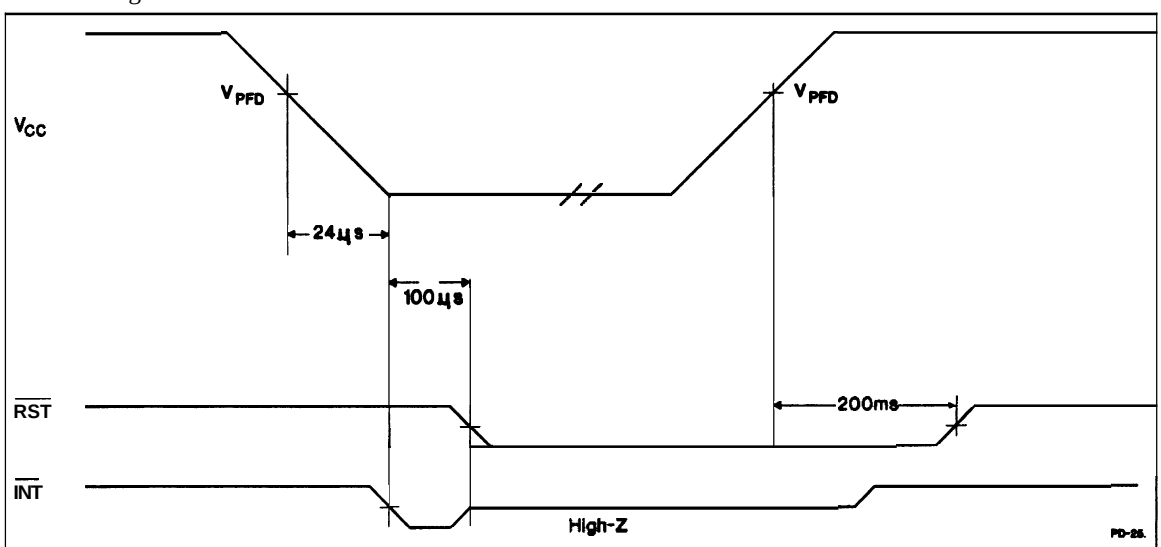


Figure 8. Frequency Adjustment

grammed in register B according to Table 2. The bq4845 retains this time-out period through power cycles as long as battery power is valid. If the bq4845 loses backup power in data-retention mode, the default time-out period is 1.5s. The watchdog timer is disabled only if WDI is left floating.

If a watchdog time-out occurs, the run time of the subsequent initialization routine must be less then the programmed time-out period or the system may never recover.



Notes: PWRIE set to "1" to enable power-fall interrupt
RST and INT are open drain and require an external pull-up resistor.

Figure 9. Power-Down/Power-Up Timing

Table 2. Watchdog Time-Out Rates

WD2	WD1	WD0	Watchdog Time-out Period
0	0	0	1.5s
0	0	1	23.4375ms
0	1	0	46.875ms
0	1	1	93.75ms
1	0	0	187.5ms
1	0	1	375ms
1	1	0	750ms
1	1	1	3s

$\overline{WDO}$ can be used to indicate to the system that the reset was caused by a watchdog fault and not a power failure. $\overline{WDO}$ is reset after a watchdog fault by a transition on WDI. $\overline{WDO}$ can be connected to an audible alarm or a controller input I/O pin. $\overline{WDO}$ is held high when Vcc is below the power-fail threshold, battery-backup mode is enabled, or WDI is left floating.

Backing Up Multiple SRAMs

While monolithic SRAMs come in a wide variety of densities, some memory configurations may require the use of two external memory chips.

Word-Wide Configurations

For a word-wide or x16 configuration, two L-L rated SRAMs can be put in parallel as shown in Figure 10. The combined active current of the memory at the operating cycle must be less than 100mA. The total data-retention current is $I_{DR} = I_{RTC} + 2 * I_{SRAM}$.

Odd Configurations

To build an odd memory configuration like a 2Mbit RTC/NVSRAM subsystem, additional logic may be needed. One 7400 CMOS NAND gate provides the chip select decoding for the 256Kx8 NVSRAM configuration shown in Figure 11.

Additional Integration—bq4847

The bq4847 combines the bq4845 with a crystal and lithium coin cell in a 600-mil dual-in-line package to offer an additional level of integration. The only component required for the RTC/NVSRAM subsystem is the static RAM connected directly to the bq4847. The internal battery has over 130mAh of capacity to provide greater than 10 years of data retention in most applications. To prevent inadvertent battery discharge during handling, the bq4847 battery is isolated from the V_{OUT} and $\overline{CE}_{OUT}$ pine until the initial application of Vcc. After V_{CC} is applied, the battery connects to V_{OUT} whenever V_{CC} drops below V_{SO} (typically 3V).

The internal crystal meets the specifications described in Table 1. The bq4847 is caliited at the factory to provide clock accuracy better than one minute per month at 25°C.

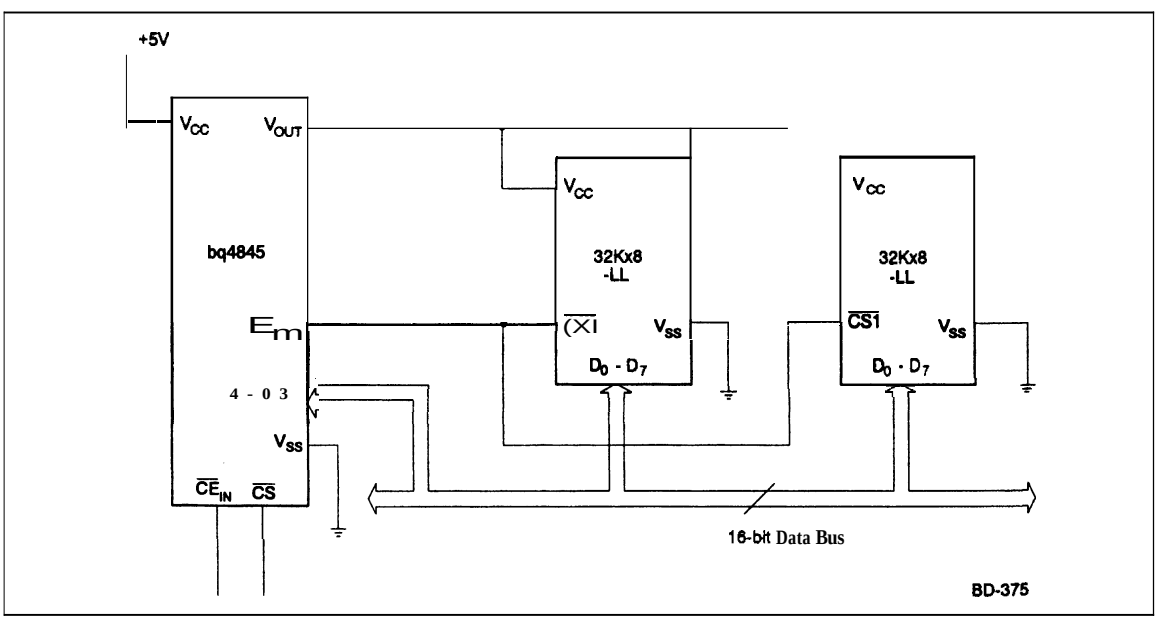


Figure 10. 32Kx16 Memory Configuration

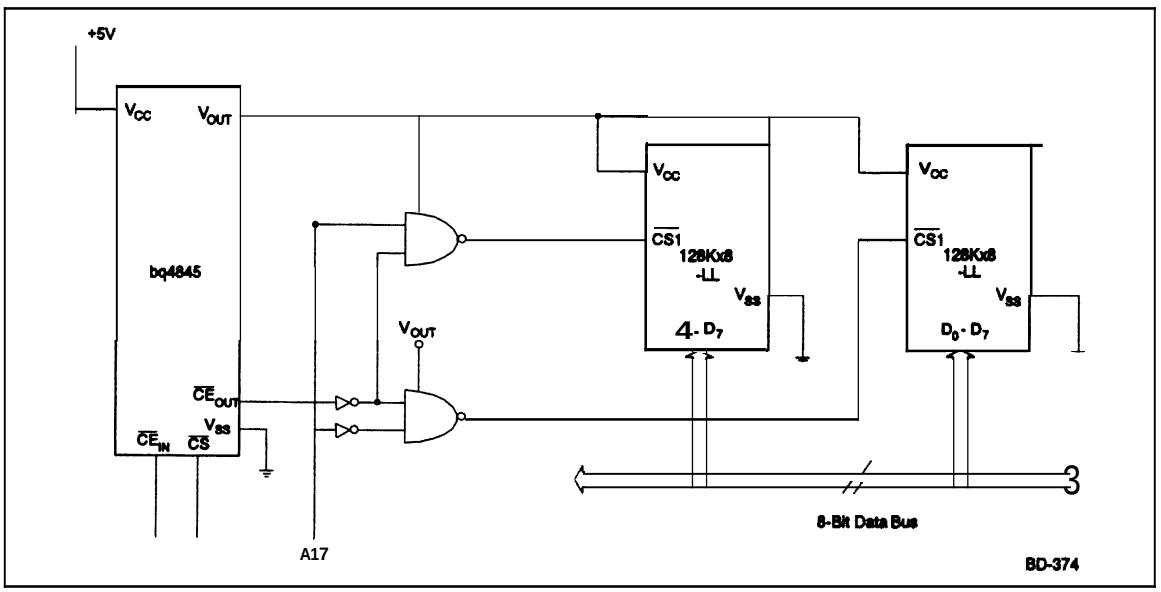


Figure 11. 256Kx8 Memory Configuration

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Notes

Typical PC Hookups For Real-Time Clocks

Introduction

The following pages contain diagrams showing how Benchmarq's Real-Time Clocks are used in existing circuits with minor or no redesign. Parts lists are included for each diagram.

The circuits shown are actual PC implementations of Motorola RTCs. The proposed Benchmarq replacementa save numerous components and reduce the cost of the motherboard. Pin conversions from the MC146818A to the bq3285 and bq3287/A are shown in Tables 1 and 2.

All of Benchmarq module products are U.L. recognized under U.L. file number E1340146.

Remember that the bq3285/87/87A are socket replacements for the DS1285/87/87A/885/887/887A and MK48T85/87/87A. See Chapter 1 for the RTC cross-reference table.

Examples are included for ISA and EISA PC systems.

- ISA (PC/AT) systems:
  - Example MC146818A PC/AT design (*Figure* 1, Table 3)
  - Equivalent bq3285 design (Figure 2, Table 4)
  - MC146818A/bq3285 design (Figure 3, Table 4)
  - Equivalent bq3287 design (Figure 4 , Table 5)
- EISA or MCA systems:
  - Example MC146818A plus external 8Kx8 SRAM design (*Figure* 5, Table 6)
  - Example DS1287 plus external 8Kx8 NVSRAM design (Figure 6, Table 7)
  - Equivalent bq4285 design (Figure 7, Table 8)
  - Equivalent bq4287 design (Figure 8, Table 9)

5

Table 1. Converting MC146818A to bq3285/87/87A

MC146818 Pin No.		DIP and SOIC Packages		
		bq3285P/S Pin No.	bq3287MT Pin No.	bq3287AMT Pin No.
1–15	→	No change	No change	No change
16	→	No connect	No change	No change
17–19	→	No change	No change	No change
20	→	< 4.0V	No change	No change
21	→	Tie to V_{CC}	No change	Tie to V_{CC}
22–24	→	No change	No change	No change

Table 2. Converting MC146818A to bq4285/87

MC146818 Pin No.		DIP and SOIC Packager	
		bq4285P/S Pin No.	bq4287MT Pin No.
1	→	VOW	V_{OUT}
2–20	→	No change	No change
21	→	$\overline{CE}_{IN}$: Tied to V_{SS}	$\overline{CE}_{IN}$: Tied to V_{SS}
22	→	$\overline{CE}_{OUT}$	$\overline{CE}_{OUT}$
23–24	→	No change	No change

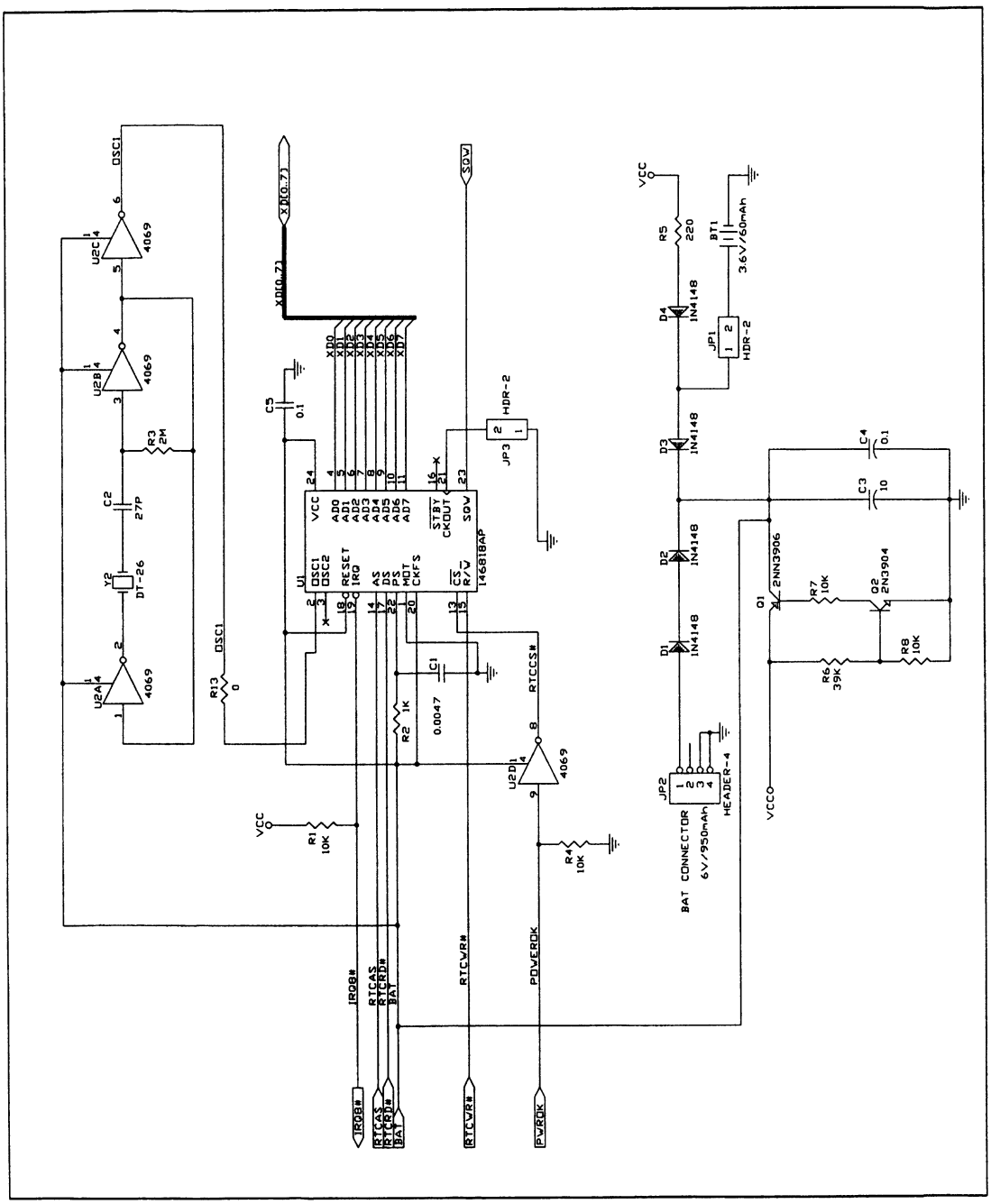

Figure 1. MC146818A ISA (PC/AT) Example

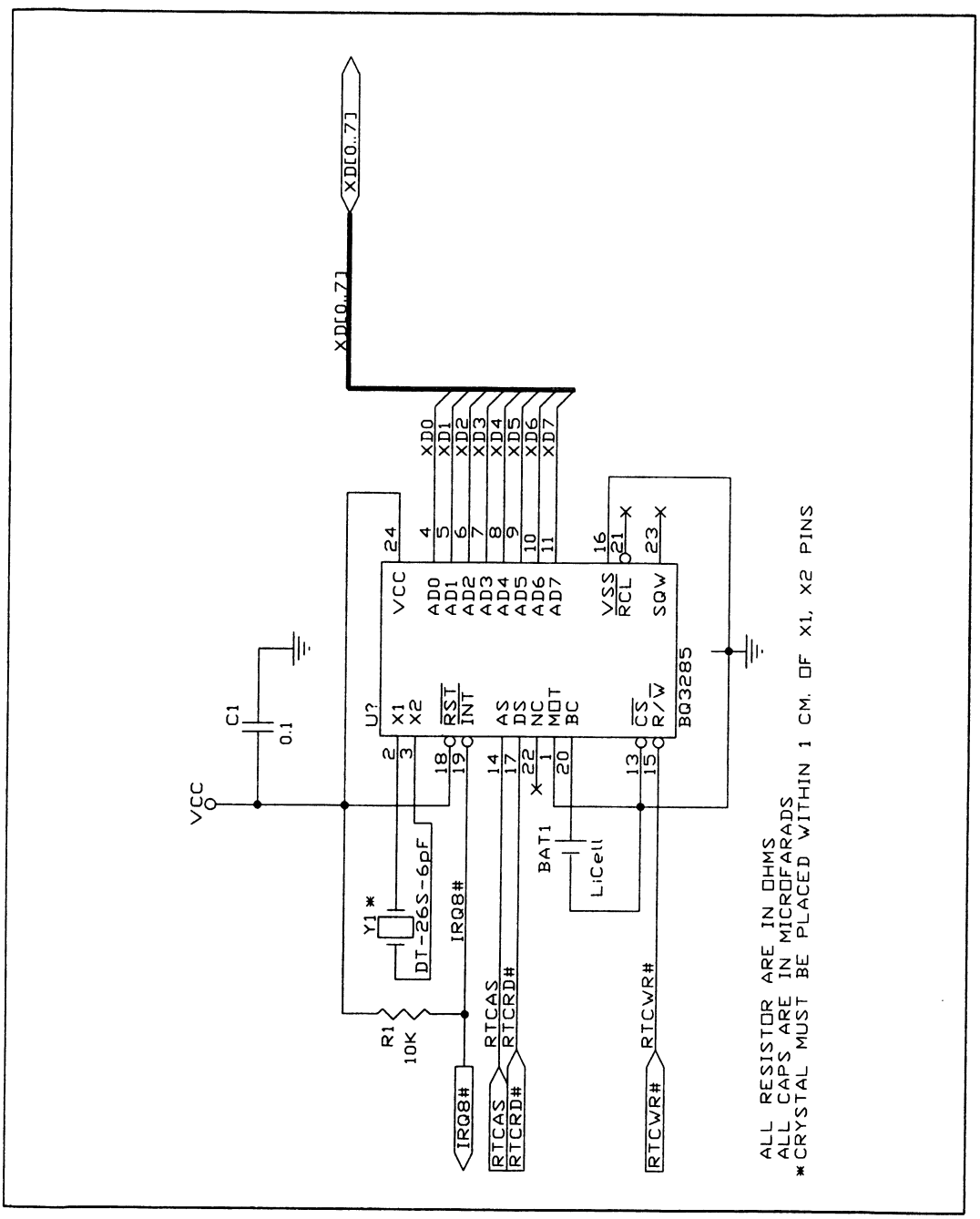

Figure 2. bq3285 ISA (PC/AT) Example

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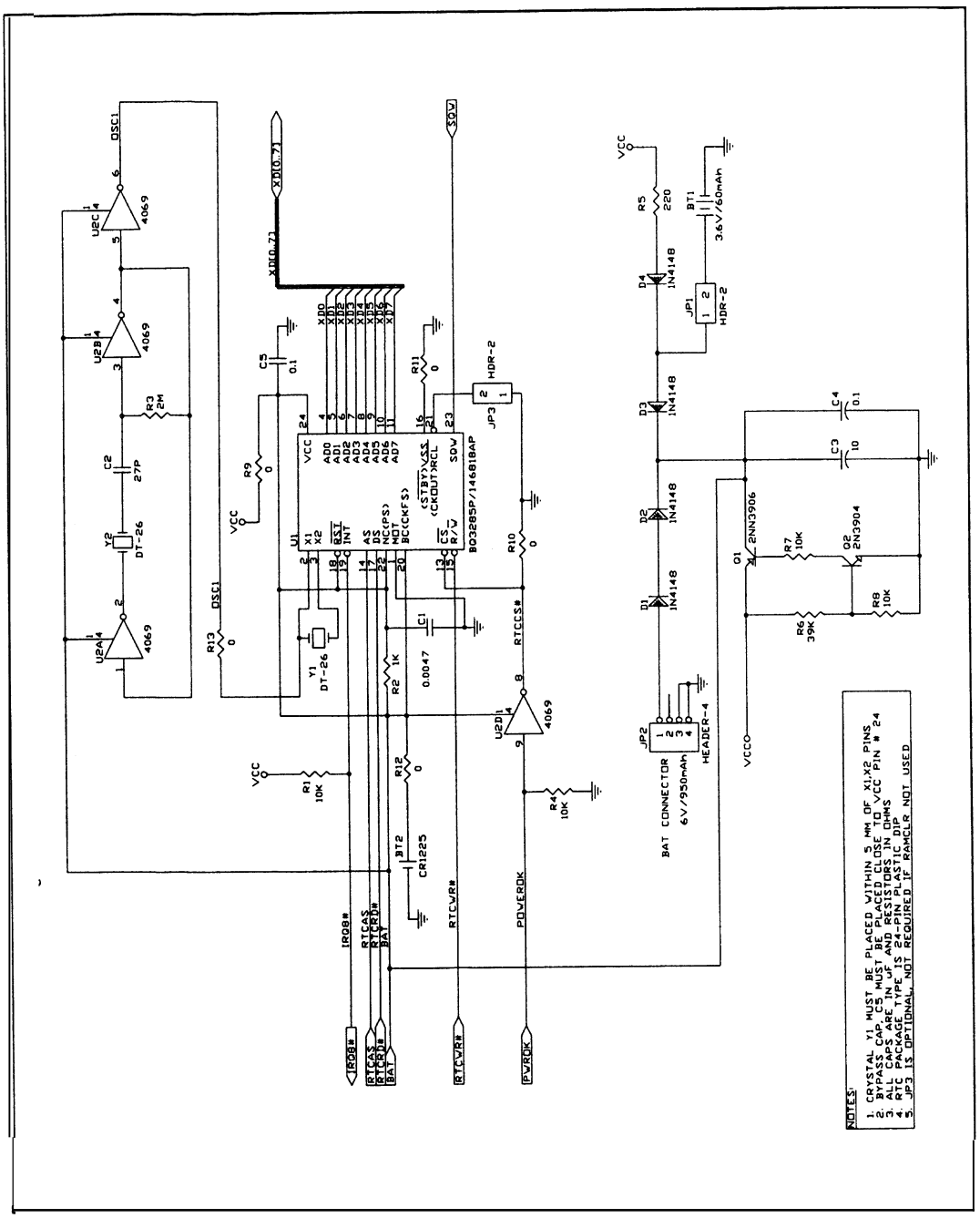


Figure 3. bq3285 or MC146818A ISA (PC/AT) Example

Table 3. MC146818A ISA (PC/AT) Parts List (Figures 1 and 3)

Item	Quantity	Reference	Put
1	1	BT1	3.6V/60mAh
2	1	C1	0.0047
3	1	C2	27P
4	1	C3	10
5	1	C4	0.1
6	4	D1, D2, D3, D4	1N4148
7	1	JP1	HEADER2
8	1	JP2	HEADER-4
9	1	Q1	2NN3906
10	1	Q2	2N3904
11	4	R1, R4, R7, R8	10K
12	1	R2	1K
13	1	R3	2M
14	1	R5	220
15	1	R6	39K
16	1	U1	MC146818A
17	1	U2	4069

5

Table 4. bq3285 ISA (PC/AT) Parts List (Figures 2 and 3)

Item	Quantity	Reference	Put
1	1	R1	10K
2	1	U1	bq3285
3	1	BT1	Li cell
4	1	Y1	DT-26
5	1	C1	0.0047

Notes: Possible crystal/battery suppliers include:

- Daiwa DT-26 or equivalent crystal
- Rayovac/Panasonic lithium coin cells:

  BR1225 38–39mAh
  BR2032 180–200mAh
  BR2325 165–180mAh

  These cells and cells of other sizes are available =tabbed" for soldering directly into boards. These types of lithium coin cells are safe for all modes of transportation per U.S. Department of Transportation records.

- Rayovac U.L. #MH12542
- Panasonic U.L. #MH12210

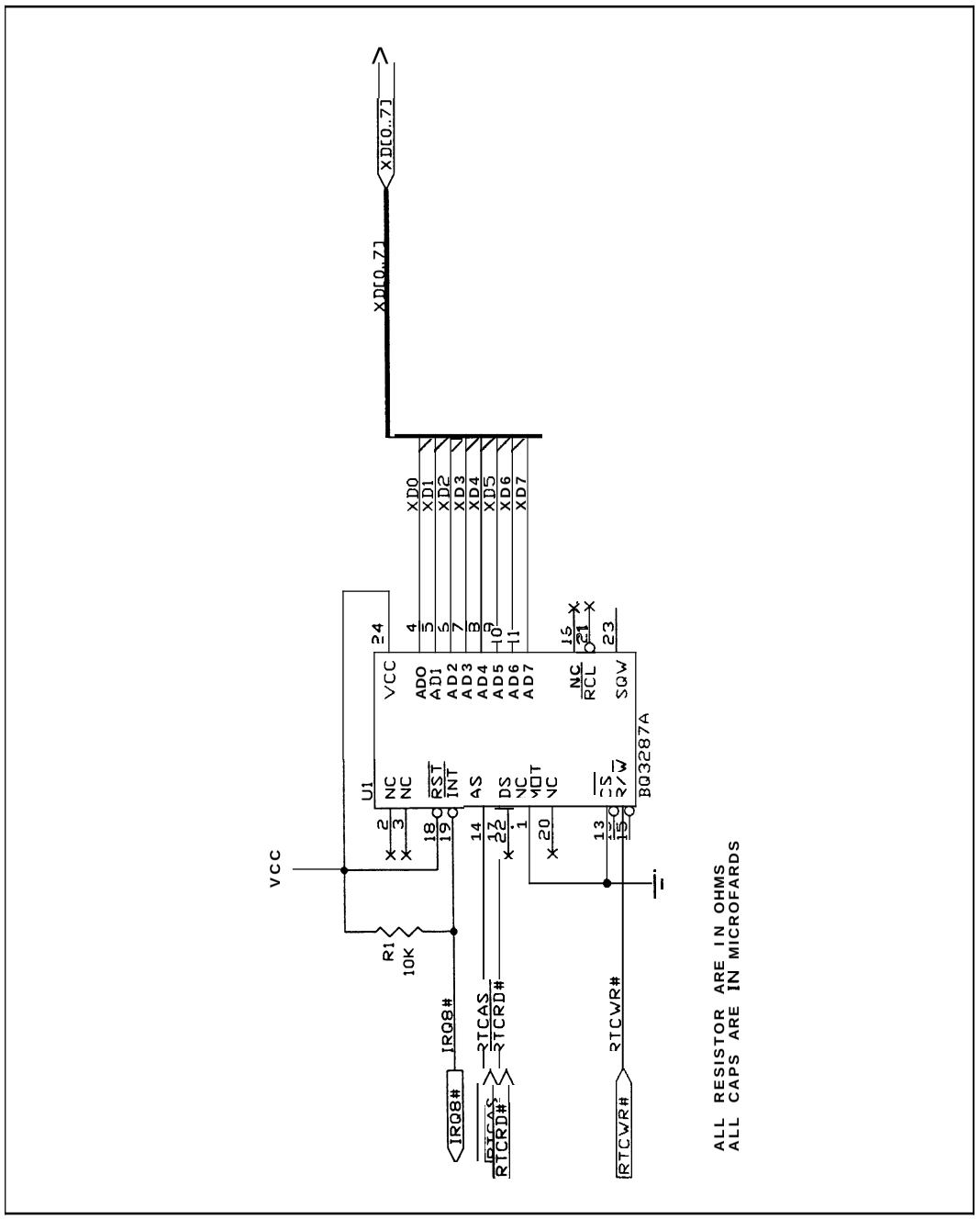


Figure 4. bq3287 ISA (PC/AT) Example

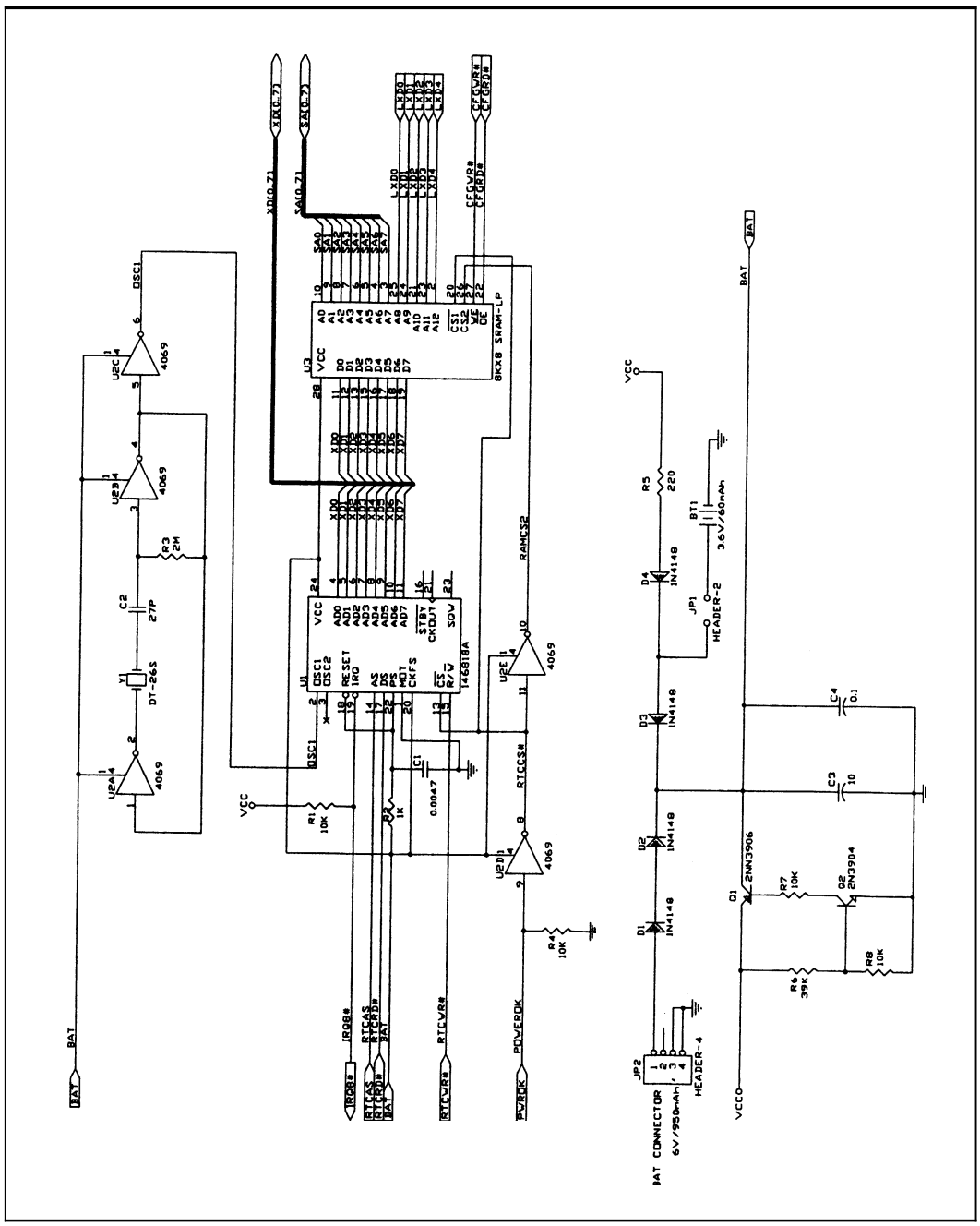


Figure 5. **MC146818A** w/ External SRAM **EISA** or MCA Example

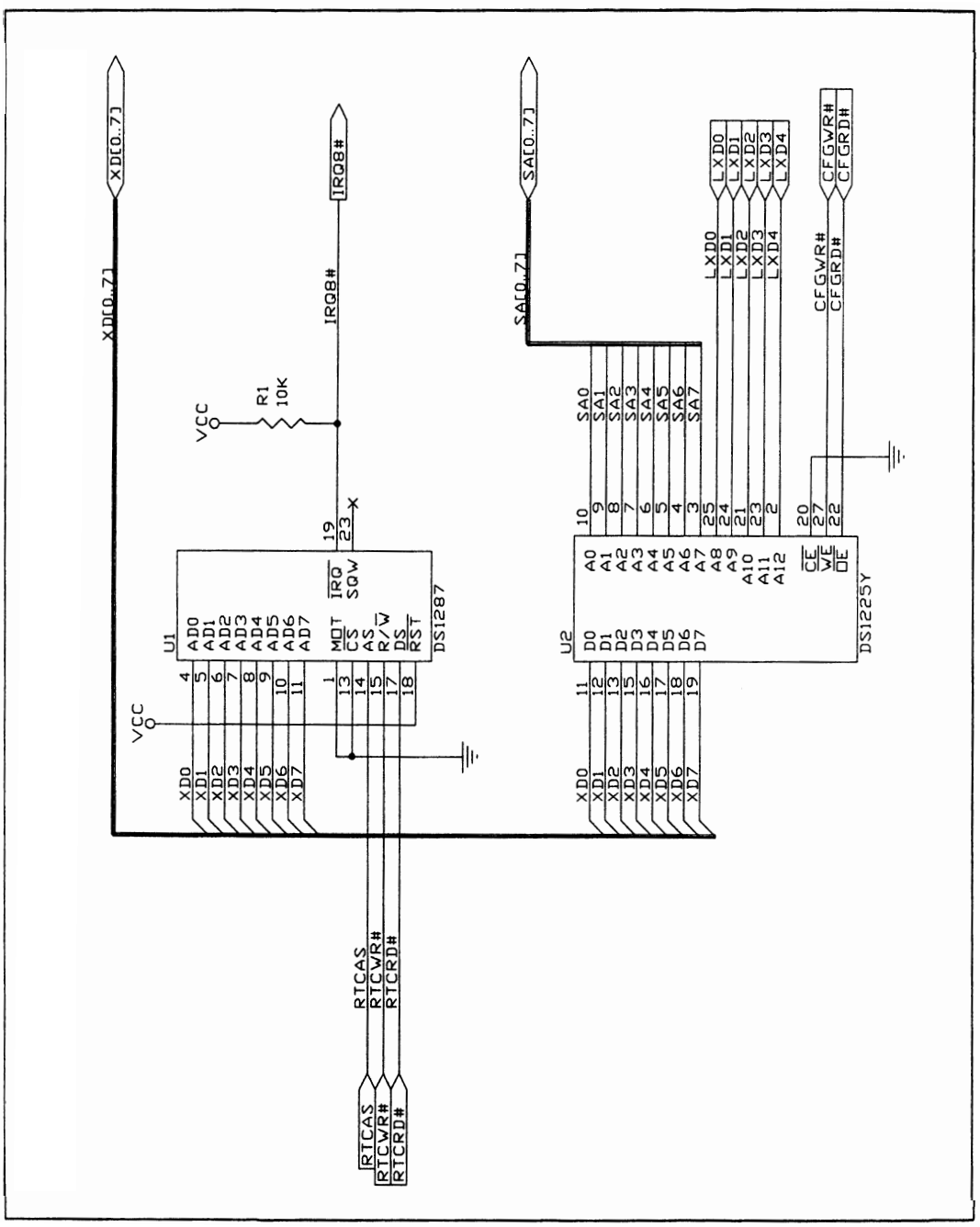


Figure 6. DS1287 w/ NVSRAM EISA or MCA Example

Table 5. bq3287 ISA (PC/AT) Parts List (Figure 4)

Item	Quantity	Reference	Part
1	1	R1	10K
2	1	U1	bq3287

Table 6. MC146818A w/ External SRAM Parts List (Figure 5)

Item	Quantity	Reference	Part
1	1	BT1	3.6V/60mAh
2	1	C1	0.0047
3	1	C2	27P
4	1	C3	10
5	1	C4	0.1
6	4	D1, D2, D3, D4	1N4148
7	1	JP1	HEADER-2
8	1	JP2	HEADER-4
9	1	Q1	2NN3906
10	1	Q2	2N3904
11	4	R1, R4, R7, R8	10K
12	1	R2	1K
13	1	R3	2M
14	1	R5	220
15	1	R6	39K
16	1	U1	MC146818A
17	1	U2	4069
18	1	U3	8Kx8 SRAM-LP
19	1	Y1	DT-26

Table 7. DS1287 w/ NVSRAM EISA or MCA Parts List (Figure 6)

Item	Quantity	Reference	Part
1	1	R1	10K
2	1	U1	DS1287 or bq3287
3	1	U2	DS1225Y or bq4010Y

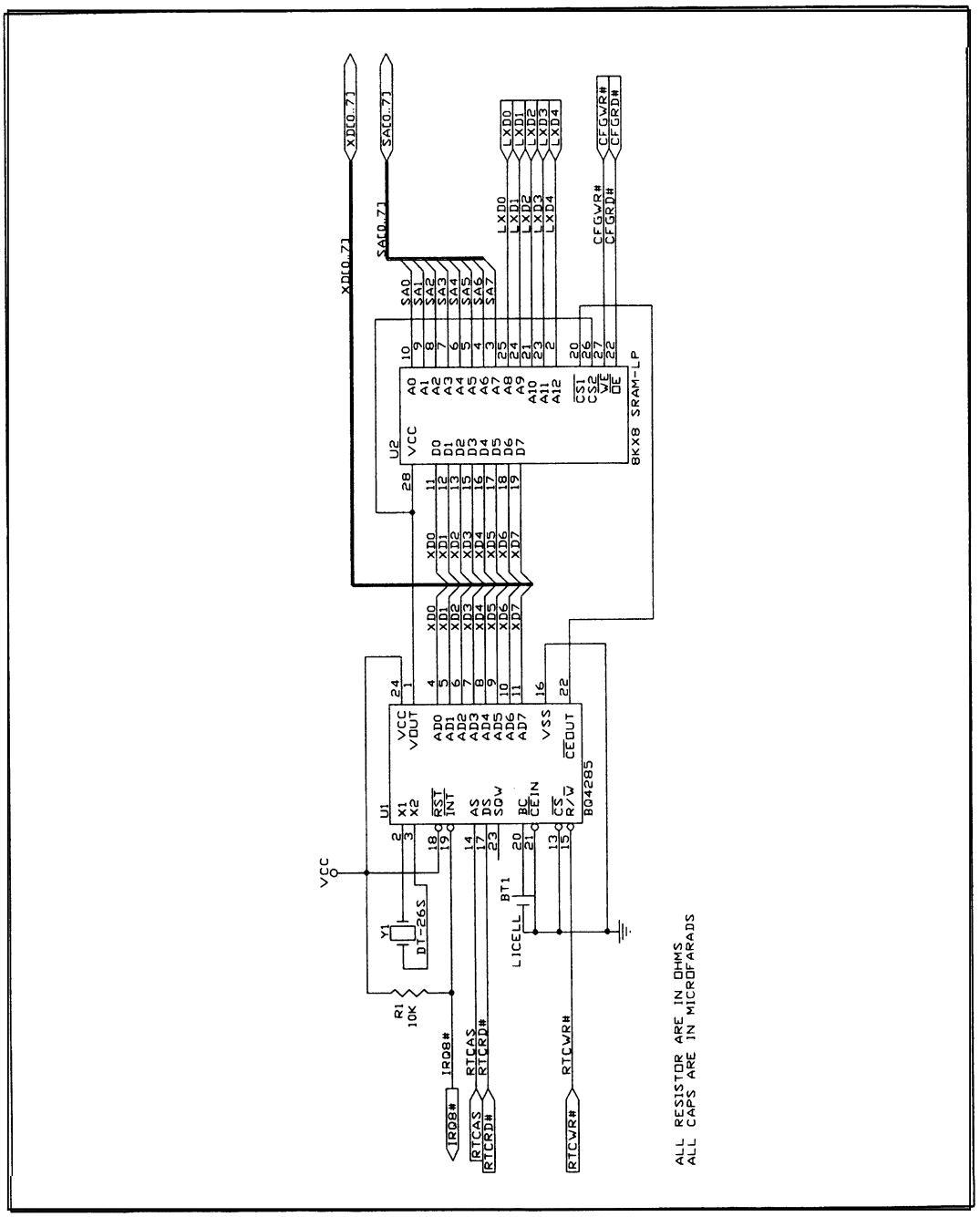


Figure 7. bq4285 EISA or MCA Example

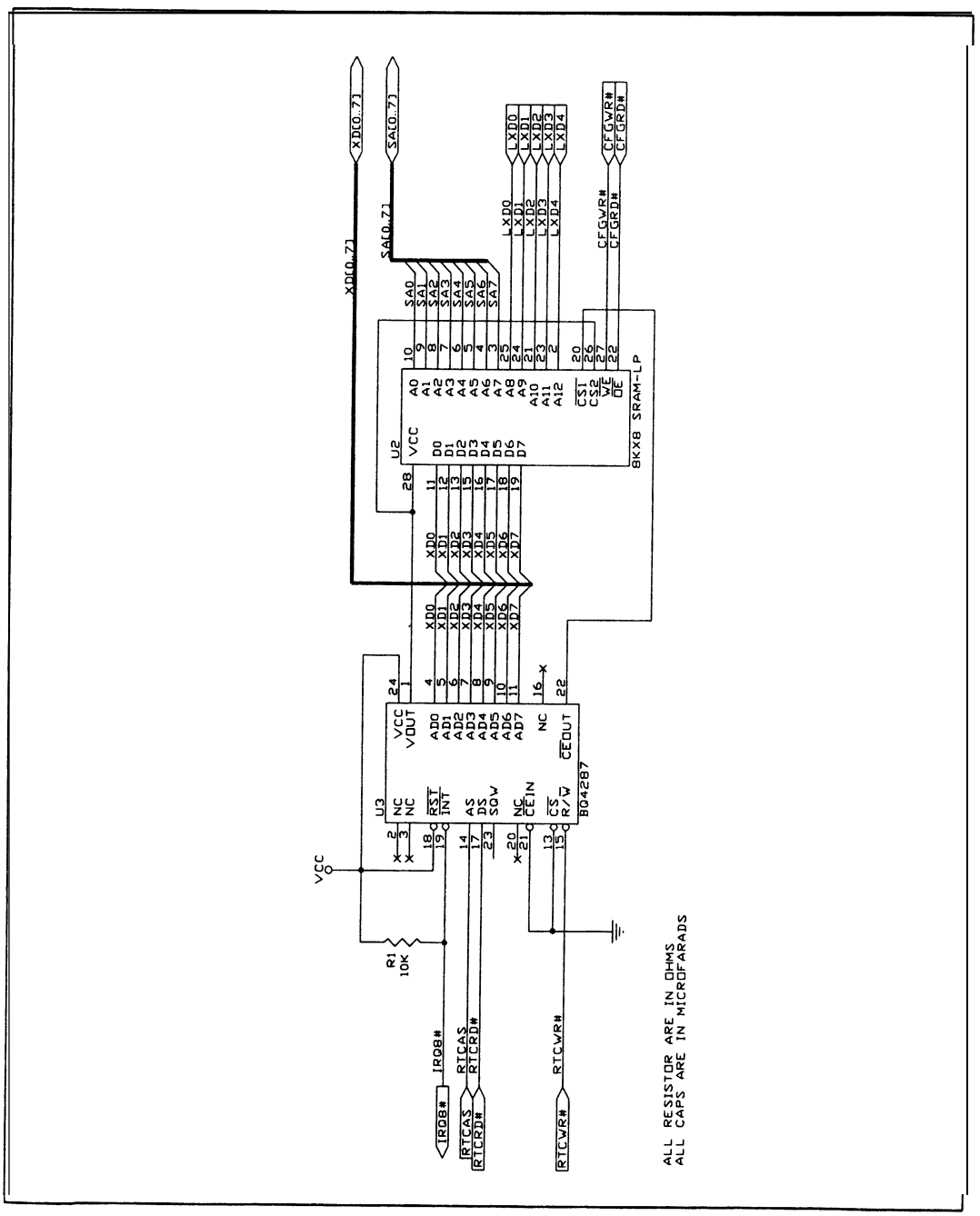


Figure 8. bq4287 EISA or MCA Example

5

Table 8. bq4285 EISA or MCA Parts List (Figure 7)

item	Quantity	Reference	Part
1	1	BT1	Li cell
2	1	R1	10K
3	1	U1	bq4285
4	1	U2	8Kx8 SRAM-LP
5	1	Y1	DT-26

Notes: Possible crystal/battery suppliers include:

- Daiwa DT-26 or equivalent crystal
- Rayovac/Panasonic lithium coin cells:

  BR1225 38–39mAh
  BR2032 180–200mAh
  BR2325 165–180mAh

  These cells and cells of other sizes are available 'tabbed' for soldering directly into boards. These types of lithium coin cells are safe for all modes of transportation per U.S. Department of Transportation records.

- Rayovac U.L. #MH12542
- Panasonic U.L. #MH12210

Table 9. bq4287 EISA or MCA Parts List (Figure 8)

Item	Quantity	Reference	Part
1	1	R1	10K
2	1	U2	8Kx8 SRAM-LP
3	1	U3	bq4287

BENCHMARQ Using RAM Clear Function With bq3285/bq3287A RTCs

Introduction

The RAM clear function is useful for resetting data in battery-backed CMOS RAM. This function can, however, be detrimental when inadvertently activated. When activated, the RAM clear function on the bq3285 and bq3287A RTCs sets the contents of the 114 (or 242) bytes of CMOS RAM to "FF" (hex).

Figure 1 shows the circuit configuration required to use the RAM clear function. The Benchmarq RTC uses the on-chip time-base oscillator to de-bounce the momentary switch, SW1, over a period of 100 ms. This requires that the time-base oecillator and the divider chain must be turned on by writing a 02 (hex) in bit locations OSC2–OSCO of register A. Although Figure 1 shows a momentary switch, an electronic signal can also be used with the same considerations.

All CMOS RAM locations are 'cleared' when the Benchmarq RTC senses a low-level pulse of at least 100ms on the RAM clear pin, $\overline{RCL}$, when V_{CC} = 5V.

Clearing RAM

Follow theee steps to clear RAM using the Benchmarq and Dallas Semiconductor RTCs:

1. Turn on the oecillator (this is a normal part of initialization when power is on).

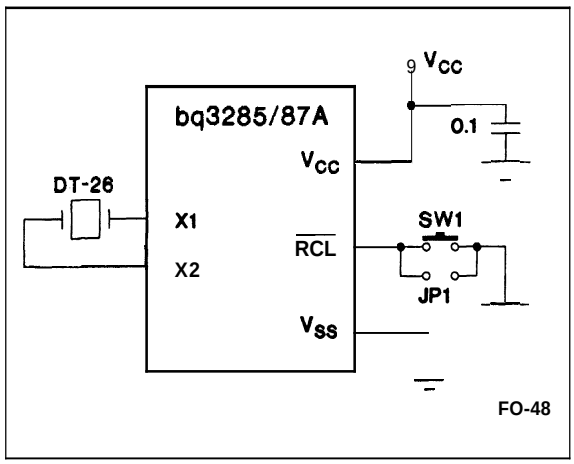


Figure 1. Recommended Hookup for RAM Clear Function

2. Clear the RAM: Jumper JP1.
3. Remove the JP1 jumper.

Implementation Differences

Although the hardware requirements for activating the Dallas Semiconductor RAM clear pin, $\overline{RCLR}$, are identical to those for activating the Benchmarq $\overline{RCL}$ pin, the function is implemented differently:

- Dallas Semiconductor's RAM clear function provides access to the internal lithium power source. *Shorting $\overline{RCLR}$ to ground drains the lithium cell.*
- Benchmarq's $\overline{RCL}$ pin is internally de-bounced (oscillator on).
- Benchmarq's $\overline{RCL}$ pin is active when power is on.

Benchmarq Advantages

The Benchmarq RTCs have the following advantages over the Dallas Semiconductor parts:

1. When the Dallas Semiconductor $\overline{RCLR}$ pin is exposed to any low-impedance path including metal trays, conductive bags, conductive foam, ground, etc., the battery will be drained. This may severely limit the battery life of the RTC. The battery in the Benchmarq RTC will not be drained.
2. The Dallas Semiconductor RTC is prone to inadvertent clearing of RAM while the system is off because the RAM clear function is active when power is not valid.
3. The de-bouncing capability of the Benchmarq RTC preventa inadvertent clearing of the CMOS RAM as a result of spurious noise on the $\overline{RCL}$ pin.

Notes

Time-Base Oscillator For RTC ICs

Introduction

The operation of the time-base oscillator is critical to the time-keeping functions of the bq3285, bq4285, and bq4845 series of Real-Time-Clocks. For simplicity, the term "RTC" refers to this product family.

This application note describes some basic characteristics of the piezoelectric crystal and the on-chip crystal oscillator circuitry designed into the RTC. This application note also includes suggestions for achieving time-keeping accuracy and circumventing oscillator start-up problems.

Time-Base Crystal

The RTC time-base oscillator is designed to work with an external piezoelectric 32.768kHz crystal. A crystal can be represented by its electrical equivalent circuit and associated parameters as shown in Figure 1 and Table 1, respectively.

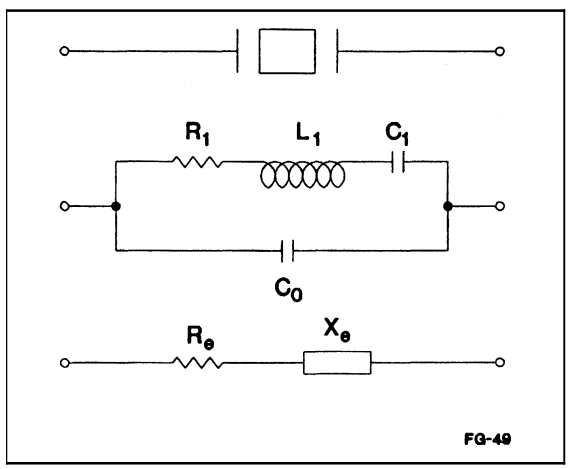


Figure 1. Equivalent Circuit of a Quartz Crystal

L_1, C_1, and R_1 are known as the motional arm of the circuit. L_1 is the motional inductance, C1 represents the motional capacitance of the quartz, and R_1 represents the equivalent motional arm resistance or series resistance. C_0 is the static or shunt capacitance and is the sum of the capacitance between electrodes and the capacitances added by the leads and mounting structure. The basic circuit can be resolved into equivalent resistive (R_e) and reactive (X_e) components.

Table 1. Crystal Parameters

Parameter	Symbol	Unit
Nominal frequency	F	kHz
Load capacitance	C_L	pF
Motional inductance	L_1	H
Motional capacitance	C_1	pF
Motional resistance	R_1	KΩ
Shunt capacitance	C_0	pF

Crystal Operating Mode

The equivalent crystal impedance varies with the frequency & oscillation. 2 and 3 show the variation of the equivalent reactance, X_e, with respect to frequency for KDS's DT-26 *crystal.* *Figure* 2 shows two points at which the crystal appears purely resistive (points at which X_e = 0). These points are defined as the series resonant (Fs) and anti-meonant (Fa) frequencies. Series

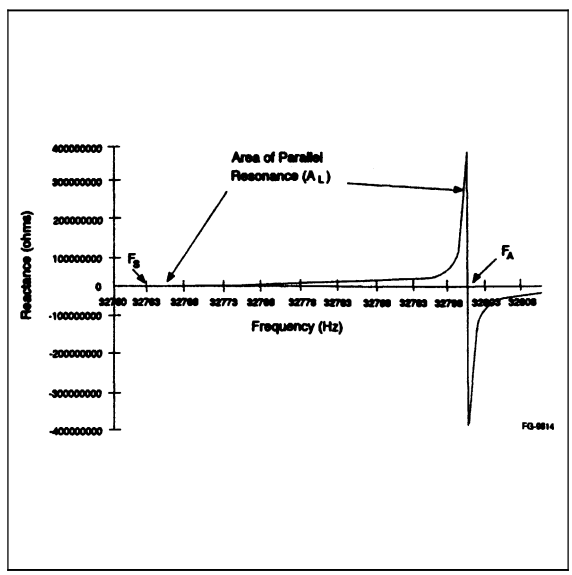


Figure 2. Variation of Reactance Around Resonance Points

resonant oecillator **circuits** are designed to oscillate at or near **Fs**. Parallel **resonant** circuits oscillate between Fs and Fa, depending upon the value of a parallel loading capacitor, C_L. The Benchmarq RTC **uses** a parallel resonant oscillator circuit.

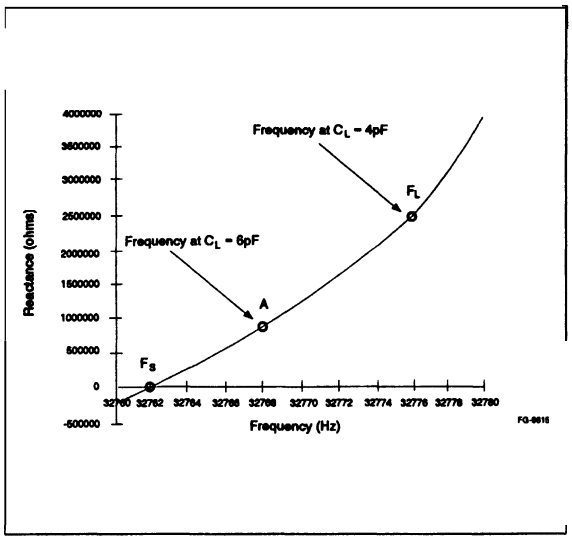


Figure 3. Detailed Area of Parallel Resonance

When a crystal is operating at parallel **resonance,** it **looks** inductive in a circuit (see Figure 4). Frequency will increase as load capacitance decreases. The load capacitance is the dynamic capacitance of the total circuit as measured or computed across the crystal terminals. In parallel circuit designs, the load capacitance should be selected to operate the crystal at a stable point on the Fs-Fa reactance curve as close to Fs as possible.

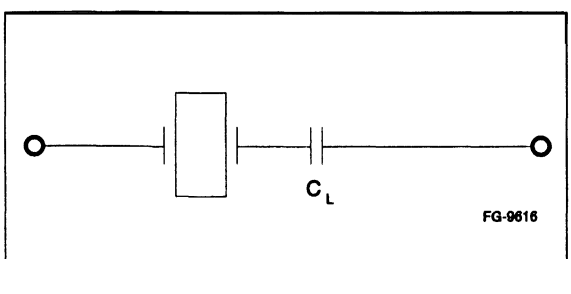


Figure 4. Parallel Resonance

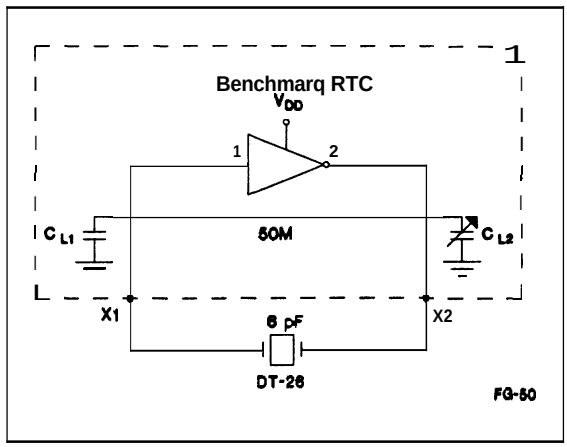


Figure 5. RTC Oscillator Circuit Block Diagram

Benchmarq RTC Oscillator

The parallel resonant RTC oecillator circuit **comprises** an **inverting** micro-power amplifier with a PI-type feedback network. Figure 5 **illustrates** a block diagram of the **oscillator** circuit with the crystal **as** part of the PI-feedback network. The oecillator ***circuit ensures*** that the crystal is operating in the area of parallel resonance **(A_L)** as shown in Figure **2.**

Again, the actual frequency at which the circuit will **oscillate** depends on the load capacitance, C_L. A parallel resonant crystal, such as the DT-26 with a specified C_L = **6pF,** is calibrated using a parallel resonant **circuit.** The approximate **expression** of the load capacitance, C_L, is computed from C_{L1} and C_{L2} as given below:

$$C_L \approx \frac{(C_{L1} * C_{L2})}{(C_{L1} + C_{L2})}$$

The **RTC** C_{L1} and C_{L2} **values** are trimmed to provide approximately a load capacitance of **6pF** *across* the *crystal* terminals, thus matching the specified load capacitance at which the crystal is calibrated to resonate at the nominal frequency of **32.768kHz. Referring** to the impedance curve of Figure **3,** 'A' indicates the point of resonance when C_L equals the specified load capacitance of the crystal.

Time-Keeping Accuracy

The RTC time-keeping accuracy **mostly** depends on the accuracy of the crystal, even though other **considerations** may affect it. The accuracy of the frequency of **oscillation** depends on the following:

- Crystal frequency tolerance
- Crystal frequency stability
- Crystalaging
- Effective load capacitance in oscillator circuit
- Board layout
- Drive level

Crystal Frequency Tolerance

The frequency tolerance parameter is the maximum frequency deviation from the nominal frequency (in this case, 32.768kHz) at a specified temperature, expressed in ppm of nominal frequency. The frequency tolerance, Δf/f, should typically be around ±20ppm at 25°C, which is the case for the Grade A, DT-26 crystal.

Crystal Frequency Stability

The maximum allowable deviation from nominal frequency over a specified range is the stability tolerance or temperature coefficient. This factor depends upon the angle of cut, the width/length ratio, the mode of vibration, and harmonics. This factor is normally expressed in terms of ppm or % of nominal frequency. Figure 6 shows a typical curve of frequency variation with temperature for the KDS DT-26 crystal.

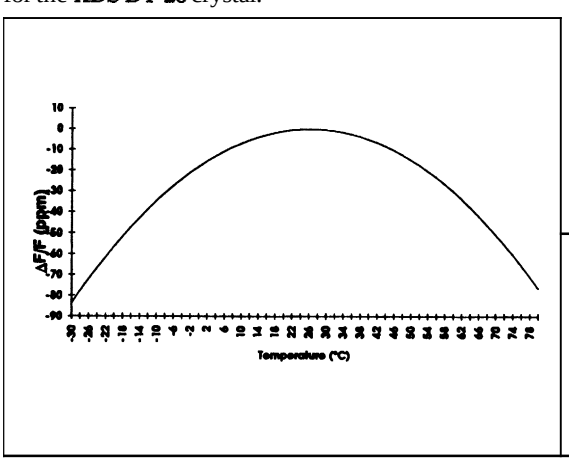


Figure 6. Typical Temperature Characteristics

Crystal Aging

Quartz crystal aging refers to the permanent change in operating frequency which occurs over time. The rate of change in frequency is fastest during the first 45 days of operation. Many factors affect aging, and the most common include the following: drive level, internal contamination, crystal surface change, ambient temperature, wire fatigue, and frictional wear. Drift with age is typically 4 ppm for the first year and 2 pprn per year for the life of the DT-26 crystal.

Load Capacitance

For a parallel remnant calibrated crystal, the crystal manufacturer specifies the bad capacitance at which the crystal will "parallel" resonate at the nominal frequency. As the graph in Figure 3 displays, increasing the effective load capacitance by hanging additional capacitors on either of the RTC's X_1 or X_2 pins will effectively lower the resonant frequency, point "A," toward Fs. The resonant frequency with load capacitance, % is given by the

$$F_L = F_S\left(1 + \frac{C_1}{2(C_0 + C_L)}\right)$$

where C_L is the effective load capacitance across the crystal inputs, which includes any stray capacitances.

Allowing for capacitance due to board layout traces leading to the X_1 and X_2 pins, the RTC oscillator circuit is trimmed internally to provide an effective load capacitance of less than 6pF. Therefore, if the X_1 and X_2 pine were bent up from the PCB traces and a crystal specified with a C_L of 6pF was soldered directly to these pins, the clock should oscillate approximately 40-50 ppm faster than the nominal frequency of 32.768kHz.

Load Capacitance Trimming

If the RTC clock is running faster than the nominal frequency, a small trim capacitor (preferably <8pF) should be placed from the X_2 pin to ground to move the remnant point closer to the nominal *frequency.* The graph of Figure 7 shows the variation of frequency with additional load capacitance on the RTC X_2 pin.

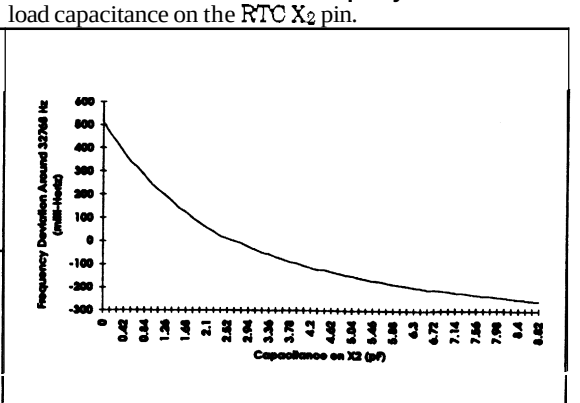


Figure 7. Frequency Variation Versus Load Capacitance

The trimming capacitors normally should be ceramic. Ideally, use a COG- or NPO-type of ceramic or a polyester film capacitor, as these are better suited for timing applications.

Here is a practical rule of thumb deriving from the data in Figure 7: for every additional 1.54pF capacitance on the X_2 pin, the frequency will decrease by 0.8Hz or a $\Delta f/f$ of -24.4 ppm around 32.768kHz.

Using Crystals with C_L other than 6pF

Sometimes, a crystal with a C_L specification other than 6pF is used, either because of availability or a stocking issue. Again, because Benchmarq's RTCs are trimmed for use with C_L = 6pF crystals, timing accuracy will most likely be outside ±20 ppm.

A popular alternative is a crystal with a C_L = 12.5pF. By using a crystal with this load capacitance specification, the RTC will resonate much closer to the anti-resonant frequency, Fa. Thus, a larger trim capacitor is necessary. Benchmarq suggests using a 10pF from the X_2 pin to ground in order to achieve ±30 ppm accuracy. Please take into consideration board trace capacitances.

Parallel trim capacitors can also be used, which would place the trim capacitor directly across the X_1, X_2 pins. Parallel trim capacitors, however, require an increased voltage on the BC pin to maintain oscillations in battery backup mode. Hence, Benchmarq still suggests using a trim capacitor from the X_2 pin to ground.

Table 2 represents typical data taken with a bq3285 using a KDS crystal with a C_L = 12.5pF and parallel trim capacitors. The leads were bent up, directly connecting the crystal to them, so a 2-3pF capacitor from both the X_1, X_2 pins to ground were added to simulate trace capacitances. The part was monitored by using an HP5370B Universal Time Interval Counter tied to the SQW output pin.

This data shows that a 6.8pF parallel trim capacitor has better ppm performance, but the oscillator was not sustained in battery back-up mode at the minimum battery voltage of 2.5V. Benchmarq suggests using a 4.7pF parallel trim capacitor if using a crystal with a C_L = 12.5pF.

Board Layout

Given the high-input impedance of the crystal input pins X_1 and X_2, take care to route high-speed switching signal traces away from them. Preferably use a ground-plane layer around the crystal area to isolate capacitive-coupling of high-frequency signals. The traces from the crystal leads to the X_1, X_2 pins must be kept short with minimal bends. A good rule of thumb is to keep the crystal traces within 5mm of the X_1, X_2 pins.

Table 2. Parallel Trim Capacitance Data

Cp	BC Voltage	pprn	Oscillator sustained	Start-up
6.8pF	2.1V	+7-10	No	Yes
	2.15V		No	Yes
	2.5V		No	Yes
	3.0V		Yea	Yes
4.7pF	<2.15V	+15-20	No	No
	2.15V		Yes	Yes
	2.5V		Yes	Yes
	3.0V		Yes	Yes

Notes:
1) Cp = Parallel trim capacitor
2) BC voltage = Voltage present on BC pin
3) pprn = pprn data
4) Osc. sustained = Oscillator running in battery backup mode?
5) Start-up = Did oscillator start up on power-up?

Finally, place a 0.1µF ceramic by-pass capacitor close to the RTC V_{CC} pin to provide an improved supply into the clock.

Drive Level

The drive level is the power dissipated through a crystal in an operating circuit. A drive level (measured in microwatts) which is too high or too low can cause undesirable effects. If the level is too high, it can cause the oscillator frequency to change, cause a fracture of the quartz element, or lead to a permanent shift in frequency output. If the drive level is too low, it can prevent oscillator function completely. Generally, keep the drive level at the minimum level required for high stability and adequate oscillator output. Benchmarq designs RTCs for minimum drive level for reduced power dissipation to achieve maximum battery life when oscillating in battery backup mode.

Measuring for Accuracy

When checking for clock accuracy, use either a scope or a universal time counter connected to the SQW output pin.

Do not place probes on the X_1 or X_2 pins to check for oscillations, as this action may load the crystal and reduce the output amplitude or prevent the oscillator from functioning.

Oscillator Start-up

Barring accuracy issues, the RTC will oscillate with any 32.768kHz crystal. When hooked to the X_1, X_2 pins in

certain configurations, however, passive components can lead to oscillator start-up problems through the following:

- Excessive loading on the crystal input pins Xi, X_2.

  Table 2 shows a 6.8pF parallel trim cap trimming in a 12.5pF C_L crystal. The 6.8pF trim cap provides for better ppm accuracy, but the oscillator will not oscillate in battery backup mode with the minimum battery voltage of 2.5V, even though the oscillator will start-up upon power-up.

- Use of a resistive feedback element across the crystal.

  Benchmarq builds the feedback element into the RTC for start-up, so no resistive feedback external to the part is required.

Also, for start-up, a voltage within the V_{BC} voltage range must be present on the BC pin upon power-up for the oscillator to start-up. This voltage provides biasing to the oscillator circuit for operation.

Figure 8 shows "good" and "bad" circuit configurations for the RTC oscillator.

References

1. **KDS** America, ***Quartz Crystals and Oscillators User's Guide***
2. **Eaton, S. S.**, ***Timekeeping Advances Through COS/MOS Technology, RCA*** Application Note **ICAN 6086**.

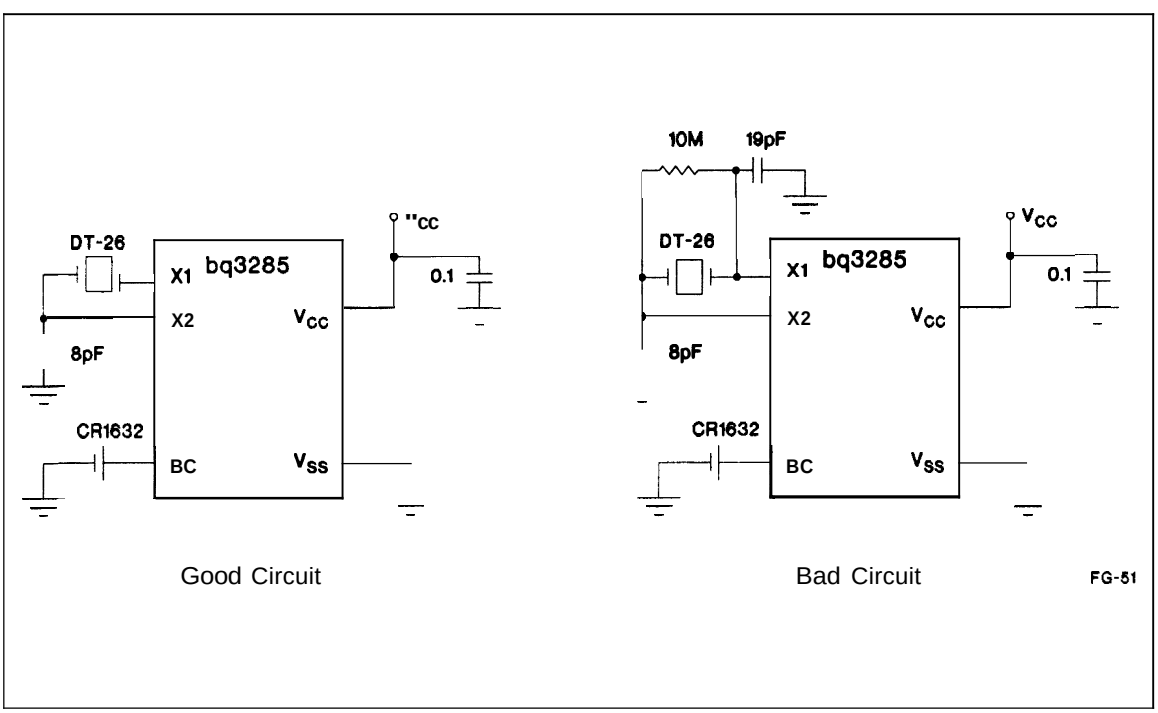


Figure 8. Typical Crystal Hookup Circuits

Suggested Crystals and Manufacturers

Here are a few suggestions for 32.768kHz crystals for use with Benchmarq RTCs:

Item		Symbol	KDS DT-26	Epson C-002RX	Epson MC-306	Epson MC-405/406
Frequency range		f	32.768kHz			
Temperature range	Storage	T_{STG}	-30°C to +70°C	-10°C to +60°C	-55°C to +125°C	-55°C to +125°C
	Operating	T_{OPR}	-lO°C to +60°C	-10°C to +60°C	-40°C to +85°C	-40°C to +85°C
Maximum drive level		GL	1.0µW			
Soldering condition		T_{SOL}	240°C-250°C 10s maximum	under 280°C within 5s	under 230°C within 3 min.	under 230°C within 3 min.
Frequency tolerance		Δf/f	Grade A: ±20 ppm Grade B: ±30 ppm	±20 ppm	±20 ppm or ±50 ppm	±20 ppm or ±50 ppm
Peak temperature (frequency)		θT	25°C ± 5°C			
Temperature coefficient (freq.)		a	-0.04 ppm / $°C^2$ max.			
Load capacitance		C_L	6pF (please specify)			
Series resistance		R_1	45kΩ max.	50kΩ max.	50kΩ max.	50kΩ max.
Motional capacitance		C_1	2.6fF typ.	2.0fF typ.	1.8fF typ.	2.0fF typ.
Shunt capacitance		C_0	1.1pF typ.	0.8pF typ.	0.9pF typ.	0.85pF typ.
Insulation resistance		IR	500MΩ min.			
Aging		fa	-	±5 ppm/year max.	±3 ppm/year max.	±3 ppm/year max.
Shock resistance		S.R.	±3 ppm max.	±5 ppm max.	±5 ppm max.	±5 ppm max.
Package type			cylinder	cylinder	SOIC	SOIC

KDS America
10901 Granada Lane
Overland Park, Kansas 66211
Tel: (913) 491-6825
Fax: (913) 491-6812

Epson America, Inc.
20770 Madrona Avenue
P.O. Box 2842
Torrance, California 90509-2842
Tel: (310) 787-6300
Fax: (310) 782-5320

Epson Korea, Inc.
IOF. KLI 63 Building
60 Yoido-Dong Youngdeungpo-Ku
Seoul, Korea
Tel: (02) 784-6027
Fax: (02) 784-0087

Epson Taiwan, Inc.
10 F, No. 287, Nanking E. Road
Sec. 3, Taipei, Taiwan, ROC
Tel: (02) 717-7360
Fax: (02) 718-9366

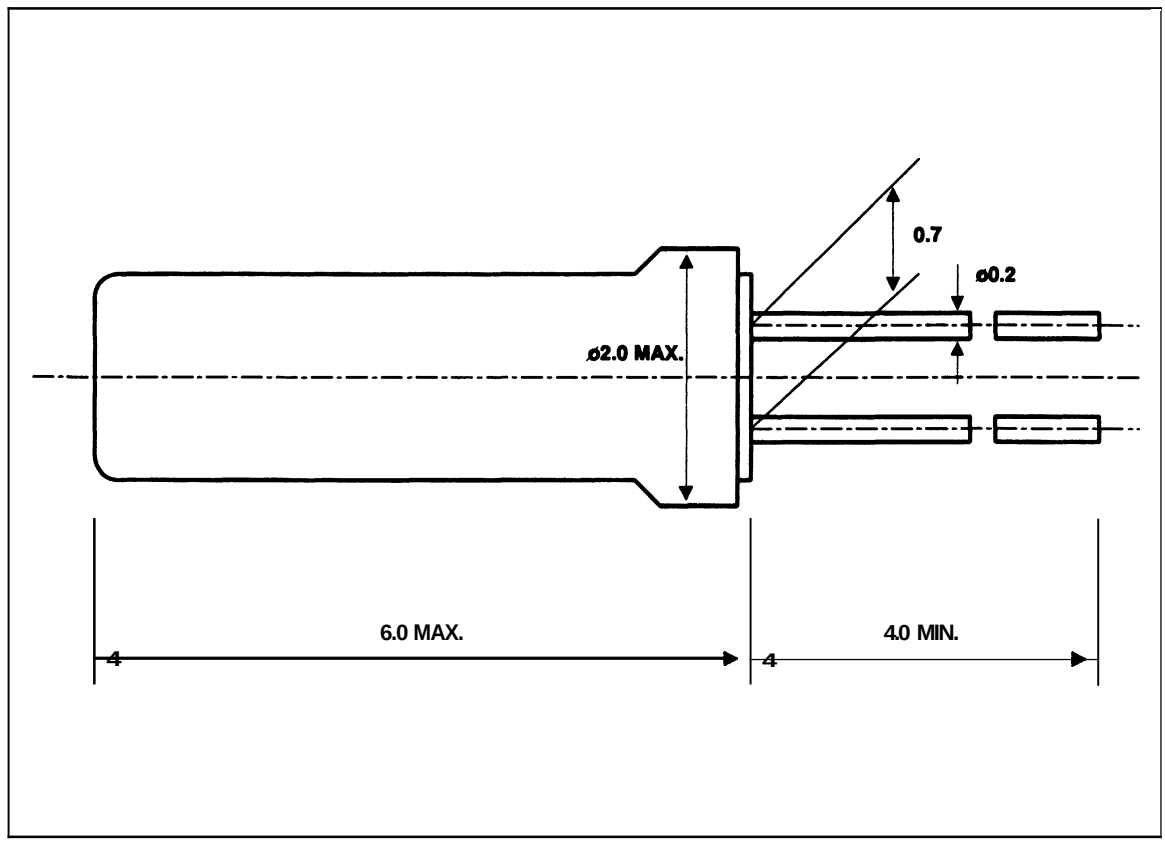
Epson Hong Kong Limited
20/F Harbour Centre
25 Harbour Road
Wancha, Hong Kong
Tel: (852) 2585-4600
Fax: (852) 2827-4346,2152

Epson Singapore PTE LTD
No. 1 Raffles Place
OUB Centre #25-00
Singapore 048616
Tel: 5330477
Fax: 5345109

External Dimensions

- DT-26, C-002RX

(Unit : *mm)*

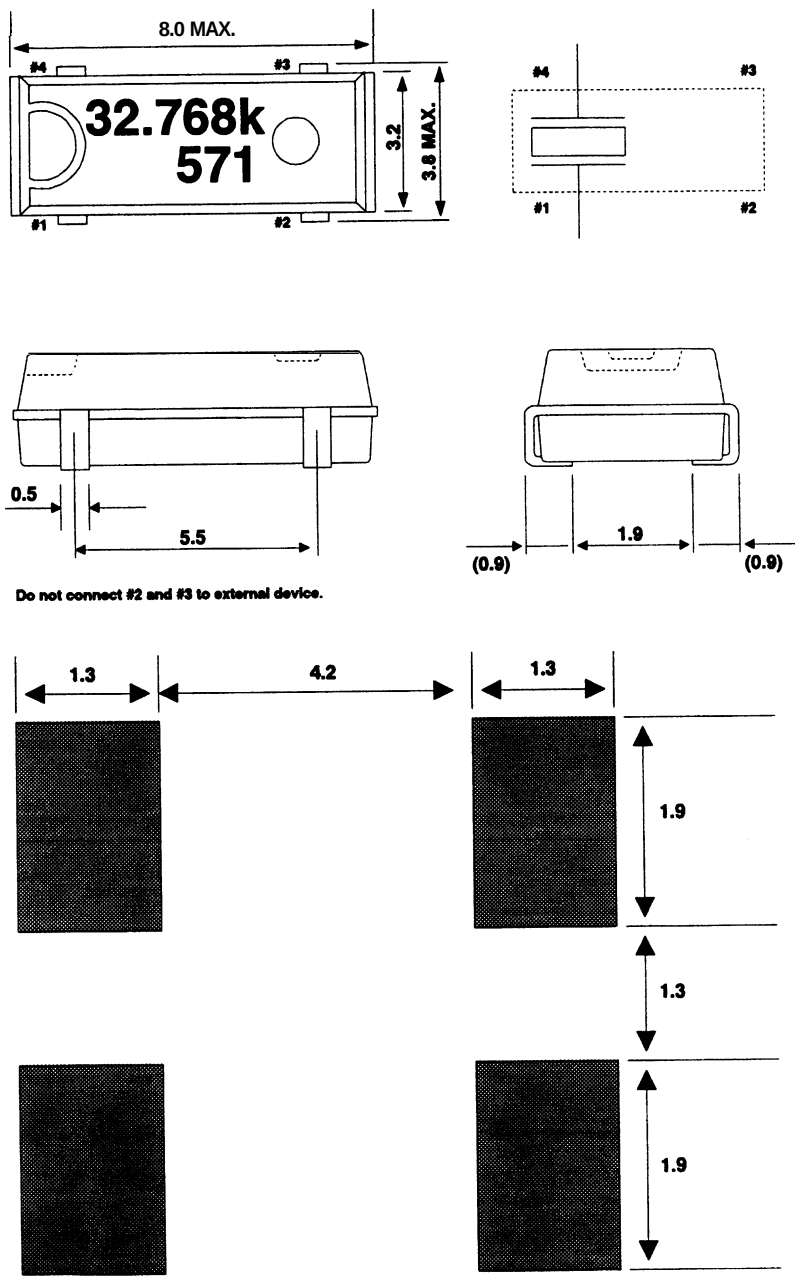


5

External Dimensions and Soldering Patterns

■ MC-306

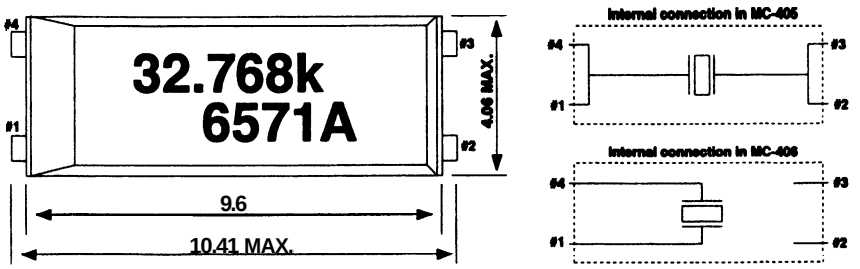
(Unit : mm)

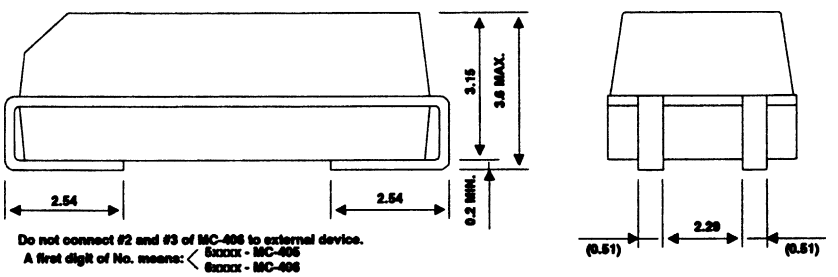


External Dimensions and Soldering Patterns

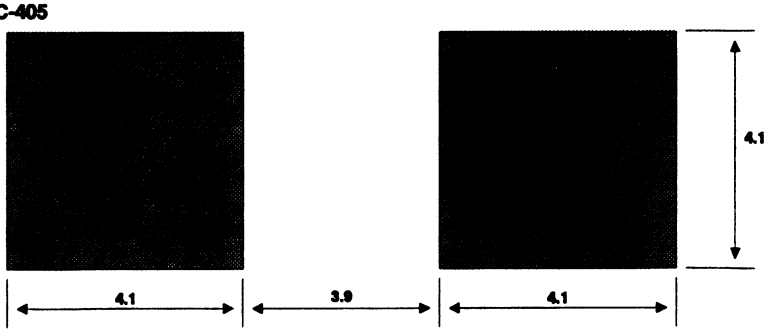
■ MC-405/406

(Unit : mm)

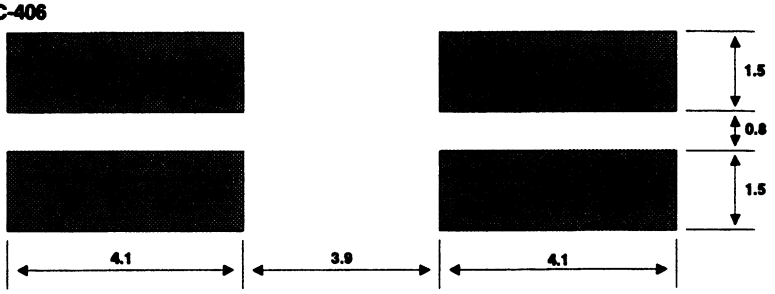




MC-405



MC-406



5

Notes

Using the bq3285/7E in a Green or Portable Environment

Introduction

The bq3285/7E Real-Time Clock is a PC/AT-compatible real-time clock that incorporates three enhanced features to facilitate power management in Green desktop or portable computers:

- 32kHz output
- 128 extra bytes of CMOS nonvolatile SRAM
- Alarm interrupt active in battery-backup mode

The 32kHz output provides a clock signal for power management timers and DRAM refresh control in power-sensitive systems. The output must be enabled with software and appears on the SQW pin.

Most RTCs and chip sets on the market have 114 bytes of general-purpose CMOS RAM. The bq3285/7E adds 128 additional bytes of memory to give the designer and user greater flexibility in defining system configuration settings. The added CMOS RAM is paged to by asserting the EXTRAM pin on the bq3285/7E. It can be used to store power management time-out settings, plug-and-play configuration data, or additional chip set parameters.

The bq3285/7E allows the alarm interrupt from the real-time clock to be active when no power is applied to the part. This enables a properly designed system to be programmed to "wake-up" from a power-off state and perform a function, minimizing the system on time.

32.768kHz Output

The bq3285/7E can be configured to generate a buffered 32.768kHz output on the SQW pin. This signal can be used as a timebase for system timers in a power management environment and as a clock reference for DRAM refresh.

In a Green or portable system, a number of timers are needed to track system and peripheral activity in order to enter different power states and turn off peripherals like hard drives and monitors. For example, a power-managed system may require countdown power state timers to transition the computer from full operation to doze, standby, and suspend states. Peripheral timers may be needed to count how long each peripheral has been inactive. Some chip sets allow the DRAM refresh rate to be slowed to rates based on the 32kHz timer when in suspended states. The power management controller (PMC) on the core logic takes the timer inputs and minimizes system power consumption by generating the appropriate control signals to the rest of the system.

Enabling the 32.768kHz Output

The 32.768kHz output is only available when Vcc to the RTC is valid (5V ± 10%). The following settings in the control registers A, B, and C enable the 32.768kHz output onto the SQW pin.

1. *Set* the Register A OS2–OS0 bits as shown:
2. *Set* the Register B SQWE bit as shown:

Register A Bits							
7	6	5	4	3	2	1	0
UIP	OS2	OS1	OS0	Rs3	Rs2	RS1	Rso
-	0	1	1	-	-	-	-

3. Set the Register C 32KE bit as shown:

Register B Bits							
7	6	5	4	3	2	1	0
UTI	PIE	AIE	UIE	SQWE	HF	DSE	RS0
-	-	-	-	1	-	-	-

The above settings do not affect the periodic interrupt

Register C Bits							
7	6	5	4	3	2	1	0
INTF	PF	AF	UF	0	32KE	0	0
					1	-	

rate or other time-keeping functions.

Disabling the 32.768kHz Output

The 32.768kHz output is disabled under the following conditions.

1. Clearing either of the SQWE/32KE bits or the OS1/OS0 bits in the above registers.
2. Asserting the $\overline{RST}$ pin low.
3. Putting the device in battery-backup mode ($V_{CC} < V_{BC}$).

Extra CMOS NVSRAM

Because bit 7 at I/O port address 70H in a PC/AT environment is the NMI, additional I/O ports are needed to access the extra 128 bytes of CMOS RAM. The following table shows the I/O ports used by the PC/AT BIOS to access CMOS RAM. Note the CMOS RAM includes the RTC information in the uppermost 14 locations.

I/O Address	Read/ Write	Description
070H	W	CMOS RAM address register port, where: Bit 7 = 1; NMI disabled = 0; NMI enabled Bits 6–0 = Register and CMOS RAM address
071H	R/W	CMOS RAM data register port
074H	W	Extended CMOS RAM address register port, least-significant byte
075H	W	Extended CMOS RAM address register port, most-significant byte
076H	R/W	Extended CMOS RAM data register port

The two CMOS RAM data areas are shown below.

Data Area	I/O Locations	Size (bytes)	Description
Default CMOS Data Area	070H and 071H	Default: 64 Maximum: 128	All BIOS variations use this area to store RTC, POST, and system configuration data.
Extended CMOS RAM Data Area	074H, 075H, and	Default: 2K Maximum: 64K	The PS/2 uses this area to store POS data. The Intel SL uses 074H and 076H to provide 'extended' 128 CMOS RAM bytes for APM data.

The EXTRAM pin controls access to the extra 128 bytes of memory on the bq3285/7E. The EXTRAM signal can be generated in two ways:

1. Hook up SA3, SA2, or SA1 from the ISA address bus to the EXTRAM pin. The address/data ports through which the 'extra' 128 bytes are accessed depend on which address line is used, as shown in the following table.

Address Line	I/O Ports	Read/ Write	Description
SA3	078H	W	Extra CMOS RAM address register port, where: Bit 7 = Reserved Bits 6–0 = Extra CMOS RAM address
SA3	079H	R/W	Extra CMOS RAM data register port
SA2	074H	W	Same as 078H
SA2	075H	R/W	Same as 079H
SA1	072H	W	Same as 078H
SA1	073H	R/W	Same as 079H

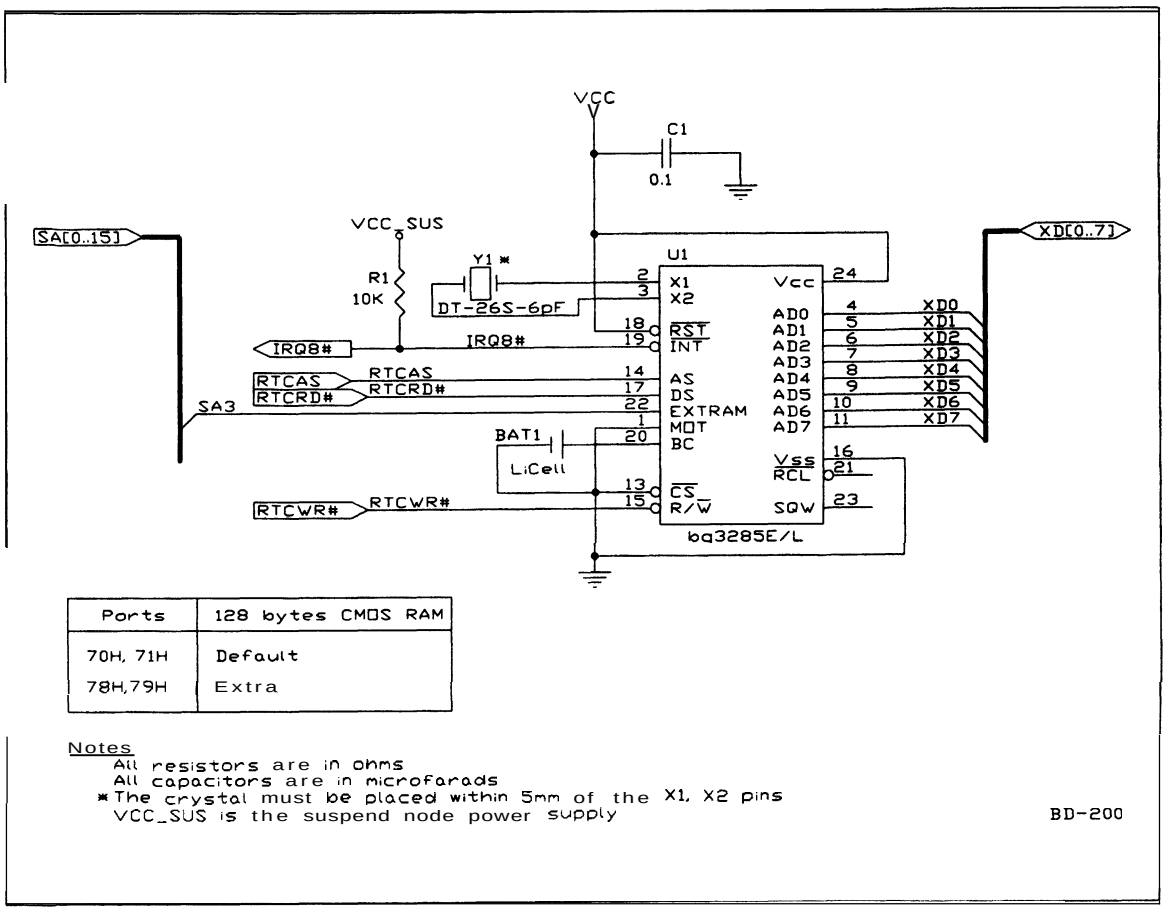
   Any one of the above I/O port pains that asserts RTC control signal AS, DS, or $\overline{WR}$ should be selected.

2. Hook up an unused general-purpose I/O port pin to EXTRAM pin. When this pin is asserted high on a write to the assigned I/O port, successive accesses to port 070H and 071H are directed to the extra 128-byte RAM bank.

Refer to Figure 1 for a diagram of a complete PC/AT interface.

Alarm Interrupt

The alarm interrupt on the bq3285/7E functions with or without V_{CC} power. It can be used in a power-managed system to wake the system up from suspend mode or turn the system or parts of the system on from the power-off mode. In suspend mode, most of the computer is shut down except for the power management controller and the DRAM. The PMC needs an interrupt from a push-button resume switch, an incoming modem ring, or the RTC to resume operation. The bq3285/7E RTC can either be left on or turned off during suspend mode depending on the level of functionality required. In 0V suspend mode, the 32kHz output may not be needed because all the DRAM information is stored to disk and refresh is not required. In this case, the bq3285/7E can be powered



Ports	128 bytes CMOS RAM
70H, 71H	Default
78H,79H	Extra

Notes
All resistors are in ohms
All capacitors are in microfarads
* The crystal must be placed within 5mm of the X1, X2 pins
VCC_SUS is the suspend node power supply

BD-200

Figure 1. bq3285/7E PC/AT Design Example

off during suspend and still be able to supply the alarm interrupt to the power management controller. In 3V/5V suspend where the DRAM is kept alive, the bq3285/7E should be in the powered-up mode. This has little impact on power consumption, however, because the bq3285/7E has low standby current when deselected.

The bq3285/7E can be also be used to turn a system on from the power-off mode for periods of short duration. Figure 2 shows how this could be implemented. The $\overline{INT}$ pin alerts the power management controller, which in turn activates a p-FET to turn on the necessary subsystems to perform the required function. After completion of the task, the system shuts down except for the power management controller.

PC/AT Environment

Most advanced power-managed chip sets have a direct input for a 32kHz signal. A common way of generating this signal is to use a CMOS buffered inverter like the MC14069 with a 32.768kHz quartz crystal and R-C components. The bq3285/7E contains its own built-in 32.768kHz quartz crystal for the real-time clock oscillator. To eliminate redundancy and component count, the 32kHz output on the bq3285/7E SQW pin can be used in place of the MC14069, external crystal, and other passive components. The SQW pin has not been used in PC/AT designs in the past, so using it for this function does not impact other aspects of the motherboard design.

Figure 3 shows a real-time clock and timer generation using the MC146818A and the MC14069 in conjunction with Green core logic chips. Figure 4 shows the much simplified bq3285/7E design using the 32kHz output on the SQW pin and the extra NVSRAM enabled. Ports 70H and 71H address the upper 128 bytes of CMOS RAM including the RTC information. Ports 78H and 79H address the extra 128 bytes of CMOS RAM.

From a software standpoint, the PC BIOS must incorporate the appropriate routine to enable the 32kHz output and use the extra NVSRAM. The 32kHz enable routine should be placed as part of the system cold-boot initialization procedure.

Other Considerations

If the height of the bq3285/7E DIP module is an issue in portable designs, the part is also available in a 300-mil SOIC and a 150-mil SSOP (bq3285ES and bq3285ESS). Both variations provide direct connections for an external crystal and battery. The devices are also available with 3V Vcc operation (bq3285LS and bq3285LSS) for use in 3V systems.

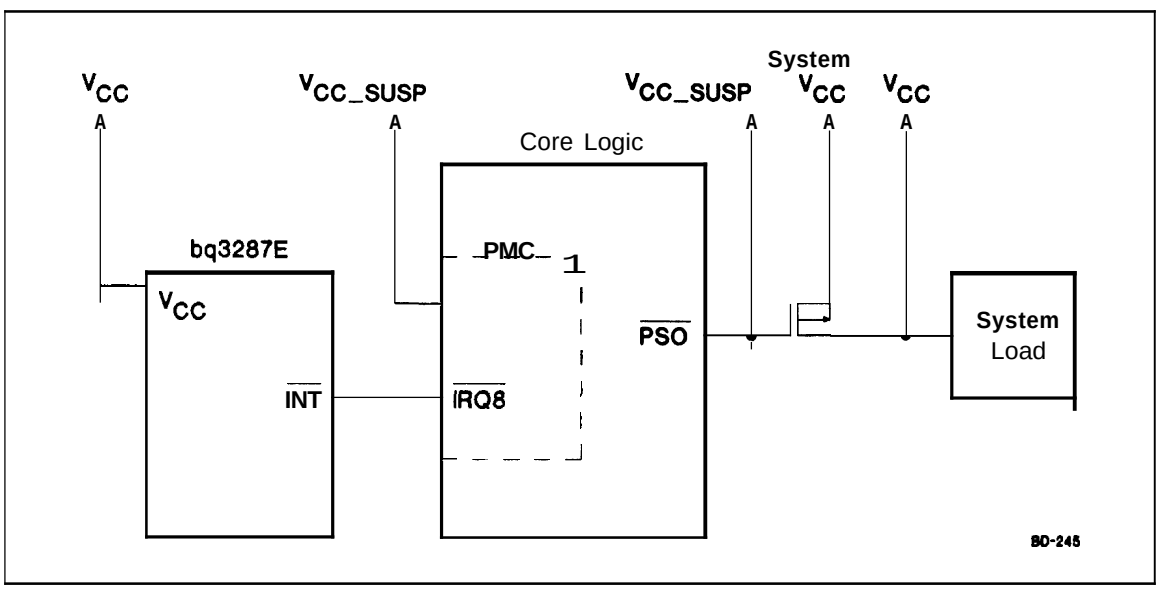


Figure 2. System Wake-up Alarm

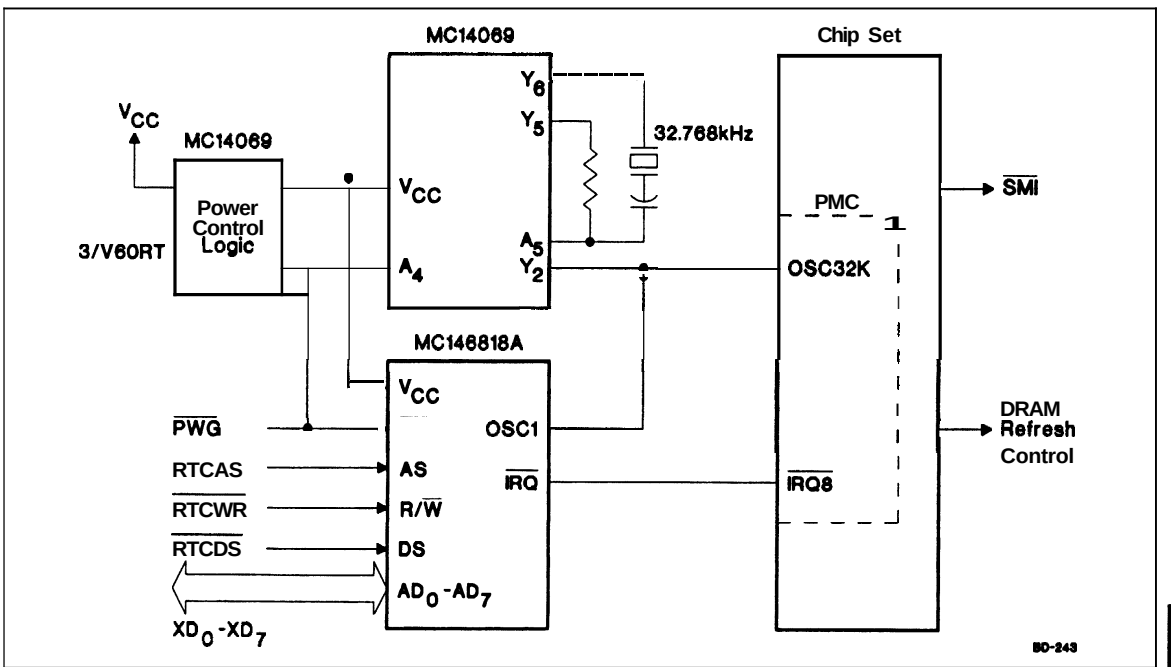


Figure 3. MC14069 Implementation

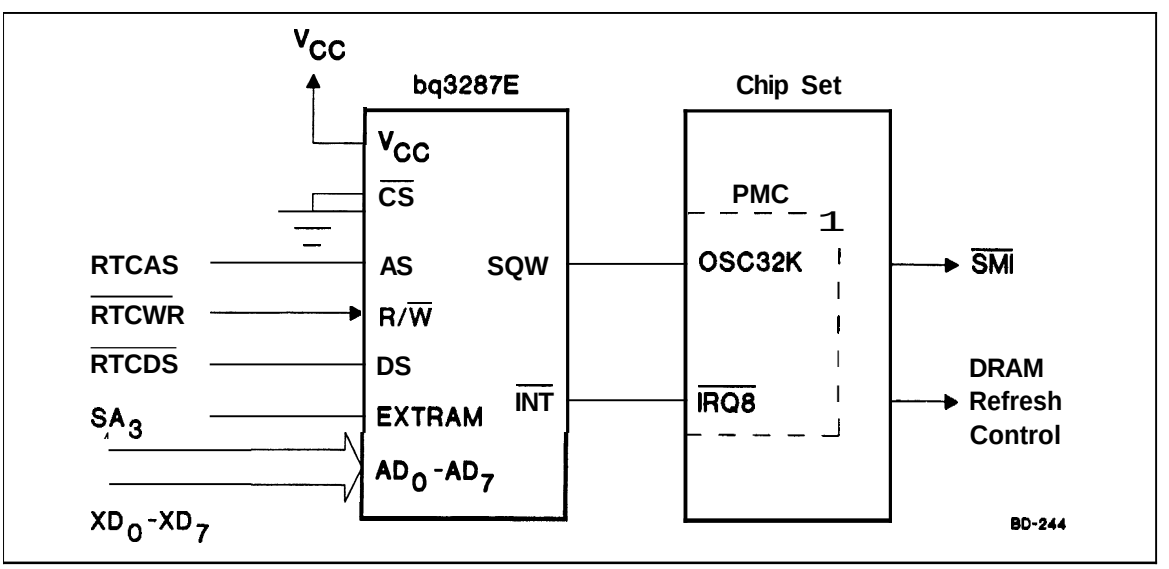


Figure 4. bq3285/7E Implementation

Notes

bq4010/bq4010Y

8Kx8 Nonvolatile SRAM

Features

- Data retention in the absence of power
- Automatic write-protection during power-up/power-down cycles
- Industry-standard 28-pin 8K x 8 pinout
- Conventional SRAM operation; unlimited write cycles
- 10-year minimum data retention in absence of power
- Battery internally isolated until power is applied

General Description

The CMOS bq4010 is a nonvolatile 65,536-bit static RAM organized as 8,192 words by 8 bite. The integral control circuitry and lithium energy source provide reliable nonvolatility coupled with the unlimited write cycles of standard SRAM.

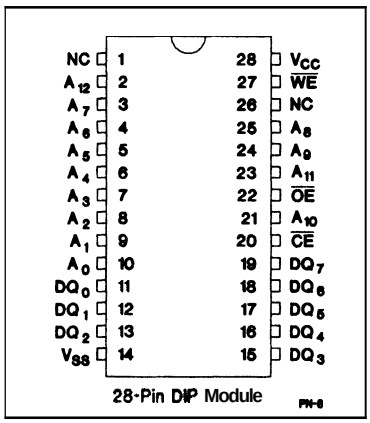
The control circuitry constantly monitors the single 5V supply for an out-of-tolerance condition. When Vcc falls out of tolerance, the SRAM is unconditionally write-protected to prevent inadvertent write operation.

At this time the integral energy source is switched on to sustain the memory until after Vcc returns valid.

The bq4010 uses an extremely low standby current CMOS SRAM, coupled with a small lithium coin cell to provide nonvolatility without long write-cycle timer, and the write-cycle limitations associated with EEPROM.

The bq4010 requires no external circuitry and is socket-compatible with industry-standard SRAMs and most EPROMs and EEPROMs.

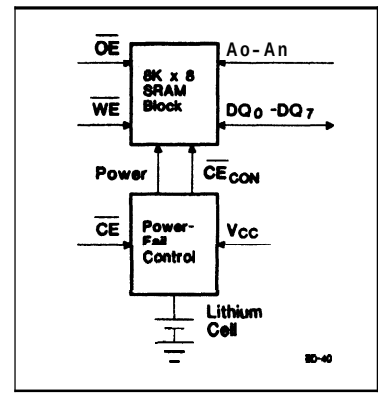
Pin Connections



Pin Names

$A_0 - A_{12}$	Address inputs
$DQ_0 - DQ_7$	Data input/output
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable *input*
$\overline{WE}$	Write enable input
NC	No connect
VCC	+5 volt supply input
VSS	Ground

Block Diagram



Selection Guide

Part Number	Maximum Access Time (ns)	Negative Supply Tolerance	Part Number	Maximum Access Time (ns)	Negative Supply Tolerance
			bq4010Y -70	70	-10%
bq4010 -85	85	-5%	bq4010Y -85	85	-10%
bq4010 -150	150	-5%	bq4010Y -150	150	-10%
bq4010 -200	200	-5%	bq4010Y -200	200	-10%

Functional Description

When power is valid, the bq4010 operates as a standard CMOS SRAM. During power-down and power-up cycles, the bq4010 acts as a nonvolatile memory, automatically protecting and preserving the memory contents.

Power-down/power-up control circuitry constantly monitors the V_{CC} supply for a power-fail-detect threshold V_{PFD}. The bq4010 monitors for V_{PFD} = 4.62V typical for use in systems with 5% supply tolerance. The bq4010Y monitors for V_{PFD} = 4.37V typical for use in systems with 10% supply tolerance.

When V_{CC} falls below the V_{PFD} threshold, the SRAM automatically write-protects the data. All outputs become high impedance, and all inputs are treated as 'don't care." If a valid access is in process at the time of power-fail detection, the memory cycle continues to completion. If the memory cycle fails to terminate within time t_{WPT}, write-protection takes place.

As V_{CC} falls past V_{PFD} and approaches 3V, the control circuitry switches to the internal lithium backup supply, which provides data retention until valid V_{CC} is applied.

When Vcc returns to a level above the internal backup cell voltage, the supply is switched back to V_{CC}. After Vcc ramps above the V_{PFD} threshold, write-protection continues for a time t_{CER} (120ms maximum) to allow for processor stabilization. Normal memory operation may resume after this time.

The internal coin cell used by the bq4010 has an extremely long shelf life and provides data retention for more than 10 years in the absence of system power.

As shipped from Benchmarq, the integral lithium cell is electrically isolated from the memory. (Self-&charge in this condition is approximately 0.5% per year.) Following the f i t application of Vcc, this isolation is broken, and the lithium backup cell provides data retention on subsequent power-downs.

Truth Table

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Operation	Power
Not selected	H	X	X	High Z	Standby
Output disable	L	H	H	High Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding Vcc relative to V_{SS}	-0.3 to 7.0	V	$V_T \le V_{CC}$ + 0.3
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
		-40 to +85	°C	Industrial "N"
T_{STG}	Storage temperature	-40 to +70	°C	Commercial
		-40 to +85	°C	Industrial "N"
T_{BIAS}	Temperature under bias	-10 to +70	°C	Commercial
		-40 to +85	°C	Industrial "N"
T_{SOLDER}	Soldering temperature	+260	°C	For 10 seconds

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions (T_A = TOPR)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	bq4010Y/bq4010Y-xxxN
		4.75	5.0	5.5	V	bq4010
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3		0.8	V	
V_{IH}	Input high voltage	2.2		Vcc + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C.

DC Electrical Characteristics (T_A = TOPR, $V_{CCmin} \le V_{CC} \le V_{CCmax}$)

Symbd	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current			± 1	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output leakage current			± 1		$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}
V_{OH}	Output high voltage	2.4			V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage			0.4	V	I_{OL} = 2.1 mA
I_{SB1}	Standby supply current		4	7	mA	$\overline{CE}$ = V_{IH}
I_{SB2}	Standby supply current		2.5	4		$\overline{CE} \ge V_{CC}$ - 0.2V, $0V \le V_{IN} \le 0.2V$, or $V_{IN} \ge V_{CC}$ - 0.2V
I_{CC}	Operating supply current		65	75	mA	$\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0 at 100%,
V_{PFD}	Power-fail-detect voltage	4.55	4.62	4.75	V	bq4010
		4.30	4.37	4.50	V	bq4010Y
V_{SO}	Supply switch-over voltage		3		V	

Note: Typical values indicate operation at T_A = 25°C, Vcc = 5V.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance			10	pF	Output voltage = 0V
C_{IN}	Input capacitance			10	pF	Input voltage = 0V

Note: These parameters are sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 1 and 2

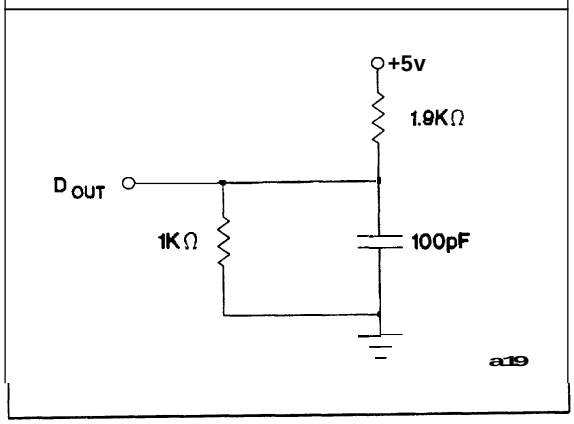


Figure 1. Output Load A

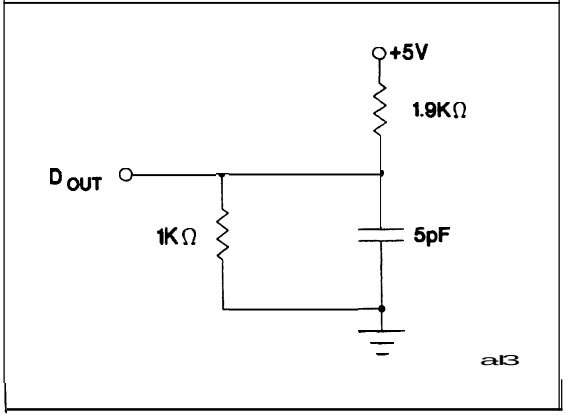
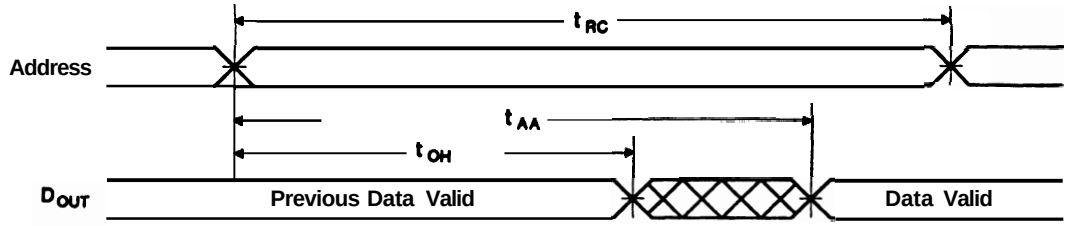


Figure 2. Output Load B

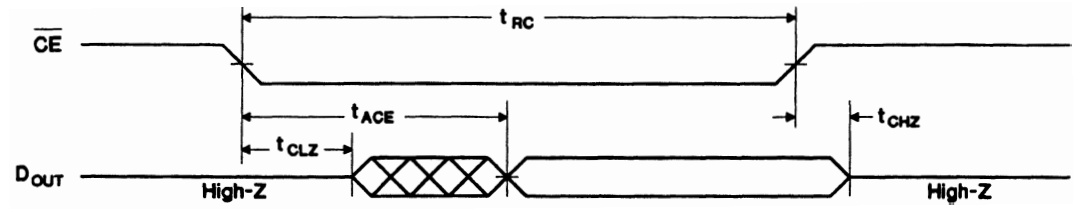
Read Cycle (TA = TOPR, VCCmin ≤ VCC ≤ VCCmax)

Symbol	Parameter	-70/-70N		-85/-85N		-150/-150N		-200		Unit	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read cycle time	70	-	85	-	150	-	200	-	ns	
t_{AA}	Address access time	-	70	-	85	-	150	-	200	ns	Output load A
t_{ACE}	Chip enable access time	-	70	-	85	-	150	-	200	ns	Output load A
t_{OE}	Output enable to output valid	-	35	-	45	-	70	-	90	ns	Output load A
t_{CLZ}	Chip enable to output in low Z	5	-	5	-	10	-	10	-	ns	Output load B
t_{OLZ}	Output enable to output in low Z	5	-	5	-	5	-	5	-	ns	Output load B
t_{CHZ}	Chip disable to output in high Z	0	25	0	40	0	60	0	70	ns	Output load B
t_{OHZ}	Output disable to output in high Z	0	25	0	30	0	50	0	70	ns	Output load B
t_{OH}	Output hold from address change	10	-	10	-	10	-	10.	-	ns	Output load A

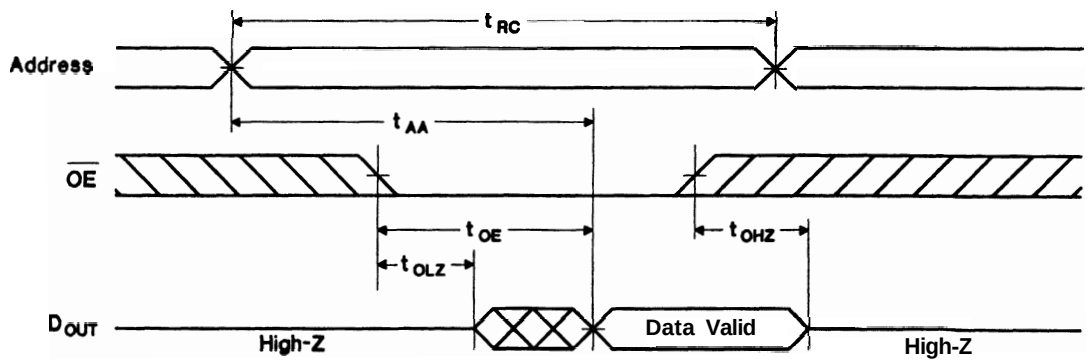
Read Cycle No. 1 (Address Access) [1,2]



Read Cycle No. 2 ($\overline{CE}$ Access) [1,3,4]



Read Cycle No. 3 ($\overline{OE}$ Access)



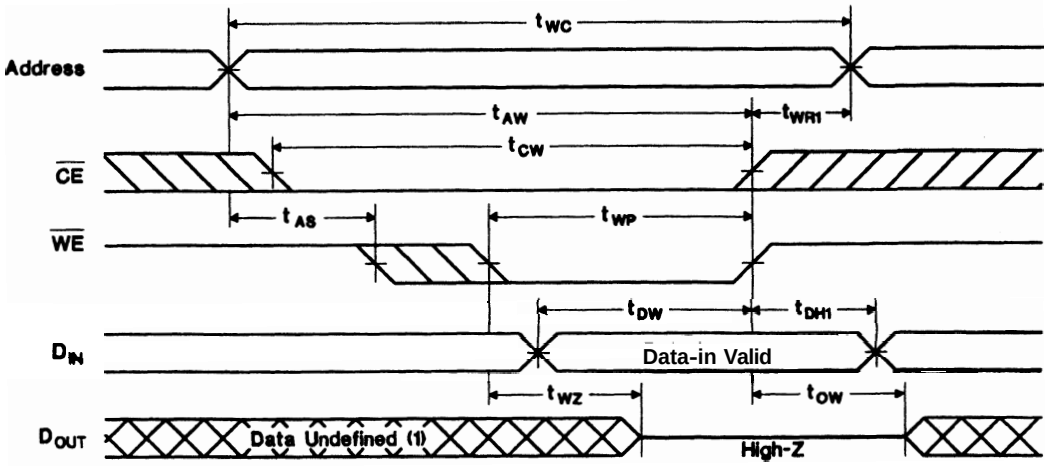
Notes:
1. $\overline{WE}$ is held high for a read cycle.
2. Device is continuously selected: $\overline{CE}$ = $\overline{OE}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ transition low,
4. $\overline{OE}$ = V_{IL}.
6. Device is continuously selected: $\overline{CE}$ = V_{IL}.

Write Cycle ($T_A = T_{OPR}$, $V_{CCmin} \le V_{CC} \le V_{CCmax}$)

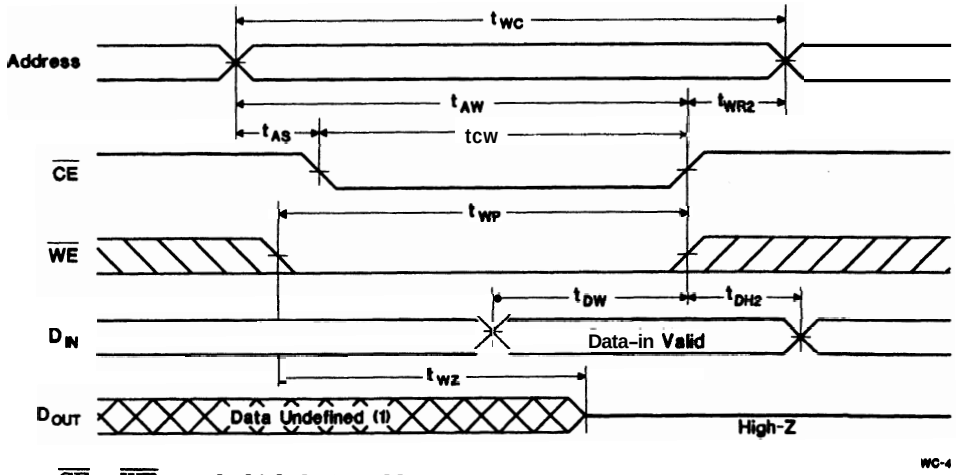
Symbol	Parameter	-70/-70N		-85/-85N		-150/-150N		-200		Units	Conditions/Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{WC}	Write cycle time	70	-	85	-	150	-	200	-	ns	
t_{CW}	Chip enable to end of write	55	-	75	-	100	-	150	-	ns	(1)
t_{AW}	Address valid to end of write	55	-	75	-	90	-	150	-	ns	(1)
t_{AS}	Address setup time	0	-	0	-	0	-	0	-	ns	Measured from address valid to beginning of write. (2)
t_{WP}	Write pulse width	55	-	65	-	90	-	130	-	ns	Measured from beginning of write to end of write. (1)
t_{WR1}	Write recovery time (write cycle 1)	5	-	5	-	5	-	5	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
t_{WR2}	Write recovery time (write cycle 2)	15	-	15	-	15	-	15	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (3)
t_{DW}	Data valid to end of write	30	-	35	-	50	-	70	-	ns	Measured from first low-to-high transition of either $\overline{CE}$ or $\overline{WE}$.
t_{DH1}	Data hold time (write cycle 1)	0	-	0	-	0	-	0	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (4)
t_{DH2}	Data hold time (write cycle 2)	10	-	10	-	0	-	0	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (4)
t_{WZ}	Write enabled to output in high Z	0	25	0	30	0	50	0	70	ns	I/O pins are in output state. (5)
t_{OW}	Output active from end of write	5	-	5		5		5		ns	I/O pins are in output state. (5)

Notes:
1. A write ends at the earlier transition of $\overline{CE}$ going high and $\overline{WE}$ going high.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CE}$ going low and $\overline{WE}$ going low.
3. Either t_{WR1} or t_{WR2} must be met.
4. Either t_{DH1} or t_{DH2} must be met.
5. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

Write Cycle No. 1 ($\overline{WE}$-Controlled) [1,2,3]



Write Cycle No. 2 ($\overline{CE}$-Controlled) [1,2,3,4,5]



Notes:

1. $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
2. Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
3. If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.
4. Either t_{WR1} or t_{WR2} must be met.
5. Either t_{DH1} or t_{DH2} must be met.

Power-Down/Power-Up Cycle (T_A = TOPR)

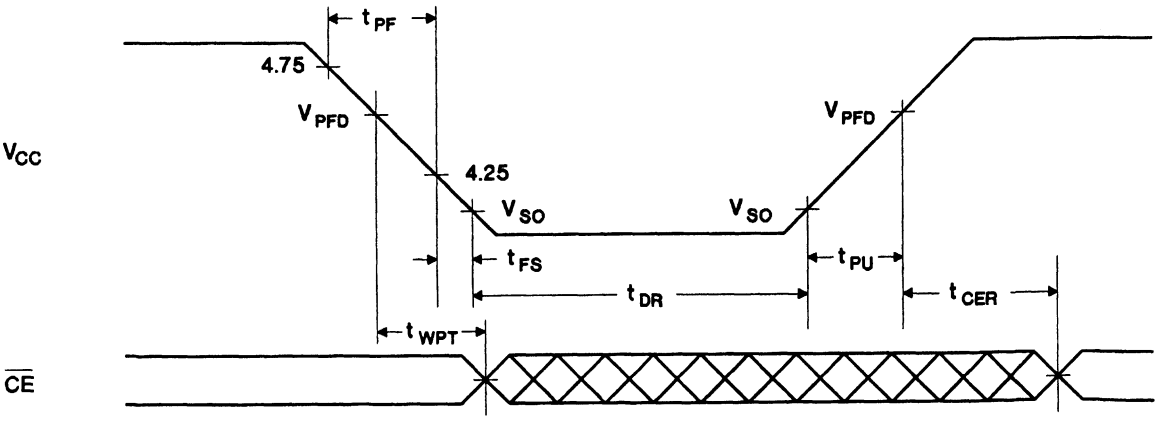
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{PF}	V_{CC} slew, 4.75 to 4.25 V	300			µs	
t_{FS}	V_{CC} slew, 4.25 to V_{SO}	10			µs	
t_{PU}	V_{CC} slew, V_{SO} to V_{PFD} (max.)	0			µs	
t_{CER}	Chip enable recovery time	40	80	120	ms	Time during which SRAM is write-protected after V_{CC} passes V_{PFD} on power-up.
t_{DR}	Data-retention time in absence of V_{CC}	10			years	T_A = 25°C. (2)
t_{DR-N}	Data-retention time in absence of V_{CC}	6			years	T_A = 25°C (2); industrial temperature range (-N) only.
t_{WPT}	Write-protect time	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.

Notes: 1. Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.

2. Battery is disconnected from circuit until after V_{CC} is applied for the first time. t_{DR} is the accumulated time in absence of power beginning when power is first applied to the device.

Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

Power-Down/Power-Up Timing



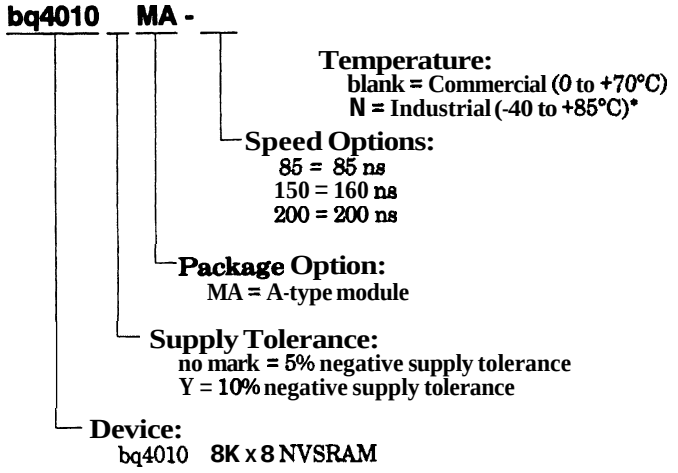
PD-B

Data Sheet Revision History

Change No.	Page No.	Description
1	2, 3, 4, 6, 8, 9	Added industrial temperature range for bq4010YMA-85N and -150N.
2	1, 4, 6, 9	Added 70 ns speed grade for bq4010-70 and bq4010Y-70 and added industrial temperature range for bq4010YMA-70N.
3	1	Removed 70ns speed grade for bq4010-70.

Notes: Change 1 = Sept 1991 B changes from Sept. 1990 A.
Change 2 = Feb. 1994 C changes from Sept. 1991 B.
Change 3 = Sept 1996 D changes from Feb. 1994 C.

Ordering Information



*Note: Only 10% supply ("Y") version is available in industrial temperature range; contact factory for speed grade availability.

bq4011/bq4011Y

32Kx8 Nonvolatile SRAM

Features

- Data retention in the absence of power
- Automatic write-protection during power-up/power-down cycles
- Industry-standard 28-pin 32K x 8 pinout
- Conventional SRAM operation; unlimited write cycles
- 10-year minimum data retention in absence of power
- Battery internally isolated until power is applied

General Description

The CMOS bq4011 is a nonvolatile 262,144-bit static RAM organized as 32,768 words by 8 bits. The integral control circuitry and lithium energy source provide reliable nonvolatility coupled with the unlimited write cycles of standard SRAM.

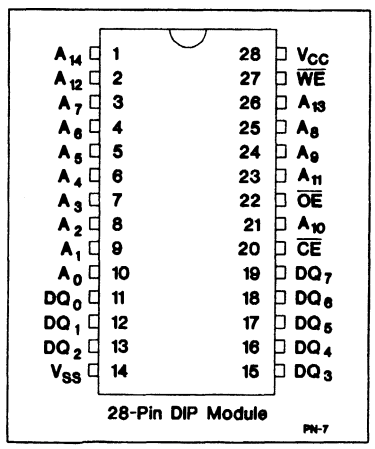
The control circuitry constantly monitors the single 5V supply for an out-of-tolerauce condition. When Vcc falls out of tolerance, the SRAM is unconditionally write-protected to prevent inadvertent write operation.

At this time the integral energy source is switched on to sustain the memory until after Vcc returns valid.

The bq4011 uses an extremely low standby current CMOS SRAM, coupled with a small lithium coin cell to provide nonvolatility without long write-cycle times and the write-cycle limitations associated with EEPROM.

The bq4011 requires no external circuitry and is socket-compatible with industry-standard SRAMs and most EPROMs and EEPROMs.

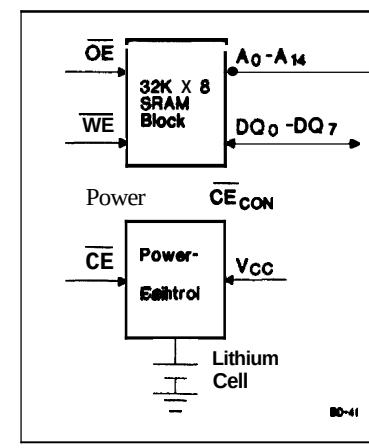
Pin Connections



Pin Names

A_0 - A_{14}	Address inputs
DQ_0 - DQ_7	Data input/output
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input
$\overline{WE}$	Write enable input
Vcc	+5 volt supply input
Vss	Ground

Block Diagram



Selection Guide

Part Number	Maximum Access Time (ns)	Negative Supply Tolerance	Part Number	Maximum Access Time (ns)	Negative Supply Tolerance
			bq4011Y-70	70	-10%
bq4011-100	100	-5%	bq4011Y-100	100	-10%
bq4011-150	150	-5%	bq4011Y-150	150	-10%
bq4011-200	200	-5%	bq4011Y-200	200	-10%

Functional Description

When power is valid, the bq4011 operates as a standard CMOS SRAM. During power-down and power-up cycles, the bq4011 acts as a nonvolatile memory, automatically protecting and preserving the memory contents.

Power-down/power-up control circuitry constantly monitors the V_{CC} supply for a power-fail-detect threshold V_{PFD}. The bq4011 monitors for V_{PFD} = 4.62V typical for use in systems with 5% supply tolerance. The bq4011Y monitors for V_{PFD} = 4.37V typical for use in systems with 10% supply tolerance.

When V_{CC} falls below the V_{PFD} threahold, the SRAM automatically write-protects the data. All outputs become high impedance, and all inputs are treated as 'don't care.' If a valid access is in process at the time of power-fail detection, the memory cycle continues to completion. If the memory cycle fails to terminate within time t_{WPT}, write-protectiontakes place.

As V_{CC} falls past V_{PFD} and approaches 3V, the control circuitry switches to the internal lithium backup supply, which provides data retention until valid V_{CC} is applied.

When V_{CC} returns to a level above the internal backup cell voltage, the supply is switched back to V_{CC}. After V_{CC} ramps above the V_{PFD} threshold, write-protection continues for a time t_{CER} (120ms maximum) to allow for processor stabilization. Normal memory operation may resume after this time.

The internal coin cell used by the bq4011 has an extremely long shelf life and provides data retention for more than 10 years in the absence of system power.

As shipped from Benchmarq, the integral lithium cell is electrically isolated from the memory. (Self-discharge in this condition is approximately 0.5% per year.) Following the first application of V_{CC}, this isolation is broken, and the lithium backup cell provides data retention on subsequent power-downs.

Truth Table

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Operation	Power
Not selected	H	X	X	High Z	Standby
Output disable	L	H	H	High Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to Vss	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to Vss	-0.3 to 7.0	V	$V_T \le V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
		4 0 to +85	°C	Industrial "N"
T_{STG}	Storage temperature	-40 to +70	°C	Commercial
		-40 to +85	°C	Industrial "N"
T_{BIAS}	Temperature under bias	-10 to +70	°C	Commercial
		-40 to +85	°C	Industrial "N"
T_{SOLDER}	Soldering temperature	+260	°C	For 10 seconds

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	bq4011Y/bq4011Y-xxxN
		4.75	5.0	5.5	V	bq4011
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at $T_A = 25°C$.

DC Electrical Characteristics ($T_A = T_{OPR}$, $V_{CCmin} \leq V_{CC} \leq V_{CCmax}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current			±1	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current			±1	µA	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
V_{OH}	Output high voltage	2.4			V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage			0.4	V	I_{OL} = 2.1 mA
I_{SB1}	Standby supply current		4	7	mA	$\overline{CE} = V_{IH}$
I_{SB2}	Standby supply current		2.5	4	mA	$\overline{CE} \geq V_{CC}$ - 0.2V, 0V ≤ $V_{IN} \leq$ 0.2V, or $V_{IN} \geq V_{CC}$ - 0.2V
I_{CC}	Operating supply current		65	75	mA	Min. cycle, duty = 100%, $\overline{CE} = V_{IL}$, $I_{I/O}$ = 0mA
V_{PFD}	Power-fail-detectvoltage	4.55	4.62	4.76	V	bq4011
		4.30	4.37	4.50	V	bq4011Y
V_{SO}	Supply switch-over voltage		3		V	

Note: Typical values indicate operation at $T_A = 25°C$, $V_{CC} = 5V$.

Capacitance ($T_A = 25°C$, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance			10	pF	Output voltage = 0V
C_{IN}	Input capacitance			10	pF	Input voltage = 0V

Note: These parameters are sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 1 and 2

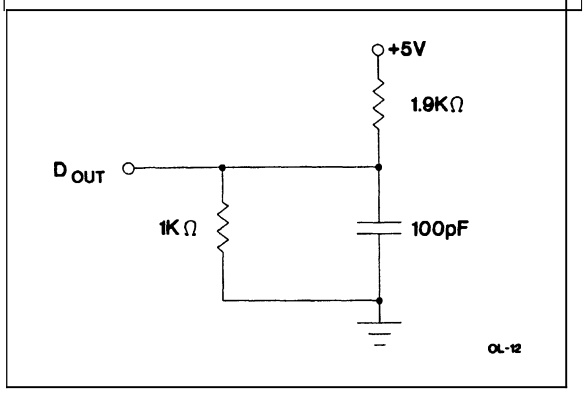


Figure 1. Output Load A

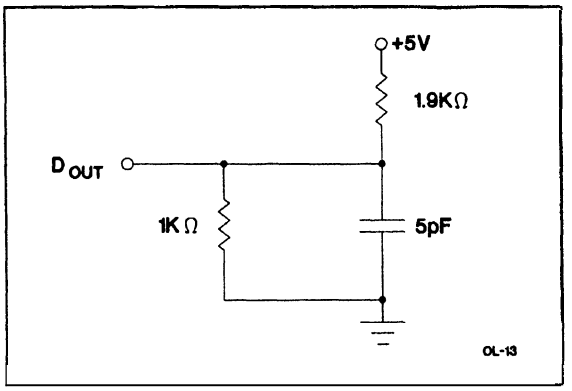
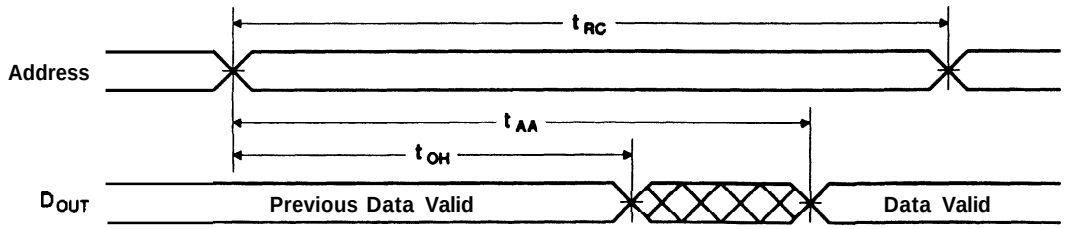


Figure 2. Output Load B

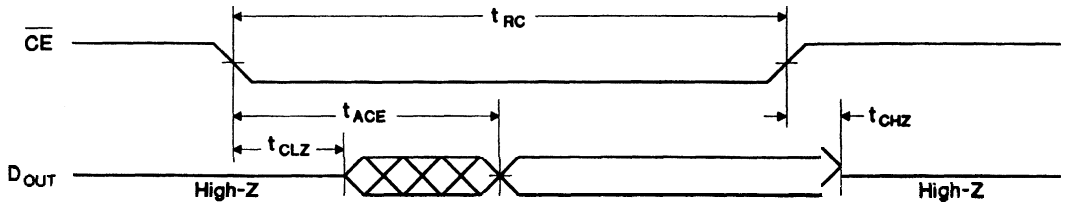
Read Cycle (TA = TOPR, VCCmin ≤ VCC ≤ VCCmax)

Symbol	Parameter	-70/-70N		-100		-150/-150N		-200		Unit	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read cycle time	70	-	100	-	150	-	200	-	ns	
t_{AA}	Address access time	-	70	-	100	-	150	-	200	ns	Output load A
t_{ACE}	Chip enable access time	-	70	-	100	-	150	-	200	ns	Output load A
t_{OE}	Output enable to output valid	-	35	-	50	-	70	-	90	ns	Output load A
t_{CLZ}	Chip enable to output in low Z	5	-	5	-	10	-	10	-	ns	Output load B
t_{OLZ}	Output enable to output in low Z	5	-	5	-	5	-	5	-	ns	Output load B
t_{CHZ}	Chip disable to output in high Z	0	25	0	40	0	60	0	70	ns	Output load B
t_{OHZ}	Output disable to output in high Z	0	25	0	35	0	50	0	70	ns	Output load B
t_{OH}	Output hold from address change	10	-	10	-	10	-	10	-	ns	Output load A

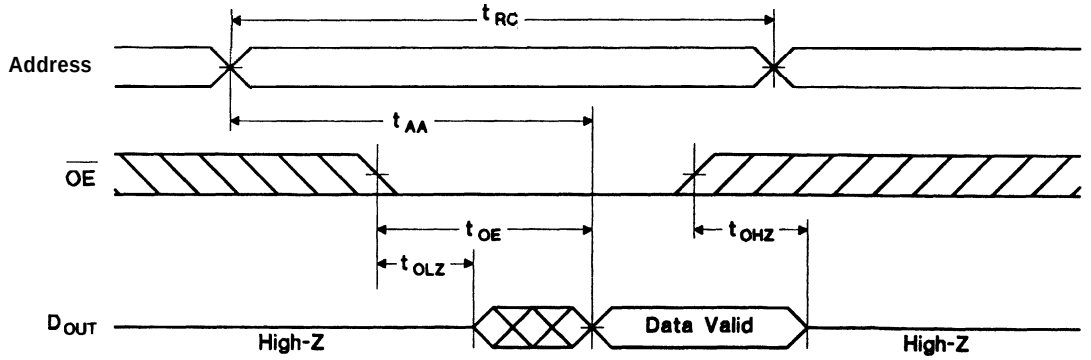
Read Cycle No. 1 (Address Access) [1,2]



Read Cycle No. 2 ($\overline{CE}$ Access) [1,3,4]



Read Cycle No. 3 ($\overline{OE}$ Access) [1,5]



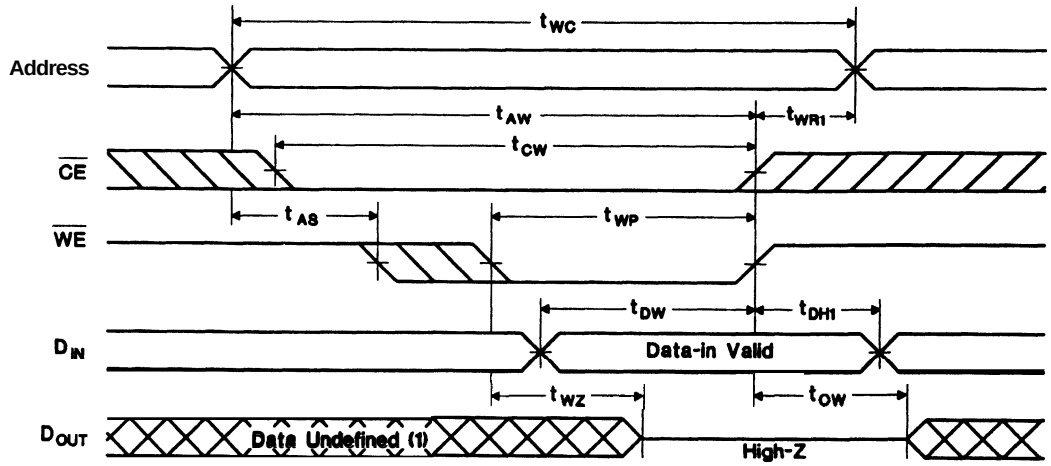
Notes:
1. $\overline{WE}$ is held high for a read cycle.
2. Device is continuously selected: $\overline{CE} = \overline{OE} = V_{IL}$.
3. Address is valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Device is continuously selected: $\overline{CE} = V_{IL}$.

Write Cycle (TA = TOPR, VCCmin ≤ VCC ≤ VCCmax)

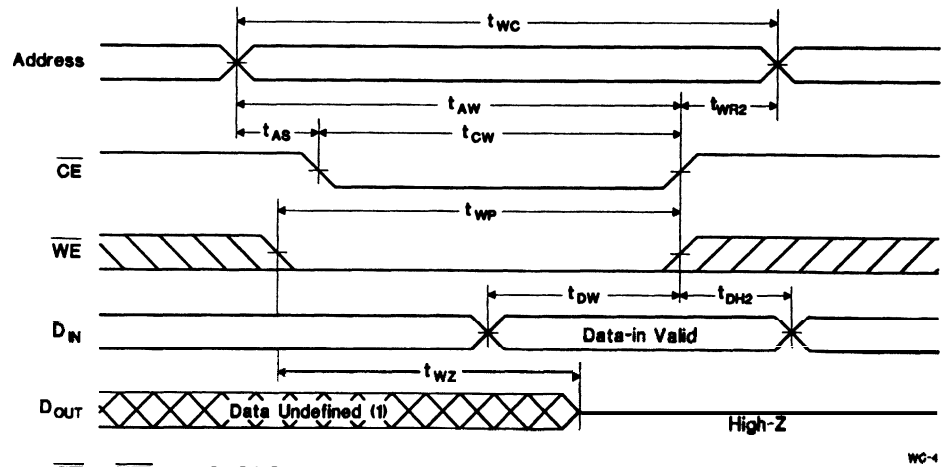
Symbol	Parameter	-70/-70N		-100		-150/-150N		-200		Units	Conditions/Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{WC}	Writecycletime	70	-	100	-	150	-	200	-	ns	
t_{CW}	Chip enable to end of write	55		90		100	-	150	-	ns	(1)
t_{AW}	Address valid to end of write	55		80	-	90	-	150	-	ns	(1)
t_{AS}	Address setup time	0	-	0	-	0	-	0	-	ns	Measured from address valid to beginning of write. (2)
t_{WP}	Write pulse width	55	-	75	-	90	-	130	-	ns	Measured from beginning of write to end of write. (1)
t_{WR1}	Write recovery time (write cycle 1)	5	-	5	-	5	-	5	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
t_{WR2}	Write recovery time (write cycle 2)	15	-	15	-	15	-	15	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (3)
t_{DW}	Data valid to end of write	30		40	-	50	-	70	-	ns	Measured from first low-to-high transition of either $\overline{CE}$ or $\overline{WE}$.
t_{DH1}	Data hold time (write cycle 1)	0		0	-	0	-	0	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (4)
t_{DH2}	Data hold time (write cycle 2)	0		0	-	0	-	0	-	ns	Measured from $\overline{CE}$ going high to end of write cycle.(4)
t_{WZ}	Write enabled to output in high Z	0	25	0	35	0	50	0	70	ns	I/O pine are in output state. (5)
t_{OW}	Output active from end of write	5		5		5		5	-	ns	I/O pins are in output state. (5)

Notes:
1. A write ends at the earlier transition of $\overline{CE}$ going high and $\overline{WE}$ going high.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CE}$ going low and $\overline{WE}$ going low.
3. Either t_{WR1} or t_{WR2} must be met.
4. Either t_{DH1} or t_{DH2} must be met.
5. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

Write Cycle No. 1 ($\overline{WE}$-Controlled) 1,2,3



Write Cycle No. 2 ($\overline{CE}$-Controlled) 1,2,3,4,5



Notes:
1. $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
2. Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
3. If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.
4. Either t_{WR1} or t_{WR2} must be met.
5. Either t_{DH1} or t_{DH2} must be met.

Power-Down/Power-Up Cycle (T_A = TOPR)

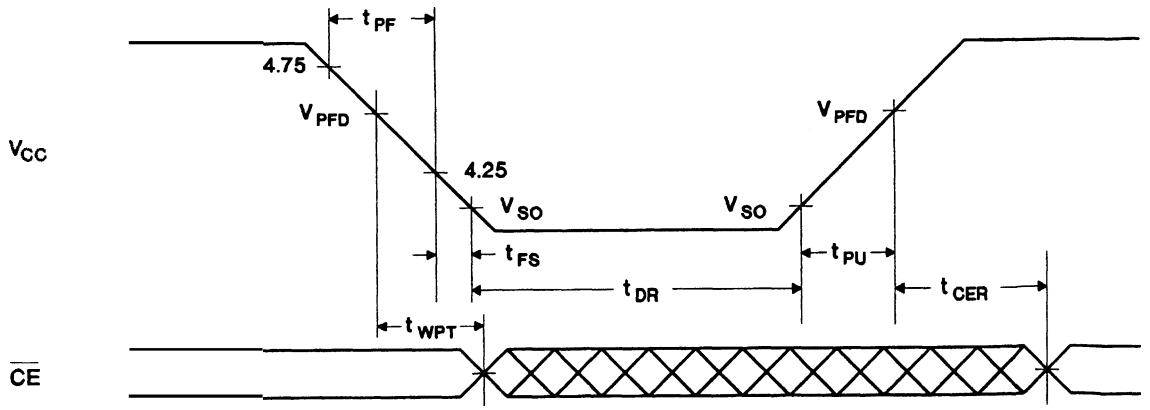
Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_{PF}	V_{CC} slew, 4.75 to 4.25 V	300			lre	
t_{FS}	V_{CC} slew, 4.25 to V_{SO}	10			µs	
t_{PU}	V_{CC} slew, V_{SO} to V_{PFD} (max.)	0			lre	
t_{CER}	Chip enable recovery time	40	80	120	ms	Time during which SRAM is write-protected after V_{CC} passes V_{PFD} on power-up.
t_{DR}	Data-retention time in absence of V_{CC}	10			years	T_A = 25°C.(2)
t_{DR-N}	Data-retention time in absence of V_{CC}	6			years	T_A = 25°C(2); industrial temperature range (-N) only.
t_{WPT}	Write-prokt time	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.

Notes: 1. Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.

2. Battery is disconnected from circuit until after V_{CC} is applied for the first time. t_{DR} is the accumulated time in absence of power beginning when power is first applied to the device.

Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

Power-Down/Power-Up Timing



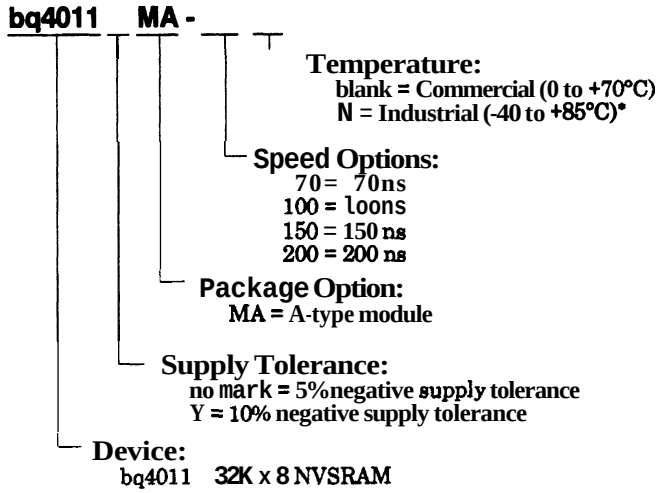
PD-B

Data Sheet Revision History

Change No.	Page No.	Description
1	2, 3, 4, 6, 8, 9	Added industrial temperature range for bq4011YMA-150N.
2	1, 4, 6, 9	Added 70 ns speed grade for bq4011Y-70 and added industrial temperature range for bq4011YMA-70N.

Notes: Change 1 = Sept 1992 B changes from Sept 1990 A.
Change 2 = Aug. 1993 C changes from Sept. 1991 B.

Ordering Information



*Note: Only 10% supply ("Y") version is available in industrial temperature range; contact factory for speed grade availability.

bq4013/bq4013Y

128Kx8 Nonvolatile SRAM

Features

- ➤ Data retention in the absence of power
- ● Automatic write-protection during power-up/power-down cycles
- ➤ Induetry-standard 32-pin 128K x 8 pinout
- ➤ Conventional SRAM operation; unlimited write cycles
- ➤ 10-year minimum data retention in absence of power
- ● Battery internally isolated until power is applied

General Description

The CMOS bq4013 is a nonvolatile 1,048,576-bit static RAM organized as 131,072 words by 8 bits. The integral control circuitry and lithium energy source provide reliable nonvolatility coupled with the unlimited write cycles of standard SRAM.

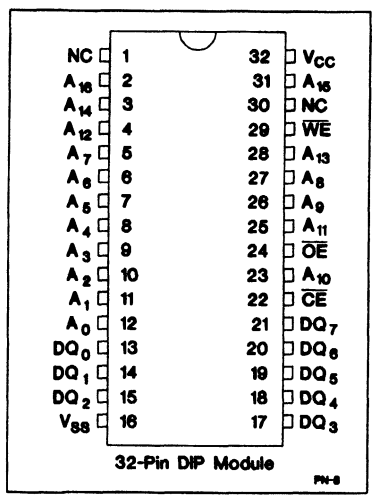
The control circuitry constantly monitors the single 5V supply for an out-of-tolerance condition. When Vcc falls out of tolerance, the SRAM is unconditionally write-protected to prevent inadvertent write operation.

At this time the integral energy source is switched on to sustain the memory until after Vcc returns valid.

The bq4013 uses an extremely low standby current CMOS SRAM, coupled with a small lithium coin cell to provide nonvolatility without long write-cycle times and the write-cycle limitations associated with EEPROM.

The bq4013 requires no external circuitry and is socket-compatible with induetry-standard SRAMs and most EPROMs and EEPROMs.

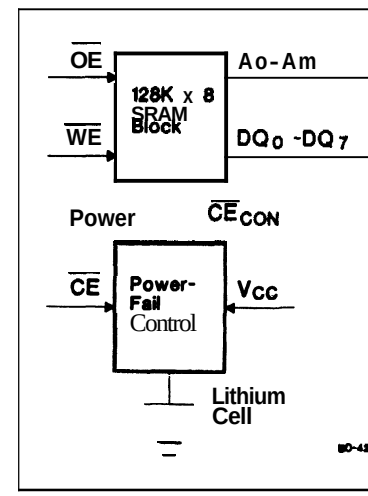
Pln Connections



Pin Names

A_0-A_{16}	Address inputs
DQ_0-DQ_7	Data input/output
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input
$\overline{WE}$	Write enable input
NC	No connect
Vcc	+5 volt supply input
Vss	Ground

Block Diagram



Selection Guide

Part Number	Maximum Access Time (ns)	Negative Supply Tolerance	Part Number	Maximum Access Time (ns)	Negative Supply Tolerance
			bq4013Y -70	70	-10%
bq4013 -85	85	-5%	bq4013Y -85	85	-10%
bq4013 -120	120	-5%	bq4013Y -120	120	-10%

Functional Description

When power is valid, the bq4013 operates as a standard CMOS SRAM. During power-down and power-up cycles, the bq4013 acts as a nonvolatile memory, automatically protecting and preserving the memory contents.

Power-down/power-up control circuitry constantly monitors the V_{CC} supply for a power-fail-detect threshold V_{PFD}. The bq4013 monitors for V_{PFD} = 4.62V typical for use in systems with 5% supply tolerance. The bq4013Y monitors for V_{PFD} = 4.37V typical for use in systems with 10% supply tolerance.

When V_{CC} falls below the V_{PFD} threshold, the SRAM automatically write-protects the data. All outputs become high impedance, and all inputs are treated as "don't care." If a valid access is in process at the time of power-fail detection, the memory cycle continua to completion. If the memory cycle fails to terminate within time t_{WPT}, write-protection takes place.

As V_{CC} falls past V_{PFD} and approaches 3V, the control circuitry switches to the internal lithium backup supply, which provides data retention until valid V_{CC} is applied.

When V_{CC} returns to a level above the internal backup cell voltage, the supply is switched back to V_{CC}. After V_{CC} ramps above the V_{PFD} threshold, write-protection continues for a time t_{CER} (120ms maximum) to allow for processor stabilization. Normal memory operation may resume after this time.

The internal coin cell used by the bq4013 has an extremely long shelf life and provides data retention for more than 10 years in the absence of system power.

As shipped from Benchmarq, the integral lithium cell is electrically isolated from the memory. (Self-discharge in this condition is approximately 0.5% per year.) Following the first application of V_{CC}, this isolation is broken, and the lithium backup cell provides data retention on subsequent power-downs.

Truth Table

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Operation	Power
Not selected	H	X	X	High Z	Standby
Output disable	L	H	H	High Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \le V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
		-40 to +85	°C	Industrial "N"
T_{STG}	Storage temperature	-40 to +70	°C	Commercial
		-40 to +85	°C	Industrial "N"
T_{BIAS}	Temperature under bias	-10 to +70	°C	Commercial
		-40 to +85	°C	Industrial "N"
T_{SOLDER}	Soldering temperature	+260	°C	For 10 seconds

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	bq4013Y/bq4013Y-xxxN
		4.75	5.0	5.5	V	bq4013
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at $T_A = 25°C$.

DC Electrical Characteristics (T_A = TOPR, $V_{CCmin} \leq V_{CC} \leq V_{CCmax}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current			± 1	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current			± 1	µA	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
V_{OH}	Output high voltage	2.4			V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage			0.4	V	I_{OL} = 2.1 mA
I_{SB1}	Standby supply current		4	7	mA	$\overline{CE} = V_{IH}$
I_{SB2}	Standby supply current		2.5	4	mA	$\overline{CE} \geq V_{CC}$ - 0.2V, 0V ≤ $V_{IN} \leq$ 0.2V, or $V_{IN} \geq V_{CC}$ - 0.2V
I_{CC}	Operating supply current		75	105	mA	Min. cycle, duty = 100%, $\overline{CE} = V_{IL}$, $I_{I/O}$ = 0mA
V_{PFD}	Power-fail-detectvoltage	4.55	4.62	4.75	V	bq4013
		4.30	4.37	4.50	V	bq4013Y
V_{SO}	Supply switch-over voltage		3		V	

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance			10	pF	Output voltage = 0V
C_{IN}	Input capacitance			10	pF	Input voltage = 0V

Note: These parameters are sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 1 and 2

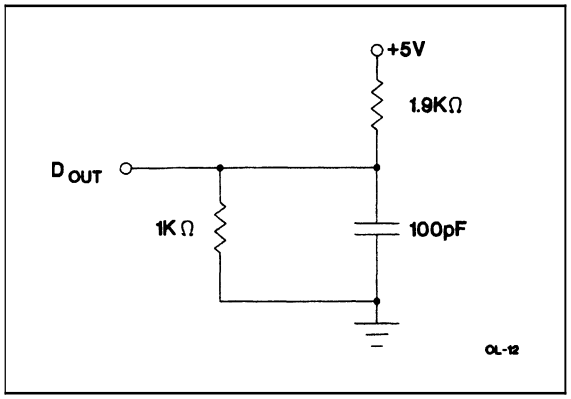


Figure 1. Output Load A

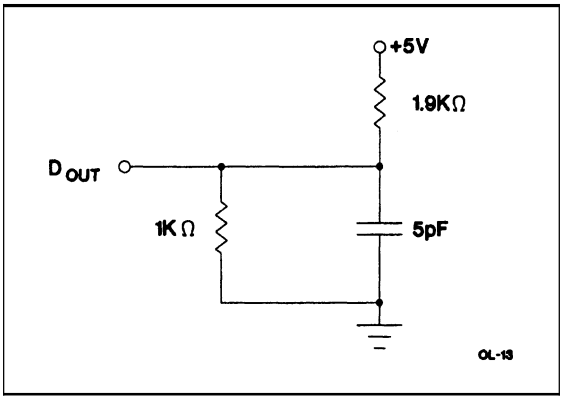
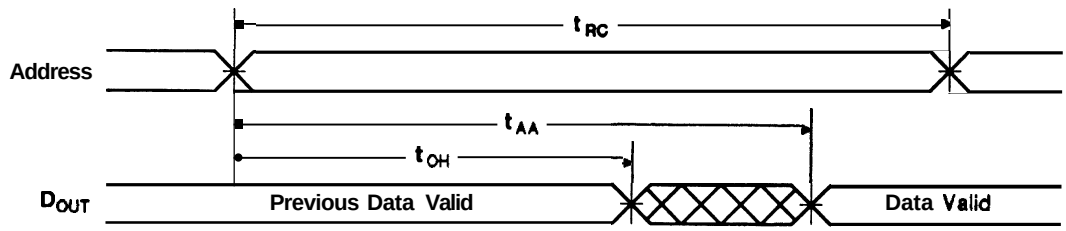


Figure 2. Output Load B

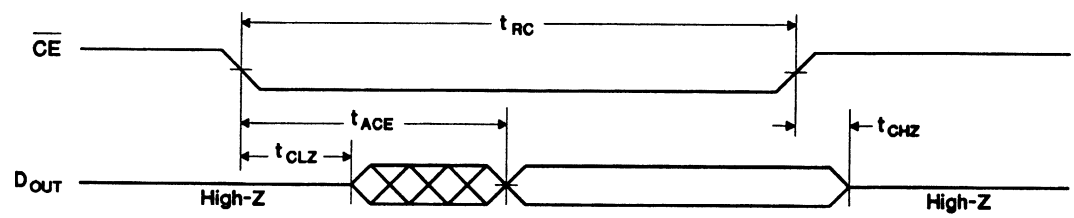
Read Cycle (T_A = TOPR, V_{CC}min ≤ V_{CC} ≤ V_{CC}max)

Symbol	Parameter	-70/-70N		-85/-85N		-120		Unit	Conditions
		Min.	Min.	Min.	Max.	Min.	Max.		
t_{RC}	Read cycle time	70	-	85	-	120	-	ns	
t_{AA}	Address access time	-	70	-	85	-	120	ns	Output load A
t_{ACE}	Chip enable access time	-	70	-	85	-	120	ns	Output load A
t_{OE}	Output enable to output valid	-	35	-	45	-	60	ns	Output load A
t_{CLZ}	Chip enable to output in low Z	5	-	5	-	5	-	ns	Output load B
t_{OLZ}	Output enable to output in low Z	0	-	0	-	0	-	ns	Output load B
t_{CHZ}	Chip disable to output in high Z	0	25	0	35	0	45	ns	Output load B
t_{OHZ}	Output disable to output in high Z	0	25	0	25	0	35	ns	Output load B
t_{OH}	Output hold from address change	10	-	10	-	10	-	ns	Output load A

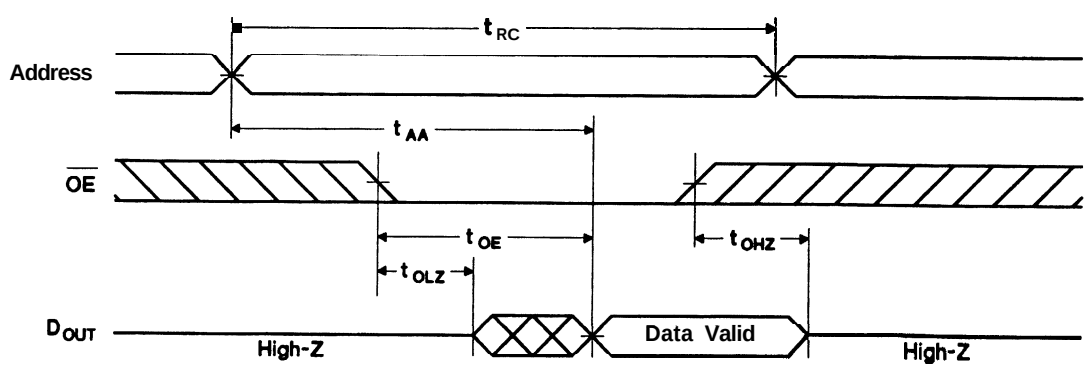
Read Cycle No. 1 (Address Access) [1,2]



Read Cycle No. 2 ($\overline{CE}$ Access) [1,3,4]



Read Cycle No. 3 ($\overline{OE}$ Access) [1,5]



Notes:
1. $\overline{WE}$ is held high for a read cycle.
2. Device is continuously selected: $\overline{CE}$ = $\overline{OE}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Device is continuously selected: $\overline{CE}$ = V_{IL}

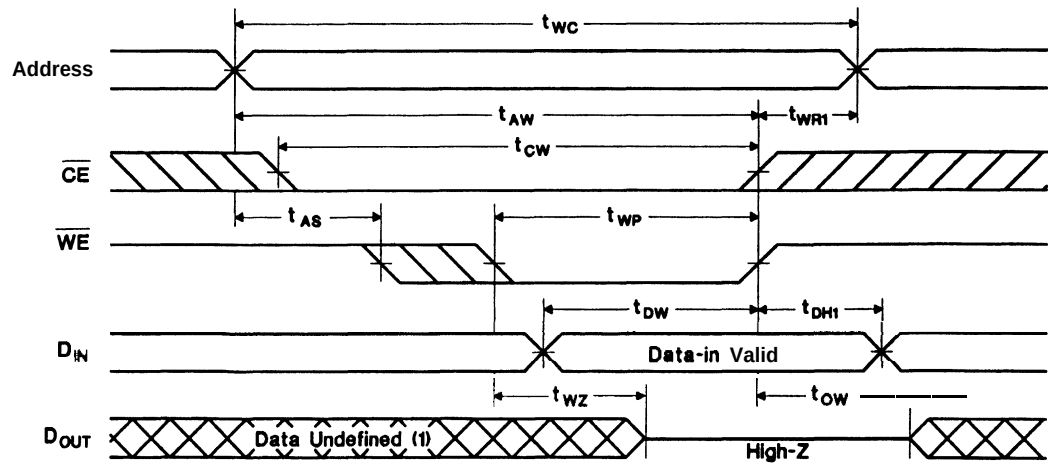
Write Cycle ($T_A = T_{OPR}$, $V_{CCmin} \le V_{CC} \le V_{CCmax}$)

Symbol	Parameter	-70/-70N		-85/-85N		-120		Units	Conditions/Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{WC}	Write cycle time	70	-	85	-	120	-	ns	
t_{CW}	Chip enable to end of write	65	-	75	-	100	-	ns	(1)
t_{AW}	Address valid to end of write	65	-	75	-	100	-	ns	(1)
t_{AS}	Address setup time	0	-	0	-	0	-	ns	Measured from address valid to beginning of write. (2)
t_{WP}	Write pulse width	55	-	65	-	85	-	ns	Measured from beginning of write to end of write. (1)
t_{WR1}	Write recovery time (write cycle 1)	5	-	5	-	5	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
t_{WR2}	Write recovery time (write cycle 2)	15	-	15	-	15	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (3)
t_{DW}	Data valid to end of write	30	-	35	-	45	-	ns	Measured to first low-to-high transition of either $\overline{CE}$ or $\overline{WE}$.
t_{DH1}	Data hold time (write cycle 1)	0		0	-	0		ns	Measured from $\overline{WE}$ going high to end of write cycle. (4)
t_{DH2}	Data hold time (write cycle 2)	10	-	10	-	10	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (4)
t_{WZ}	Write enabled to output in high Z	0	25	0	30	0	40	ns	I/O pins are in output state. (5)
t_{OW}	Output active from end of write	0	-	0	-	0	-	ns	I/O pins are in output state. (5)

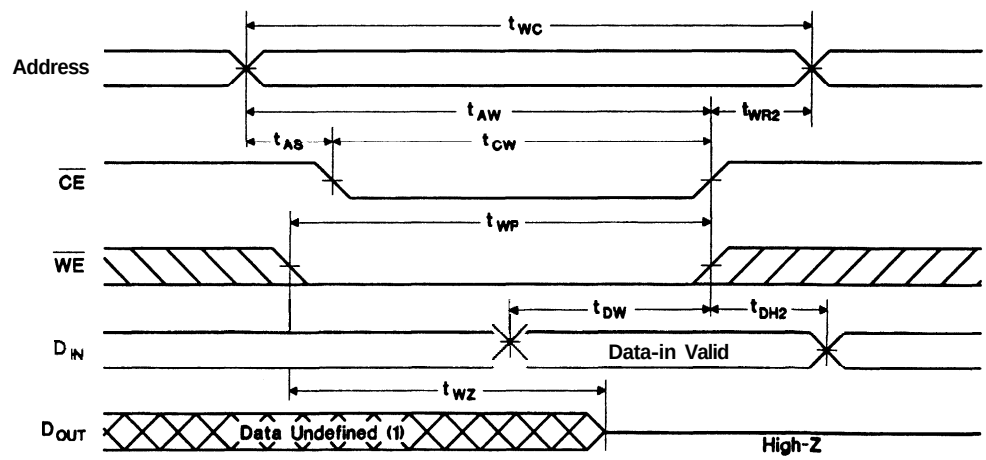
Notes:

1. A write ends at the earlier transition of $\overline{CE}$ going high and $\overline{WE}$ going high.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CE}$ going low and $\overline{WE}$ going low.
3. Either t_{WR1} or t_{WR2} must be met.
4. Either t_{DH1} or t_{DH2} must be met.
5. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

Write Cycle No. 1 ($\overline{WE}$-Controlled) 1,2,3



Write Cycle No. 2 ($\overline{CE}$-Controlled) 1,2,3,4,5



Notes:
1. $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
2. Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
3. If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.
4. Either t_{WR1} or t_{WR2} must be met.
5. Either t_{DH1} or t_{DH2} must be met.

Power-Down/Power-Up Cycle ($T_A = T_{OPR}$)

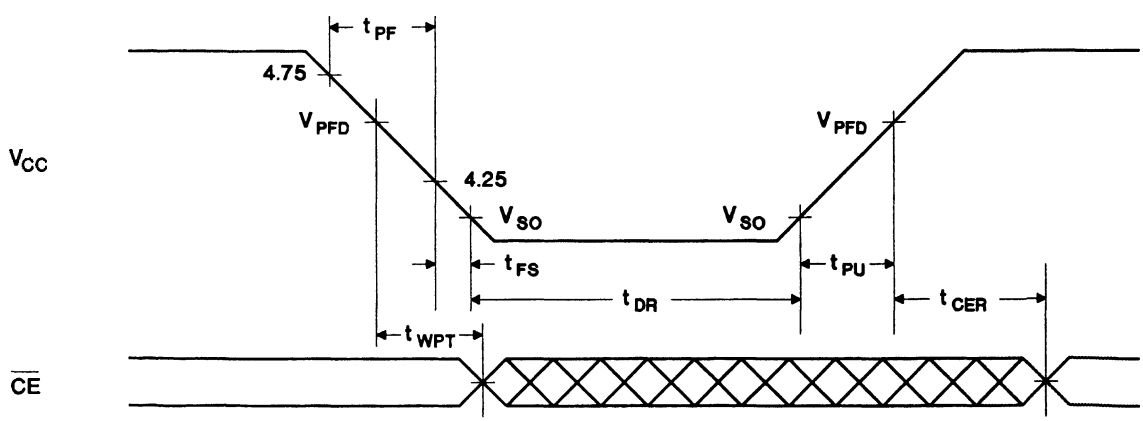
Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_{PF}	V_{CC} slew, 4.75 to 4.25 V	300			µs	
t_{FS}	V_{CC} slew, 4.25 to V_{SO}	10			µs	
t_{PU}	V_{CC} slew, Vso to V_{PFD} (max.)	0			µs	
t_{CER}	Chip enable recovery time	40	80	120	ms	Time during which SRAM is write-protected after V_{CC} passes V_{PFD} on power-up.
t_{DR}	Data-retention time in absence of V_{CC}	10			years	T_A = 25°C. (2)
t_{DR-N}	Data-retention time in absence of V_{CC}	6			years	T_A = 25°C (2); industrial temperature range only
t_{WPT}	Write-protect time	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.

Notes: 1. Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.

2. Battery is disconnected from circuit until after V_{CC} is applied for the first time. t_{DR} is the accumulated time in absence of power beginning when power is first applied to the device.

Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

Power-Down/Power-Up Timing



PD-8

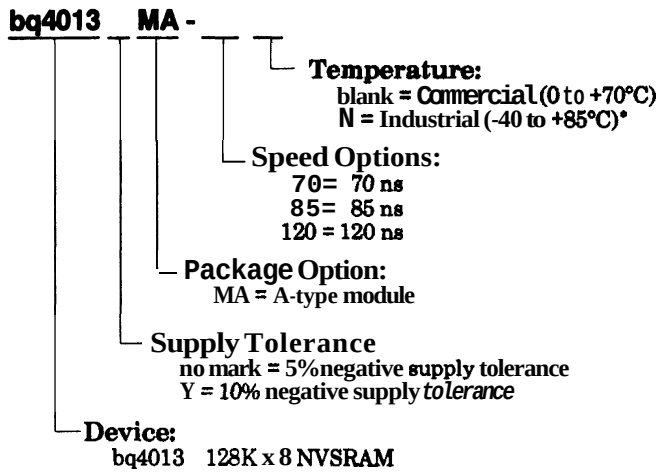
Data Sheet Revision History

Change No.	Page No.	Description
1	4 3, 4, 6, 8, 9	Added industrial temperature range.
2	1, 4, 6, 9	Added 70 ns speed grade far bq4013Y-70.
3		Removed industrial temperature range far bq4013YMA-120N

Notes: Change 1 = Sept 1992 B changes from Sept. 1990 A.
Change 2 = Aug. 1993 C changes from Sept. 1991 B.
Change 3 = Sept. 1996 D changes from Aug. 1003 C.

6

Ordering Information



'Note: Only 10% supply ("Y") version is available in industrial temperature range; contact factory for speed grade availability.

BENCHMARQ bq4014/bq4014Y

256Kx8 Nonvolatile SRAM

Features

- Data retention in the absence of power
- Automatic write-protection during power-up/power-down cycles
- Industry-standard 32-pin 256K x 8 pinout
- Conventional SRAM operation; unlimited write cycles
- 10-year minimum data retention in absence of power
- Battery internally isolated until power is applied

General Description

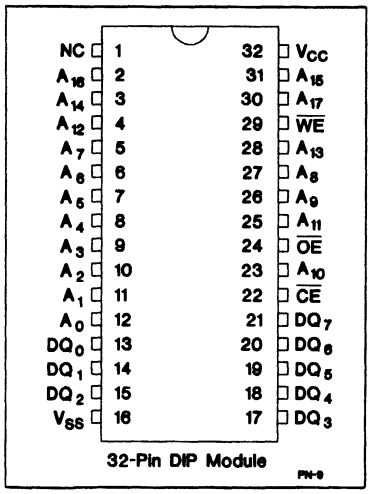
The CMOS bq4014 is a nonvolatile 2,097,152-bit static RAM organized as 262,144 words by 8 bits. The integral control circuitry and lithium energy source provide reliable nonvolatility coupled with the unlimited write cycles of standard SRAM.

The control circuitry constantly monitors the single 5V supply for an out-of-tolerance condition. When Vcc falls out of tolerance, the SRAM is unconditionally write-protected to prevent inadvertent write operation. At this time the integral energy source is switched on to sustain the memory until after Vcc returns valid.

The bq4014 ueee extremely low etandby current CMOS SRAMs, coupled with small lithium coin cells to provide nonvolatility without long write-cycle times and the write-cycle limitations aeeociated with EEPROM.

The bq4014 requires no external circuitry and ie compatible with the industry-standard 2Mb SRAM pinout.

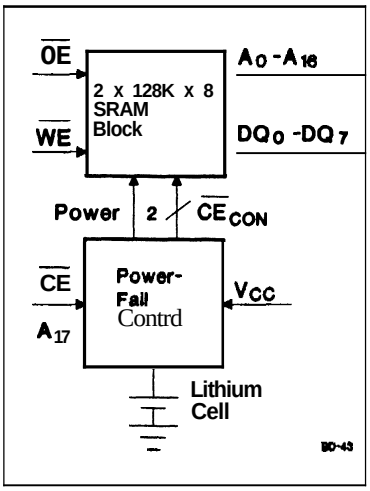
Pin Connections



Pin Names

A_0-A_{17}	Address inputs
DQ_0-DQ_7	Data input/output
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input
$\overline{WE}$	Write enable input
NC	No connect
V_{CC}	+5 volt supply input
V_{SS}	Ground

Block Diagram



Selection Guide

Part Number	Maximum Access Time (ns)	Negative Supply Tolerance	Part Number	Maximum Access Time (ns)	Negative Supply Tolerance
bq4014-85	85	-5%	bq4014Y-85	85	-10%
bq4014-120	120	-5%	bq4014Y-120	120	-10%

Sept. 1992 1/10

6

Functional Description

When power is valid, the bq4014 operates as a standard CMOS SRAM. During power-down and power-up cycles, the bq4014 acts as a nonvolatile memory, automatically protecting and preserving the memory contents.

Power-down/power-up control circuitry constantly monitors the V_{CC} supply for a power-fail-detect threshold V_{PFD}. The bq4014 monitors for V_{PFD} = 4.62V typical for use in systems with 5% supply tolerance. The bq4014Y monitors for V_{PFD} = 4.37V typical for use in systems with 10% supply tolerance.

When V_{CC} falls below the V_{PFD} threshold, the SRAM automatically write-protects the data. All outputs become high impedance, and all inputs are treated as 'don't care.' If a valid access is in process at the time of power-fail detection, the memory cycle continues to completion. If the memory cycle fails to terminate within time t_{WPT}, write-protection takes place.

As V_{CC} falls past V_{PFD} and approaches 3V, the control circuitry switches to the internal lithium backup supply, which provides data retention until valid V_{CC} is applied.

When V_{CC} returns to a level above the internal backup cell voltage, the supply is switched back to V_{CC}. After V_{CC} ramps above the V_{PFD} threshold, write-protection continues for a time t_{CER} (120ms maximum) to allow for processor stabilization. Normal memory operation may resume after this time.

The internal coin cells used by the bq4014 have an extremely long shelf life and provide data retention for more than 10 years in the absence of system power.

As shipped from Benchmarq, the integral lithium cells are electrically isolated from the memory. (Self-diecharge in this condition is approximately 0.5% per year.) Following the first application of V_{CC}, this isolation is broken, and the lithium backup provides data retention on subsequent power-downs.

Truth Table

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Operation	Power
Not selected	H	X	X	High Z	Standby
Output disable	L	H	H	High Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
Vcc	DC voltage applied on V_{CC} relative to Vss	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding Vcc relative to V_{SS}	-0.3 to 7.0	V	$V_T \le V_{CC} + 0.3$
Tom	Operating temperature	0 to +70	°C	
T_{STG}	Storage temperature	-40 to +70	°C	
T_{BIAS}	Temperature under bias	-10 to +70	"C	
T_{SOLDER}	Soldering temperature	+260	°C	For 10 seconds

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
vcc	Supply voltage	4.5	5.0	5.5	V	bq4014Y
		4.75	5.0	5.5	V	bq4014
vss	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3		0.8	V	
V_{IH}	Input high voltage	2.2		V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C.

DC Electrical Characteristics (T_A = 0 to 70°C, $V_{CCmin} \le V_{CC} \le V_{CCmax}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current			± 2	µA	V_{IN} = Vss to V_{CC}
I_{LO}	Output leakage current			± 2	µA	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}
V_{OH}	Output high voltage	2.4			V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage			0.4	V	I_{OL} = 2.1 mA
I_{SB1}	Standby supply current		5	12	mA	$\overline{CE}$ = V_{IH}
I_{SB2}	Standby supply current		2.5	5	mA	$\overline{CE} \ge V_{CC}$ - 0.2V, 0V ≤ $V_{IN} \le$ 0.2V, or $V_{IN} \ge V_{CC}$ - 0.2
I_{CC}	Operating supply current		75	110	mA	Min. cycle, duty = 100%, $\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0mAV, A17 < V_{IL} or A17 > V_{IH}
V_{PFD}	Power-fail-detect voltage	4.55	4.62	4.75	V	bq4014
		4.30	4.37	4.50	V	bq4014Y
V_{SO}	Supply switch-over voltage		3		V	

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance			40	pF	Output voltage = 0V
C_{IN}	Input capacitance			40	pF	Input voltage = 0V

Note: These parameters are sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 1 and 2

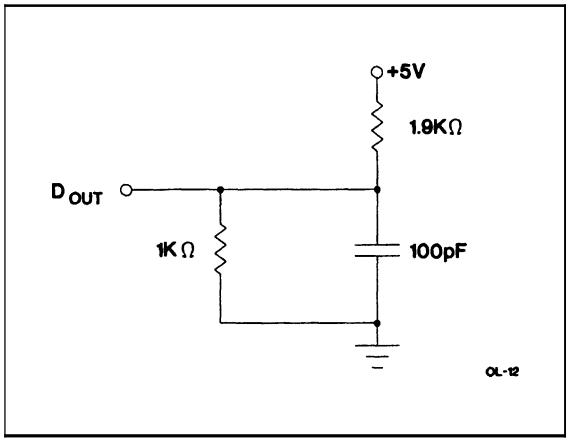


Figure 1. Output Load A

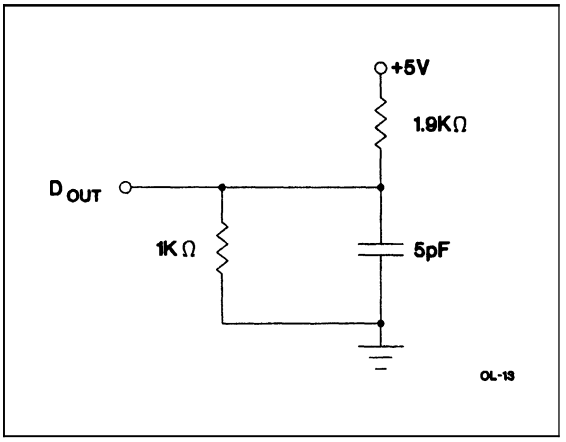
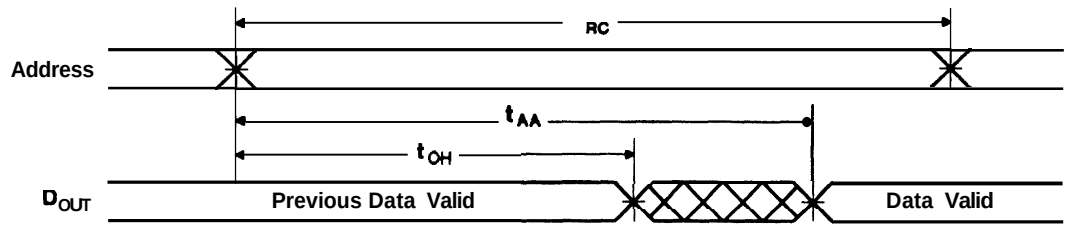


Figure 2. Output Load B

Read Cycle (TA = 0 to 70°C, VCCmin ≤ VCC ≤ VCCmax)

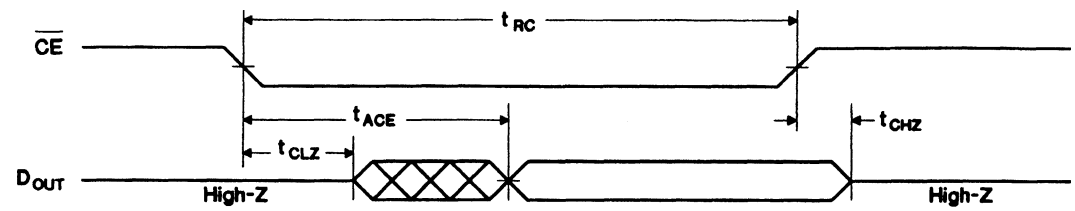
Symbol	Parameter	-85		-120		Unit	Conditions
		Min.	Max.	Min.	Max.		
t_{RC}	Read cycle time	85	-	120	-	ns	
t_{AA}	Address access time	-	85	-	120	ns	Output load A
t_{ACE}	Chip enable access time	-	85	-	120	ns	Output load A
t_{OE}	Output enable to output valid	-	45	-	60	ns	Output load A
t_{CLZ}	Chip enable to output in low Z	5	-	5	-	ns	Output load B
t_{OLZ}	Output enable to output in low Z	0	-	0	-	ns	Output load B
t_{CHZ}	Chip disable to output in high Z	0	35	0	45	ns	Output load B
t_{OHZ}	Output disable to output in high Z	0	25	0	35	ns	Output load B
t_{OH}	Output hold from address change	10	-	10	-	ns	Output load A

Read Cycle No. 1 (Address Access) [1,2]



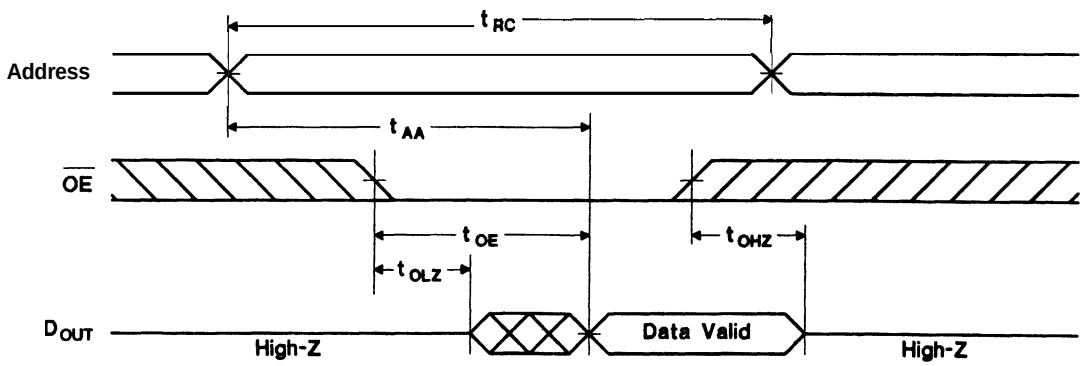
RC-1

Read Cycle No. 2 ($\overline{CE}$ Access) [1,3,4]



RC-2

Read Cycle No. 3 ($\overline{OE}$ Access)



RC-3

Notes:

1. $\overline{WE}$ is held high for a read cycle.
2. Device is continuously selected: $\overline{CE}$ = $\overline{OE}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Device is continuously selected: $\overline{CE}$ = V_{IL}.

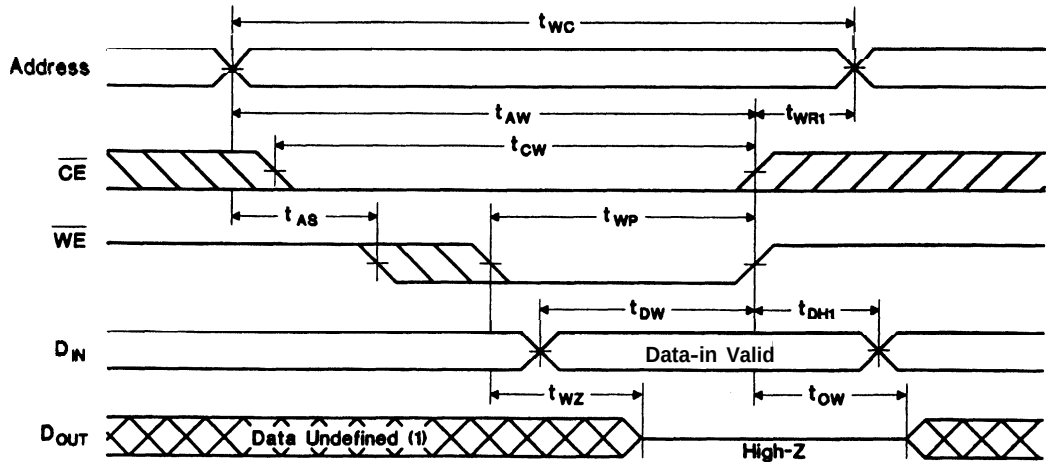
Write Cycle (T_A = 0 to 70°C, $V_{CCmin} \le V_{CC} \le V_{CCmax}$)

Symbol	Parameter	-85		120		Units	Conditions/Notes
		Min.	Max.	Min.	Max.		
t_{WC}	Write cycle time	85	-	120	-	ns	
t_{CW}	Chip enable to end of write	75	-	100	-	ns	(1)
t_{AW}	Address valid to end of write	75	-	100	-	ns	(1)
t_{AS}	Addreea setup time	0		0		ns	Measured from address valid to beginning of write. (2)
t_{WP}	Write pulse width	65		85		ns	Measured from beginning of write to end of write. (1)
t_{WR1}	Write recovery time (write cycle 1)	5		5	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
t_{WR2}	Write recovery time (write cycle 2)	15	-	15	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (3)
t_{DW}	Data valid to end of write	35	-	45		ns	Measured to first low-to-high transition of either $\overline{CE}$ or $\overline{WE}$.
t_{DH1}	Data hold time (write cycle 1)	0		0		ns	Measured from $\overline{WE}$ going high to end of write cycle. (4)
t_{DH2}	Data hold time (write cycle 2)	10	-	10	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (4)
t_{WZ}	Write enabled to output in high Z	0	30	0	40	na	I/O pins are in output state. (5)
t_{OW}	Output active from end of write	0	-	0	-	ns	I/O pine are in output state. (5)

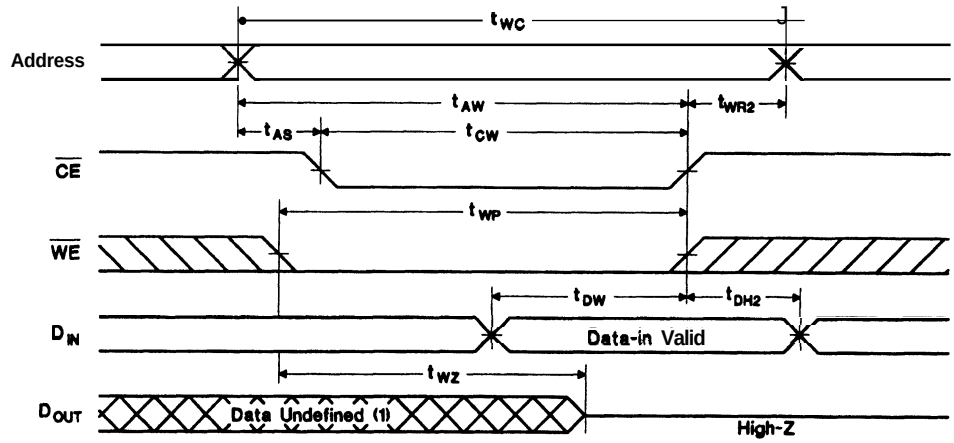
Notes:

1. A write ends at the earlier transition of $\overline{CE}$ going high and $\overline{WE}$ going high.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CE}$ going low and $\overline{WE}$ going low.
3. Either t_{WR1} or t_{WR2} must be met.
4. Either t_{DH1} or t_{DH2} must be met.
5. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

Write Cycle No. 1 ($\overline{WE}$-Controlled) 1,2,3



Write Cycle No. 2 ($\overline{CE}$-Controlled) 1,2,3,4,5



Notes:
1. $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
2. Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
3. If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.
4. Either t_{WR1} or t_{WR2} must be met.
5. Either t_{DH1} or t_{DH2} must be met.

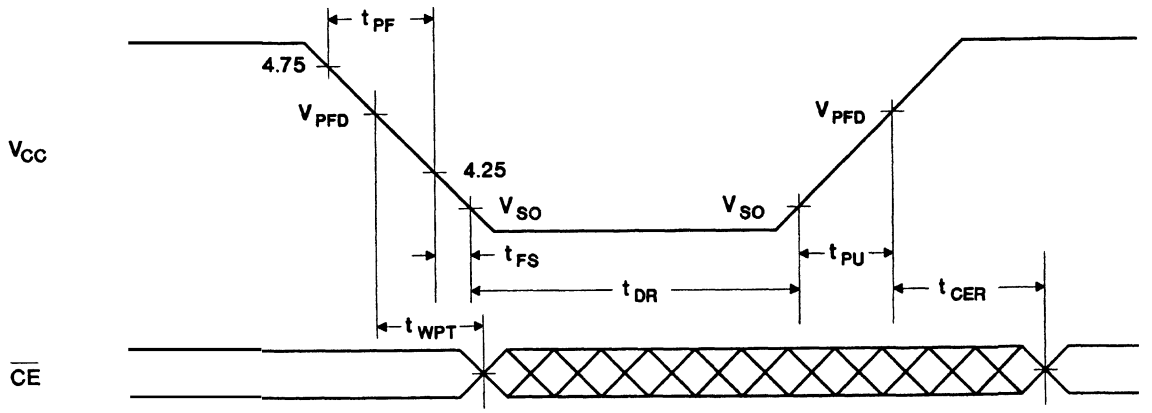
Power-Down/Power-Up Cycle (TA = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_{PF}	V_{CC} slew, 4.75 to 4.25 V	300			µs	
t_{FS}	V_{CC} slew, 4.25 to V_{SO}	10			µs	
t_{PU}	V_{CC} slew, V_{SO} to V_{PFD} (max.)	0			µs	
t_{CER}	Chip enable recovery time	40	80	120	ms	Time during which SRAM is write-protected after V_{CC} passes V_{PFD} on power-up.
t_{DR}	Data-retention time in absence of V_{CC}	10			years	T_A = 25°C.(2)
t_{WPT}	Write-protect time	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.

Notes:
1. Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.
2. Batteries are disconnected from circuit until after V_{CC} is applied for the first time. t_{DR} is the accumulated time in absence of power beginning when power is first applied to the device.

Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

Power-Down/Power-Up Timing

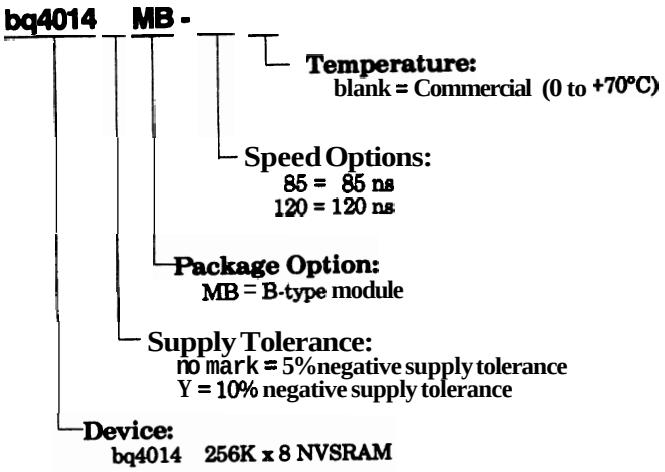


PD-8

Data Sheet Revision History (Sept. 1992 Changes From Sept 1990)

Clarification of I_{CC} test conditions, page 3.

Ordering Information



bq4015/bq4015Y

512Kx8 Nonvolatile SRAM

Features

- Data retention in the absence of power
- Automatic write-protection during power-up/power-down cycles
- ➤ Industry-standard 32-pin 512K x 8 pinout
- ➤ Conventional SRAM operation; unlimited write cycles
- ➤ 10-year minimum data retention in absence of power
- Battery internally isolated until power is applied
- Industrial temperature operation

General Description

The CMOS bq4015 is a nonvolatile 4,194,304-bit static RAM organized as 524,288 words by 8 bits. The integral control circuitry and lithium energy source provide reliable nonvolatility coupled with the unlimited write cycles of standard SRAM.

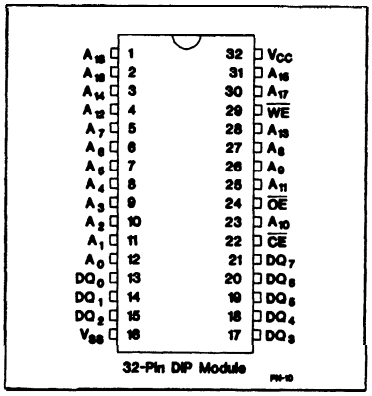
The control circuitry constantly monitors the single 5V eupply for an out-of-tolerance condition. When Vcc falls out of tolerance, the SRAM is unconditionally write-protected to prevent an inadvertent write operation.

At this time the integral energy source is switched on to sustain the memory until after Vcc returns valid.

The bq4015 uses extremely low etandby current CMOS SRAMs, coupled with small lithium coin cells to provide nonvolatility without long write-cycle times and the write-cycle limitations associated with EEPROM.

The bq4015 requires no external circuitry and is compatible with the industry-standard 4Mb SRAM pinout.

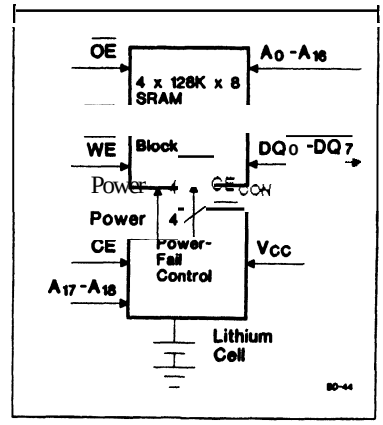
Pin Connections



Pin Names

AO-A18	Address inputs
DQ0-DQ7	Data input/output
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input
$\overline{WE}$	Write enable input
Vcc	+5 voh supply input
Vss	Ground

Block Diagram



Selection Guide

Part Number	Maximum Access Time (ns)	Negative Supply Tolerance	Part Number	Maximum Access Time (ns)	Negative Supply Tolerance
bq4015MA -70	70	-5%	bq4015YMA -70	70	-10%
bq4015MA -85 bq4015MB -85	85	-5%	bq4015YMA -85 bq4015YMB -85	85	-10%
bq4015MB -120	120	-5%	bq4015YMB -120	120	-10%

Functional Description

When power is valid, the bq4015 operates as a standard CMOS SRAM. During power-down and power-up cycles, the bq4015 acts as a nonvolatile memory, automatically protecting and preserving the memory contents.

Power-down/power-up control circuitry constantly monitors the V_{CC} supply for a power-fail-detect threshold V_{PFD}. The bq4015 monitors for $V_{PFD} = 4.62V$ typical for use in systems with 5% supply tolerance. The bq4015Y monitors for $V_{PFD} = 4.37V$ typical for use in systems with 10% supply tolerance.

When V_{CC} falls below the V_{PFD} threshold, the SRAM automatically write-protects the data. All outputs become high impedance, and all inputs are treated as 'don't care.' If a valid access is in process at the time of power-fail detection, the memory cycle continues to completion. If the memory cycle fails to terminate within time t_{WPT}, write-protection takes place.

As V_{CC} falls past V_{PFD} and approaches 3V, the control circuitry switches to the internal lithium backup supply, which provides data retention until valid V_{CC} is applied.

When V_{CC} returns to a level above the internal backup cell voltage, the supply is switched back to V_{CC}. *After* V_{CC} ramps above the V_{PFD} threshold, write-protection continues for a time t_{CER} (120ms maximum) to allow for processor stabilization. Normal memory operation may resume after this time.

The internal coin cells used by the bq4015 have an extremely long shelf life and provide data retention for more than 10 years in the absence of system power.

As shipped from Benchmarq, the integral lithium cells are electrically isolated from the memory. (Self-discharge in this condition is approximately 0.5% per year.) Following the first application of V_{CC}, this isolation is broken, and the lithium backup provides data retention on subsequent power-downs.

Truth Table

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Operation	Power
Not selected	H	X	X	High Z	Standby
Output disable	L	H	H	High Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \le V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
		-40 to +85	°C	Industrial "N"
T_{STG}	storage temperature	-40 to +70	°C	Commercial
		-40 to +85	°C	Industrial "N"
T_{BIAS}	Temperature under bias	-10 to +70	°C	Commercial
		-40 to +85	°C	Industrial "N"
T_{SOLDER}	Soldering temperature	+260	°C	For 10 seconds

Note: Pennanent device damage may occur if **Absolute Maximum Ratings are exceeded. Functional** operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. *Exposure* to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	bq4015Y
		4.75	5.0	5.5	V	bq4015
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at $T_A = 25°C$.

DC Electrical Characteristics ($T_A = T_{OPR}$, $V_{CCmin} \leq V_{CC} \leq V_{CCmax}$)

Symbol	Parameter	Minimum	Typical	Mulmum	Unit	Conditions/Notes
I_{LI}	Input leakage current (bq4015MA)			± 1	µA	$V_{IN} = V_{SS}$ to V_{CC}
	Input leakage current (bq4015MB)			± 4	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current (bq4015MA)			± 1	µA	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
	Output leakage current (bq4015MB)			± 4	µA	
V_{OH}	Output high voltage	2.4			V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage			0.4	V	I_{OL} = 2.1 mA
I_{SB1}	Standby supply current (bq4015MA)		3	5	mA	$\overline{CE} = V_{IH}$
	Standby supply current (bq4015MB)		7	17	mA	
I_{SB2}	Standby supply current (bq4015MA)		0.1	1	mA	$\overline{CE} \geq V_{CC}$ - 0.2V, 0V ≤ $V_{IN} \leq$ 0.2V, or $V_{IN} \geq V_{CC}$ - 0.2
	Standby supply current (bq4015MB)		2.5	5	mA	
I_{CC}	Operating supply current (bq4015MA)			90	mA	Min. cycle, duty = 100%, $\overline{CE} = V_{IL}$, $I_{I/O}$ = 0mA, A17 < V_{IL} or A17 > V_{IH}, A18 < V_{IL} or A18 > V_{IH}
	Operating supply current (bq4015MB)		75	115	mA	
V_{PFD}	Power-fail-detect voltage	4.55	4.62	4.75	V	bq4015
		4.30	4.37	4.50	V	bq4015Y
V_{SO}	Supply switch-over voltage		3		V	

Note: Typical values indicate operation at $T_A = 25°C$, $V_{CC} = 5V$.

6

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance (bq4015MA)	-	-	8	pF	Output voltage = 0V
	Input/output capacitance (bq4015MB)	-	-	40	pF	
C_{IN}	Input capacitance (bq4015MA)	-	-	10	pF	Input voltage = 0V
	Input capacitance (bq4015MB)	-	-	40	pF	

Note: These parameters are sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 1 and 2

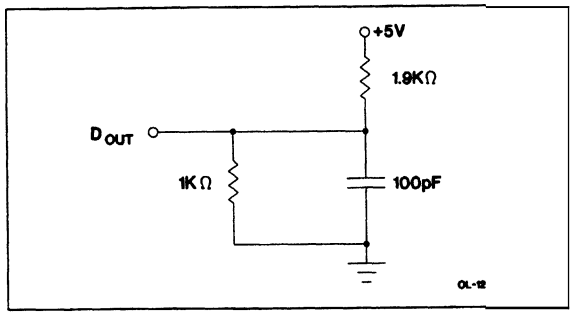


Figure 1. Output Load A

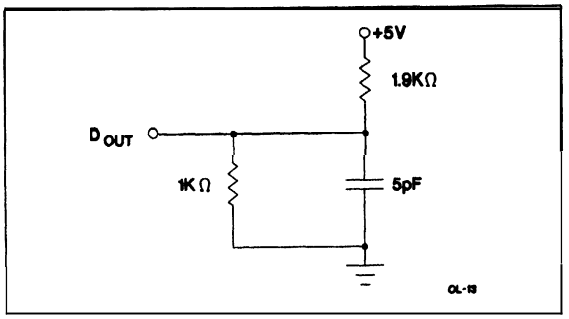
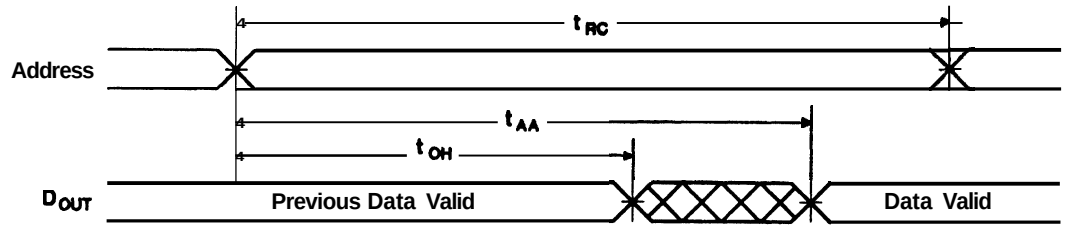


Figure 2. Output Load B

Read Cycle (T_A = TOPR, V_{CC}min ≤ V_{CC} ≤ V_{CC}max)

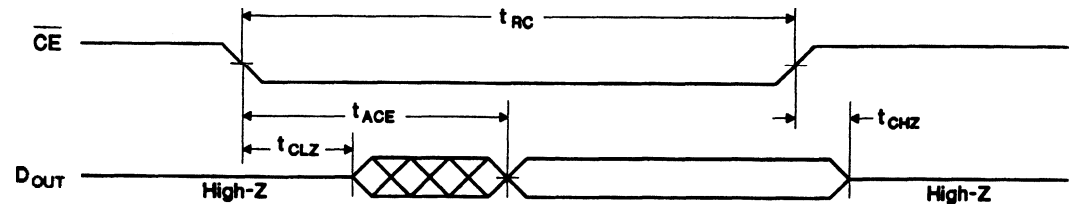
Symbol	Parameter	-70		-85/-85N		-120/-120N		Unit	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read cycle time	70	-	85	-	120	-	ns	
t_{AA}	Address access time	-	70	-	85	-	120	ns	Output load A
t_{ACE}	Chip enable access time	-	70	-	85	-	120	ns	Output load A
t_{OE}	Output enable to output valid	-	35	-	45	-	60	ns	Output load A
t_{CLZ}	Chip enable to output in low Z	5	-	5	-	5	-	ns	Output load B
t_{OLZ}	Output enable to output in low Z	5	-	0	-	0	-	ns	Output load B
t_{CHZ}	Chip disable to output in high Z	0	25	0	35	0	45	ns	Output load B
t_{OHZ}	Output disable to output in high Z	0	25	0	25	0	35	ns	Output load B
t_{OH}	Output hold from address change	10	-	10	-	10	-	ns	Output load A

Read Cycle No. 1 (Address Access) [1,2]



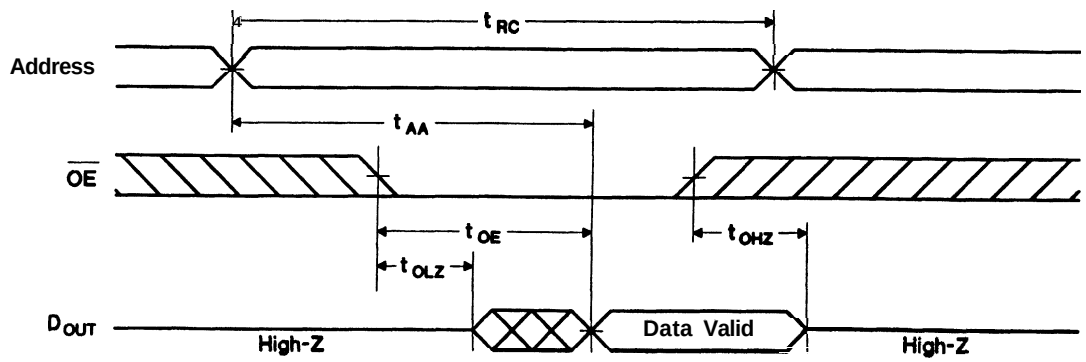
RC-1

Read Cycle No. 2 ($\overline{CE}$ Access) 1,3,4



RC-2

Read Cycle No. 3 ($\overline{OE}$ Access)



RC-3

Notes:
1. $\overline{WE}$ is held high for a read cycle.
2. Device is continuously selected: $\overline{CE} = \overline{OE} = V_{IL}$.
3. Address is valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Device is continuously selected: $\overline{CE} = V_{IL}$.

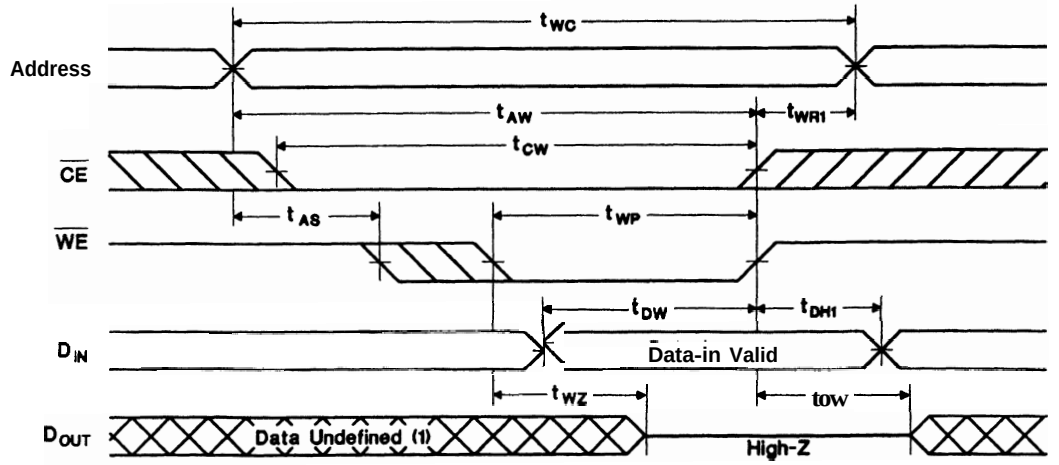
Write Cycle (TA = TOPR, VCCmin ≤ VCC ≤ VCCmax)

Symbol	Parameter	-70		-85/-85N		-120/-120N		Units	Conditions/Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{WC}	Write cycle time	70	-	85	-	120	-	ns	
t_{CW}	Chip enable to end of write	65	-	75	-	100	-	ns	(1)
t_{AW}	Address valid to end of write	65	-	75	-	100	-	ns	(1)
t_{AS}	Address setup time	0	-	0	-	0	-	ns	Measured from address valid to beginning of write. (2)
t_{WP}	Write pulse width	55	-	65	-	85	-	ns	Measured from beginning of write to end of write. (1)
t_{WR1}	Write recovery time (write cycle 1)	5	-	5	-	5	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
t_{WR2}	Write recovery time (write cycle 2)	15	-	15	-	15	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (3)
t_{DW}	Data valid to end of write	30	-	35	-	45	-	ns	Measured to first low-to-high transition of either $\overline{CE}$ or $\overline{WE}$.
t_{DH1}	Data hold time (write cycle 1)	0	-	0	-	0	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (4)
t_{DH2}	Data hold time (write cycle 2)	10	-	10	-	10	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (4)
t_{WZ}	Write enabled to output in high Z	0	25	0	30	0	40	ns	I/O pins are in output state. (5)
tow	Output active from end of write	5	-	0	-	0	-	ns	I/O pins are in output state. (5)

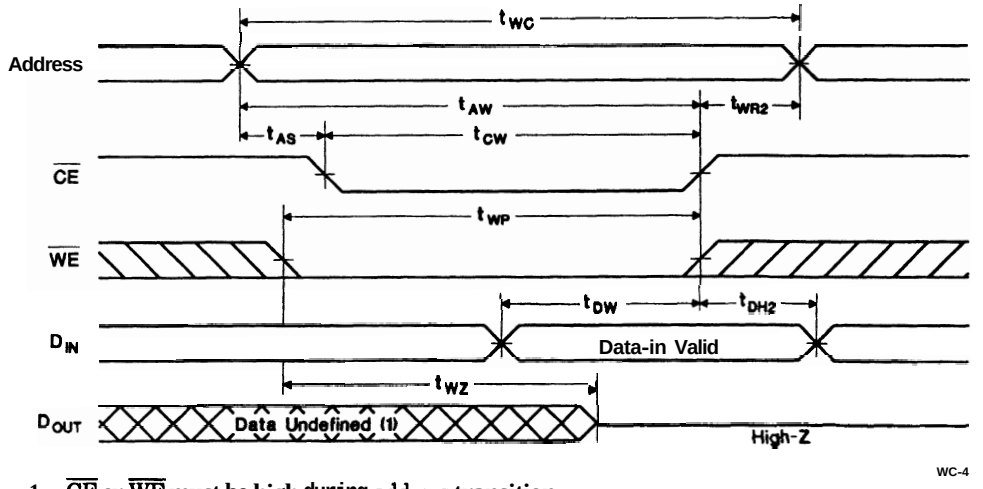
Notes:

1. A write ends at the earlier transition of $\overline{CE}$ going high and $\overline{WE}$ going high.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CE}$ going low and $\overline{WE}$ going low.
3. Either t_{WR1} or t_{WR2} must be met.
4. Either t_{DH1} or t_{DH2} must be met.
5. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

Write Cycle No. 1 ($\overline{WE}$-Controlled) 1,2,3



Write Cycle No. 2 (%Controlled) 1,2,3,4,5



Notes:
1. $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
2. Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
3. If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.
4. Either t_{WR1} or t_{WR2} must be met.
5. Either t_{DH1} or t_{DH2} must be met.

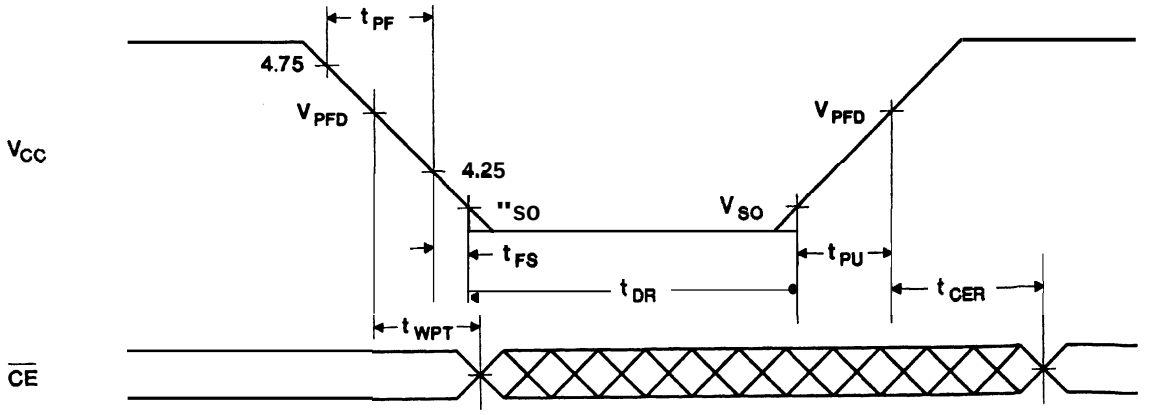
Power-Down/Power-Up Cycle (T_A = TOPR)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_{PF}	V_{CC} slew, 4.75 to 4.25 V	300			µs	
t_{FS}	V_{CC} slew, 4.25 to V_{SO}	10			µs	
t_{PU}	V_{CC} slew, V_{SO} to V_{PFD} (max.)	0			µs	
t_{CER}	Chip enable recovery time	40	80	120	ms	Time during which SRAM is Write-protected after V_{CC} passes V_{PFD} on power-up.
t_{DR}	Data-retention time in absence of V_{CC}	10			years	T_A = 25°C.(2)
t_{WPT}	Write-protect time	40	100	150	µs	Delay after Vcc slews down past V_{PFD} before SRAM is write-protected.

Notes:
1. Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.
2. Batteries are disconnected from circuit until after V_{CC} is applied for the first time. t_{DR} is the accumulated time in absence of power beginning when power is first applied to the device.

Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

Power-Down/Power-Up Timing



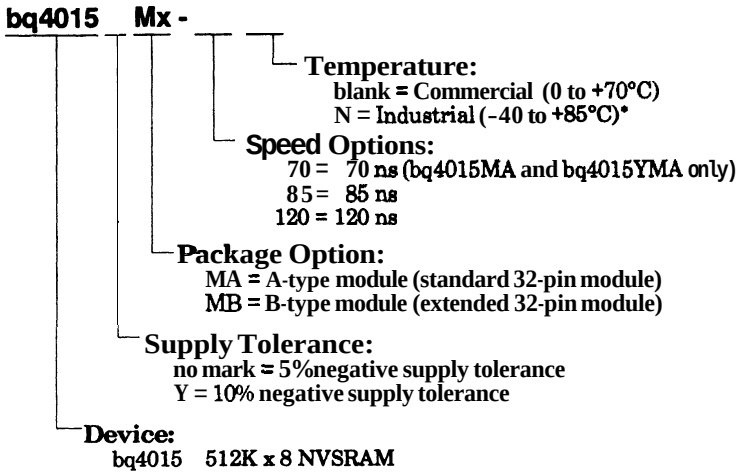
PD-B

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	3	I_{CC} test conditions	Clarification
2	1, 2, 3, 4, 7, 8, 10	bq4015MA part	Addition
3	2, 10	Added industrial temperature range	Addition

Note: Change 1 = Sept. 1992 B changes from Sept. 1990 A
Change 2 = Nov. 1993 C changw fromSept. 1992 B.
Change 3 = June 1996 C changes from Nov. 1993 C.

Ordering Information



*Note:
Only 10% supply "Y" version is available in industrial temperature range; contact factory for speed grade availability.

bq4016/bq4016Y

1024Kx8 Nonvolatile SRAM

Features

- Data retention in the absence of power
- Automatic write-protection during power-up/power-down cycles
- Conventional SRAM operation; unlimited write cycles
- 10-year minimum data retention in absence of power
- Battery internally isolated until power is applied

General Description

The CMOS **bq4016** is a nonvolatile 8,388,608-bit static RAM organized as 1,048,576 words by 8 bits. The integral control circuitry and lithium energy source provide reliable nonvolatility coupled with the unlimited write cycles of standard SRAM.

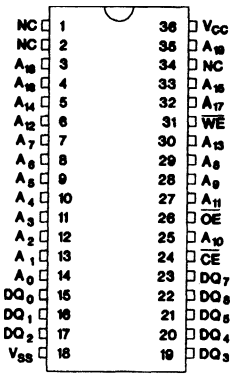
The control circuitry conetantly monitors the single 5V supply for an out-of-tolerance condition. When V_{CC} falls out of tolerance, the SRAM in unconditionally write-protected to prevent an inadvertent write operation.

At this time the integral energy source is switched on to sustain the memory until after V_{CC} returns valid.

The **bq4016** uees extremely low standby current CMOS SRAMs, coupled with a small lithium coin cell to provide nonvolatility without long write-cycle times and the write-cycle limitations associated with EEPROM.

The **bq4016** has the same interface as industry-standard SRAMs and requires no external circuitry.

Pin Connections

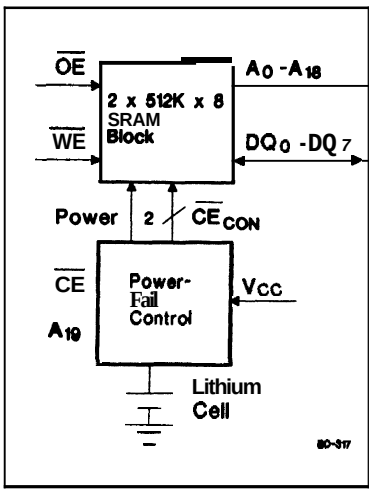


36-Pin DIP Module

Pin Names

A_0-A_{19}	Address inputs
DQ_0-DQ_7	Data input/output
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input
$\overline{WE}$	Write enable input
V_{CC}	+5 volt supply input
V_{SS}	Ground
NC	No connect

Block Diagram



Selection Guide

Part Number	Maximum Access Time (ns)	Negative Supply Tolerance	Part Number	Maximum Access Time (ns)	Negative Supply Tolerance
bq4016MC-70	70	-5%	bq4016YMC-70	70	-10%

Functional Description

When power is valid, the bq4016 operates as a standard CMOS SRAM. During power-down and power-up cycles, the bq4016 acts as a nonvolatile memory, automatically protecting and preserving the memory contents.

Power-down/power-up control circuitry constantly monitors the V_{CC} supply for a power-fail-detect threshold V_{PFD}. The bq4016 monitors for V_{PFD} = 4.62V typical for use in systems with 5% supply tolerance. The bq4016Y monitors for V_{PFD} = 4.37V typical for use in systems with 10% supply tolerance.

When V_{CC} falls below the V_{PFD} threshold, the SRAM automatically write-protects the data. All outputs become high impedance, and all inputs are treated as 'don't care.' If a valid access is in process at the time of power-fail detection, the memory cycle continues to completion. If the memory cycle fails to terminate within time t_{WPT}, write-protectiontakes place.

As V_{CC} falls past V_{PFD} and approaches 3V, the control circuitry switches to the internal lithium backup supply, which provides data retention until valid V_{CC} is applied.

When V_{CC} returns to a level above the internal backup cell voltage, the supply is switched back to V_{CC}. After V_{CC} ramps above the V_{PFD} threshold, write-protection continues for a time t_{CER} (120ms maximum) to allow for processor stabilization. Normal memory operation may resume after this time.

The internal coin cells used by the bq4016 have an extremely long shelf life. The bq4016 provides data retention for more than 10 years in the absence of system power.

As shipped from Benchmarq, the integral lithium cells are electrically isolated from the memory. (Self-discharge in this condition is approximately 0.5% per year.) Following the first application of V_{CC}, this isolation is broken, and the lithium backup provides data retention on subsequent power-downs.

Truth Table

Mode	$\overline{CE}$	WE	$\overline{OE}$	I/O Operation	Power
Not selected	H	X	X	High Z	Standby
Output disable	L	H	H	High Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \le V_{CC}$ + 0.3
T_{OPR}	Operating temperature	0 to +70	"C	
T_{STG}	Storage temperature	-40 to +70	°C	
T_{BIAS}	Temperature under bias	-10 to +70	"C	
T_{SOLDER}	Soldering temperature	+260	°C	For 10 seconds

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operationallimits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	bq4016Y
		4.75	5.0	5.5	V	bq4016
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3		0.8	V	
V_{IH}	Input high voltage	2.2		V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C.

DC Electrical Characteristics (T_A = 0 to 70°C, $V_{CCmin} \leq V_{CC} \leq V_{CCmax}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 2	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current	-	-	± 2	µA	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 2.1 mA
I_{SB1}	Standby supply current		5	12	mA	$\overline{CE} = V_{IH}$
I_{SB2}	Standby supply current		2.5	5	mA	$0V \leq Vm \leq 0.2V$, $\overline{CE} \geq V_{CC} - 0.2V$, or $V_{IN} \geq V_{CC} - 0.2$
I_{CC}	Operating supply current		75	115	mA	Min. cycle, duty = 100%, $\overline{CE} = V_{IL}$, $I_{I/O}$ = 0mA, A19 < V_{IL} or A19 > V_{IH},
V_{PFD}	Power-fail-detect voltage	4.55	4.62	4.75	V	bq4016
		4.30	4.37	4.50	V	bq4016Y
V_{SO}	Supply switch-over voltage		3		V	

Note: Typical values indicate operation at T_A = 25°C, Vcc = 5V.

6

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	20	pF	Output voltage = 0V
C_{IN}	Input capacitance	-	-	20	pF	Input voltage = 0V

Note: These parameters are sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)

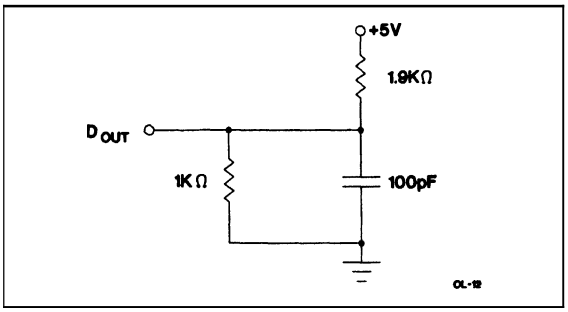


Figure 1. Output Load A

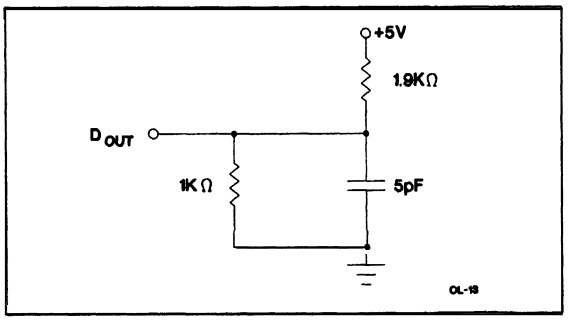
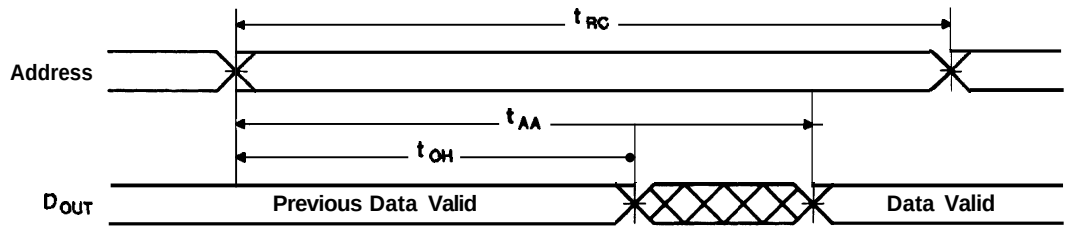


Figure 2. Output Load B

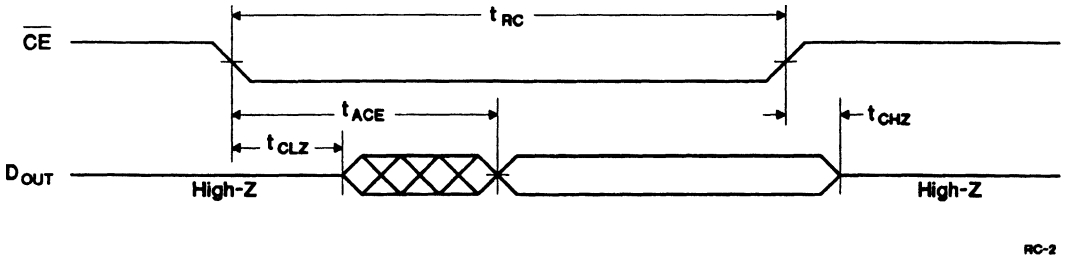
Read Cycle (T_A = 0 to 70°C, $V_{CCmin} \le V_{CC} \le V_{CCmax}$)

Symbol	Parameter	-70 Min.	-70 Max.	Unit	Conditions
t_{RC}	Read cycle time	70		ns	
t_{AA}	Address access time		70	ns	Output load A
t_{ACE}	Chip enable access time		70	ns	Output load A
t_{OE}	Output enable to output valid		35	ne	Output load A
t_{CLZ}	Chip enable to output in low Z	5		ns	Output load B
t_{OLZ}	Output enable to output in low Z	5		ns	Output load B
t_{CHZ}	Chip disable to output in high Z	0	25	ns	Output load B
t_{OHZ}	Output disable to output in high Z	0	25	ns	Output load B
t_{OH}	Output hold from address change	10		ns	Output load A

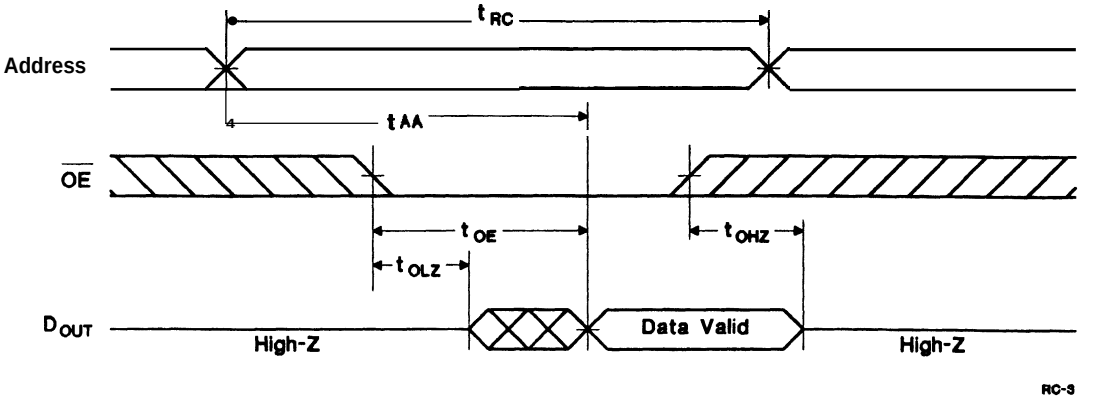
Read Cycle No. 1 (Address Access) [1,2]



Read Cycle No. 2 ($\overline{CE}$ Access) [1,3,4]



Read Cycle No. 3 ($\overline{OE}$ Access) [1,5]



Notes:
1. $\overline{WE}$ is held high for a read cycle.
2. Device is continuously selected: $\overline{CE} = \overline{OE} = V_{IL}$.
3. Address is valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Device is continuously selected: $\overline{CE} = V_{IL}$.

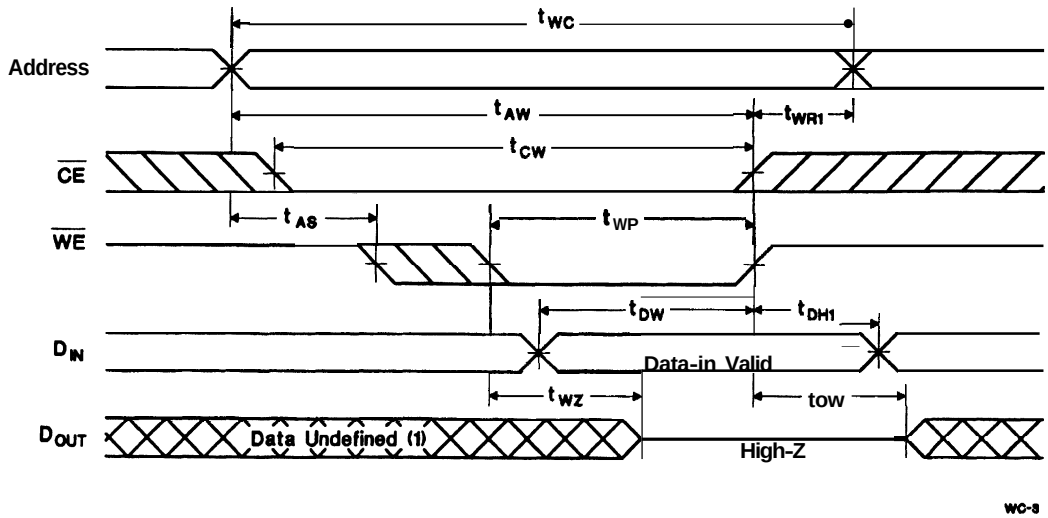
Write Cycle (TA = 0 to 70°C, VCCmin ≤ VCC ≤ VCCmax)

Symbol	Parameter	-70 Min.	-70 Max.	Units	Conditions/Notes
t_{WC}	Write cycle time	70		ns	
t_{CW}	Chip enable to end of write	66		ns	(1)
t_{AW}	Address valid to end of write	66		ns	(1)
t_{AS}	Address setup time	0		ns	Measured from address valid to beginning of write. (2)
t_{WP}	Write pulse width	55		ns	Measured from beginning of write to end of write. (1)
t_{WR1}	Write recovery time (write cycle 1)	5		ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
t_{WR2}	Write recovery time (write cycle 2)	15		ns	Measured from $\overline{CE}$ going high to end of write cycle. (3)
t_{DW}	Data valid to end of write	30	-	ns	Measured to first low-to-transition of either $\overline{CE}$ or
t_{DH1}	Data hold time (write cycle 1)	0		ns	Measured from $\overline{WE}$ going high to end of write cycle. (4)
t_{DH2}	Data hold time (write cycle 2)	10		ns	Measured from $\overline{CE}$ going high to end of write cycle. (4)
t_{WZ}	Write enabled to output in high Z	0	25	ns	I/O pins are in output state. (5)
tow	Output active from end of write	5		ns	I/O pins are in output state. (5)

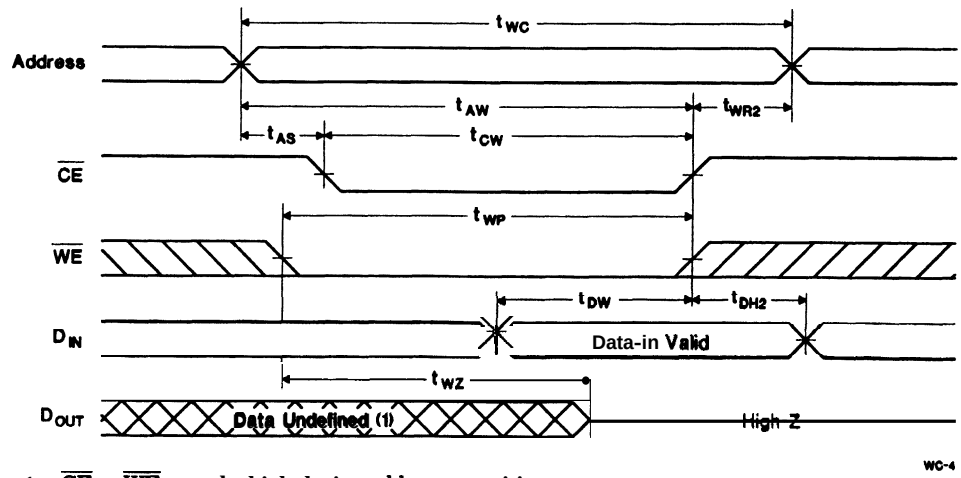
Notes:

1. A write ends at the earlier transition of $\overline{CE}$ going high and $\overline{WE}$ going high.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CE}$ going low and $\overline{WE}$ going low.
3. Either t_{WR1} or t_{WR2} must be met,
4. Either t_{DH1} or t_{DH2} must be met.
5. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

Write Cycle No. 1 ($\overline{WE}$-Controlled) 1,2,3



Write Cycle No. 2 ($\overline{CE}$-Controlled) 1,2,3,4,5



6

Notes:

1. $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
2. Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
3. If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.
4. Either t_{WR1} or t_{WR2} must be met.
5. Either t_{DH1} or t_{DH2} must be met.

Power-Down/Power-Up Cycle (T_A = 0 to 70°C)

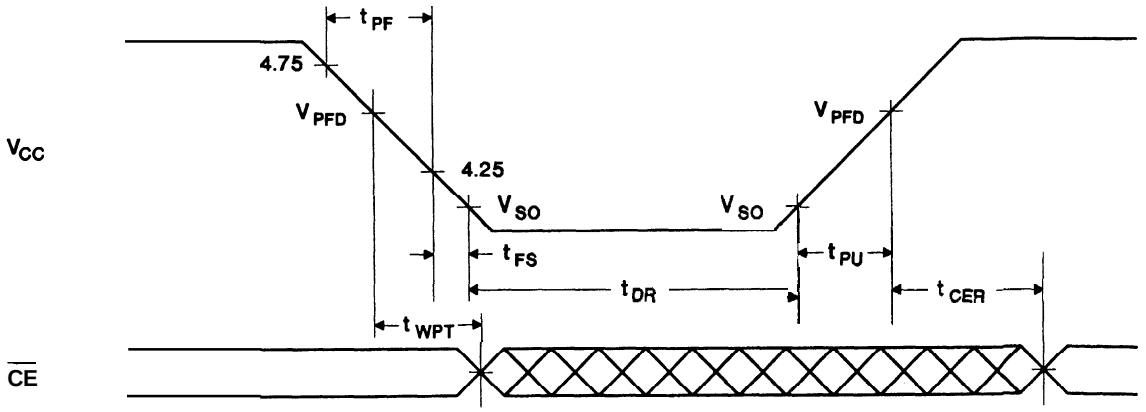
Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_{PF}	V_{CC} slew, 4.75 to 4.25 V	300			µs	
t_{FS}	V_{CC} slew, 4.25 to V_{SO}	10			µs	
t_{PU}	V_{CC} slew, V_{SO} to V_{PFD} (max.)	0			µs	
t_{CER}	Chip enable recovery time	40	80	120	ms	Time during which SRAM is write-protected after V_{CC} passes V_{FPD} on power-up.
t_{DR}	Data-retention time in absence of V_{CC}	10			years	T_A = 25°C.(2)
t_{WPT}	Write-protect time	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.

Notes: 1. Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.

2. Batteries are disconnected from circuit until after V_{CC} is applied for the first time. t_{DR} is the accumulated time in absence of power beginning when power is first applied to the device.

Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

Power-Down/Power-Up Timing



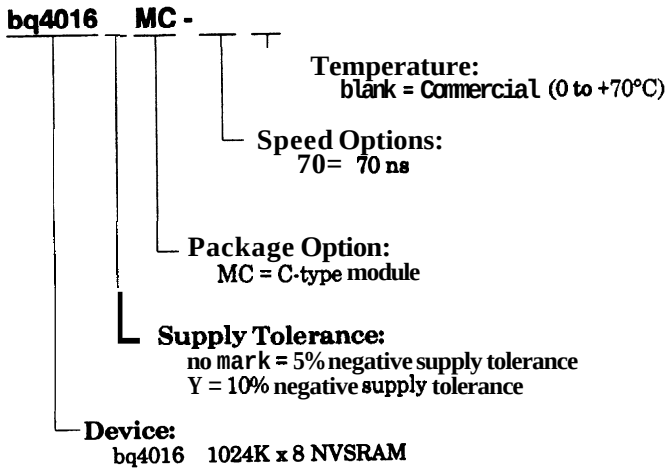
PD-B

Data Sheet Revision History

Change No.	Page No.	Description
1	All	Changed from "Preliminary" to 'Final* data sheet

Notes: Change 1 = Sept 1996 B changes from June 1996.

Ordering Information



bq4017/bq4017Y

2048Kx8 Nonvolatile SRAM

Features

- Data retention in the absence of power
- Automatic write-protection during power-up/power-down cycles
- Conventional SRAM operation; unlimited write cycles
- 6-year minimum data retention in absence of power
- Battery internally isolated until power is applied

General Description

The CMOS bq4017 is a nonvolatile 16,777,216-bit static RAM organized as 2,097,152 words by 8 bits. The integral control circuitry and lithium energy source provide reliable nonvolatility coupled with the unlimited write cycles of standard SRAM.

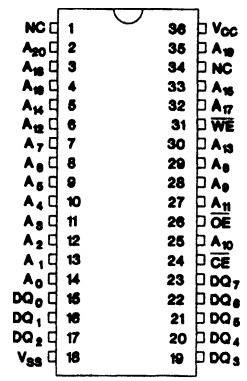
The control circuitry conetantly monitors the single 5V supply for an out-of-tolerance condition. When V_{CC} falls out of tolerance, the SRAM is unconditionally write-protected to prevent an inadvertent write operation.

At this time the integral energy source is switched on to sustain the memory until after V_{CC} returns valid.

The bq4017 user extremely low standby current CMOS SRAMs, coupled with small lithium coin cells to provide nonvolatility without long write-cycle times and the write-cycle limitations associated with EEPROM.

The bq4017 has the same interface as industry-standard SRAMs and requires no external circuitry.

Pin Connections

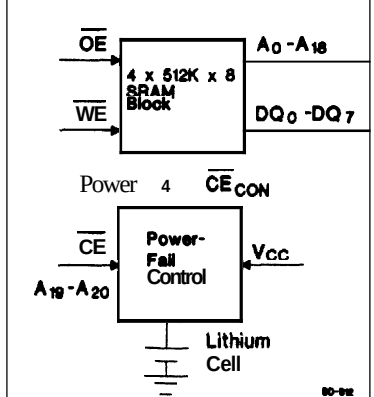


36-Pin DIP Module

Pin Names

A_0-A_{20}	Address inputs
DQ_0-DQ_7	Data input/output
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input
$\overline{WE}$	Write enable input
V_{CC}	+5 volt supply input
V_{SS}	Ground
NC	No connect

Block Diagram



Selection Guide

Part Number	Maximum Access Time (ns)	Negative Supply Tolerance	Part Number	Maximum Access Time (ns)	Negative Supply Tolerance
bq4017MC-70	70	-5%	bq4017YMC-70	70	-10%

Functional Description

When power is valid, the bq4017 operates as a standard CMOS SRAM. During power-down and power-up cycles, the bq4017 acts as a nonvolatile memory, automatically protecting and preserving the memory contents.

Power-down/power-up control circuitry constantly monitors the V_{CC} supply for a power-fail-detect threshold V_{PFD}. The bq4017 monitors for V_{PFD} = 4.62V typical for use in systems with 5% supply tolerance. The bq4017Y monitors for V_{PFD} = 4.37V typical for use in systems with 10% supply tolerance.

When V_{CC} falls below the V_{PFD} threshold, the SRAM automatically write-protects the data. All outputs become high impedance, and all inputa are treated as 'don't care.' If a valid access is in process at the time of power-fail detection, the memory cycle continues to completion. If the memory cycle fails to terminate within time t_{WPT}, write-protection takes place.

As V_{CC} falls past V_{PFD} and approaches 3V, the control circuitry switches to the internal lithium backup supply, which provides data retention until valid V_{CC} is applied.

When V_{CC} returns to a level above the internal backup cell voltage, the supply is switched back to V_{CC}. After V_{CC} ramps above the V_{PFD} threshold, write-protection continues for a time t_{CER} (120ms maximum) to allow for processor stabilization. Normal memory operation may resume after this time.

The internal coin cells used by the bq4017 have an extremely long shelf life. The bq4017 provides data retention for more than 5 years in the absence of system power.

As shipped from Benchmarq, the integral lithium cells are electrically isolated from the memory. (Self-discharge in this condition is approximately 0.5% per year.) Following the first application of V_{CC}, this isolation is broken, and the lithium backup provides data retention on subsequent power-downs.

Truth Table

Mode	$\overline{CE}$	WE	$\overline{OE}$	I/O Operation	Power
Not selected	H	X	X	High Z	Standby
Output disable	L	H	H	High Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \le V_{CC}$ + 0.3
T_{OPR}	Operating temperature	0 to +70	°C	
T_{STG}	Storage temperature	-40 to +70	°C	
T_{BIAS}	Temperature under bias	-10 to +70	°C	
T_{SOLDER}	Soldering temperature	+260	°C	For 10 seconds

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	bq4017Y
		4.75	5.0	5.5	V	bq4017
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3		0.8	V	
V_{IH}	Input high voltage	2.2		V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C.

DC Electrical Characteristics (T_A = 0 to 70°C, $V_{CCmin} \le V_{CC} \le V_{CCmax}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current			±4	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current			±4	µA	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
V_{OH}	Output high voltage	2.4			V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage			0.4	V	I_{OL} = 2.1 mA
I_{SB1}	Standby supply current		7	17	mA	$\overline{CE} = V_{IH}$
I_{SB2}	Standby supply current		2.5	5	mA	0V ≤ V_{IN} ≤ 0.2V, $\overline{CE}$ ≥ V_{CC} - 0.2V, or $V_{IN} \ge V_{CC}$ - 0.2
I_{CC}	Operating supply current		75	115	mA	Min. cycle, duty = 100%, $\overline{CE} = V_{IL}$, $I_{I/O}$ = 0mA, A19 < V_{IL} or A19 > V_{IH}, A20 < V_{IL} or A20 > V_{IH}
V_{PFD}	Power-fail-detect voltage	4.55	4.62	4.75	V	bq4017
		4.30	4.37	4.50	V	bq4017Y
V_{SO}	Supply switch-over voltage		3		V	

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.

6

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance			40	pF	Output voltage = 0V
C_{IN}	Input capacitance			40	pF	Input voltage = 0V

Note: These parameters are sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 1 and 2

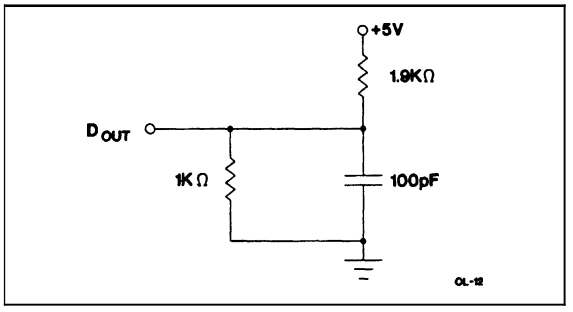


Figure 1. Output Load A

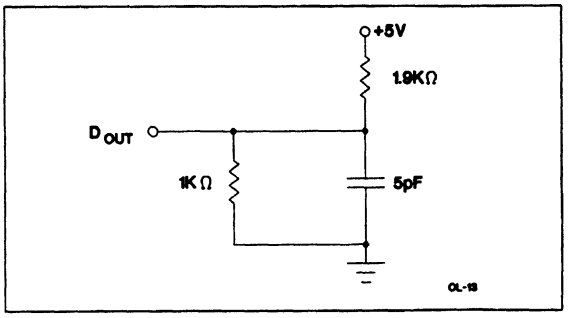
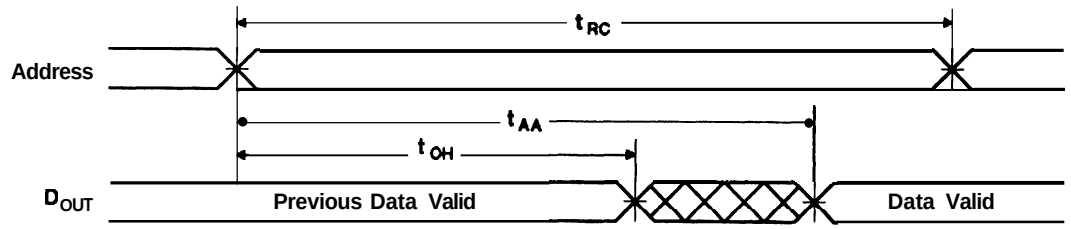


Figure 2. Output Load B

Read Cycle (T_A = 0 to 70°C, $V_{CCmin} \le V_{CC} \le V_{CCmax}$)

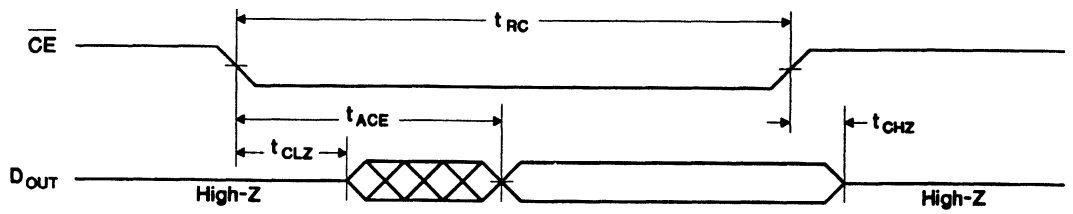
Symbol	Parameter	-70		Unit	Conditions
		Min.	Max.		
t_{RC}	Read cycle time	70		ns	
t_{AA}	Address access time		70	ns	Output load A
t_{ACE}	Chip enable access time		70	ns	Output load A
t_{OE}	Output enable to output valid		35	ns	Output load A
t_{CLZ}	Chip enable to output in low Z	6		ns	Output load B
t_{OLZ}	Output enable to output in low Z	5		ns	Output load B
t_{CHZ}	Chip disable to output in high Z	0	25	ns	Output load B
t_{OHZ}	Output disable to output in high Z	0	25	ns	Output load B
t_{OH}	Output hold from address change	10		ns	Output load A

Read Cycle No. 1 (Address Access) [1,2]



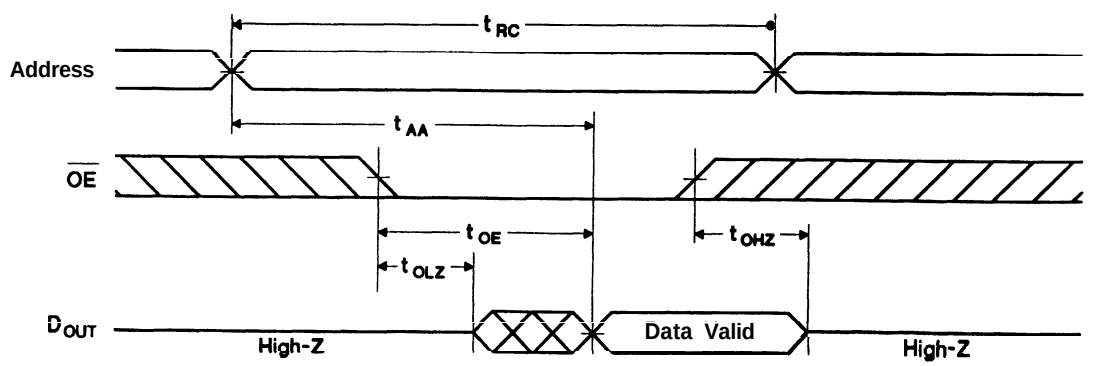
RC-1

Read Cycle No. 2 ($\overline{CE}$ Access) [1,3,4]



RC-2

Read Cycle No. 3 ($\overline{OE}$ Access) [1,5]



RC-3

Notes:
1. $\overline{WE}$ is held high for a read cycle.
2. Device is continuously selected: $\overline{CE} = \overline{OE} = V_{IL}$.
3. Address is valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Device is continuously selected: $\overline{CE} = V_{IL}$.

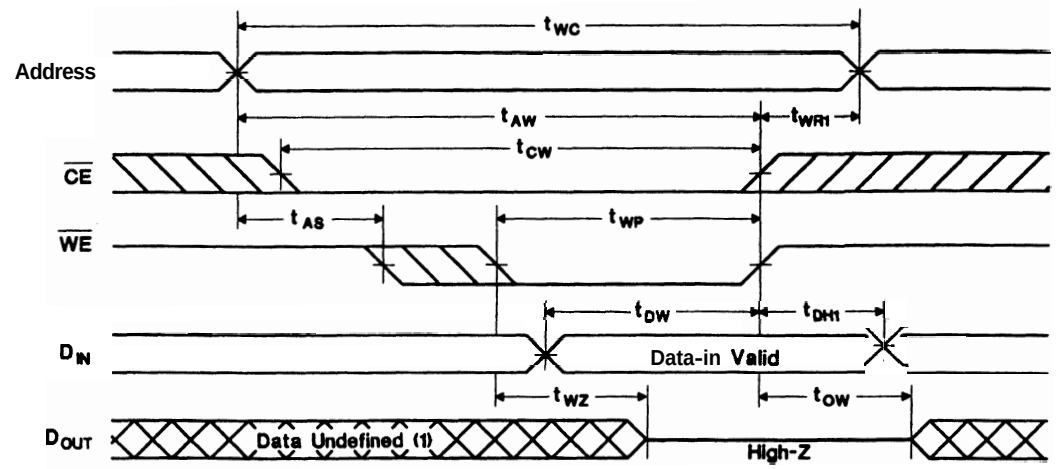
Write Cycle (T_A = 0 to 70°C, $V_{CCmin} \le V_{CC} \le V_{CCmax}$)

Symbol	Parameter	-70 Min.	-70 Max.	Units	Conditions/Notes
t_{WC}	Write cycle time	70		ns	
t_{CW}	Chip enable to end of write	65		ns	(1)
t_{AW}	Address valid to end of write	65		ns	(1)
t_{AS}	Address setup time	0		ns	Measured from address valid to beginning of writs. (2)
t_{WP}	Write pulse width	55		ns	Measured from beginning of write to end of write. (1)
t_{WR1}	Write recovery time (write cycle 1)	5		ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
t_{WR2}	Write recovery time (write cycle 2)	15		ns	Measured from $\overline{CE}$ going high to end of write cycle. (3)
t_{DW}	Data valid to end of write	30		ns	Measured to first low-to-high transition of either $\overline{CE}$ or $\overline{WE}$.
t_{DH1}	Data hold time (write cycle 1)	0		ns	Measured from $\overline{WE}$ going high to end of write cycle. (4)
t_{DH2}	Data hold time (write cycle 2)	10		ns	Measured fmm $\overline{CE}$ going high to end of write cycle. (4)
t_{WZ}	Write enabled to output in high Z	0	25	ns	I/O pins are in output state. (5)
tow	Output active from end of write	5	-	ns	I/O pins are in output state. (5)

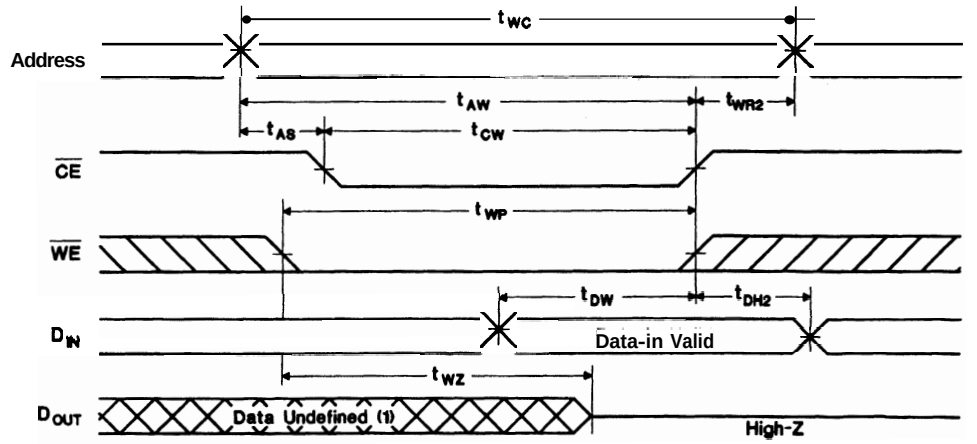
Notes:

1. A write ends at the earlier transition of $\overline{CE}$ going high and $\overline{WE}$ going high.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CE}$ going low and $\overline{WE}$ going low.
3. Either t_{WR1} or t_{WR2} must be met.
4. Either t_{DH1} or t_{DH2} must be met.
5. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

Write Cycle No. 1 ($\overline{WE}$-Controlled) 1,2,3



Write Cycle No. 2 ($\overline{CE}$-Controlled) 1,2,3,4,5



Notes:

1. $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
2. Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
3. If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.
4. Either t_{WR1} or t_{WR2} must be met.
5. Either t_{DH1} or t_{DH2} must be met.

Power-Down/Power-Up Cycle (T_A = 0 to 70°C)

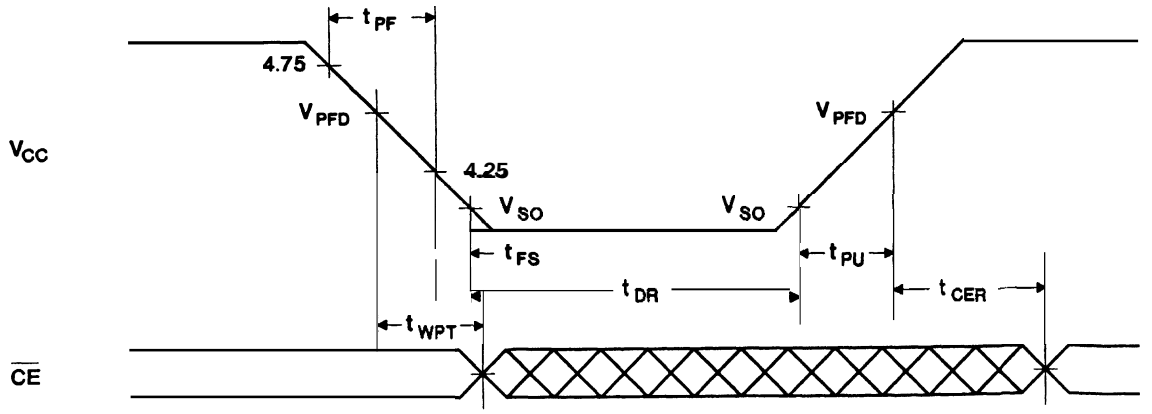
Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_{PF}	V_{CC} slew, 4.75 to 4.25 V	300			µs	
t_{FS}	V_{CC} slew, 4.25 to V_{SO}	10			µs	
t_{PU}	V_{CC} slew. V_{SO} to V_{PFD} (max.)	0			µs	
t_{CER}	Chip enable recovery time	40	80	120	ms	Time during which SRAM is write-protected after V_{CC} passes V_{FPD} on power-up.
t_{DR}	Data-retention time in absence of V_{CC}	5			years	T_A = 25°C. (2)
t_{WPT}	Write-protect time	40	100	150	µs	Delay after Vcc slews down past V_{PFD} before SRAM is write-protected.

Notes: 1. Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.

2. Batteries are disconnected from circuit until after V_{CC} is applied for the first time. t_{DR} is the accumulated time in absence of power beginning when power is first applied to the device.

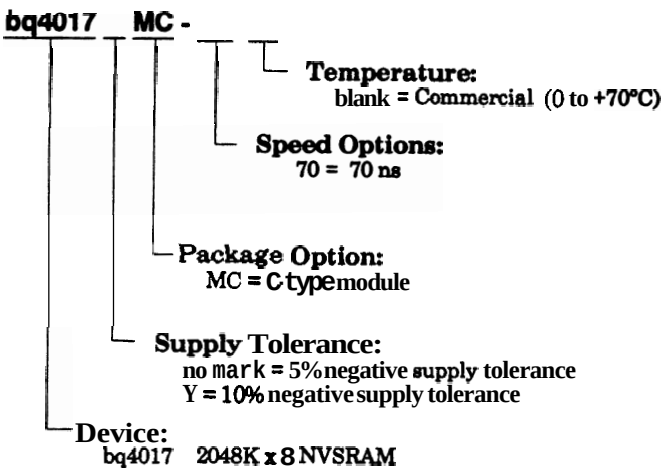
Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

Power-Down/Power-Up Timing



PD-8

Ordering Information



6

Notes

bq4024/bq4024Y

128Kx16 Nonvolatile SRAM

Features

- Data retention in the absence of power
- Automatic write-protection during power-up/power-down cycles
- Industry-standard 40-pin 128K x 16 pinout
- Conventional SRAM operation; unlimited write cycles
- 10-year minimum data retention in absence of power
- Battery internally isolated until power is applied

General Description

The CMOS **bq4024** is a nonvolatile 2,097,152-bit static **RAM** organized as 131,072 words by 16 **bits.** The integral control circuitry and lithium energy source provide reliable **nonvolatility** coupled with the unlimited write cycles of standard SRAM.

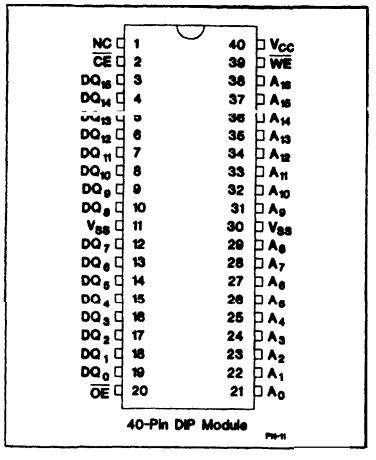
The control circuitry constantly **monitors** the **single** 5V **supply** for an out-of-tolerance condition. When **Vcc** falls out of tolerance, the SRAM is unconditionally write-protected to prevent an inadvertent write **operation.**

At this time the integral energy source is switched on to sustain the memory until after Vcc returns valid.

The **bq4024 uses** extremely low standby current CMOS **SRAMs,** coupled with small **lithium** coin **cells** to **provide** nonvolatility without long **write-cycle** times and **the** write-cycle **limitations associated** with **EEPROM.**

The bq4024 requires no external circuitry and is compatible with the industry-standard 2Mb SRAM **pinout.**

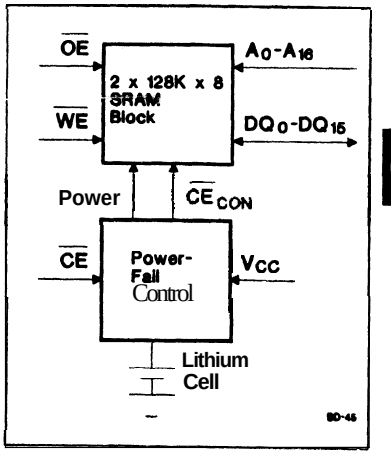
Pin Connections



Pin Names

A_0-A_{16}	Address inputs
DQ_0-DQ_{15}	Data input/output
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input
$\overline{WE}$	Write enable input
NC	No connect
Vcc	+5 volt supply input
Vss	Ground

Block Diagram



Selection Guide

Part Number	Maximum Access Time (ns)	Negative Supply Tolerance	Part Number	Maximum Access Time (ns)	Negative Supply Tolerance
bq4024 -85	85	-5%	bq4024Y -85	85	-10%
bq4024 -120	120	-5%	bq4024Y -120	120	-10%

Functional Description

When power is valid, the bq4024 operates as a standard CMOS SRAM. During power-down and power-up cycles, the bq4024 acts as a nonvolatile memory, automatically protecting and preserving the memory contents.

Power-down/power-up control circuitry constantly monitors the V_{CC} supply for a power-fail-detect threshold V_{PFD}. The bq4024 monitors for V_{PFD} = 4.62V typical for use in systems with 5% supply tolerance. The bq4024Y monitors for V_{PFD} = 4.37V typical for use in systems with 10% supply tolerance.

When V_{CC} falls below the V_{PFD} threshold, the SRAM automatically write-protect8 the data. All outputs become high impedance, and all inputs are treated as 'don't care.' If a valid access is in process at the time of power-fail detection, the memory cycle continues to completion. If the memory cycle fails to terminate within time t_{WPT}, write-protection takes place.

As V_{CC} falls past V_{PFD} and approaches 3V, the control circuitry switches to the internal lithium backup supply, which provides data retention until valid V_{CC} is applied.

When V_{CC} returns to a level above the internal backup cell voltage, the supply is switched back to V_{CC}. *After* V_{CC} ramps above the V_{PFD} threshold, write-prokction continues for a time t_{CER} (120ms maximum) to allow for processor stabilization. Normal memory operation may resume after this time.

The internal coin cells used by the bq4024 have an extremely long shelf life and provide data retention for more than 10 years in the absence of system power.

As shipped from Benchmarq, the integral lithium cells are electrically isolated from the memory. (Self-discharge in this condition is approximately 0.5% per year.) Following the first application of V_{CC}, this isolation is broken, and the lithium backup provides data retention on subsequent power-downs.

Truth Table

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Operation	Power
Not selected	H	X	X	High Z	Standby
Output disable	L	H	H	High Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	Dm	Active

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \le V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	
T_{STG}	Storage temperature	-40 to +70	°C	
T_{BIAS}	Temperature under bias	-10 to +70	°C	
T_{SOLDER}	Soldering temperature	+260	°C	For 10 seconds

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions (T_A = 0 to 70%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.6	5.0	5.5	V	bq4024Y
		4.75	5.0	5.5	V	bq4024
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3		0.8	V	
V_{IH}	Input high voltage	2.2		V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C.

DC Electrical Characteristics (T_A = 0 to 70°C, $V_{CCmin} \leq V_{CC} \leq V_{CCmax}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current			± 2	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current			± 1	µA	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
V_{OH}	Output high voltage	2.4			V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage			0.4	V	I_{OL} = 2.1 mA
I_{SB1}	Standby supply current		5	11	mA	$\overline{CE} = V_{IH}$
I_{SB2}	Standby supply current		2.5	5	mA	$\overline{CE} \geq V_{CC}$ - 0.2V, 0V ≤ $V_{IN} \leq$ 0.2V, or $V_m \geq V_{CC}$ - 0.2V
I_{CC}	Operating supply current		95	200	mA	Min. cycle, duty = 100%, $\overline{CE} = V_{IL}$, $I_{I/O}$ = 0mA
V_{PFD}	Power-fail-detect voltage	4.55	4.62	4.75	V	bq4024
		4.30	4.37	4.50	V	bq4024Y
V_{SO}	Supply switch-over voltage		3		V	

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.

Capacitance (T_A = 25°C, F = 1MHz, VCC = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance			10	pF	Output voltage = 0V
C_{IN}	Input capacitance			20	pF	Input voltage = 0V

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

Parameter	Ted Condition8
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 1 and 2

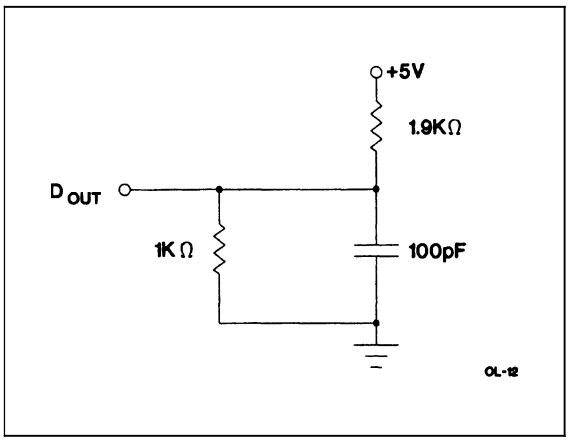


Figure 1. Output Load A

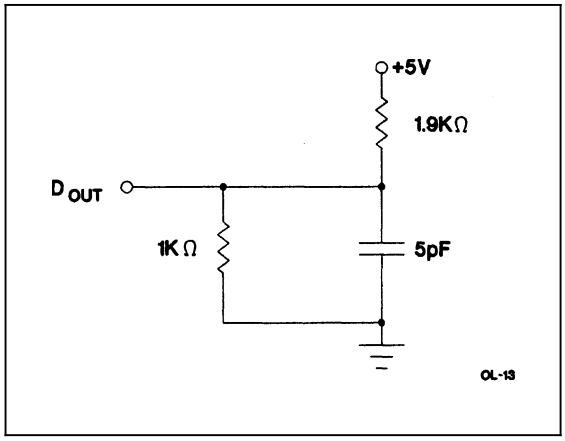
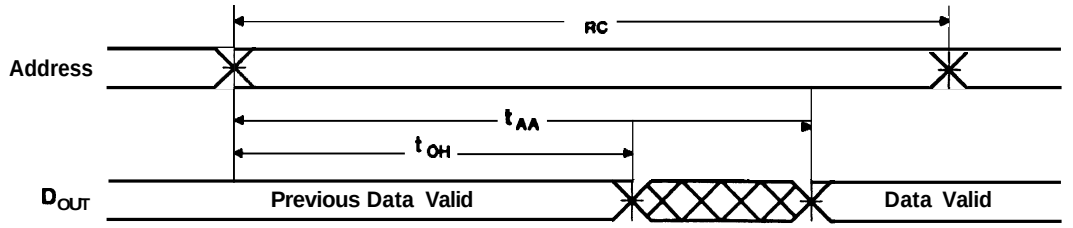


Figure 2. Output Load B

Read Cycle (TA = 0 to 70°C, VCCmin ≤ VCC ≤ VCCmax)

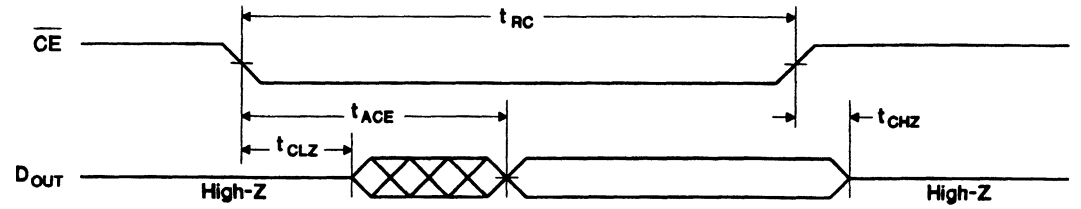
Symbol	Parameter	-85		120		Unit	Conditions
		Min.	Max.	Min.	Max.		
tRC	Read cycle time	85	-	120	-	ns	
tAA	Address access time	-	85	-	120	ns	Output load A
tACE	Chip enable access time	-	85	-	120	ns	Output load A
tOE	Output enable to output valid	4	5	6	0	ns	Output load A
tCLZ	Chip enable to output in low Z	5	-	5	-	ns	Output load B
tOLZ	Output enable to output in low Z	0	-	0	-	ns	Output load B
tCHZ	Chip disable to output in high Z	0	35	0	45	ns	Output load B
tom	Output disable to output in high Z	0	25	0	35	ns	Output load B
tOH	Output hold from address change	10	-	10	-	ns	Output load A

Read Cycle No. 1 (Address Access) [1,2]



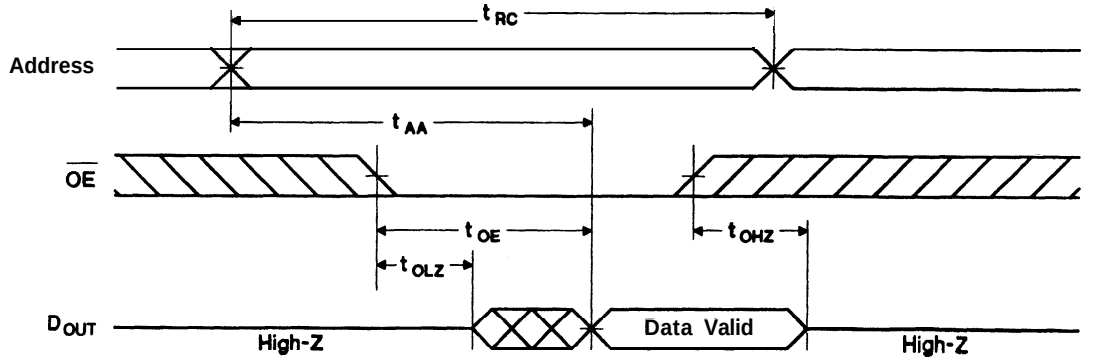
RC-1

Read Cycle No. 2 ($\overline{CE}$ Access) [1,3,4]



RC-2

Read Cycle No. 3 ($\overline{OE}$ Access) [1,5]



RC-3

Notes:

1. $\overline{WE}$ is held high for a read cycle.
2. Device is continuously selected: $\overline{CE}$ = $\overline{OE}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Device is continuously selected: $\overline{CE}$ = V_{IL}.

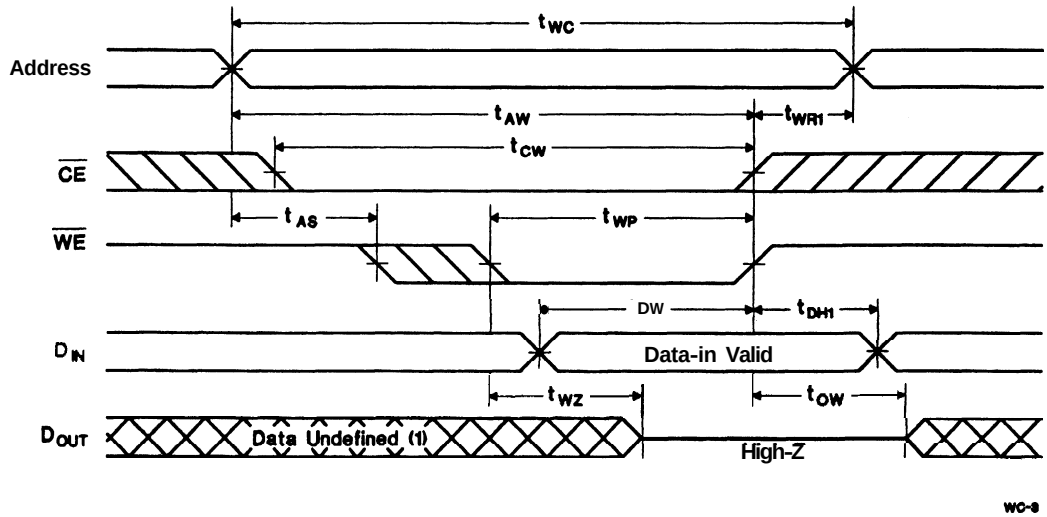
Write Cycle (TA = 0 to 70°C, VCCmin ≤ VCC ≤ VCCmax)

Symbol	Parameter	-85		-120		Units	Conditions/Notes
		Min.	Max.	Min.	Max.		
t_{WC}	Write cycle time	85	-	120	-	ns	
t_{CW}	Chip enable to end of write	75	-	100	-	ns	(1)
t_{AW}	Address valid to end of write	75	-	100	-	ns	(1)
t_{AS}	Address setup time	0		0		ns	Measured from address valid to beginning of write. (2)
t_{WP}	Write pulse width	65		85		ns	Measured from beginning of write to end of write. (1)
t_{WR1}	Write recovery time (write cycle 1)	5		5		ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
t_{WR2}	Write recovery time (write cycle 2)	15	-	15	-	ns	Measured from $\overline{CE}$ *going* high to end of write cycle. (3)
t_{DW}	Data valid to end of write	35		45		ns	Measured to first low-to-high transition of either $\overline{CE}$ or $\overline{WE}$.
t_{DH1}	Data hold time (write cycle 1)	0		0		ns	Measured from $\overline{WE}$ going high to end of write cycle.(4)]
t_{DH2}	Data hold time (write cycle 2)	10	-	10	-	ns	Measured from $\overline{CE}$ *going* high *to* end of write cycle. (4)
t_{WZ}	Write enabled to output in high-Z	0	30	0	40	ns	I/O pins are in output state. (5)
t_{OW}	Output active from end of write	0	-	0	-	ns	I/O pins are in output state. (5)

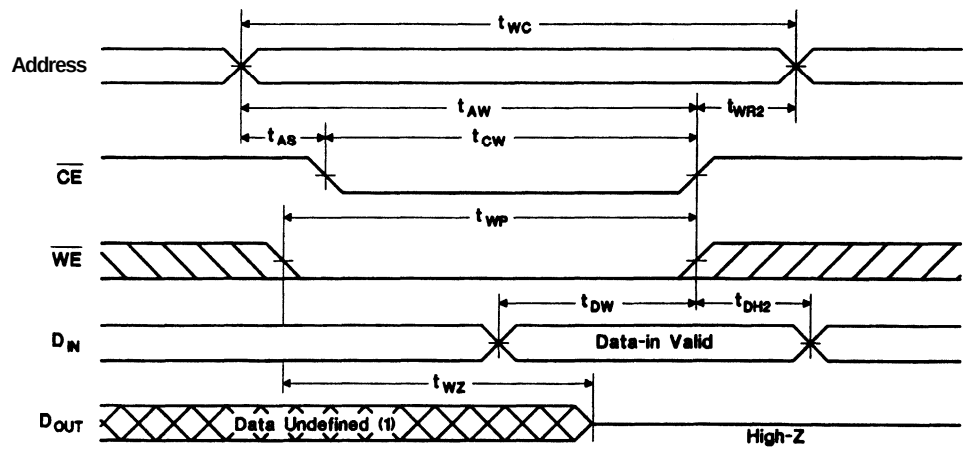
Notes:

1. A write ends at the earlier transition of $\overline{CE}$ going high and $\overline{WE}$ going high.
2. A write occur-during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. A write begins at the later transition of CE going low and $\overline{WE}$ going low.
3. Either t_{WR1} or t_{WR2} must be met.
4. Either t_{DH1} or t_{DH2} must be met.
5. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

Write Cycle No. 1 ($\overline{WE}$-Controlled) 1,2,3



Write Cycle No. 2 ($\overline{CE}$-Controlled) 1,2,3,4,5



Notes:
1. $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
2. Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
3. If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.
4. Either t_{WR1} or t_{WR2} must be met.
5. Either t_{DH1} or t_{DH2} must be met.

Power-Down/Power-Up Cycle (T_A = 0 to 70°C)

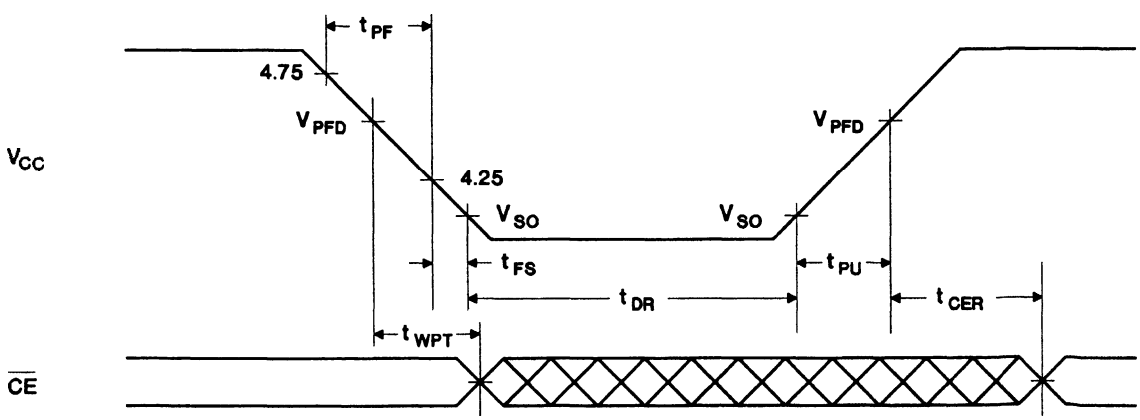
Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_{PF}	V_{CC} slew, 4.75 to 4.25 V	300			µs	
t_{FS}	V_{CC} slew, 4.25 to V_{SO}	10			µs	
t_{PU}	V_{CC} slew, V_{SO} to V_{PFD} (max.)	0			µs	
t_{CER}	Chip enable recovery time	40	80	120	ms	Time during which SRAM is write-protected after V_{CC} passes V_{PFD} on power-up.
t_{DR}	Data-retention time in absence of V_{CC}	10			years	T_A = 25°C. (2)
t_{WPT}	Write-protect time	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.

Notes: 1. *Typical* values indicate operation at T_A = 25°C, V_{CC} = 5V.

2. Batteries are disconnected from circuit until after V_{CC} is applied for the first time. t_{DR} is the accumulated time in absence of power beginning when power is first applied to the device.

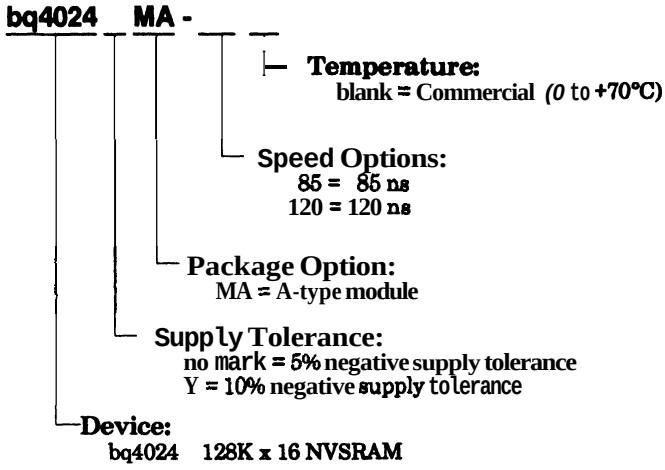
Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

Power-Down/Power-Up Timing



PD-B

Ordering Information



6

Notes

bq4025/bq4025Y

256Kx16 Nonvolatile SRAM

Features

- Data retention in the absence of power
- Automatic write-protection during power-up/power-down cycles
- ➤ Industry-standard 40-pin 256K x 16 pinout
- Conventional SRAM operation; unlimited write cycles
- 5-year minimum data retention in absence of power
- Battery internally isolated until power is applied

General Description

The CMOS **bq4025** is a nonvolatile 4,194,304-bit static RAM organized as 262,144 words by 16 bits. The integral control circuitry and lithium energy source provide reliable nonvolatility coupled with the unlimited write cycles of standard SRAM.

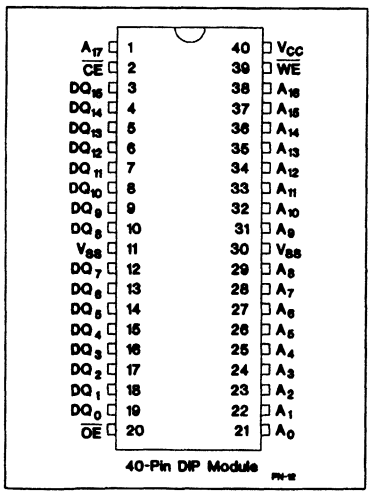
The control circuitry constantly monitors the single 5V supply for an out-of-tolerance condition. When V_{CC} falls out of tolerance, the SRAM is unconditionally write-protected to prevent inadvertent write operation.

At this time the integral energy source is switched on to sustain the memory until after V_{CC} returns valid.

The **bq4025** uses extremely low standby current CMOS SRAMs, coupled with small lithium coin cells to provide nonvolatility without long write-cycle times and the write-cycle limitations associated with EEPROM.

The bq4025 requires no external circuitry and is compatible with the industry-standard 4Mb SRAM pinout.

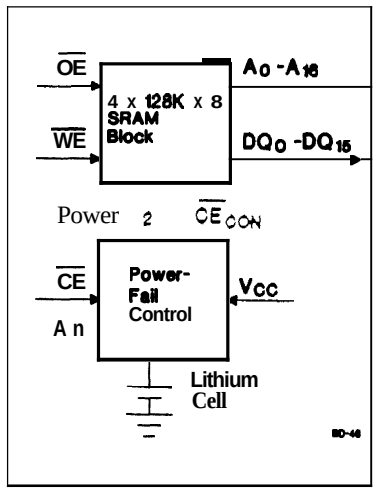
Pin Connections



Pin Names

A_0-A_{17}	Address inputs
DQ_0-DQ_{15}	Data input/output
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input
$\overline{WE}$	Write enable input
V_{CC}	+5 volt supply input
V_{SS}	Ground

Block Diagram



Selection Guide

Part Number	Maximum Access Time (ns)	Negative Supply Tolerance	Part Number	Maximum Access Time (ns)	Negative Supply Tolerance
bq4025-85	85	-5%	bq4025Y-85	85	-10%
bq4025-120	120	-5%	bq4025Y-120	120	-10%

Functional Description

When power is valid, the bq4025 operates as a standard CMOS SRAM. During power-down and power-up cycles, the bq4025 acts as a nonvolatile memory, automatically protecting and preserving the memory contents.

Power-down/power-up control circuitry constantly monitors the V_{CC} supply for a power-fail-detect threehold V_{PFD}. The bq4025 monitors for V_{PFD} = 4.62V typical for use in systems with 5% supply tolerance. The bq4025Y monitors for V_{PFD} = 4.37V typical for use in systems with 10% supply tolerance.

When V_{CC} falls below the V_{PFD} threshold, the SRAM automatically write-protects the data. All outputs become high impedance, and all inputs are treated as 'don't care.' If a valid access is in process at the time of power-fail detection, the memory cycle continues to completion. If the memory cycle fails to terminate within time t_{WPT}, write-protection takes place.

As V_{CC} falls past V_{PFD} and approaches 3V, the control circuitry switches to the internal lithium backup supply, which provides data retention until valid V_{CC} is applied.

When V_{CC} returns to a level above the internal backup cell voltage, the supply is switched back to V_{CC}. *After* V_{CC} ramps above the V_{PFD} threshold, write-protection continues for a time t_{CER} (120ms maximum) to allow for processor stabilization. Normal memory operation may resume after this time.

The internal coin cells used by the bq4025 have an extremely long shelf life and provide data retention for more than 6 years in the absence of system power.

As shipped from Benchmarq, the integral lithium cells are electrically isolated from the memory. (Self-discharge in this condition is approximately 0.5% per year.) Following the first application of V_{CC}, this isolation is broken, and the lithium backup provides data retention on subsequent power-downs.

Truth Table

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Operation	Power
Not selected	H	X	X	High Z	Standby
Output disable	L	H	H	High Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \le V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	
T_{STG}	Storage temperature	-40 to +70	°C	
T_{BIAS}	Temperature under bias	-10 to +70	°C	
T_{SOLDER}	Soldering temperature	+260	°C	For 10 seconds

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	6.0	6.5	V	bq4025Y
		4.75	5.0	5.5	V	bq4025
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3		0.8	V	
V_{IH}	Input high voltage	2.2		Vcc + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C.

DC Electrical Characteristics (T_A = 0 to 70°C, $V_{CCmin} \leq V_{CC} \leq V_{CCmax}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current			±4	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output leakage current			±2	µA	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}
V_{OH}	Output high voltage	2.4			V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage			0.4	V	I_{OL} = 2.1 mA
I_{SB1}	Standby supply current		7	18	mA	$\overline{CE}$ = V_{IH}
I_{SB2}	Standby supply current		2.5	5	mA	$\overline{CE} \geq V_{CC}$ - 0.2V, 0V ≤ $V_{IN} \leq$ 0.2V, or $V_{IN} \geq V_{CC}$ - 0.2V
I_{CC}	Operating supply current		95	200	mA	Min. cycle, duty = 100%, $\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0mA, A17 < V_{IL} or A17 > V_{IH}
V_{PFD}	Power-fail-detect voltage	4.55	4.62	4.75	V	bq4025
		4.30	4.37	4.50	V	bq4025Y
V_{SO}	Supply switch-over voltage		3		V	

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance			20	pF	Output voltage = 0V
C_{IN}	Input capacitance			40	pF	Input voltage = 0V

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 1 and 2

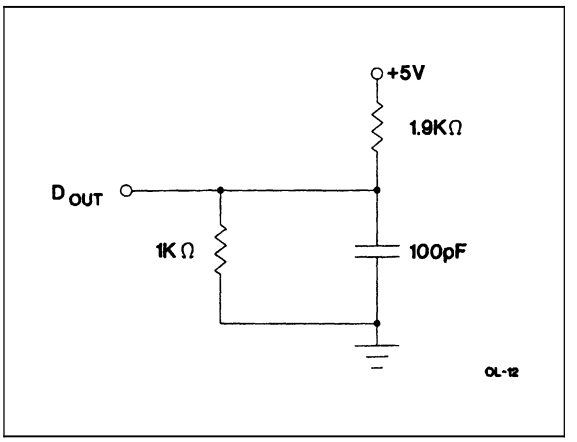


Figure 1. Output Load A

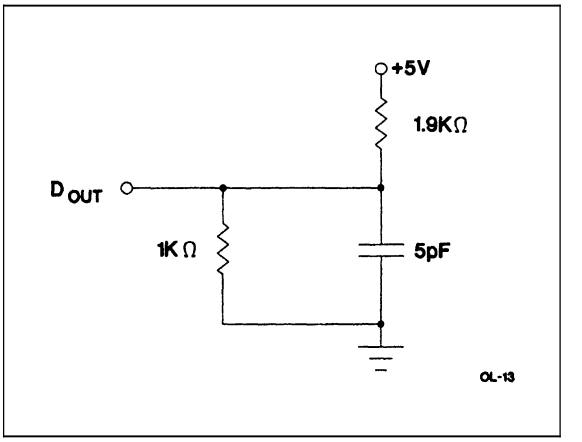
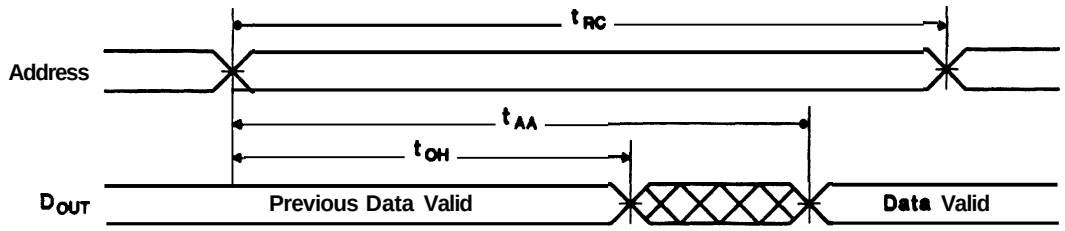


Figure 2. Output Load B

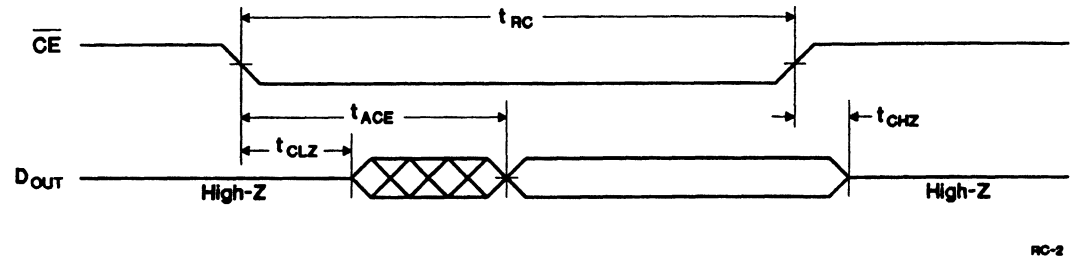
Read Cycle (TA = 0 to 70°C, VCCmin 5 VCC ≤ VCCmax)

Symbol	Parameter	-85		-120		Unit	Conditions
		Min.	Max.	Min.	Max.		
t_{RC}	Read cycle time	85	-	120	-	ns	
t_{AA}	Address access time	-	85	-	120	ns	Output load A
t_{ACE}	Chip enable access time	-	85	-	120	ns	Output load A
t_{OE}	Output enable to output valid	-	45	-	60	ns	Output load A
t_{CLZ}	Chip enable to output in low Z	5	-	5	-	ns	Output load B
t_{OLZ}	Output enable to output in low Z	0	-	0	-	ns	Output load B
t_{CHZ}	Chip disable to output in high Z	0	35	0	45	ns	Output load B
t_{OHZ}	Output disable to output in high Z	0	25	0	35	ns	Output load B
t_{OH}	Output hold from address change	10	-	10	-	ns	Output load A

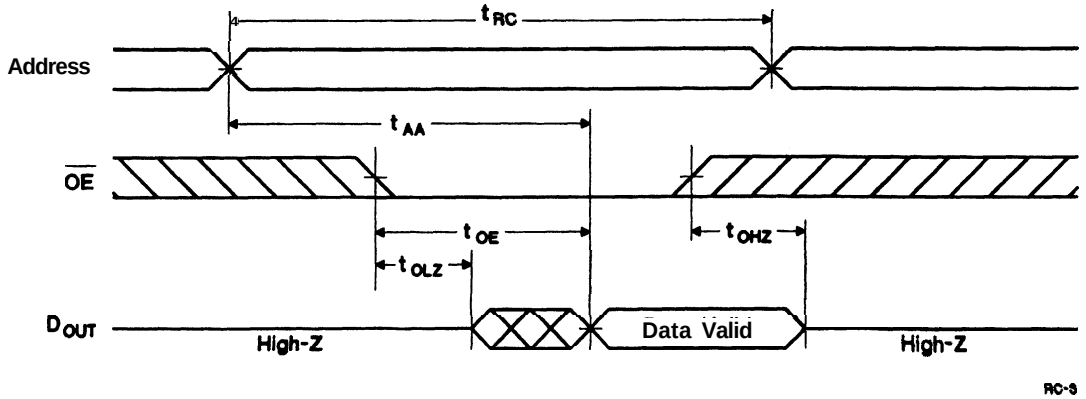
Read Cycle No. 1 (Address Access) [1,2]



Read Cycle No. 2 ($\overline{CE}$ Access) [1,3,4]



Read Cycle No. 3 ($\overline{OE}$ Access) [1,5]



Notes:
1. $\overline{WE}$ is held high for a read cycle.
2. Device is continuously selected: $\overline{CE} = \overline{OE} = V_{IL}$.
3. Address is valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Device is continuously selected: $\overline{CE} = V_{IL}$.

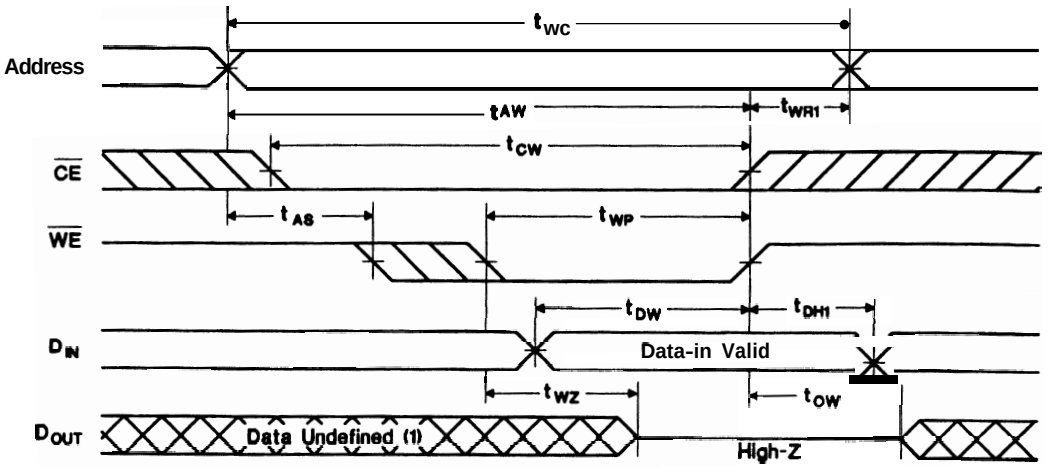
Write Cycle (T_A = 0 to 70°C, $V_{CCmin} \le V_{CC} \le V_{CCmax}$)

Symbol	Parameter	-85 Min.	-85 Max.	120 Min.	120 Max.	Units	Conditions/Notes
t_{WC}	Write cycle time	85	-	120	-	ns	
t_{CW}	Chip enable to end of write	75	-	100	-	ns	(1)
t_{AW}	Address valid to end of write	75	-	100	-	ns	(1)
t_{AS}	Address setup time	0		0		ns	Measured from address valid to beginning of write. (2)
t_{WP}	Write pulse width	65		85		ns	Measured from beginning of write to end of write. (1)
t_{WR1}	Write recovery time (write cycle 1)	5		5	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
t_{WR2}	Write recovery time (write cycle 2)	15	-	15	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (3)
t_{DW}	Data valid to end of write	35	-	45	-	ns	Measured to first low-to-high transition of either $\overline{CE}$ or $\overline{WE}$.
t_{DH1}	Data hold time (write cycle 1)	0	-	0		ns	Measured from $\overline{WE}$ going high to end of write cycle. (4)
t_{DH2}	Data hold time (write cycle 2)	10	-	10	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (4)
t_{WZ}	Write enabled to output in high-Z	0	30	0	40	ns	I/O pins are in output state. (5)
t_{OW}	Output active from end of write	0	-	0	-	ns	I/O pine are in output state. (5)

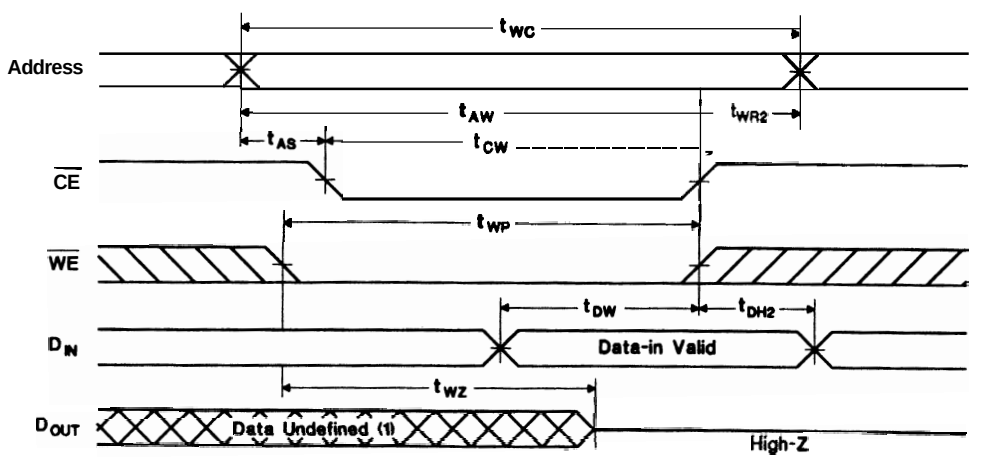
Notes:

1. A write ends at the earlier transition of $\overline{CE}$ going high and $\overline{WE}$ going high.
2. A write occurs—during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. A write begins at the later transition of CE going low and $\overline{WE}$ going low.
3. Either t_{WR1} or t_{WR2} must be met.
4. Either t_{DH1} or t_{DH2} must be met.
5. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

Write Cycle No. 1 ($\overline{WE}$-Controlled) [1,2,3]



Write Cycle No. 2 ($\overline{CE}$-Controlled) [1,2,3,4,5]



Notes:

1. $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
2. Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
3. If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.
4. Either t_{WR1} or t_{WR2} must be met.
5. Either t_{DH1} or t_{DH2} must be met.

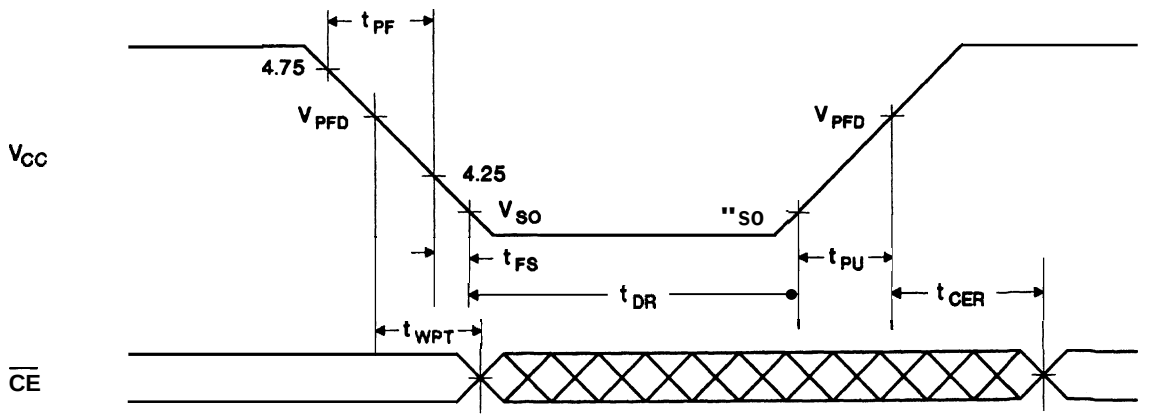
Power-Down/Power-Up Cycle (T_A = 0 to 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{PF}	V_{CC} slew, 4.75 to 4.25 V	300			µs	
t_{FS}	V_{CC} slew, 4.25 to V_{SO}	10			µs	
t_{PU}	V_{CC} slew, V_{SO} to V_{PFD} (max.)	0			µs	
t_{CER}	Chip enable recovery time	40	80	120	ms	Time during which SRAM is write-protected after V_{CC} passes V_{PFD} on power-up.
t_{DR}	Data-retention time in absence of V_{CC}	5			years	T_A = 25°C. (2)
t_{WPT}	Write-protect time	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.

Notes:
1. Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.
2. Batteries are disconnected from circuit until after V_{CC} is applied for the first time. t_{DR} is the accumulated time in absence of power beginning when power is first applied to the device.

Caution. Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

Power-Down/Power-Up Timing

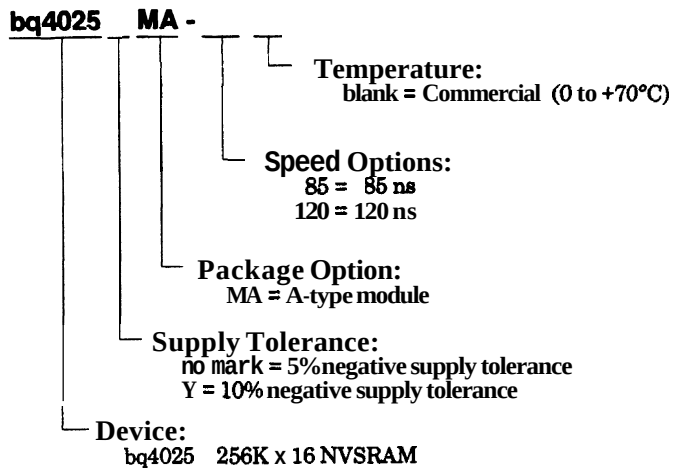


PD-B

Revision History (Sept. 1992 Changes From Sept. 1990)

:c test conditions, page 3.

Ordering Information



Package Drawings

Benchmarq's standard packages are described in the following tables.

Package Type	Description	No. Pins	Device
MA	DIP Module, A-Type	12	bq2502
		28	bq4010/bq4010Y
			bq4011/bq4011Y
			bq4830Y
		32	bq4013/bq4013Y
			bq4015/bq4015Y
			bq4832Y
			bq4842Y
			bq4850Y
		40	bq4024/bq4024Y
			bq4025/bq4025Y
MB	DIP Module, B-Type	32	bq4014/bq4014Y
			bq4015/bq4015Y
MC	DIP Module, C-Type	36	bq4016/4016Y
			bq4017/4017Y
			bq4852Y
MT	DIP Module, T-Type	24	bq3287/bq3287A
			bq3287E/bq3287EA
			bq4287/bq4287E
		28	bq4847/bq4847Y
P	Plastic DIP, 0.600"	24	bq3285
			bq3285E
			bq3285EC
			bq3285L
			bq3285LC
			bq4285
			bq4285E
			bq4285L
		28	bq4845/bq4845Y

Package Type	Description	No. Pins	Device
	Plastic DIP, 0.300"	8	bq2002
			bq2002T
			bq2201
			bq2902
		14	bq2903
		16	bq2003
			bq2004
			bq2004E
			bq2031
			bq2054
			bq2202
			bq2203A
			bq2204A
		20	bq2005
		24	bq2007

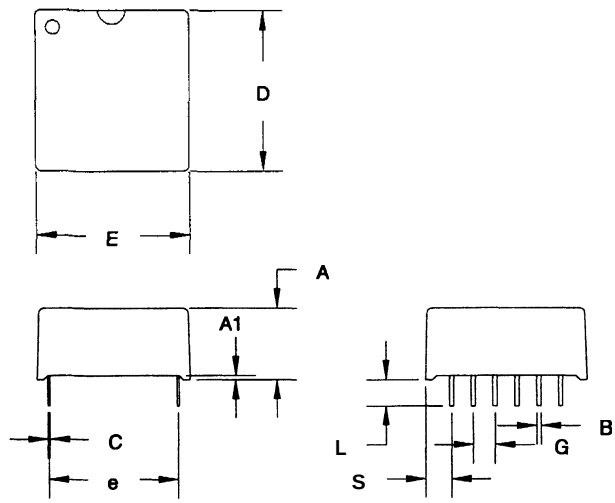
7

Package Drawings

Package Type	Description	No. Pins	Device
Q	Quad PLCC	28	bq3285
			bq3285E
			bq4285
			bq4285E
S	SOIC, 0.300"	16	bq2003
		20	bq2005
		24	bq2007
			bq3285
			bq3285E
			bq3285EC
			bq3285L
			bq3285LC
			bq4285
			bq4285E
			bq4285L
		28	bq4845/Y

Package Type	Description	No. Pins	Device
SN	SOIC Narrow, 0.150"	8	bq2002
			bq2002T
			bq2201
			bq2053
			bq2902
		14	bq2903
		16	bq2004
			bq2004E
			bq2010
			bq2011
			bq2011J
			bq2011K
			bq2012
			bq2014
			bq2014H
			bq2031
			bq2040
			bq2050
			bq2050H
			bq2054
			bq2058
			bq2090
			bq2091
			bq2202
			bq2203A
			bq2204A
SS	SSOP, 0.150"	24	bq3285E
			bq3285EC
			bq3285L
			bq3285LC

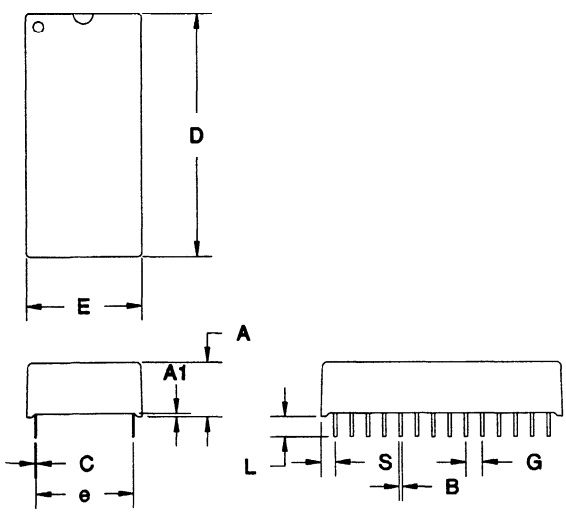
MA: 12-Pin A-Type Module



12-Pin MA (A-Type Module)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.365	0.375	9.27	8.53
A1	0.015	-	0.38	-
B	0.017	0.023	0.43	0.58
C	0.008	0.013	0.20	0.33
D	0.710	0.740	18.03	18.80
E	0.710	0.740	18.03	18.80
e	0.590	0.630	14.99	16.00
G	0.090	0.110	2.29	2.79
L	0.120	0.150	3.05	3.81
S	0.105	0.130	2.67	3.30

MA: 28-Pin A-Type Module

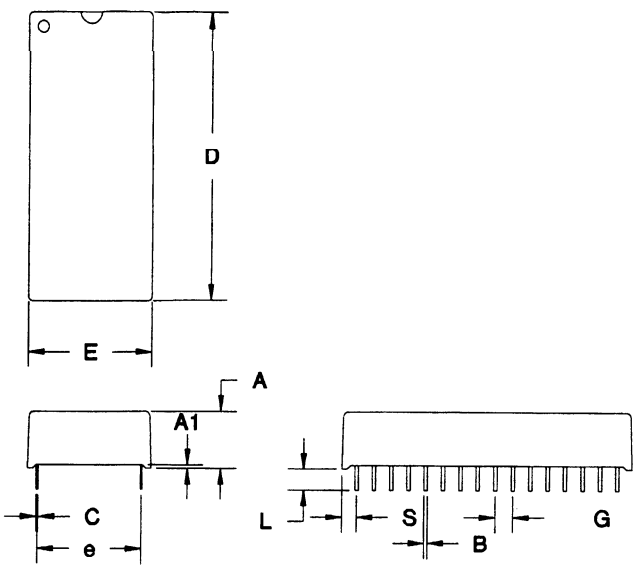


28-Pin MA (A-Type Module)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.365	0.375	9.27	9.53
A1	0.015	-	0.38	-
B	0.017	0.023	0.43	0.58
C	0.008	0.013	0.20	0.33
D	1.470	1.500	37.34	38.10
E	0.710	0.740	18.03	18.80
e	0.590	0.630	14.99	16.00
G	0.090	0.110	2.29	2.79
L	0.120	0.150	3.05	3.81
S	0.075	0.110	1.91	2.79

Package Drawings

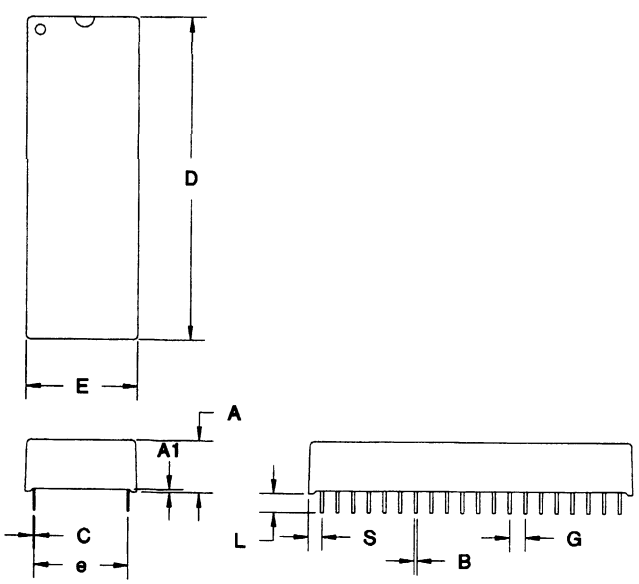
MA: 32-Pin A-Type Module



32-Pin MA (A-Type Module)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.365	0.375	9.27	9.53
A1	0.015	-	0.38	-
B	0.017	0.023	0.43	0.58
C	0.008	0.013	0.20	0.33
D	1.670	1.700	42.42	43.18
E	0.710	0.740	18.03	18.80
e	0.590	0.630	14.99	16.00
G	0.090	0.110	2.29	2.79
L	0.120	0.150	3.05	3.81
S	0.075	0.110	1.91	2.79

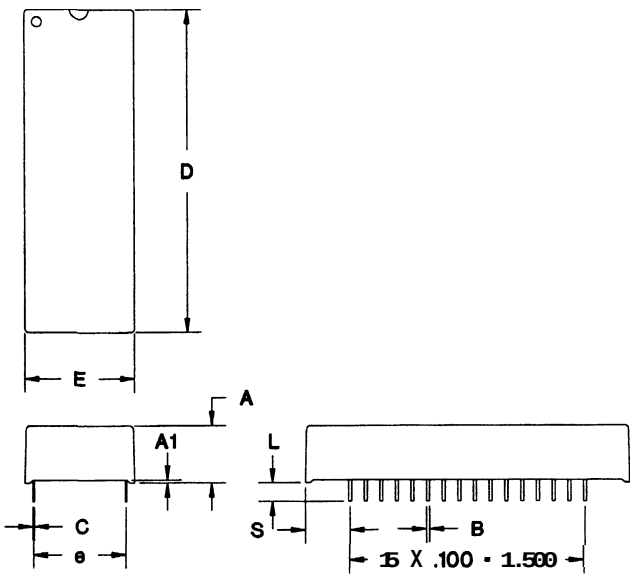
MA: 40-Pin A-Type Module



40-Pin MA (A-Type Module)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.365	0.375	9.27	9.53
A1	0.015	-	0.38	-
B	0.017	0.023	0.43	0.58
C	0.008	0.013	0.20	0.33
D	2.070	2.100	52.58	53.34
E	0.710	0.740	18.03	18.80
e	0.590	0.630	14.99	16.00
G	0.090	0.110	2.29	2.79
L	0.120	0.150	3.05	3.81
S	0.075	0.110	1.91	2.79

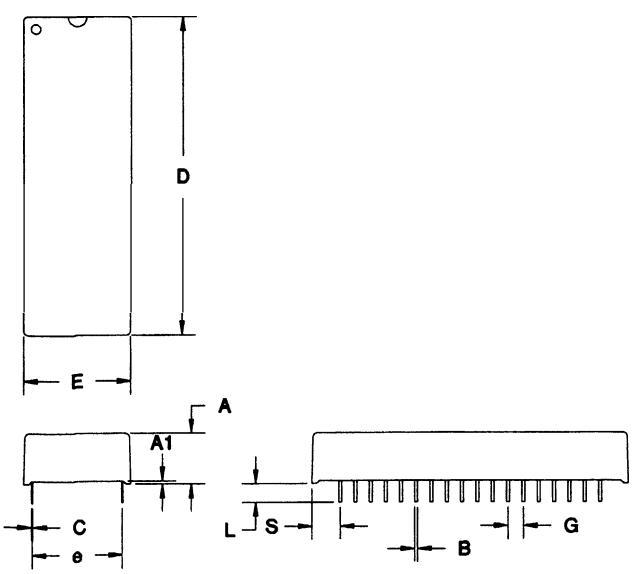
MB: 32-Pin B-Type Module



32-Pin MB (B-Type Module)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.365	0.375	9.27	9.53
A1	0.015	-	0.38	-
B	0.017	0.023	0.43	0.58
C	0.008	0.013	0.20	0.33
D	2.070	2.100	52.58	53.34
E	0.710	0.740	18.03	18.80
e	0.590	0.630	14.99	16.00
G	0.090	0.110	2.29	2.79
L	0.120	0.150	3.05	3.81
S	0.275	0.310	6.99	7.87

MC: 36-Pin C-Type Module

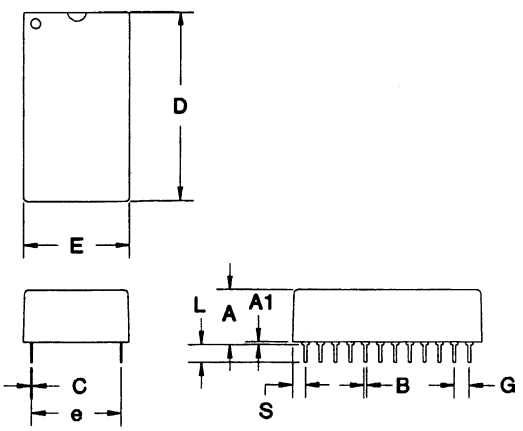


36-Pin MC (C-Type Module)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.365	0.375	9.27	9.53
A1	0.015	-	0.38	-
B	0.017	0.023	0.43	0.58
C	0.008	0.013	0.20	0.33
D	2.070	2.100	52.58	53.34
E	0.710	0.740	18.03	18.80
e	0.590	0.630	14.99	16.00
G	0.090	0.110	2.29	2.79
L	0.120	0.150	3.05	3.81
S	0.175	0.210	4.45	5.33

Package Drawings

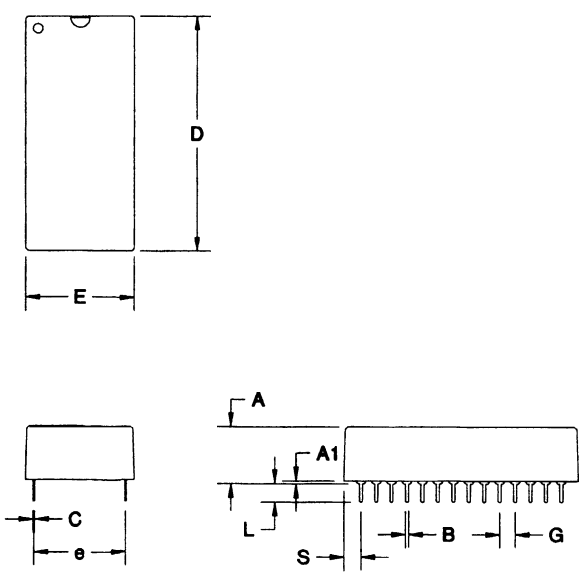
MT: 24-Pin T-Type Module



24-Pin MT (T-Type Module)

Dimension	Inches		Millimeters	
	Min.	Mu.	Min.	Max.
A	0.360	0.390	9.14	9.91
A1	0.015	-	0.38	-
B	0.015	0.022	0.38	0.56
C	0.008	0.013	0.20	0.33
D	1.320	1.335	33.53	33.91
E	0.710	0.740	18.03	18.80
e	0.590	0.620	14.99	15.75
G	0.090	0.110	2.29	2.79
L	0.110	0.130	2.79	3.30
S	0.100	0.120	2.54	3.05

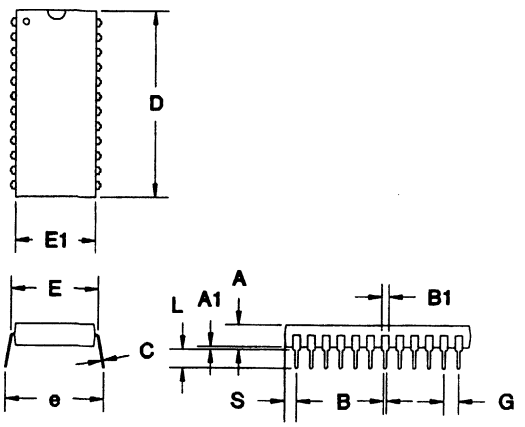
MT: 28-Pin T-Type Module



28-Pin MT (T-Type Module)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.360	0.390	9.14	9.91
A1	0.015	-	0.38	-
B	0.015	0.022	0.38	0.56
C	0.008	0.013	0.20	0.33
D	1.520	1.535	38.61	38.99
E	0.710	0.740	18.03	18.80
e	0.590	0.620	14.99	15.75
G	0.090	0.110	2.29	2.79
L	0.110	0.130	2.79	3.30
S	0.100	0.120	2.54	3.05

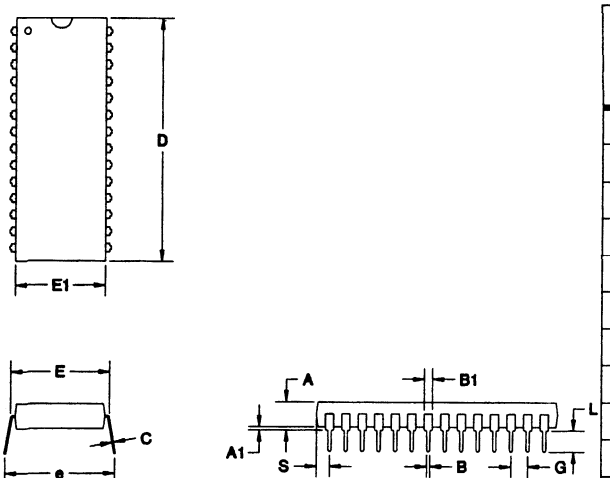
P: 24-Pin DIP *(0.600")*



24-Pin DIP (0.600" DIP)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.160	0.190	4.06	4.83
A1	0.015	0.040	0.38	1.02
B	0.015	0.022	0.38	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.013	0.20	0.33
D	1.240	1.280	31.50	32.51
E	0.600	0.625	15.24	15.88
E1	0.530	0.570	13.46	14.48
e	0.600	0.670	15.24	17.02
G	0.090	0.110	2.29	2.79
L	0.115	0.150	2.92	3.81
S	0.070	0.090	1.78	2.29

P: 28-Pin DIP *(0.600")*

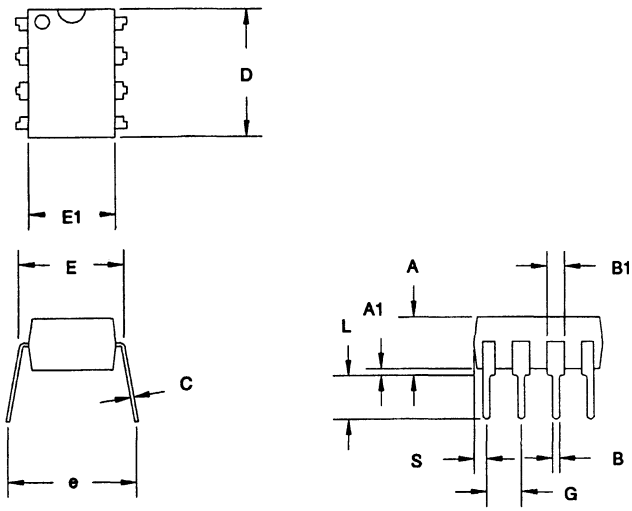


28-Pin DIP (0.600" DIP)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.160	0.190	4.06	4.83
A1	0.015	0.040	0.38	1.02
B	0.015	0.022	0.38	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.013	0.20	0.33
D	1.440	1.480	36.58	37.59
E	0.600	0.625	15.24	15.88
E1	0.530	0.570	13.46	14.48
e	0.600	0.670	15.24	17.02
G	0.090	0.110	2.29	2.79
L	0.115	0.150	2.92	3.81
S	0.070	0.090	1.78	2.29

Package Drawings

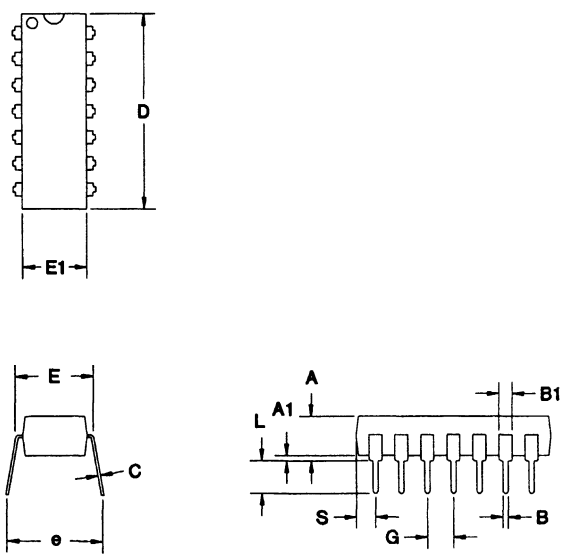
PN: 8-Pin DIP (0.300")



8-Pin PN (0.300" DIP)

Dimension	Inches		Millimeters	
	Mln.	Max.	Min.	Max.
A	0.160	0.180	4.06	4.57
A1	0.015	0.040	0.38	1.02
B	0.015	0.022	0.38	0.56
B1	0.055	0.065	1.40	1.65
C	0.008	0.013	0.20	0.33
D	0.350	0.380	8.89	9.65
E	0.300	0.325	7.62	8.26
E1	0.230	0.280	5.84	7.11
e	0.300	0.370	7.62	9.40
G	0.090	0.110	2.29	2.79
L	0.115	0.150	2.92	3.81
S	0.020	0.040	0.51	1.02

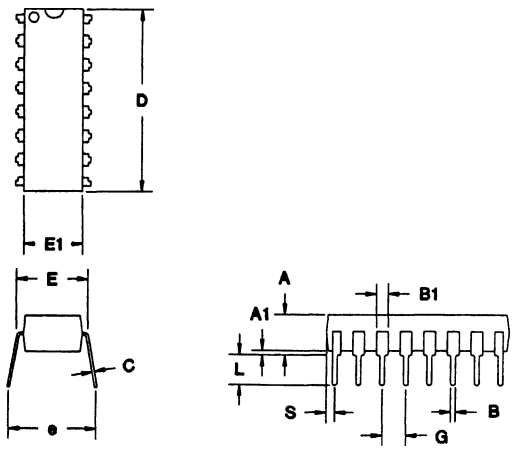
PN: 14-Pin DIP (0.300")



14-Pin PN (0.300" DIP)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.160	0.180	4.06	4.57
A1	0.015	0.040	0.38	1.02
B	0.015	0.022	0.38	0.56
B1	0.055	0.065	1.40	1.65
C	0.008	0.013	0.20	0.33
D	0.740	0.770	18.80	19.56
E	0.300	0.325	7.62	8.26
E1	0.230	0.280	5.84	7.11
e	0.300	0.370	7.62	9.40
G	0.090	0.110	2.29	2.79
L	0.115	0.150	2.92	3.81
S	0.070	0.090	1.78	2.29

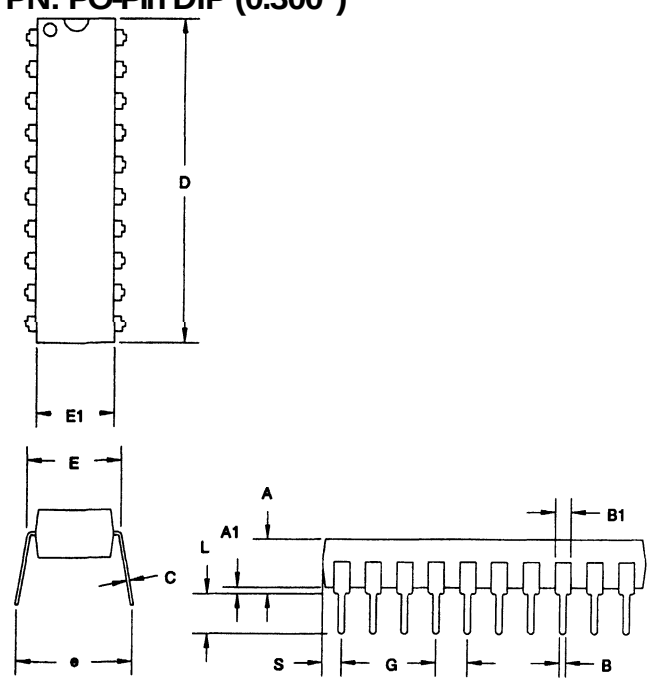
PN: 16-Pin DIP (0.300")



16-Pin PN (0.300" DIP)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.160	0.180	4.06	4.57
A1	0.015	0.040	0.38	1.02
B	0.015	0.022	0.38	0.56
B1	0.055	0.065	1.40	1.65
C	0.008	0.013	0.20	0.33
D	0.740	0.770	18.80	19.56
E	0.300	0.325	7.62	8.26
E1	0.230	0.280	5.84	7.11
e	0.300	0.370	7.62	9.40
G	0.090	0.110	2.29	2.79
L	0.115	0.150	2.92	3.81
S	0.020	0.040	0.51	1.02

PN: PO-Pin DIP (0.300")



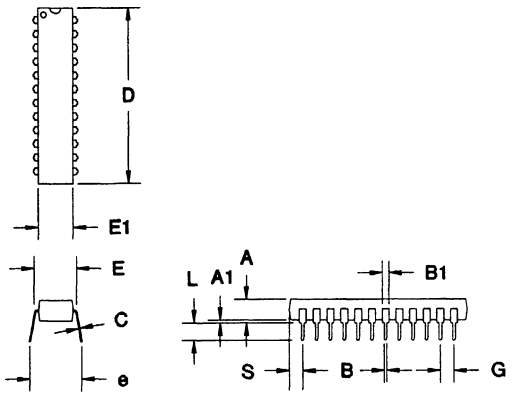
20-Pin PN (0.300" DIP)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.160	0.180	4.06	4.57
A1	0.015	0.040	0.38	1.02
B	0.015	0.022	0.38	0.56
B1	0.055	0.065	1.40	1.65
C	0.008	0.013	0.20	0.33
D	1.010	1.060	25.65	26.92
E	0.300	0.325	7.62	8.26
E1	0.230	0.280	5.84	7.11
e	0.300	0.370	7.62	9.40
G	0.090	0.110	2.29	2.79
L	0.115	0.135	2.92	3.43
S	0.055	0.080	1.40	2.03

7

Package Drawings

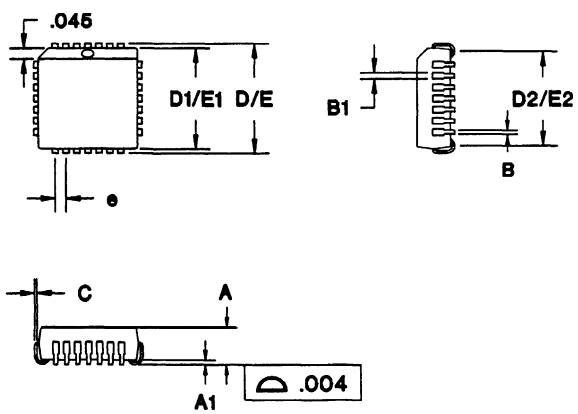
PN: 24-Pin DIP (0.300")



24-Pin PN (0.300" DIP)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.160	0.180	4.06	4.57
A1	0.015	0.040	0.38	1.02
B	0.015	0.022	0.38	0.56
B1	0.045	0.055	1.14	1.40
C	0.008	0.013	0.20	0.33
D	1.240	1.280	31.50	32.51
E	0.300	0.325	7.62	8.26
E1	0.250	0.300	6.35	7.62
e	0.300	0.370	7.62	9.40
G	0.090	0.110	2.29	2.79
L	0.115	0.150	2.92	3.81
S	0.070	0.090	1.78	2.29

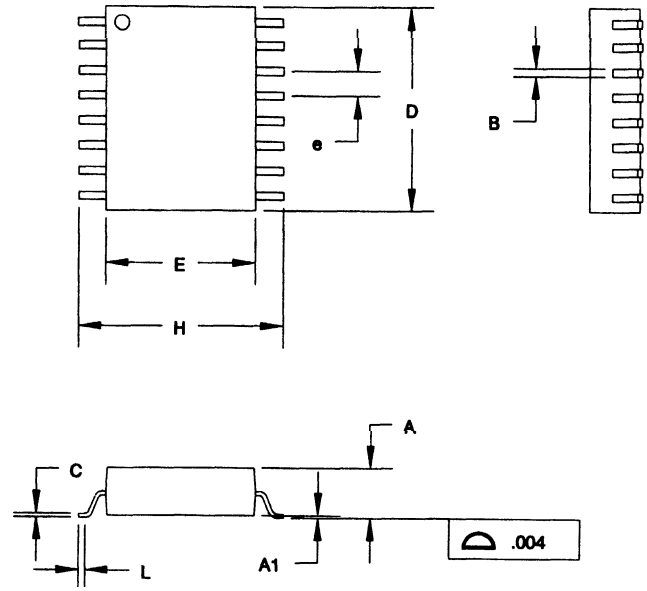
Q: 28-Pin Quad PLCC



28-Pin Q (Quad PLCC)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.165	0.180	4.19	4.57
A1	0.020	-	0.51	-
B	0.012	0.021	0.30	0.53
B1	0.025	0.033	0.64	0.84
C	0.008	0.012	0.20	0.30
D	0.485	0.495	12.32	12.57
D1	0.445	0.455	11.30	11.56
D2	0.390	0.430	9.91	10.92
E	0.485	0.495	12.32	12.57
E1	0.445	0.455	11.30	11.56
E2	0.390	0.430	9.91	10.92
e	0.045	0.055	1.14	1.40

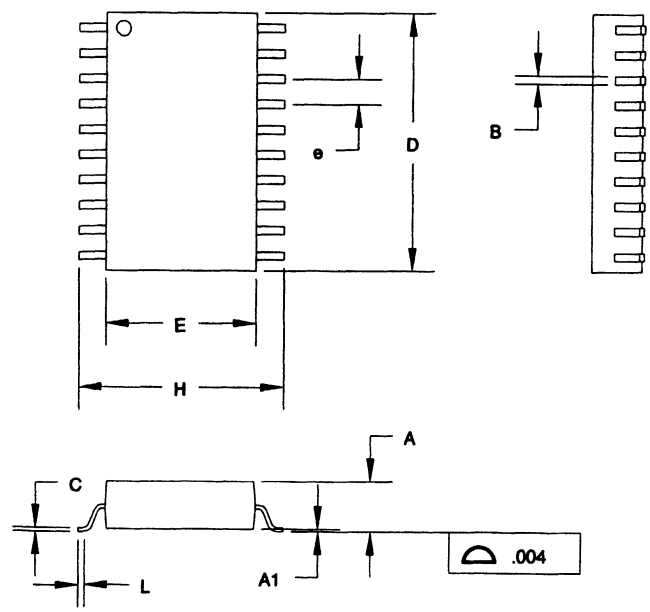
S: 16-Pin S (0.300" SOIC)



16-Pin S (0.300" SOIC)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.095	0.105	2.41	2.67
A1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.008	0.013	0.20	0.33
D	0.400	0.415	10.16	10.54
E	0.290	0.305	7.37	7.75
e	0.045	0.055	1.14	1.40
H	0.395	0.415	10.03	10.54
L	0.020	0.040	0.51	1.02

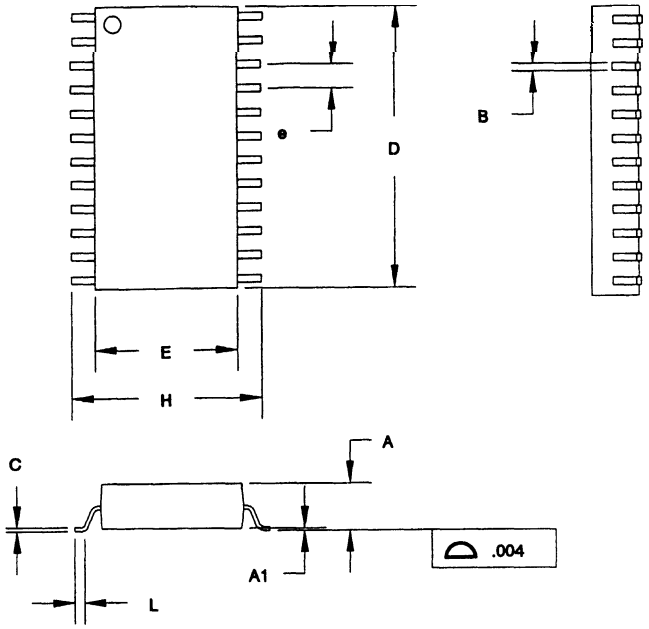
S: PO-Pin S (0.300" SOIC)



20-Pin S (0.300" SOIC)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.095	0.105	2.41	2.67
A1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.008	0.013	0.20	0.33
D	0.500	0.515	12.70	13.08
E	0.290	0.305	7.37	7.75
e	0.045	0.055	1.14	1.40
H	0.395	0.415	10.03	10.54
L	0.020	0.040	0.51	1.02

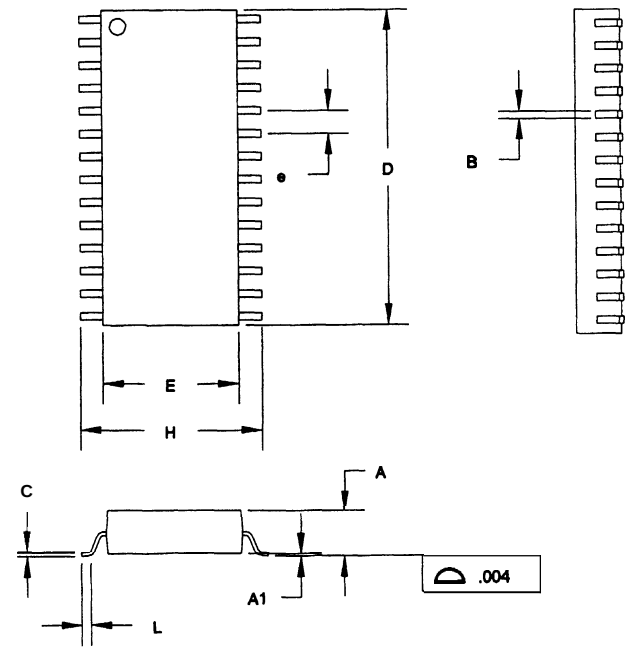
S: 24-Pin S (0.300" SOIC)



24-Pin S (0.300" SOIC)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.095	0.105	2.41	2.67
A1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.008	0.013	0.20	0.33
D	0.600	0.615	15.24	15.62
E	0.290	0.305	7.37	7.75
e	0.045	0.055	1.14	1.40
H	0.395	0.415	10.03	10.54
L	0.020	0.040	0.51	1.02

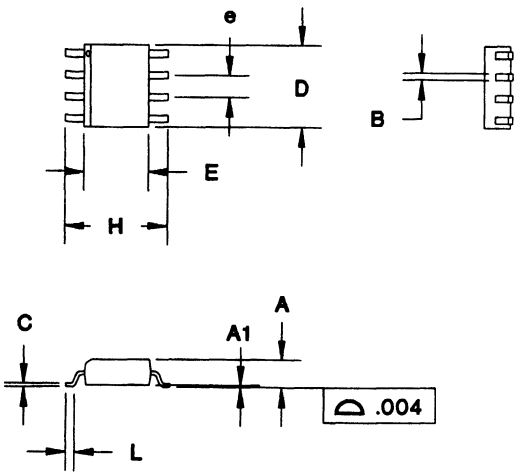
S: 28-Pin S (0.300" SOIC)



28-Pin S (0.300" SOIC)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.095	0.105	2.41	2.67
A1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.008	0.013	0.20	0.33
D	0.700	0.715	17.78	18.16
E	0.290	0.305	7.37	7.75
e	0.045	0.055	1.14	1.40
H	0.395	0.415	10.03	10.54
L	0.020	0.040	0.51	1.02

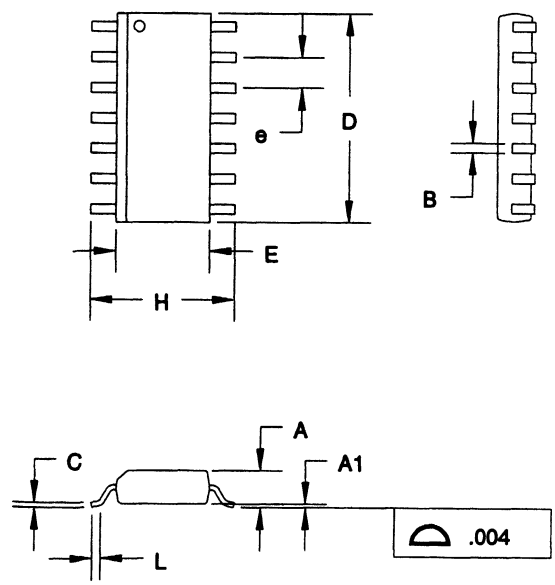
SN: 8-Pin SN (0.150" SOIC)



8-Pin SN (0.150" SOIC)

Dimension	inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.060	0.070	1.52	1.78
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.18	0.25
D	0.185	0.200	4.70	5.08
E	0.150	0.160	3.81	4.06
e	0.045	0.055	1.14	1.40
H	0.225	0.245	5.72	6.22
L	0.015	0.035	0.38	0.89

SN: 14-Pin SN (0.150" SOIC)

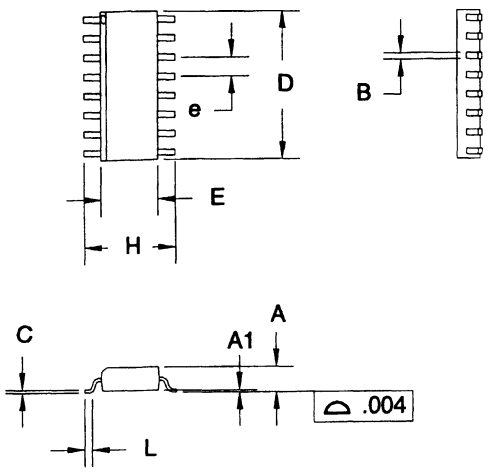


14-Pin SN (0.150" SOIC)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.060	0.070	1.52	1.78
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.18	0.25
D	0.335	0.350	8.51	8.89
E	0.150	0.160	3.81	4.06
e	0.045	0.055	1.14	1.40
H	0.225	0.245	5.72	6.22
L	0.015	0.035	0.38	0.89

Package Drawings

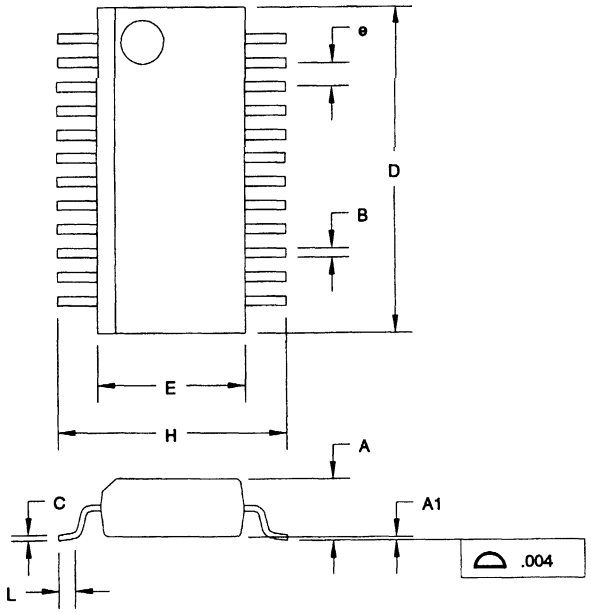
SN : 16-Pin SN (0.150" SOIC)



16-Pin SN (0.150" SOIC)

Dimension	Inches		Millimeters	
	Mln.	Max.	Mln.	Max.
A	0.060	0.070	1.52	1.78
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.18	0.25
D	0.385	0.400	9.78	10.16
E	0.150	0.160	3.81	4.06
e	0.045	0.055	1.14	1.40
H	0.225	0.245	5.72	6.22
L	0.015	0.035	0.38	0.89

24-Pin SSOP (SS)



24-Pin SS (0.150" SSOP)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.061	0.068	1.55	1.73
A1	0.004	0.010	0.10	0.25
B	0.008	0.012	0.20	0.30
C	0.007	0.010	0.18	0.25
D	0.337	0.344	8.56	8.74
E	0.150	0.157	3.81	3.99
e	.025 BSC		0.64 BSC	
H	0.230	0.244	5.84	6.20
L	0.016	0.035	0.41	0.89

BENCHMARQ Quality and Reliability

The Benchmarq Quality Policy

It is the policy of Benchmarq to provide the highest-quality products in support of our customers' needs. We recognize that we are in the business of providing not only the physical product, but also documentation, technical support, sales and marketing support, and timely product delivery. Our commitment to our customers begins with product concept and must extend long after actual product purchase and receipt.

We are dedicated to establishing partnerships with our customers and know that to succeed we must help our customers succeed. We will do this by:

Holding ourselves and our vendors accountable for establishing carefully considered methods and procedures for design, test, and production with clear and concise documentation,

Responding professionally and expeditiously to customer or vendor problems that arise, bringing to bear the company's strongest resources,

Developing an industry-leading "Quality Technology" to drive incremental improvements in all the products we provide, and to contribute to a continuous reduction in new product time to market, and

Continuously providing products and services that meet or *exceed* the best expectations of our customers.

In pursuing this commitment to quality, we have performed extensive qualification testing on our devices to help ensure the highest levels of product reliability.

We feel confident that the reliability levels demonstrated by our qualification testing will allow us to provide a high-quality product that will meet or exceed our customers' needs. Benchmarq is continuously working toward improving product reliability.

An integral part of quality improvement is customer feedback. We encourage our customers to contact us with any questions or suggestions regarding their individual quality requirements or for information concerning up-to-date product enhancements.

Call us – we want to hear from you.

Underwriters Laboratory Recognition

Benchmarq's ICs and modules have been recognized by Underwriters Laboratory (U.L.®) under file E134016 (R). This helps to hasten U.L. approval of our customers' end equipment.

'For detailed *Quality* and *Reliability* Reports, contact the factory or your sales representative.

Quality Procedures

To help ensure that our final product is both consistent and reliable, the following quality tests and procedures have been implemented.

Test Probe

Each wafer is electrically tested at test probe to verify parametric integrity. Any wafer not meeting parametric specifications is rejected.

Wafer IQC

Wafer samples are periodically subjected to physical cross-sectional analysis to verify conformance to design and process specifications.

Final Visual

All lots are subjected to QC final visual inspection. The travelers are checked to make sure that the product was properly burned-in and tested. Additionally, lot numbers and counts are verified, and the devices are checked for mechanical integrity.

Board-Level Products

All printed circuit board level products are manufactured to meet ANSI/IPC-A-610A and ANSI/IPC-A-600D Class 2 specifications.

Traceability

N l traceability is maintained on all products. The devices are traceable to front-end wafer lot and to assembly lot. Top brand includes the Benchmarq logo, part number, date code, and unique lot number (module products).

Electrostatic Discharge (ESD)

It is recognized that electronic components are susceptible to damage due to electrostatic discharge. To help minimize this risk, the following safeguards have been put into place:

- All personnel who handle devices wear grounded wrist and heel straps and have been trained to use proper device-handling procedures.
- All work surfaces used in the test and QC areas have been grounded. Antistatic flooring is used in the test, QC, and finished goods areas.
- All device testers and handlers have adequate grounding.
- Devices are placed into antistatic tubes and kept in conductive totes or boxes during the manufacturing process.

  Finished goods are stored in conductive boxes. Boxes and shipping containers are labeled with ESD warnings.

Packing and Shipping

Great care is taken to ensure that finished product reaches the customer in perfect condition. All devices are placed in antistatic tubes during the assembly and test operations. Before shipping, device tubes are placed in conductive boxes that are marked with ESD warning labels. The conductive boxes are then placed into non-conductive shipping containers for additional protection against rough handling. The shipping containers are also marked with ESD caution labels.

Process Monitoring

The materials, assembly process, and test process are constantly monitored for problems and inconsistencies. Operator traceability and accountability are maintained so that any problems can be identified earlier and corrections implemented quicker. The wafer foundry and assembly contractor are required to use Statistical Process Control (SPC) techniques to demonstrate that their manufacturing processes and hence, their final products, are in control and will not vary from lot to lot. This constant effort is provided to ensure the highest possible product quality.

Qualification Strategy

Benchmarq's goal is to provide the most reliable products possible. Hence, a combination of devices and packages representative of the front-end and back-end processes are selected for reliability testing. Three levels of qualification and reliability testing are performed on each product family. They are as follows:

Wafer Level

Wafer-level qualification is performed so that the reliability of the front-end process may be ascertained. Wafers from three front-end wafer lots are analyzed. Design rules such as critical dimensions, film thicknesses, step coverages, and oxide integrity are verified using a combination of electrical and visual analysis. Also, a series of tests designed to check the reliability of passivation, thin oxides, metal, and transistors are performed.

By analyzing the device in wafer form, any major process or design reliability problems are uncovered early in the product development phase where they can be more quickly corrected.

Package Level

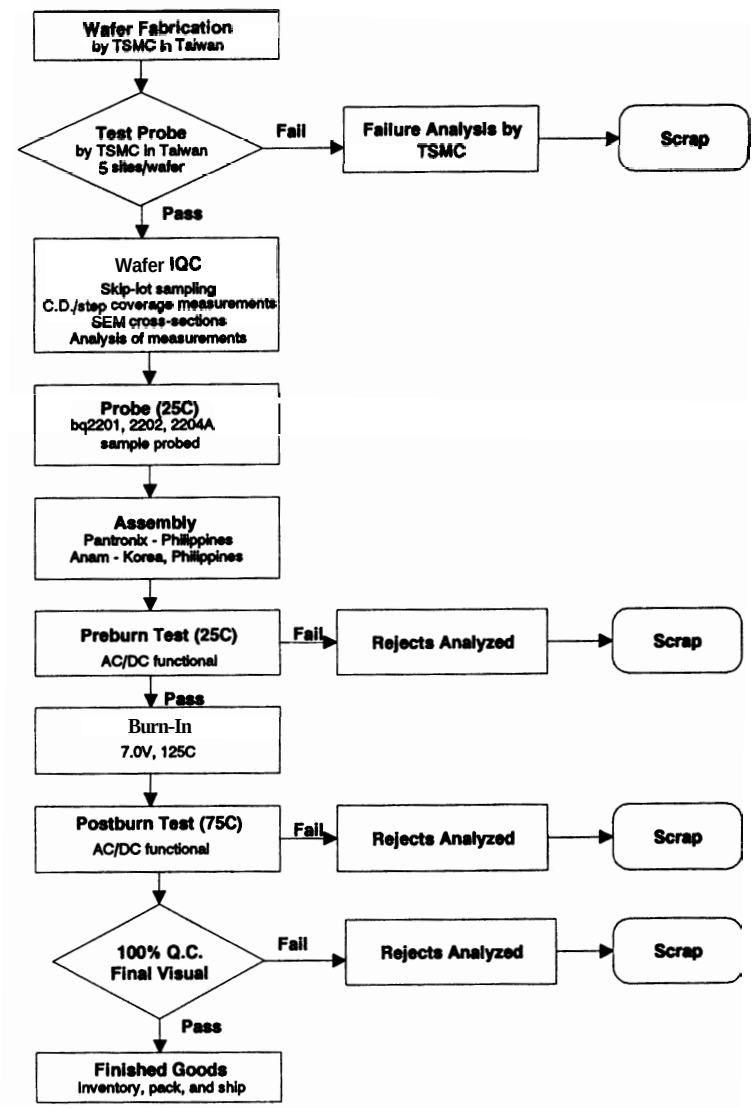
An assessment is performed on various package types to determine the reliability and manufacturability of the packaging process and materials.

System Level

Finally, a series of stringent environmental and operating life stresses are performed on packaged devices so that the short-term and long-term reliability of the product may be ensured. Infant life and long-term life predictions are then made based on this data.

NVSRAM Controllers

NVSRAM Controller Process Flow



Qualification Summary—NVSRAM Controllers

Product: NVSRAM Controllers (bq2201, bq2202, bq2204)

Qual Vehicle: bq2201SN 8-pin, 150-mil SOIC
(Lot: T044002AACPA Date Code: 9046)

High-Temperature Operating Life Test (5.5V, 150°C)

48 hrs	96 hrs	168 hrs
0/100	0/100	0/100

Operating Life Test (5.5V, 125°C)

48 hrs	168 hrs	500 hrs	1000 hrs	2000 hrs
0/298	0/298	0/298	1/298 [1]	0/297

Temperature/Humidity/Bias (5.5V, 85°C, 85%RH)

48 hrs	168 hrs	500 hrs	1000 hrs	2000 hrs
0/89	0/89	0/89	1/89 [1]	0/88

High-Temperature Storage (unbiased, 150°C)

48 hrs	168 hrs	500 hrs	1000 hrs	2000 hrs
0/50	0/50	0/50	0/50	0/50

Highly Accelerated Stress Test—HAST (5.5V, 130°C, 85%RH, 1.7 atm)

24 hrs	48 hrs	72 hrs
0/50	0/50	0/50

Temperature Cycling (-65°C to +150°C)

10 cyc	100 cyc	300 cyc	600 cyc	1000 cyc
	0/100	0/97 [1]	0/97	0/97

Thermal Shock (-55°C to 125°C)

30 cyc
0/50

Moisture Resistance (unbiased, -10°C to 65°C, 90%RH)

10 cyc
0/50

Resistance to Soldering Heat (260°C, 10 seconds)

1 cyc
0/10

Solderability (245°C, 5 seconds)	0/24 leads fail
Lead Fatigue	0/16 leads fail
Lead Finish	0/24 leads fail
Resistance to Solvents	0/4 devices fail
Electrostatic Discharge	>± 1000V
Latch-up Immunity	>± 200mA

[1] Refer to the August 1992 Benchmarq *Quality and Reliability Report.*

Predicted Failure Rates—NVSRAM Controllers

Most integrated circuit failure mechanisms **are based** on physical or chemical reactions. These reactions **are** accelerated by temperature **and can** be modeled **using** the **Arrhenius** equation. The acceleration factor (AF) between any two temperatures may be calculated as follows:

$$AF_{(T_1 - T_2)} = e^{\frac{E_a}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)}$$

where:

AF	=	acceleration factor
e	=	natural log
E_a	=	activation energy in electron volts
k	=	Boltzman's constant (8.62×10^{-5} eV/°K)
T_1	=	derated temperature (OK)
T_2	=	stress temperature (OK)

The following assumptions have been made in **Benchmarq's** determination of failure rates:

Activation energy = 0.7 eV (based on 85°C/85% RH THB failure)

Temperature derated to 55°C (typical use condition)

$AF_{(55°C - 125°C)} = 77.8$

$AF_{(55°C - 150°C)} = 259.9$

Total device hours:

bq2201 2000 hours x 298 devices x 77.8 = 46,368,800 device hours
bq2201 168 hours x 100 devices x 259.9 = 4,366,320 device hours
bq1001 1000 hours x 100 devices x 77.8 = 7,780,000 **device** hours

Total device hours = 5.8515×10^7 hours

A single-point estimate of the mature life failure rate may be calculated as follows:

$$\text{Failure rate} = \frac{\text{number of failures}}{\text{total device hours}}$$

$$= 1/5.815 \times 10^{7} \text{ hours}$$

$$= 17.1 \text{ FITS}$$

Next, a Chi square approximation of the mature life failure rate can be made using the following information:

Number of failures: 1
Confidence level: 60%

$$\text{Failure rate}\left(\chi^2\right) = \frac{\chi^2_{(2f\ +\ 2,\ \alpha)}}{2 \times \text{total device hours}}$$

where:

f = number of failures
α = 1 – confidence level

$$\text{Failure rate}\left(\chi^2\right) = \frac{4 \qquad 0.4)}{2 \times (5.8515 \times 10^{7})}$$

$$= 4.1175 / (1.1703 \times 10^{8})$$

$$= 3.52 \times 10^{-8} / \text{hours}$$

$$= 35.2 \text{ FITS}$$

Therefore, for the NVSRAM controllers built using the TSMC 1.2µ single-poly, double-level metal CMOS process, the mature life FIT rate is 36 FITS.

A similar determination of the infant life failure rate can be made. Benchmarq considers a failure that occurs within 1 year (8760 hours) at normal operating conditions an infant life failure.

Derating for 125°C:

Infant life time	= AF x device stress hours
8760 hours	= 77.8 x device stress hours
Device stress hours	= 112.6 hours

Derating for 150°C:

Infant life time	= AF x device stress hours
8760 hours	= 259.9 x device stress hours
Device stress hours	= 33.7 hours

Therefore, any failure that occurs in the first 112.6 hours of 125°C operating life or in the first 33.7 hours of 150°C operating life is considered an infant life failure.

Total device hours:

bq2201 112.6 hours x 298 devices x 77.8 = 2,610,563 device hours
bq2201 33.7 hours x 100 devices x 259.9 = 875,863 device hours
bq1001 112.6 hours x 100 devices x 77.8 = 876,028 device hours

Total device hours = 4.3624×10^6 hours

A single-point estimate of the infant life failure rate may be calculated as follows:

$$\text{Failure rate} = \frac{\text{number of failures}}{\text{total device hours}}$$

$$= 0 / 4.3624 \times 10^6 \text{ hours}$$

$$= 0 \text{ FITS}$$

Next, a Chi square approximation of the infant life failure rate can be made using the following information:

Number of failures: 0
Confidence level: 60%

$$\text{Failure rate}\left(\chi^2\right) = \frac{\chi^2_{(2f\,+\,2,\ a)}}{2 \times \text{total device hours}}$$

where:

f = number of failures
a = 1 − confidence level

$$\text{Failure rate}\left(\chi^2\right) = \frac{\chi^2_{(2,\ 0.4)}}{2 \times (4.3624 \times 10^6)}$$

$$= 1.8970 / (8.7249 \times 10^6)$$

$$= 2.174 \times 10^{-7} / \text{hours}$$

$$= 217.4 \text{ FITS}$$

Therefore, for the NVSRAM controllers built using the TSMC 1.2µ single-poly, double-level metal CMOS process, the infant life FIT rate is approximately 218 FITS.

NVSRAMs

NVSRAM Module Construction

Benchmarq's NVSRAM modules are designed and built by Benchmarq in Dallas, Texas. Each module is constructed of one or more ICs mounted on a printed circuit board along with a lithium battery. This subassembly is then placed into a plastic housing and encapsulated with a specialized two-part epoxy. (The bq2502 Integrated Backup Unit is manufactured in the same manner.)

Quality Procedures

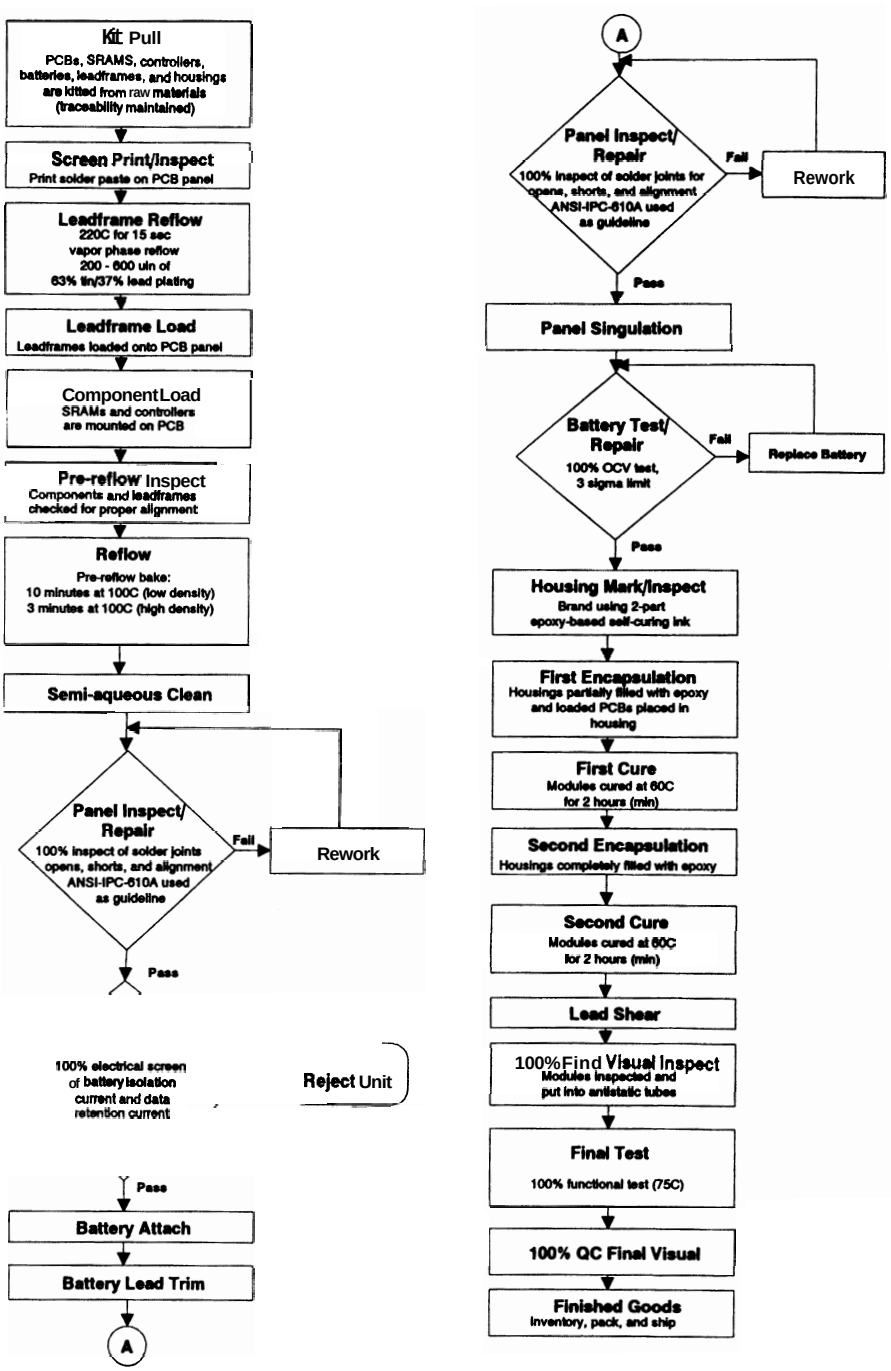
To help ensure that our final product is both consistent and reliable, the following quality inspections and tests are performed:

- **SRAMs**—Low-powered SRAMs are used in the manufacture of modules. At incoming inspection, data-retention current is measured on a representative sample from each lot. After the components are mounted on the circuit boards, the circuits are 100% tested for data-retention current.
- Batteries-Certificates of Compliance verifying the Open Circuit Voltage (OCV), Closed Circuit Voltage (CCV), and Internal Resistance (IR) are required from the manufacturer on each shipment. Historical statistical sampling indicates that a Lot Tolerant Percent Defective (LTPD) of less than 1% at a confidence level of 90% can be expected. After batteries are mounted on the circuit boards, they are 100% tested for OCV.
- **PCBs**—A sample from each lot of printed circuit boards is visually inspected for router damage, breakouts, opens, shorts, or misaligned solder masks.
- **Leads**—Certificates of Compliance verifying the plating thickness are required from the manufacturer. Periodic quality audits of the plating thickness are performed.

Traceability

N l traceability is maintained on both the integrated circuits and modules. The integrated circuits are traceable to front-end wafer lot and to assembly lot. The modules are traceable to housing, PCB, battery, controller, and SRAM lots.

NVSRAM Module Process Flow



Qualification Summary—NVSRAM Modules

Product NVSRAM Modules (bq4010, bq4011, bq4011H, bq4013, bq4014, bq4015, bq4016, bq4017, bq4024, bq4025, bq2502)

Qual Vehicle bq4010MA 28-pin, 600-mil Module
(Lot: QM04901 Date Code: 9049)

Temperature/Humidity/Bias (5.5V, 85°C, 85%RH)

48 hrs	168 hrs	500 hrs	1000 hrs	2000 hrs
0/99	0/99	0/96 [1]	0/96	0/96

Highly Accelerated Stress Test*—HAST (5.5V, 130°C, 85%RH, 1.7 atm)

24 hrs	48 hrs	72 hrs	
0/80	0/80	4/79 [1]	'(without battery)

Temperature Cycling (-40°C to +85°C)

10 cyc	100 cyc	300 cyc	600 cyc	1000 cyc
0/100	0/100	0/100	0/100	0/100

Thermal Shock (-55°C to 125°C) without battery

30 cyc
0/105

Moisture Resistance (unbiased, -10°C to 65°C, 90%RH)

10 cyc
0/50

Resistance to Soldering Heat (260°C, 10 seconds)

1 CYC
0/10

Solderability (245°C, 5 seconds)	0/56 leads fail
Lead Fatigue	0/84 leads fail
Lead Finish	0/56 leads fail
Resistance to Solvents	0/4 devices fail
Electrostatic Discharge	>± 1000V
Latch-up Immunity	>± 200mA

[1] Refer to the August 1992 Benchmarq *Quality and Reliability Report.*

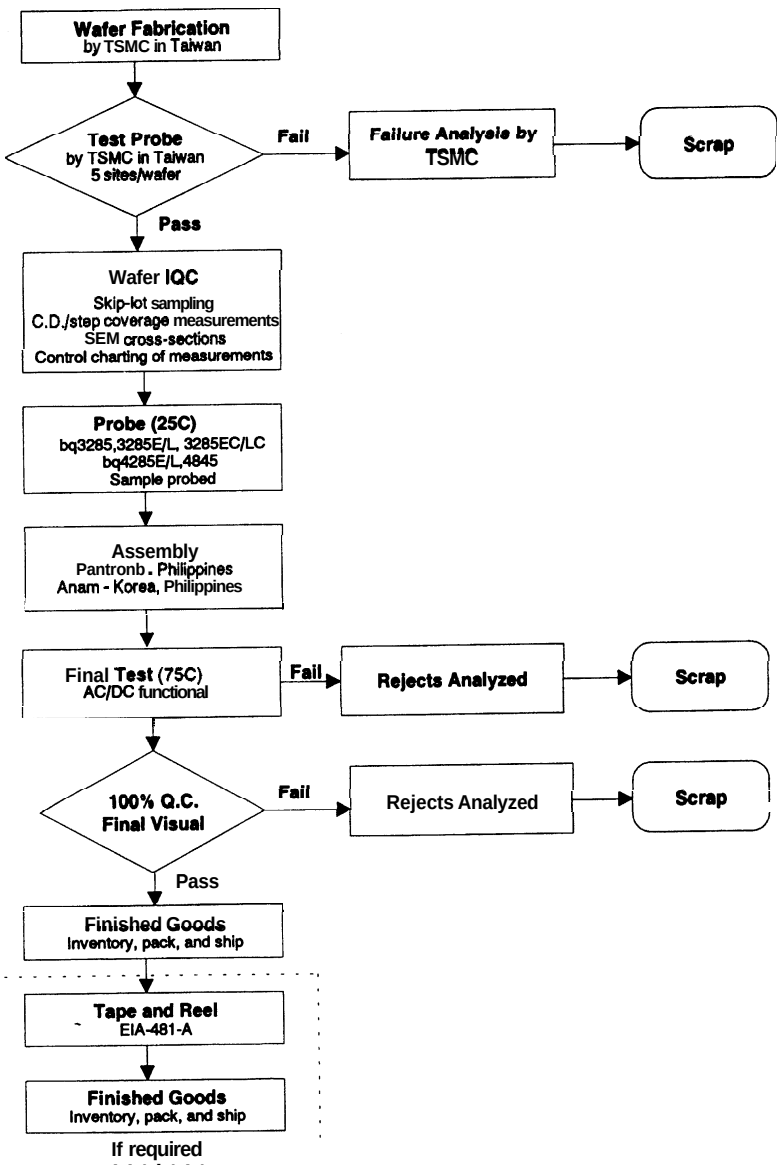
In the case of modules, an approximate FIT rate can be determined by adding together the FIT rates of the various components. The FIT rates used and their sources are listed below:

Component	FIT Rate	Source
Controller	36	Calculated in previous section
SRAM	35	SRAM manufacturer
Battery	<10	Panasonic (approximate)
Total	81 FITS	

Therefore, for Benchmarq's module products, the FIT rate is approximately 81 FITS.

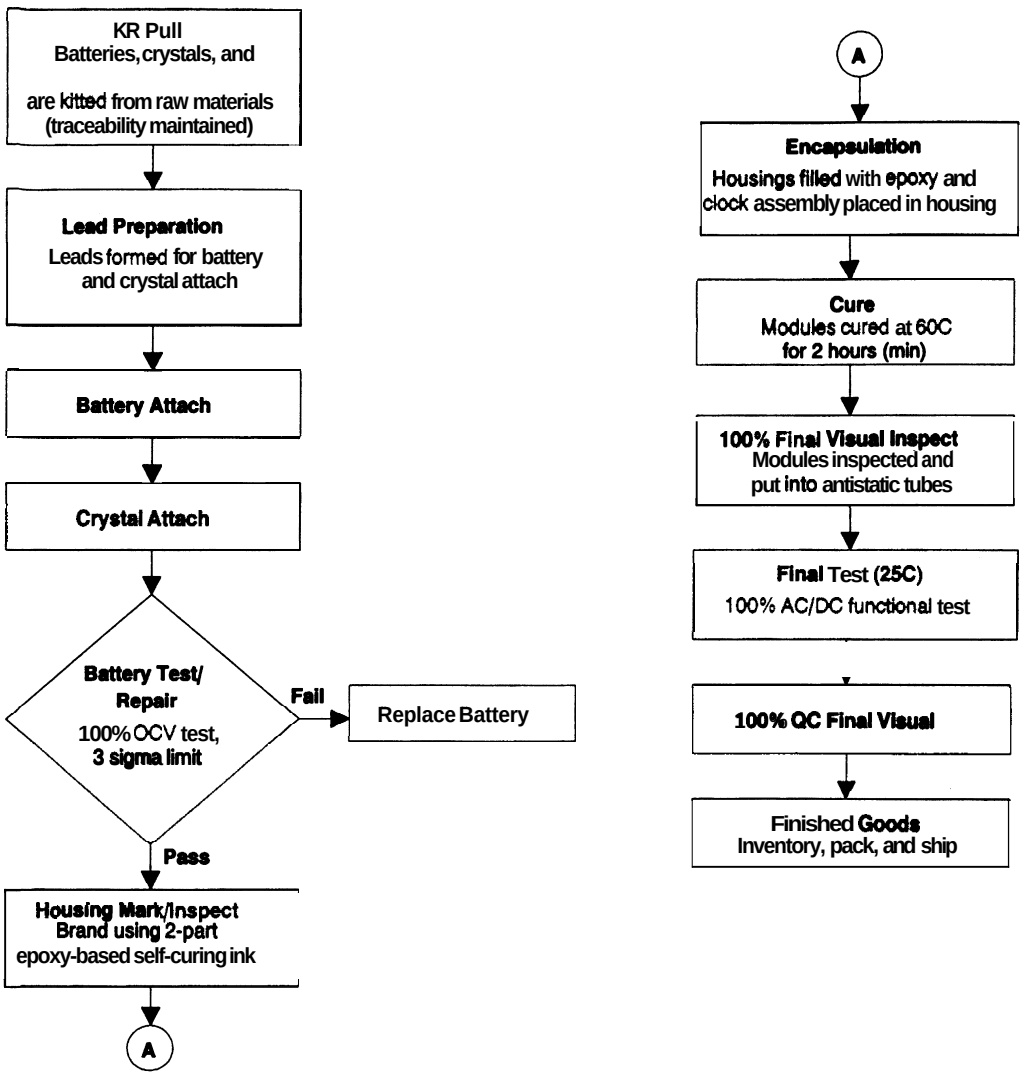
Real-Time Clocks (RTCs)

Real-Time Clock IC Process Flow



Real-Time Clock Module Process Flow

All modules are built by Benchmarq in Dallas, Texas.



Qualification Summary—Real-Time Clock ICs

Product: RealTime Clocks (bq3285, bq3285E/L, bq3285EC/LC, bq4285, bq4285E/L, bq4845)

Qual Vehicle: bq3285ES 24-pin, 300-mil SOIC

(Lot: 285AAEA, T346002, A61453.2 Date Code: 9332EP)

High-Temperature Operating Life Test (5.5V, 125°C)

48 hrs	168 hrs	500 hrs	1000 hrs	2000 hrs
0/400	0/400	0/400	0/400	0/400

Temperature/Humidity/Bias (5.5V, 85°C, 85%RH)

48 hrs	168 hrs	500 hrs	1000 hrs	2000 hrs
0/96	0/96	0/96	0/96	0/96

High-Temperature Storage (unbiased, 150°C)

48 hrs	168 hrs	500 hrs	1000 hrs	2000 hrs
0/30	0/30	0/30	0/30	* 1/30

Temperature Cycling (65°C to +150°C)

100 cyc	300 cyc	600 cyc	1000 cyc
0/100	0/100	0/100	0/100

Thermal Shock (55°C to +125°C)

30 cyc
0/50

Resistance to Soldering Heat (260°C , 10 seconds)

1 cyc
0/5

Solderability (245°C, 5 seconds)	0/120 leads fail
Lead Fatigue	0/120 leads fail
Lead Finish	0/120 leads fail
Resistance to Solvents	0/5
Electrostatic Discharge	>±2000 volts
Latchup Immunity	>±200 mA

* Intermittent single-bit failure—destroyed in analysis.

Qualification Summary—Real-Time Clock Modules

Product: Real-Time Clock Modules (bq3287, bq3287A, bq3287E, bq3287L, bq3287EA, bq3287LA, bq4287E, bq4287L, bq4847Y)

Qual Vehicle: bq3287MT 24-pin, 600-mil Module

(Lot: QM147001 Date Code: 9147)

(Lot: PM205004 Date Code: 9205)

Temperature/Humidity/Bias (5.5V, 85°C, 85%RH)

48 hrs	168 hrs	500 hrs	1000 hrs	2000 hrs
0/100		0/100	0/100	0/100

Highly Accelerated Stress Test HAST (5.5V, 130°C, 85%RH, 1.7 atm)

24 hrs	48 hrs	144 hrs
0/75	w 5	0/75

Temperature Cycling (65°C to +150°C)

10 cyc	100 cyc	300 cyc	600 cyc	1000 cyc
0/100	0/100	0/100	0/100	0/100

Thermal Shock (55°C to +125°C)

30 cyc
0/95

Resistance to Soldering Heat (260°C , 10 seconds)

1 cyc
0/10

Solderability (245°C, 5 seconds)	0/24 leads fail
Lead **Fatigue**	0/72 leads **fail**
Lead Finish	0/72 leads fail
Resistance to Solvents	4 ' Q
Physical Dimension	0/4

8

Predicted Failure Rates—Real-Time Clock ICs

Most integrated circuit failure mechanisms are based on physical or chemical reactions. These reactions are accelerated by temperature and can be modeled using the Arrhenius equation. The acceleration factor (AF) between any two temperatures may be calculated as follows:

$$AF_{(T_1 - T_2)} = e^{\frac{E_a}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)}$$

where:

AF	=	acceleration factor
e	=	natural log
E_a	=	activation energy in electron volts
k	=	Boltzman's constant (8.62×10^{-5} eV/°K)
T_1	=	derated temperature (OK)
T_2	=	stress temperature (OK)

The following assumptions have been made in Benchmarq's determination of failure rates:

- Activation energy = 0.7 eV (conservative estimate)
- Temperature derated to 55°C (typical use condition)
- $AF_{(55°C - 125°C)}$ = 77.8
- Voltage derated to 5.5V (typical use condition)

  $AF_{(5.5V - 7.0V)}$ = 5.0 (conservative estimate)

Total device hours:

bq3285 2000 hours x 400 devices x 77.8 x 5.0 = 311,200,000 device hours

Total device hours = 3.1120×10^8 hours

A single-point estimate of the mature life failure rate may be calculated as follows:

$$\text{Failure rate} = \frac{\text{number of failures}}{\text{total device hours}}$$

$$= 0 / 3.1120 \times 10^8 \text{ hours}$$

$$= 0 \text{ FITS}$$

Next, a Chi square approximation of the mature life failure rate can be made using the following information:

Number of failures: 0
Confidence level: 60%

$$\text{Failure rate}\left(\chi^2\right) = \frac{\chi^2_{(2f\ +\ 2,\ \alpha)}}{2 \times \text{total device hours}}$$

where:

f = number of failures
$\alpha = 1 -$ confidence level

$$\text{Failure rate}\left(\chi^2\right) = \frac{\chi^2_{(2,\ 0.4)}}{2 \times (1.2448 \times 10^8)}$$

$$= 1.8970 / (6.224 \times 10^8)$$

$$= 3.05 \times 10^{-9} / \text{hours}$$

$$= 3.05 \text{ FITS}$$

Therefore, for the real-time clock integrated circuit built using the TSMC 0.8µ CMOS single-poly, double-level metal process, the mature life FIT rate is approximately **3 FITS.**

A similar determination of the infant life failure rate can be made. Benchmarq considers failures that occur within 1 year (8760 hours) at normal operating conditions an infant life failure.

Derating for 125°C:

Infant life time	= AF x device stress hours
8760 hours	= 77.8 x device stress hours
Device stress hours	= 112.6 hours

Therefore, any failure that occurs in the first 112.6 hours of 125°C operating life is considered an infant life failure.

Total device hours:

bq3285 112.6 hours x 400 devices x 77.8 x 5.0 = 17,520,560 device hours

Total device hours = 1.7520×10^7 hours

A single-point estimate of the infant life failure rate may be calculated as follows:

$$\text{Failure rate} = \frac{\text{number of failures}}{\text{total device hours}}$$

$$= 0 / 1.7520 \times 10^7 \text{ hours}$$

$$= 0 \text{ FITS}$$

Next, a Chi square approximation of the infant life failure rate can be made using the following information:

$$\text{Failure rate}\left(\chi^2\right) = \frac{\chi^2_{(2f\ +\ 2,\ \alpha)}}{2 \times \text{total device hours}}$$

Number of failures: 0
Confidence level: 60%

where:

f = number of failures
$a = 1 -$ confidence level

$$\text{Failure rate}\left(\chi^2\right) = \frac{\chi^2_{(2,\ 0.4)}}{2 \times (7.0082 \times 10^6)}$$

$$= 1.8970 / (3.5041 \times 10^7)$$

$$= 5.4136 \times 10^{-8} / \text{hours}$$

$$= 54.1 \text{ FITS}$$

Therefore, for the real-time clock integrated circuit built using the TSMC 0.8 single-poly, double-level metal CMOS process, the infant life FIT rate is approximately 54 FITS.

Predicted Failure Rates—Real-Time Clock Modules

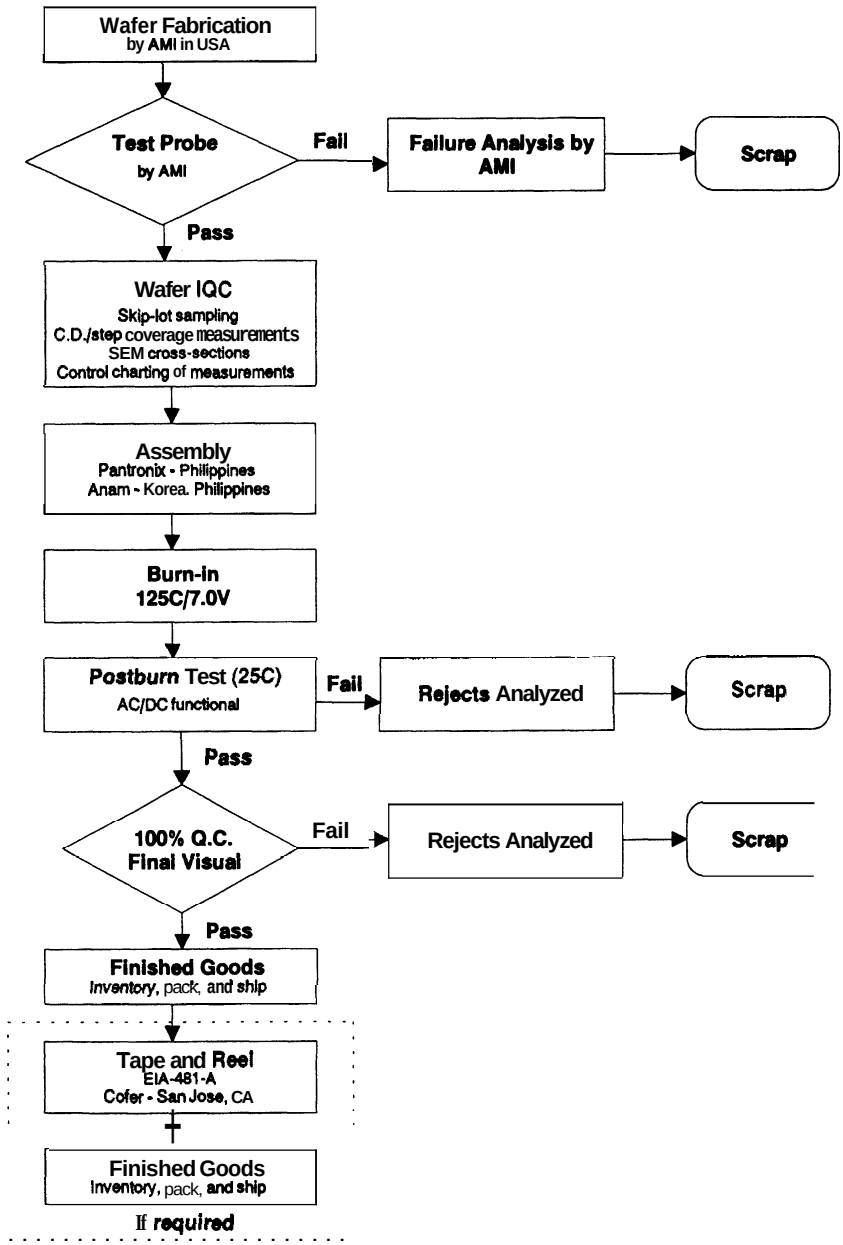
In the case of modules, an approximate FIT rate can be determined by adding together the FIT rates of the various components. The FIT rates used and their sources are listed below:

Component	FIT Rate	Source
Real-Time Clock IC	3	Calculated in previous section
Crystal	<5	Daiwa (approximate)
Battery	<2	Panasonic (approximate)
Total	10 FITS	

Therefore, for Benchmarq's RTC module products, the FIT rate is approximately 10 FITS.

Lithium Ion Pack Supervisors (bq2053 and bq2058) and Rechargeable Alkaline Charge IC (bq2903)

Process Flow



Qualification Summary—Lithium Ion Pack Supervisor ICs and Rechargeable Alkaline Charge IC

Product: bq2053, bq2058, bq2903

Qual Vehicle: bq2053 8-pin, 150-mil SOIC

High-Temperature Operating Life Test (7.0V, 125°C)

48 hrs	168 hrs	500 hrs	1000 hrs
0/498	0/498	0/498	0/498

Temperature/Humidity/Bias (5.5V, 85°C, 85%RH)

48 hrs	168 hrs	500 hrs	1000 hrs
0/100	0/100	0/100	0/100

High-Temperature Storage (unbiased, 150°C)

168 hrs	500 hrs	1000 hrs
0/50	0/50	0/50

Temperature Cycling (-65°C to +150°C)

10 cyc	300 cyc	600 cyc	1000 cyc
0/100	0/100	0/100	1/100

Thermal Shock (-55°C to +125°C)

30 cyc
0/50

Resistance to Soldering Heat (260°C , 10 seconds)

1 cyc
0/5

Solderability (245°C, 5 seconds)	0/96 leads fail
Lead **Fatigue**	0/80 leads fail
Lead Finish	0/80 leads fail
Resistance to Solvents	0/4 devices fail
Electrostatic Discharge	>± 2000 volts
Latch-up Immunity	>± 200 mA

8

Predicted Failure Rates--Lithium Ion Pack Supervisor

Most integrated circuit failure mechanisms are based on physical or chemical reactions. These reactions are accelerated by temperature and can be modeled using the Arrhenius equation. The acceleration factor (AF) between any two temperatures may be calculated as follows:

$$AF_{(T_1 - T_2)} = e^{\frac{E_a}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)}$$

where:

AF	=	acceleration factor
e	=	natural log
E_a	=	activation energy in electron volts
k	=	Boltzman's constant (8.62×10^{-5} eV/°K)
T_1	=	derated temperature (OK)
T_2	=	stress temperature (OK)

The following assumptions have been made in Benchmarq's determination of failure rates:

- Activation energy = 0.7 eV (conservative estimate)
- Temperature derated to 55°C (typical use condition)

  $AF_{(55°C - 125°C)}$ = 77.8
- Voltage derated to 5.5V (typical use condition)

  $AF_{(5.5V - 7.0V)}$ = 5.0 (conservative estimate)

Total device hours:

bq2053 1000 hours x 498 devices x 77.8 x 5.0 = 193,722,000 device hours

A single-point estimate of the mature life failure rate may be calculated as follows:

$$\text{Failure rate} = \frac{\text{number of failures}}{\text{total device hours}}$$

$$= 0 / 1.93722 \times 10^8 \text{ hours}$$

$$= 0 \text{ FITS}$$

Next, a Chi square approximation of the mature life failure rate can be made using the following information:

Number of failures: 0
Confidence level: 60%

$$\text{Failure rate}\left(\chi^2\right) = \frac{\chi^2_{(2f + 2,\ \alpha)}}{2 \times \text{total device hours}}$$

where:

f = number of failures
α = 1 – confidence level

$$\text{Failure rate}\left(\chi^2\right) = \frac{\chi^2_{(2,\ 0.4)}}{2 \times (1.93722 \times 10^8)}$$

$$= 1.8970 / (3.87444 \times 10^8)$$

$$= 4.90 \times 10^{-9} / \text{hours}$$

$$= 4.9 \text{ FITS}$$

Therefore, for the bq2053 Lithium Ion Pack Supervisor IC built using the AMI 1.5µ double-level poly, single-level metal CMOS process, the mature life FIT rate is approximately 5 FITS.

8

A similar determination of the infant life failure rate can be made. Benchmarq considers failures that occur within 1 year (8760 hours) at normal operating conditions an infant life failure.

Derating for 125°C:

Infant life time	= AF x device stress hours
8760 hours	= 77.8 x device stress hours
Device stress hours	= 112.6 hours

Therefore, any failure that occurs in the first 112.6 hours of 125°C operating life is considered an infant life failure.

Total device hours:

bq2053 112.6 hours x 498 devices x 77.8 x 5.0 = 21,813,097 device hours

A single-point estimate of the infant life failure rate may be calculated as follows:

$$\text{Failure rate} = \frac{\text{number of failures}}{\text{total device hours}}$$

$$= 0 / 2.1813097 \times 10^7 \text{ hours}$$

$$= 0 \text{ FITS}$$

Next, a Chi square approximation of the infant life failure rate can be made using the following information:

Number of failures: 0
Confidence level: 60%

$$\text{Failure rate } (\chi^2) = \frac{\chi^2_{(2f\ +\ 2,\ \alpha)}}{2 \times \text{total device hours}}$$

where:

f	=	number of failures
a	=	1 − confidence level

$$\text{Failure rate}\left(\chi^2\right) = \frac{\chi^2_{(2,\ 0.4)}}{2 \times (2.1913 \times 10^7)}$$

$$= 1.8970 / (4.3626 \times 10^7)$$

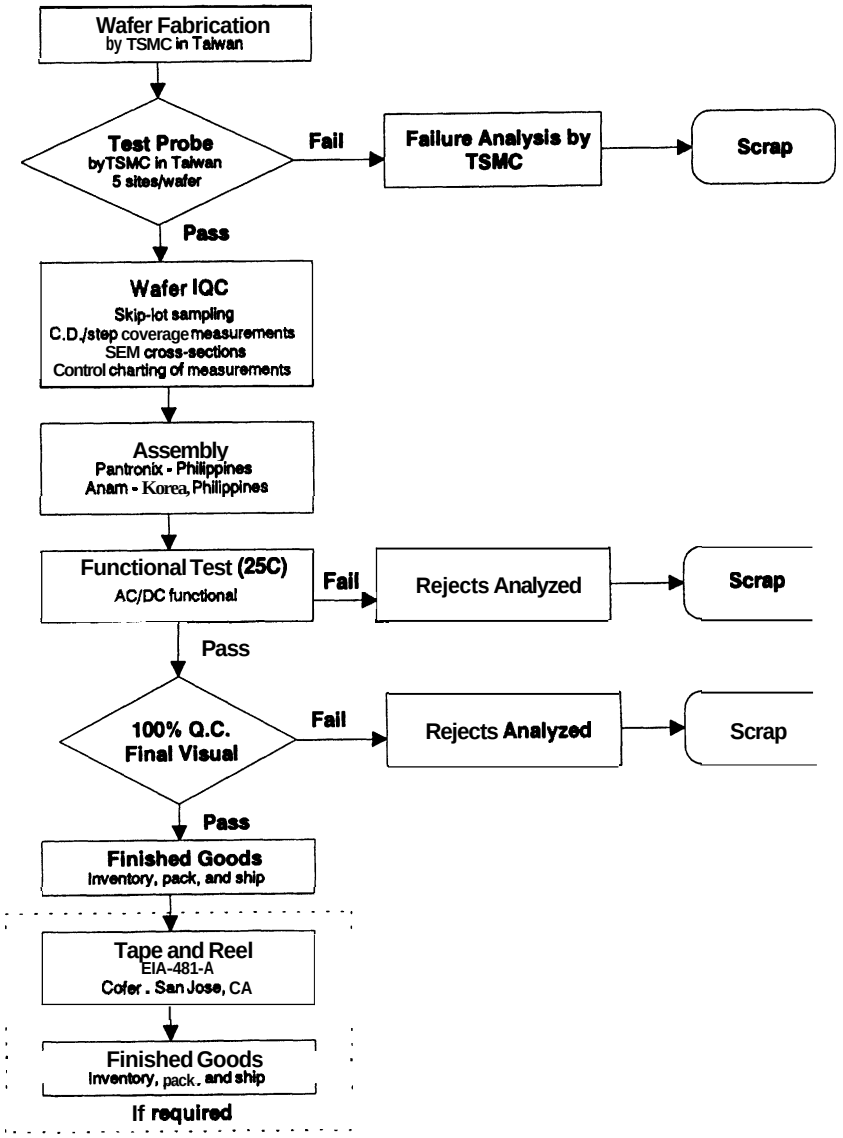
$$= 4.3483 \times 10^{-7} / \text{hours}$$

$$= 43.5 \text{ FITS}$$

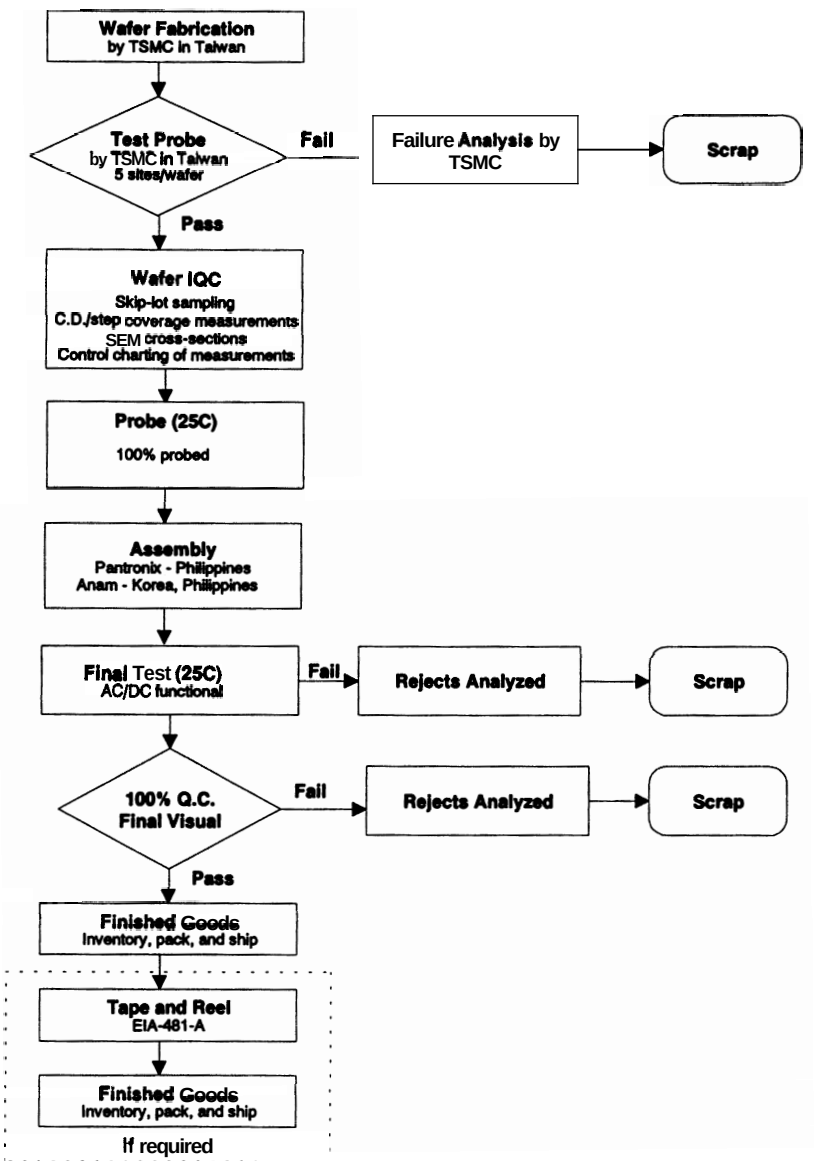
Therefore, for the bq2053 Lithium Ion Pack Supervisor IC built using the AMI 1.5µ double-level poly, single-level metal CMOS process, the infant life FIT rate is approximately 44 FITS.

Battery Management ICs

bq2002, bq2002T, bq2007 Fast Charge IC Process Flow

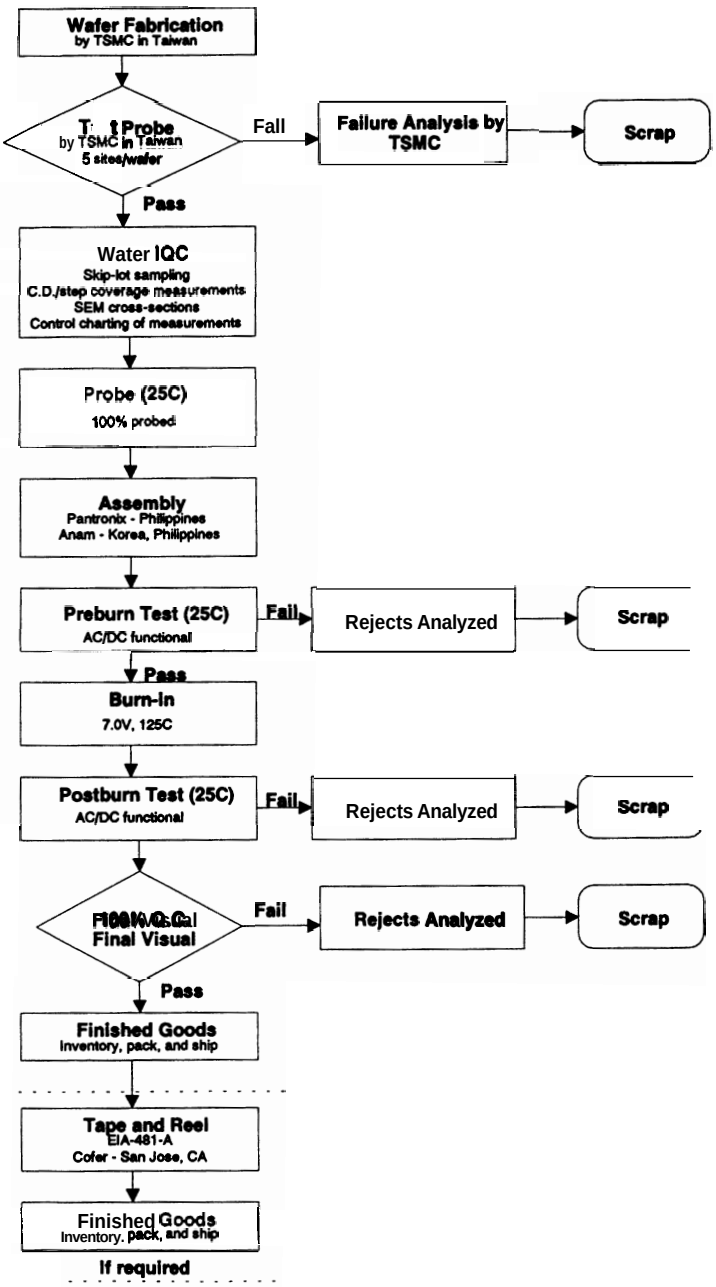


bq2003, 2004, 2004E, 2005 Fast Charge IC Process Flow



8

bq2010, bq2011, bq2011J, bq2011K, bq2012, bq2014, bq2040, bq2050, bq2090, and bq2091 Gas Gauge IC Process Flow



Qualification Summary—Fast Charge IC

Product: bq2003 Fast Charge IC

Qual Vehicle: 20-pin, 300-mil PDIP
(Lots: T221001, T237001, T244012)
(Lot: 211ABCP Date Code: 9226-EP)

High-Temperature Operating Life Test (7.0V, 125°C)

48 hrs	168 hrs	500 hrs	1000 hrs	2000 hrs
0/399	0/399	0/399	0/399	0/399

Temperature/Humidity/Bias (5.5V, 85°C, 85%RH)

48 hrs	168 hrs	500 hrs	1000 hrs	2000 hrs
0/120	0/120	0/120	0/120	0/120

High-Temperature Storage (unbiased, 150°C)

48 hrs	168 hrs	500 hrs	1000 hrs	2000 hrs
0/50	9/60	0/50	0/50	0/50

Temperature Cycling (65°C to +150°C)

10 cyc	100 cyc	300 cyc	600 cyc	1000 cyc
0/100	0/100	0/100	0/100	0/100

Thermal Shock (55°C to +125°C)

30 cyc
0/50

Resistance to Soldering Heat (260°C, 10 seconds)

1 cyc
0/5

Solderability (245°C, 5 seconds)	0/96 leads fail
Lead **Fatigue**	0/80 leads fail
Lead Finish	0/80 leads fail
Resistance to **Solvents**	0/4 devices fail
Electrostatic Discharge	>± 2000 volts
Latchup Immunity	>± 200 mA

8

Qualification Summary—Dual-Battery Fast Charge IC

Product: bq2005 Dual-Battery Fast Charge IC

Qual Vehicle: 20-pin, 300-mil SOIC

(Lot: 232AACA Date Code: 9329)

High-Temperature Operating Life Test (7.0V, 125°C)

48 hrs	168 hrs	500 hrs	1000 hrs
0/144	0/144	0/144	0/144

Temperature/Humidity/Bias (5.5V, 85°C, 85%RH)

48 hrs	168 hrs	500 hrs	1000 hrs
0/99	0/99	0/99	0/99

High-Temperature Storage (unbiased, 150°C)

48 hrs	168 hrs	500 hrs	1000 hrs
0/50	0/50	0/50	0/50

Temperature Cycling (65°C to +150°C)

100 cyc	300 cyc	600 cyc	1000 cyc
0/100	0/100	0/100	0/100

Thermal Shock (55°C to +125°C)

30 cyc
0/50

Resistance to Soldering Heat (260°C , 10 seconds)

1 cyc
0/5

Solderability (245°C, 5 seconds)	0/100 leads fail
Lead Fatigue	0/100 leads fail
Lead Finish	0/100 leads fail
Resistance to Solvents	0/5 devices fail
Electrostatic Discharge	**>± 2000 volts**
Latchup Immunity	>± 200 mA

Predicted Failure Rates—Fast Charge ICs

Most integrated circuit failure mechanisms are based on physical or chemical reactions. These reactions are accelerated by temperature and can be modeled using the Arrhenius equation. The acceleration factor (AF) between any two temperatures may be calculated as follows:

$$AF_{(T_1 - T_2)} = e^{\frac{E_a}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)}$$

where:

AF	=	acceleration factor
e	=	natural log
E_a	=	activation energy in electron volts
k	=	Boltzman's constant (8.62×10^{-5} eV/°K)
T_1	=	derated temperature (OK)
T2	=	stress temperature (OK)

The following assumptions have been made in Benchmarq's determination of failure rates:

Activation energy = 0.7 eV (conservative estimate)

Temperature derated to 55°C (typical use condition)

$AF_{(55°C - 125°C)}$ = 77.8

Voltage derated to 5.5V (typical use condition)

$AF_{(5.5V - 7.0V)}$ = 5.0 (conservative estimate)

Total equivalent device hours:

bq2003 2000 hours x 399 devices x 77.8 x 5.0 = 310,422,000 device hours
bq2005 1000 hours x 144 devices x 77.8 x 5.0 = 56,016,000 device hours

Total equivalent device hours: 366,438,000 device hours

8

A single-point estimate of the mature life failure rate may be calculated as follows:

$$\text{Failure rate} = \frac{\text{number of failures}}{\text{total device hours}}$$

$$= 0 / 3.66438 \times 10^{8} \text{ hours}$$

$$= 0 \text{ FITS}$$

Next, a Chi square approximation of the mature life failure rate can be made using the following information:

Number of failures: 0
Confidence level: 60%

$$\text{Failure rate}\left(\chi^2\right) = \frac{\chi^2_{(2f\ +\ 2,\ \alpha)}}{2 \times \text{total device hours}}$$

where:

f = number of failures
a = 1 - confidence level

$$\text{Failure rate}\left(\chi^2\right) = \frac{\chi^2_{(2,\ 0.4)}}{2 \times (3.10422 \times 10^{8})}$$

$$= 1.8970 / (7.32876 \times 10^{8})$$

$$= 2.59 \times 10^{-9} / \text{hours}$$

$$= 2.6 \text{ FITS}$$

Therefore, for the Battery Management ICs built using the TSMC 1.2µ double-level poly, double-level metal CMOS process, the mature life FIT rate is approximately 3 FITS.

A similar determination of the infant life failure rate can be made. Benchmarq considers failures that occur within 1 year (8760 hours) at normal operating conditions an infant life failure.

Derating for 125°C:

Infant life time	= A F x device stress hours
8760 hours	= 77.8 x device stress hours
Device stress hours	= 112.6 hours

Therefore, any failure that occurs in the first 112.6 hours of 125°C operating life is considered an infant life failure.

Total equivalent device hours:

bq2003 112.6 hours x 399 devices x 77.8 x 5.0 = 17,476,759 device hours
bq2005 112.6 hours x 144 devices x 77.8 x 5.0 = 6,307,402 device hours

Total equivalent device hours: 23,784,161 device hours

A single-point estimate of the infant life failure rate may be calculated as follows:

$$\text{Failure rate} = \frac{\text{number of failures}}{\text{total device hours}}$$

$$= 0 / 2.3784 \times 10^{7} \text{ hours}$$

$$= 0 \text{ FITS}$$

Next, a Chi square approximation of the infant life failure rate can be made using the following information:

Number of failures: 0
Confidence level: 60%

$$\text{Failure rate}\left(\chi^2\right) = \frac{\chi^2_{(2f\ +\ 2,\ \alpha)}}{2 \times \text{total device hours}}$$

where:

f = number of failures
a = 1 – confidence level

8

$$\text{Failure rate}\left(\chi^2\right) = \frac{\chi^2_{(2,\ 0.4)}}{2 \times (1.7477 \times 10^7)}$$

$$= 1.8970 / (4.7568 \times 10^7)$$

$$= 3.9880 \times 10^{-8} / \text{hours}$$

$$= 39.9 \text{ FITS}$$

Therefore, for the Battery Management ICs built using the TSMC 1.2μ double-level poly, double-level metal CMOS process, the infant life FIT rate is approximately 40 FITS.

BENCHMARQ Sales Offices and Distributors

Benchmarq Regional Sales Offices

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17919 Waterview Parkway
Dallas, TX 75252
(800) 966-0011
(972) 437-9195
FAX (972) 437-9198

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Cumming, GA 30131
(770) 664-8009
FAX (770) 752-0064

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(205) 881-1096
FAX (205) 881-1182

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(205) 621-1036
FAX (205) 621-1038

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Scottsdale, AZ 85260
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FAX (602) 991-0563

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FAX (609) 222-0153

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FAX (410) 740-5103

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Maitland, FL 32751
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FAX (407) 660-9407

Dyne-A-Mark Corporation
Two Prospect Park Business Center
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(305) 485-3500
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Cedar Rapids, IA 52402
(319) 393-0373
FAX (319) 393-1782

Indiana

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(317) 844-5222
FAX (317) 844-5861

Iowa

M.I.N.K. Associates, Inc.
443 Teakwood Lane
Cedar Rapids, IA 52402
(319) 393-0373
FAX (319) 393-1782

Kansas

M.I.N.K. Associates, Inc.
10100 Santa Fe, Suite 311
Overland Park, KS 66212
(913) 341-8309
FAX (913) 341-2605

M.I.N.K. Associates, Inc.
1231 Benene
Wichita, KS 67209
(316) 721-6444
FAX (316) 721-2567

Kentucky

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475 Arrowhead Springe Lane
Versailles, KY 40383
(606) 873-2330
FAX (606) 873-6233

Louisiana (South)

TL Marketing
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Houston, TX 77014
(713) 687-8100
FAX (713) 680-7517

Louisiana (North)

TL Marketing
14850 Quorum Drive, Suite 100
Dallas, TX 75240
(972) 490-9300
FAX (972) 960-6075

Maine

ProComp Associates Inc.
1049 East Street
Tewksbury, MA 01876
(508) 858-0100
FAX (508) 858-0110

Maryland

Avtek Associates, Inc.
10632 Little Patuxent Parkway, Suite 435
Columbia, MD 21044
(410) 740-5100
FAX (410) 740-5103

Massachusetts

ProComp Associates Inc.
1049 East Street
Tewksbury, MA 01876
(508) 858-0100
FAX (508) 858-0110

Michigan

Giesting & Associates
34441 Eight Mile Road, Suite 113
Livonia, MI 48152
(810) 478-8106
FAX (810) 477-6908

Minnesota

Vector Design Technology
3101 Old Highway 8, Suite 202
Roseville, MN 56113
(612) 631-1334
FAX (612) 631-1329

Mississippi

Interep Associates
Building A, Suite 203
2900 Highway 98
Daphne, AL 36526
(205) 621-1036
FAX (205) 621-1038

Missouri

M.I.N.K. Associates, Inc.
2268 Schuetz Road, Suite 114
St. Louis, MO 63146
(314) 995-5355
FAX (314) 995-5736

Montana

Delta Technical Sales, Inc.
15050 SW Koll Parkway, Suite 2D
Beaverton, OR 97006
(503) 646-7747
FAX (503) 643-9717

Nebraska

M.I.N.K. Associates, Inc.
10100 Santa Fe. Suite 311
Overland Park, KS 66212
(913) 341-8309
FAX (913) 341-2605

Nevada (North)

Criterion Sales Inc.
3350 Scott Boulevard, Bldg. #44
Santa Clara, CA 95054
(408) 988-6300
FAX (408) 986-9039

Nevada (South)

Aztech Component Sales
15230 N. 75th Street, Suite 1031
Scottsdale, AZ 85260
(602) 991-6300
FAX (602) 991-0563

New Hampshire

ProComp Associates Inc.
1049 East Street
Tewksbury, MA 01876
(508) 868-0100
FAX (508) 858-0110

New Jersey (North)

Metro Logic Corporation
271 Route 48 West, Suite D202
Fairfield, NJ 07006
(201) 575-5585
FAX (201) 575-8023

New Jersey (South)

Sunday-O'Brien
1 Executive Drive, Suite 11
Moorestown, NJ 08057
(609) 222-0151
FAX (609) 222-0153

New Mexico

Aztech Component Sales
15230 N. 75th Street, Suite 1031
Scottsdale, AZ 85260
(602) 991-6300
FAX (602) 991-0563

New York

Metro Logic Corporation
271 Route 48 West, Suite D202
Fairfield, NJ 07006
(201) 575-5585
FAX (201) 575-8023

Empire Technical Associates
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FAX (919) 847-8271

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3101 Old Highway 8, Suite 202
Roseville, MN 55113
(612) 631-1334
FAX (612) 631-1329

Ohio

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6200 S.O.M. Center Road, Suite D-20
Solon, OH 44139
(216) 498-4644
FAX (216) 498-4554

Giesting & Associates
2854 Blue Rock Road, P.O. Box 39398
Cincinnati, OH 45239
(513) 385-1105
FAX (513) 385-5069

Oklahoma

TL Marketing
14850 Quorum Drive, Suite 100
Dallas, TX 75240
(972) 490-9300
FAX (972) 960-6075

Oregon

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Beaverton, OR 97006
(503) 646-7747
FAX (503) 643-9717

Pennsylvania (East)

Sunday-O'Brien
1 Executive Drive, Suite 11
Moorestown, NJ 08057
(609) 222-0151
FAX (609) 222-0153

Pennsylvania west)

Giesting & Associates
471 Walnut Street
Pittsburgh, PA 15238
(412) 828-3553
FAX (412) 828-6160

Rhode Island

ProComp Associates Inc.
1049 East Street
Tewksbury, MA 01876
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FAX (508) 858-0110

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Charlotte, NC 28212
(704) 636-8658
FAX (704) 536-8768

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3101 Old Highway 8, Suite 202
Roseville, MN 55113
(612) 631-1334
FAX (612) 631-1329

Tennessee

Interep Associates
411-D Village Drive
Greenville, TN 37743
(423) 639-3491
FAX (423) 639-0081

Texas (El Paso)

Aztech Component Sales
15230 N. 75th Street, Suite 1031
Scottsdale, AZ 85260
(602) 991-6300
FAX (602) 991-0563

Texas

TL Marketing
8100 Shoal Creek Boulevard, Suite 250
Austin, TX 78757
(512) 371-7272
FAX (512) 371-0727

TL Marketing
14850 Quorum Drive, Suite 100
Dallas, TX 75240
(972) 490-9300
FAX (972) 960-6075

TL Marketing
14343 Torrey Chase Boulevard, Suite I
Houston, TX 77014
(713) 687-8100
FAX (713) 580-7517

Utah

Wescom Marketing
3500 South Main, Suite 110
Salt Lake City, UT 84115
(801) 269-0419
FAX (801) 269-0665

Vermont

ProComp Associates Inc.
1049 East Street
Tewksbury, MA 01876
(508) 858-0100
FAX (508) 858-0110

Virginia

Avtek Associates, Inc.
10632 Little Patuxent Parkway, Suite 435
Columbia, MD 21044
(410) 740-5100
FAX (410) 740-5103

Washington

Delta Technical Sales, Inc.
11911 NE 1st Street, Suite 204
Bellevue, WA 98004
(206) 688-0812
FAX (206) 688-0813

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Calgary, Alberta
Canada T1Y 5Z6
(403) 735-6230
FAX (403) 735-0599

Ontario

Neutronics Components, Ltd.
240 Terence Matthews Cr., Suite 105
Kanata, Ontario
Canada K2M 2C4
(613) 599-1263
FAX (613) 599-4750

Neutronics Components, Ltd.
5925 Airport Road, Suite 200
Mississauga, Ontario
Canada L4V 1W1
(905) 405-6230
FAX (905) 405-6248

Quebec

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FAX 49-89-535129

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47 Dickenson Road
Bangalore 560 042
Karnataka
India
91-812-588-323
FAX 91-812-586-872

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FAX (408) 996-3690

United Kingdom

Sequoia Technology Limited
Tekelec House
Back Lane, Spencers House
Reading Berks RG7 1PD
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44-1-734-258000
FAX 44-1-734-258020

Notes